

Low-voltage translating 8-bit I²C-bus I/O Expander**Features**

- Operation power supply voltage from 1.65V to 4.0V
- Allows bidirectional voltage-level translation and GPIO expansion between:
 - 1.8 V SCL/SDA and 1.8 V, 2.5 V, 3.3 V Port P
 - 2.5 V SCL/SDA and 1.8 V, 2.5 V, 3.3 V Port P
 - 3.3 V SCL/SDA and 1.8 V, 2.5 V, 3.3 V Port P
- Low standby current consumption:
 - 1.5 μ A typical at 3.3 V V_{DD}
- 1MHz I²C-bus interface
- Compliant with the I²C-bus Fast and Standard modes
- Programmable Pull-up/Pull-down Resistors for GPIO Inputs
- Software Reset
- Active LOW open-drain interrupt output
- Low standby current
- Latch-up tested (exceeds 100mA)
- Offered in UQFN1.8x2.6-16

Description

The PI4IOE5V6408 is an 8-bit general-purpose I/O expander that provides remote I/O expansion for most microcontroller families via the I²C-bus interface.

It provides a simple solution when additional I/Os are needed while keeping interconnections to a minimum, for example, in battery-powered mobile applications for interfacing to sensors, push buttons, keypad, etc.

It can operate from 1.65 V to 4 V on the GPIO-port side and 1.65 V to 3.6 V on the SDA/SCL side. This allows the PI4IOE5V6408 to interface with next generation microprocessors and microcontrollers on the SDA/SCL side, where supply levels are dropping down to conserve power.

The bidirectional voltage-level translation in the PI4IOE5V6408 is provided through $V_{DD(I2C_bus)}$. $V_{DD(I2C_bus)}$ should be connected to the V_{DD} of the external SCL/SDA lines. The voltage level on the GPIO-port of the PI4IOE5V6408 is determined by $V_{DD(P)}$.

At power on, the I/Os are configured as inputs; however, the system master can enable the I/Os as either inputs or outputs by writing to the I/O direction bits. The data for each input or output is kept in the corresponding Input or Output register. All registers can be read by the system master.

PI4IOE5V6408 has open-drain interrupt (\overline{INT}) output pin that goes LOW when the input state of a GPIO-port changes from the input-state default register value. The device also has an interrupt masking feature by which the user can mask the interrupt from an individual GPIO-port.

Pin Configuration

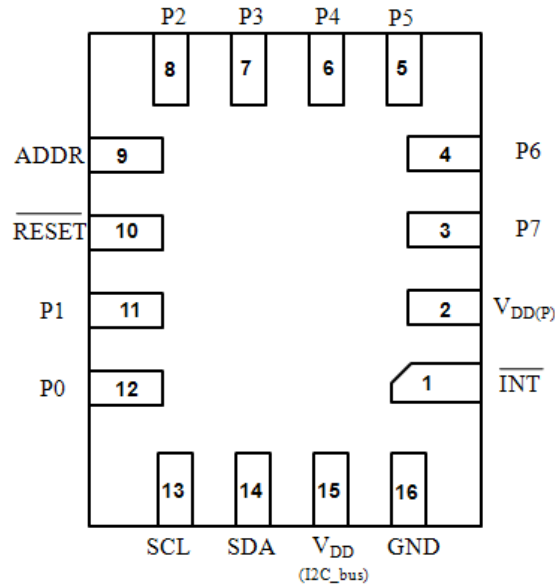


Fig 1. UQFN Top View

Pin Description

Table 1: Pin Description

| Pin Name | Pin No. | Description |
|---------------------------|---------|---|
| $\overline{\text{INT}}$ | 1 | Active-low interrupt output. Connect to $V_{\text{DD(I2C_bus)}}$ through a pull-up resistor. |
| $V_{\text{DD(P)}}$ | 2 | Supply voltage of PI4IOE5V6408 GPIO-port |
| P7 | 3 | GPIO-port input/output (push-pull design structure). At power on, P7 is configured as an input. |
| P6 | 4 | GPIO-port input/output (push-pull design structure). At power on, P6 is configured as an input. |
| P5 | 5 | GPIO-port input/output (push-pull design structure). At power on, P5 is configured as an input. |
| P4 | 6 | GPIO-port input/output (push-pull design structure). At power on, P4 is configured as an input. |
| P3 | 7 | GPIO-port input/output (push-pull design structure). At power on, P3 is configured as an input. |
| P2 | 8 | GPIO-port input/output (push-pull design structure). At power on, P2 is configured as an input. |
| ADDR | 9 | Address input. Connect directly to $V_{\text{DD(I2C_bus)}}$ or ground. |
| $\overline{\text{RESET}}$ | 10 | Active-low reset input. Connect to $V_{\text{DD(I2C_bus)}}$ through a pull-up resistor, if no active connection is used. |
| P1 | 11 | GPIO-port input/output (push-pull design structure). At power on, P1 is configured as an input. |
| P0 | 12 | GPIO-port input/output (push-pull design structure). At power on, P0 is configured as an input. |
| SCL | 13 | Serial clock bus. Connect to $V_{\text{DD(I2C_bus)}}$ through a pull-up resistor. |
| SDA | 14 | Serial data bus. Connect to $V_{\text{DD(I2C_bus)}}$ through a pull-up resistor. |
| $V_{\text{DD(I2C_bus)}}$ | 15 | Supply voltage of I ² C bus. |
| GND | 16 | Ground |

Maximum Ratings

| | |
|--|----------------|
| Power supply..... | -0.5V to +4.6V |
| Voltage on an I/O pin (Input / Output)..... | -0.5V to +4.0V |
| Input current..... | ±20mA |
| Output current on an I/O pin | ±50mA |
| Supply current..... | ±100mA |
| Ground supply current..... | ±100mA |
| Operation temperature..... | -40~85°C |
| Storage temperature | -65~150°C |
| Maximum junction temperature, T _j (max) | 125°C |
| ESD (HBM) | 2kV |

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Conditions

Table 2: Recommended operating conditions

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|-------------------------|-------------------------------------|------------|------|------|--------------------|------|
| V _{DD(IC-bus)} | I ² C-bus supply voltage | | 1.65 | - | 3.6 | V |
| V _{DD(P)} | GPIO port supply voltage | | 1.65 | - | 4 | V |
| V _{IN} | Input voltage on IO pins | | 0 | | 4 | V |
| V _{OUT} | Output Voltage | | 0 | | V _{DD(P)} | V |

Static Characteristics

$V_{DD(I2C_bus)} = 1.8\text{ V to }3.6\text{ V}$; $GND = 0\text{ V}$; Temp = $-40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$; unless otherwise specified.

Typical values are at Temp = $25\text{ }^{\circ}\text{C}$.

Table 3: Static characteristics

| Symbol | Parameter | Condition | Min. | Typ. ^[1] | Max. | Unit |
|--|---------------------------|--|---------------------------|---------------------|--------------------------------|---------------|
| Power supply | | | | | | |
| $I_{DD}^{[2]}$ | Supply current | $V_{DD(I2C_bus)} = 1.8\text{ to }3.6\text{ V}$; Standby mode V_I on SDA, ADDR and $\overline{\text{RESET}}$ = $V_{DD(I2C_bus)}$ or GND; V_I on P port = $V_{DD(P)}$ or GND; $I_O = 0\text{ mA}$; I/O = inputs; $f_{SCL} = 0\text{ kHz}$ | - | 1.2 | 1.5 | μA |
| | | $V_{DD(I2C_bus)} = 1.8\text{ to }3.6\text{ V}$; Active mode V_I on $\overline{\text{RESET}} = V_{DD(I2C_bus)}$; V_I on P port = $V_{DD(P)}$ or GND; $I_O = 0\text{ mA}$; I/O = inputs; $f_{SCL} = 400\text{ kHz}$, continuous register read | - | - | 300 | μA |
| I_{OFF} | Power off leakage current | | | - | 10 | μA |
| I_{IN} | Input leakage current | $0 \leq V_{IN} \leq V_{DD(I2C_bus)}$ | -10 | - | 10 | μA |
| V_{POR} | Power-on reset voltage | | - | - | 1.25 | V |
| Input SCL, input/output SDA | | | | | | |
| V_{IL} | Low level input voltage | | -0.5 | - | $\frac{0.3}{V_{DD(I2C_bus)}}$ | V |
| V_{IH} | High level input voltage | | 0.7 $V_{DD(I2C_bus)}$ | - | 3.6 | V |
| I_{OL} | Low level output current | $V_{OL} = 0.4\text{ V}$ | 20 | - | - | mA |
| I_L | Leakage current | $V_{IN} = V_{DD(I2C_bus)}$ or GND | -10 | - | 10 | μA |
| C_i | Input capacitance | $V_{IN} = GND$ | - | 5 | 10 | pF |
| Interrupt $\overline{\text{INT}}$ | | | | | | |
| I_{OL} | Low level output current | $V_{OL} = 0.4\text{ V}$ | 6 | | - | mA |
| C_o | Output capacitance | | | 2.1 | 10 | pF |
| Select inputs ADDR and $\overline{\text{RESET}}$ | | | | | | |
| V_{IL} | Low level input voltage | | -0.5 | - | $\frac{0.3}{V_{DD(I2C_bus)}}$ | V |
| V_{IH} | High level input voltage | | 0.7 $V_{DD(I2C_bus)}$ | - | 3.6 | V |
| I_L | Input leakage current | | -1 | | 1 | μA |
| C_i | Input capacitance | | | 2.4 | 10 | pF |

Static Characteristics Cont.

| Symbol | Parameter | Condition | Min. | Typ. ^[1] | Max. | Unit |
|----------------|-------------------------------|---|-----------------------|---------------------|------------------------|---------------|
| I/Os | | | | | | |
| V_{IL} | Low-level input voltage | P0 – P7 | -0.5 | - | $+0.3 \cdot V_{DD(P)}$ | V |
| V_{IH} | High-level input voltage | P0 – P7 | $0.7 \cdot V_{DD(P)}$ | - | 4.0 | V |
| V_{OH} | High-level output voltage | P port; $I_{OH} = -100 \mu\text{A}$; | | | | |
| | | $V_{DD(P)} = 1.8 \text{ V}$ | $V_{DD(P)} - 0.2$ | - | - | V |
| | | $V_{DD(P)} = 3.6 \text{ V}$ | $V_{DD(P)} - 0.2$ | - | - | V |
| | | $V_{DD(P)} = 4.0 \text{ V}$ | $V_{DD(P)} - 0.2$ | - | - | V |
| | | P port; $I_{OH} = -6 \text{ mA}$ | | | | |
| | | $V_{DD(P)} = 1.8 \text{ V}$ | $V_{DD(P)} - 0.2$ | - | - | V |
| | | $V_{DD(P)} = 3.6 \text{ V}$ | $V_{DD(P)} - 0.2$ | - | - | V |
| V_{OL} | Low-level output voltage | P port; $I_{OL} = 100 \mu\text{A}$; | | | | |
| | | $V_{DD(P)} = 1.8 \text{ V}$ | - | - | 0.2 | V |
| | | $V_{DD(P)} = 3.6 \text{ V}$ | - | - | 0.2 | V |
| | | $V_{DD(P)} = 4.0 \text{ V}$ | - | - | 0.2 | V |
| | | P port; $I_{OL} = 6 \text{ mA}$ | | | | |
| | | $V_{DD(P)} = 1.8 \text{ V}$ | - | - | 0.5 | V |
| | | $V_{DD(P)} = 3.6 \text{ V}$ | - | - | 0.45 | V |
| I_{OL} | Low-level output current | P0 – P7 | 6.0 | - | - | mA |
| I_{OH} | High-level output current | P0 – P7 | -6.0 | - | - | mA |
| $I_{IH}^{[3]}$ | High-level input current | P port; $V_I = V_{DD(P)}$; $V_{DD(P)} = 1.65 \text{ V to } 4.0 \text{ V}$ | -50 | - | 50 | μA |
| $I_{IL}^{[3]}$ | Low-level input current | P port; $V_I = \text{GND}$; $V_{DD(P)} = 1.65 \text{ V to } 4.0 \text{ V}$ | -50 | - | 50 | μA |
| $R_{pu(int)}$ | Internal pull-up resistance | Input/Output | - | 100 | - | k Ω |
| $R_{pd(int)}$ | Internal pull-down resistance | Input/Output | - | 100 | - | k Ω |

Note:
 [1] Includes all internal circuitry consumption from the $V_{DD(12C_bus)}$ supply. Does not include the I/O buffers, which are supplied by $V_{DD(P)}$ and are load dependent.
 [2] I_{IL} and I_{IH} specifications only apply when the outputs are configured with pull-down or pull-up resistors, respectively. Specification value assume $V_{IN} \leq V_{DD(P)}$

Dynamic Characteristics

Table 4: Dynamic characteristics

| Symbol | Parameter | Standard mode I ² C | | Fast mode I ² C | | Fast mode Plus I ² C | | Unit |
|------------------------------------|---|--------------------------------|------|----------------------------|-----|---------------------------------|------|------|
| | | Min | Max | Min | Max | Min | Max | |
| f _{SCL} | SCL clock frequency | 0 | 100 | 0 | 400 | 0 | 1000 | kHz |
| t _{BUF} | Bus free time between a STOP and START condition | 4.7 | - | 1.3 | - | 0.5 | - | μs |
| t _{HD;STA} | Hold time (repeated) START condition | 4.0 | - | 0.6 | - | 0.26 | - | μs |
| t _{SU;STA} | Set-up time for a repeated START condition | 4.7 | - | 0.6 | - | 0.26 | - | μs |
| t _{SU;STO} | Set-up time for STOP condition | 4.0 | - | 0.6 | - | 0.26 | - | μs |
| t _{VD;ACK} ^[1] | Data valid acknowledge time | - | 3.45 | - | 0.9 | - | 0.45 | μs |
| t _{HD;DAT} ^[2] | Data hold time | 0 | - | 0 | - | 0 | - | ns |
| t _{VD;DAT} | Data valid time | - | 3.45 | - | 0.9 | - | 0.45 | ns |
| t _{SU;DAT} | Data set-up time | 250 | - | 100 | - | 50 | - | ns |
| t _{LOW} | LOW period of the SCL clock | 4.7 | - | 1.3 | - | 0.5 | - | μs |
| t _{HIGH} | HIGH period of the SCL clock | 4.0 | - | 0.6 | - | 0.26 | - | μs |
| t _f | Fall time of both SDA and SCL signals | - | 300 | - | 300 | - | 120 | ns |
| t _r | Rise time of both SDA and SCL signals | - | 1000 | - | 300 | - | 120 | ns |
| t _{SP} | Pulse width of spikes that must be suppressed by the input filter | - | 50 | - | 50 | - | 50 | ns |
| Interrupt timing | | | | | | | | |
| t _{V(INT)} | Valid time on pin $\overline{\text{INT}}$ | - | 4 | - | 4 | - | 4 | μs |
| Reset timing | | | | | | | | |
| t _{w(rst)} | Reset pulse width | 150 | - | 150 | - | 150 | - | ns |
| t _{rst_glitch} | Reset recovery time ^[4] | 50 | 150 | 50 | 150 | 50 | 150 | ns |
| t _{rst} | Reset time | - | 150 | - | 150 | - | 150 | ns |

Note:

 [1]: t_{VD;ACK} = time for acknowledgement signal from SCL LOW to SDA (out) LOW.

 [2]: t_{VD;DAT} = minimum time for SDA data out to be valid following SCL LOW.

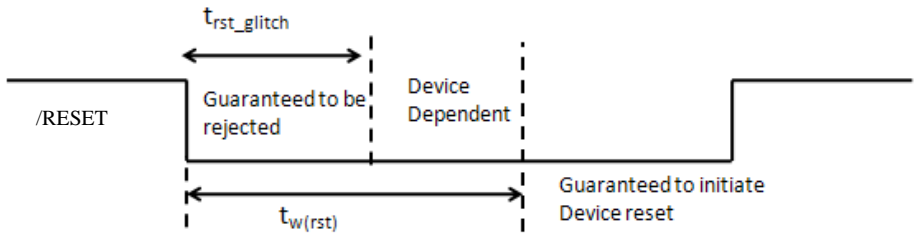


Fig 2: Reset Pulse Duration and Input Glitch Rejection Timing Diagram

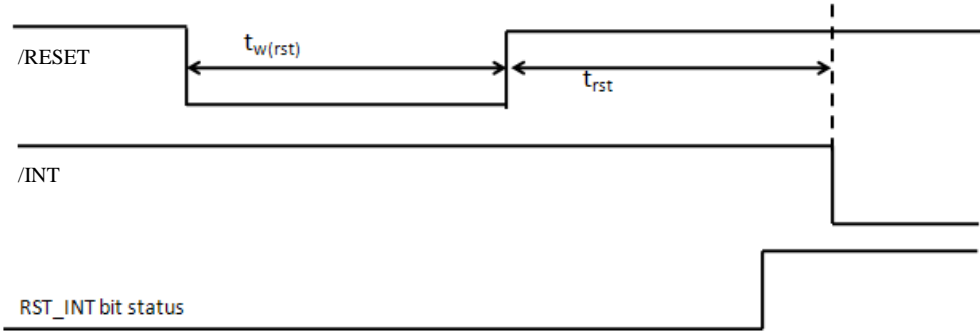


Fig 3: Reset Pulse Duration and Input Glitch Rejection Timing Diagram

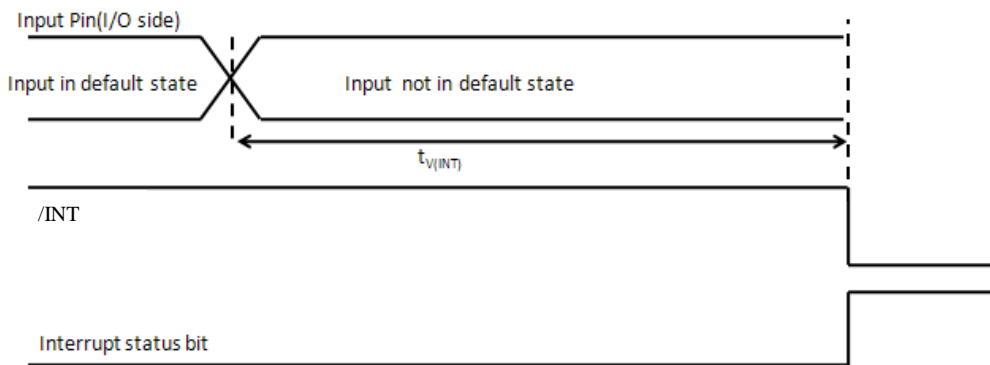


Fig 4: Time to \overline{INT} from Change in Input Default State

PI4IOE5V6408 Block Diagram

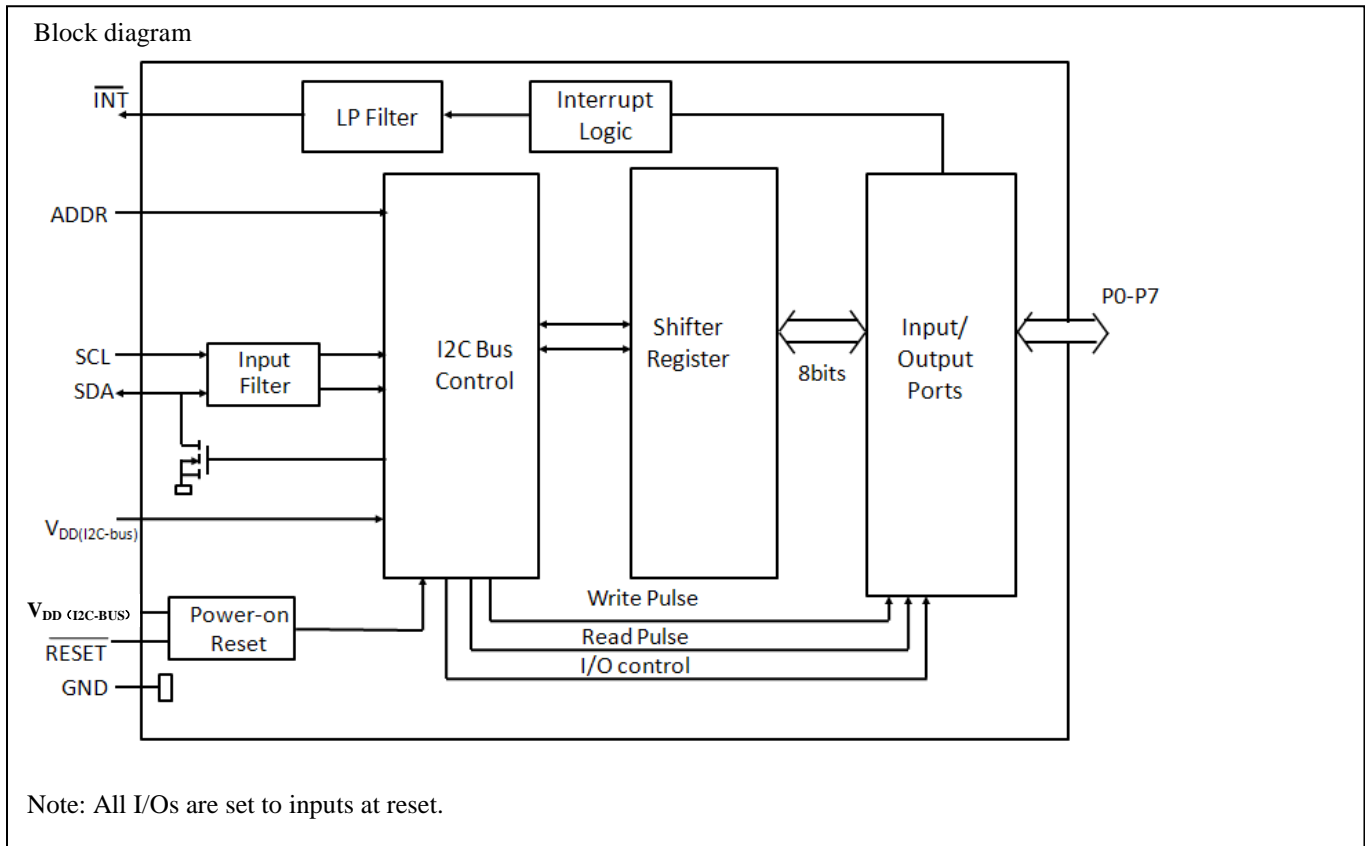


Fig 5: Block diagram

Functional Description

a. Device Address

The address of the device is shown below in Table 5. Setting ADDR pin to GND (0) results in B[3:1] bits set as 011, and setting ADDR pin to $V_{DD(I2C_{bus})}$ (1) results in B[3:1] bits set as 100.

Table 5: Device address

| ADDR | B7 (MSB) | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|------|------------|----|----|----|----|----|----|-------|
| 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | R / W |
| 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | R / W |

The last bit of the device address defines the operation to be performed. A logic 1 selects a read operation, while a logic 0 selects a write operation.

b. Register Map

Following the successful acknowledgment of the address byte, the bus master sends a command byte, which is stored in the Pointer Register in the PI4IOE5V6408. Five bits of this data byte state the operation (read or write) and the internal registers that will be affected. This register can be written or read through the I²C bus. The command byte is sent only during a write transmission.

Table 6: Register Map

| Pointer Register Bits | | | | | | | | Command byte (hexadecimal) | Register | Protocol | Power-up default |
|-----------------------|----|----|----|----|----|----|----|---|-----------------------|----------|---------------------|
| B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 01h | Device ID and Control | R/W | 1010 0010 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 03h | I/O Direction | R/W | 0000 0000 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 05h | Output State | R/W | 0000 0000 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 07h | Output High-impedance | R/W | 1111 1111 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 09h | Input Default State | R/W | 0000 0000 |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0Bh | Pull-up/down Enable | R/W | 1111 1111 |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0Dh | Pull-up/down Select | R/W | 0000 0000 |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0Fh | Input Status | R | xxxx xxxx |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 11h | Interrupt Mask | R/W | 0000 0000 |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 13h | Interrupt Status | R/W | xxxx xxxx |
| | | | | | | | | 02h, 04h, 06h, 08h, 0Ah, 0Ch, 0Eh, 10h, 12h | Reserved | R/W | |

c. Register Descriptions

i. Register 01h : Device ID and Control

The Device ID and Control register contains the manufacturer ID and firmware revision. The Control register indicates whether the device has been reset and the default values have been set.

- The Reset Interrupt is set B1 = 1 when the device is either reset by the RESET pin, a power on reset, or software reset.
- Reset Interrupt is then cleared after being read by the master.
- A software reset is issued when the master writes B0=1.
- When reading from B0, the value read will always be 0.

Table 7: Device ID and Control register (address 01h)

| Bit | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---------|----------------|----|----|-------------------|----|----|-----------------|----------------|
| Name | Manufacture ID | | | Firmware Revision | | | Reset interrupt | Software reset |
| Default | 1 | 0 | 1 | 0 | 0 | 0 | 1 | R / W |

ii. Register 03h : I/O Direction

The I/O Direction Register configures the direction of the I/O pins.

- If a bit in this register is set to 0, the corresponding port pin is enabled as an input
- If a bit in this register is set to 1, the corresponding port pin is enabled as an output.

Table 8: I/O Direction register (address 03h)

| Bit | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---------|----|----|----|----|----|----|----|----|
| Name | P7 | P6 | P5 | P4 | P3 | P2 | P1 | P0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

iii. Register 05h : Output Port Register

The Output Port Register sets the outgoing logic levels of the pins defined as outputs.

- When Bx is set to 0, Px = L; When Bx is set to 1, Px = H
- Bit values in this register have no effect on pins defined as inputs
- Reads from this register reflect the value that is in the flip-flop controlling the output selection, not the actual pin value.

Table 9: Output Port Register (address 05h)

| Bit | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---------|----|----|----|----|----|----|----|----|
| Name | P7 | P6 | P5 | P4 | P3 | P2 | P1 | P0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

iv. Register 07h : Output High-Impedance

The Output High-Impedance Register determines whether pins set as output are enabled or high-impedance

- When a bit in this register is set to 0, the corresponding GPIO-port output state follows register the output port register (05h).
- When a bit in this register is set to 1, the corresponding GPIO-port output is set to high-impedance.
- Bit values in this register have no effect on pins defined as inputs. In turn, reads from this register reflect the value that is in the flip-flop controlling the output selection, not the actual pin value.

Table 10: Output High-Impedance Register (address 07h)

| Bit | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---------|----|----|----|----|----|----|----|----|
| Name | P7 | P6 | P5 | P4 | P3 | P2 | P1 | P0 |
| Default | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

v. Register 09h : Input Default State

The Input Default State Register sets the default state of the GPIO-port input for generating interrupts.

- When a bit in this register is set to 0, the default for the corresponding input is set to LOW
- When a bit in this register is set to 1, the default for the corresponding input is set to HIGH
- Bit values in this register have no effect on pins defined as outputs. In turn, reads from this register reflect the value that is in the flip-flop controlling the default state, not the actual pin value.

Table 11. Input Default State Register (address 09h)

| Bit | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---------|----|----|----|----|----|----|----|----|
| Name | P7 | P6 | P5 | P4 | P3 | P2 | P1 | P0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

vi. Register 0bh : Pull-Up/-Down Enable

The Pull-up/-down Enable Register enables or disables the pull-up/down resistor on the GPIO-port as defined in the Pull-up/-down Select Register (0Dh).

- When a bit in this register is set to 0, the pull-up/down on the corresponding GPIO is disabled.
- When a bit in this register is set to 1, the pull-up/down on the corresponding GPIO is enabled.

Table 12. Pull-up/-down Enable Register (address 0Bh)

| Bit | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---------|----|----|----|----|----|----|----|----|
| Name | P7 | P6 | P5 | P4 | P3 | P2 | P1 | P0 |
| Default | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

vii. Register 0Dh : Pull-Up/-Down Select

The Pull-up/down Select Register allows the user to select either a pull-up or pull-down on the GPIO-port. This register only selects the pull-up/down resistor on the GPIO-port, while the enabling/disabling is controlled by the Pull-up/down Enable Register (0Bh).

- When a bit in this register is set to 0, the pull-down on the corresponding GPIO is selected.
- When a bit in this register is set to 1, the pull-up on the corresponding GPIO is selected.

Table 13. Pull-up/-down Select Register (address 0Dh)

| Bit | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---------|----|----|----|----|----|----|----|----|
| Name | P7 | P6 | P5 | P4 | P3 | P2 | P1 | P0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

viii. Register 0Fh : Input Status Register

The Input Status Register reflects the incoming logic levels of the GPIOs set as inputs.

- The default value, X, is determined by the externally applied logic level.
- It only acts on read operation. Attempted writes to this register have no effect.
- For GPIOs set as outputs this register will read LOW.

Table 14. Input Status Register (address 0Fh)

| Bit | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---------|----|----|----|----|----|----|----|----|
| Name | P7 | P6 | P5 | P4 | P3 | P2 | P1 | P0 |
| Default | X | X | X | X | X | X | X | X |

ix. Register 11h – Interrupt Mask Register

The Interrupt Mask Register controls the generation of an interrupt to the $\overline{\text{INT}}$ pin when the GPIO-port input state changes state.

- When a bit in this register is set to 0, an interrupt generated by the interrupt status register causes the $\overline{\text{INT}}$ pin to be asserted LOW.
- When a bit in this register is set to 1, the interrupt for the corresponding GPIO is disabled. The corresponding bit in the Interrupt Status Register (13h) will still be asserted.
- $\overline{\text{INT}}$ is not affected when GPIO-port is defined as outputs.

Table 15. Interrupt Mask Register (address 11h)

| Bit | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---------|----|----|----|----|----|----|----|----|
| Name | P7 | P6 | P5 | P4 | P3 | P2 | P1 | P0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

x. Register 13h – Interrupt Status Register

The Interrupt Status Register bit is asserted when the bit changes to a value opposite to the default value defined in the Input Default State Register (09h).

- This bit is cleared and the $\overline{\text{INT}}$ pin is de-asserted upon read of this register.
- The input must be asserted back to the default state before this bit is set again.
- If the GPIO-port pin is defined as an output, this bit is never set.

Table 16. Interrupt Status Register (address 13h)

| Bit | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---------|----|----|----|----|----|----|----|----|
| Name | P7 | P6 | P5 | P4 | P3 | P2 | P1 | P0 |
| Default | X | X | X | X | X | X | X | X |

d. I/O Port

When an I/O is configured as an input, the pull-up FET (Q1) and pull-down FET (Q2) are off, which creates a high-impedance input. If the I/O is configured as an output, Q1 or Q2 is enabled depending on the state of the Output Port Register. In this case, there are low impedance paths between the I/O pin and either $V_{DD(P)}$ or GND. The external voltage applied to this I/O pin should not exceed the recommended levels for proper operation. A pull-down FET series with pull-down resistor (Q3) is turned on at power-on to enable the pull-down resistor. Q3 and a pull-up FET series with pull-up resistor (Q4) are enabled accordingly to the Pull-up or Pull-down Select Register and the Pull-up or Pull-down Enable Register.

When the GPIO-port is set as an output the input buffers are disabled such that the bus is allowed to float.

e. Power-on Reset

When power is applied to $V_{DD(I2C_bus)}$, an internal power-on reset holds the PI4IOE5V6408 in a reset condition until $V_{DD(I2C_bus)}$ has reached V_{POR} . At that point, the reset condition is released and the PI4IOE5V6408 registers will initialize to their default states.

f. Reset Input ($\overline{\text{RESET}}$)

The $\overline{\text{RESET}}$ input can be asserted to initialize the system while keeping $V_{\text{DD(P)}}$ at its operating level. A reset can be accomplished by holding the $\overline{\text{RESET}}$ pin low for a minimum of t_w . The PI4IOE5V6408 registers are changed to their default state once $\overline{\text{RESET}}$ is low (0). Only when $\overline{\text{RESET}}$ is high (1), GPIO registers can be accessed by the I²C pin. This input requires a pull-up resistor to $V_{\text{DD(I2C_bus)}}$, if no active connection is used.

g. Software Reset

The PI4IOE5V6408 can be reset by the processor using an I²C write command to change bit 0 of register 01h to a 1. Immediately following this change, the PI4IOE5V6408 resets and all register values return to their default values. In this case, the software reset bit returns to 0 as soon as the reset sequence is completed.

h. Interrupt output ($\overline{\text{INT}}$)

The $\overline{\text{INT}}$ pin is a LOW-asserted open-drain output and requires an external pull-up resistor. The PI4IOE5V6408 signals an interrupt to the processor when an event occurs, removing the need for the processor to continuously poll the PI4IOE5V6408 registers.

Immediately after detecting a change at an input, the PI4IOE5V6408 writes the corresponding bit in the input interrupt status register (13h) and asserts the $\overline{\text{INT}}$ pin by pulling it LOW. The interrupt status register bit remains HIGH until the processor reads the register and clears the bit. If the input pin remains in the non-default state after the interrupt has been serviced, a new interrupt is not generated until after the input state has first returned to its default state and changed back to its non-default state. The PI4IOE5V6408 also contains an Input Status register (0Fh) used to verify the current status of the given input at the time when the interrupt is serviced by the processor. These two registers allow the processor to determine the following information about any input every time the register map is read:

- If the input state changed from the default state since the most recent register read; and
- The current state of the input pin.

The interrupt output $\overline{\text{INT}}$, once asserted, is held LOW until the interrupt is serviced by the processor. This means that the system uses level-sensitive interrupts. Interrupt signaling is asynchronous to the SCL signal.

I²C Read /Write Procedures

Figure 6 and Figure 7 illustrate compatible I²C write and read sequences. The PI4IOE5V6408 does not support burst read modes described in the I²C standard.

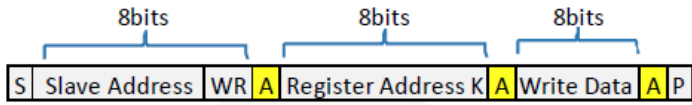
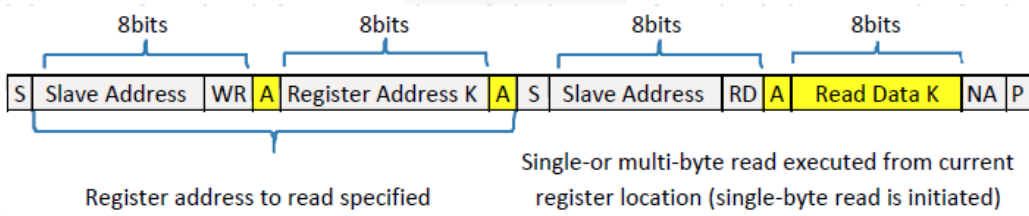


Fig 6. I²C Write Sequence



Note : if register is not specified , the master reads from the current register

Fig 7. I²C Read Sequence

| | | | | | |
|--|----------------------|---|-----------------------|----|----------------------------|
| | From Master to Slave | S | Start Condition | NA | NOT Acknowledge (SDA High) |
| | From Slave to Master | A | Acknowledge (SDA Low) | WR | Write=0 |

Application Design-In Information

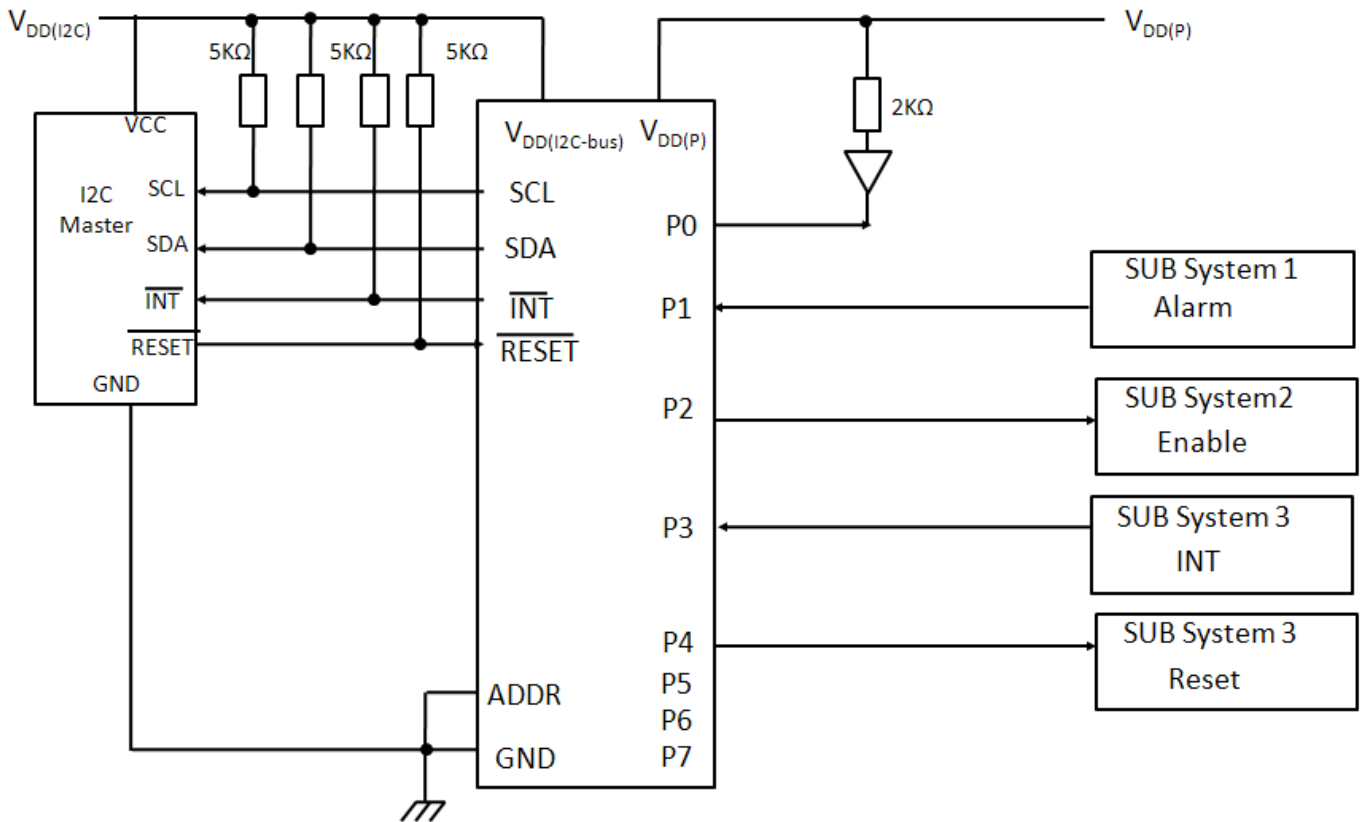


Fig 8. Typical Application

The SCL and SDA pins must be tied directly to $V_{DD(I2C-bus)}$ because if SCL and SDA are tied to an auxiliary power supply that could be powered on while $V_{DD(I2C-bus)}$ is powered off, then the supply current, I_{CC} , will increase as a result.

- A. Device address is configured as 86(h) or 87(h) for this example (depending on R/W bit).
- B. P0,P2,P4 are configured as outputs.
- C. P1,P3 are configured as inputs.
- D. P5,P6,P7 are not used.

Part Marking

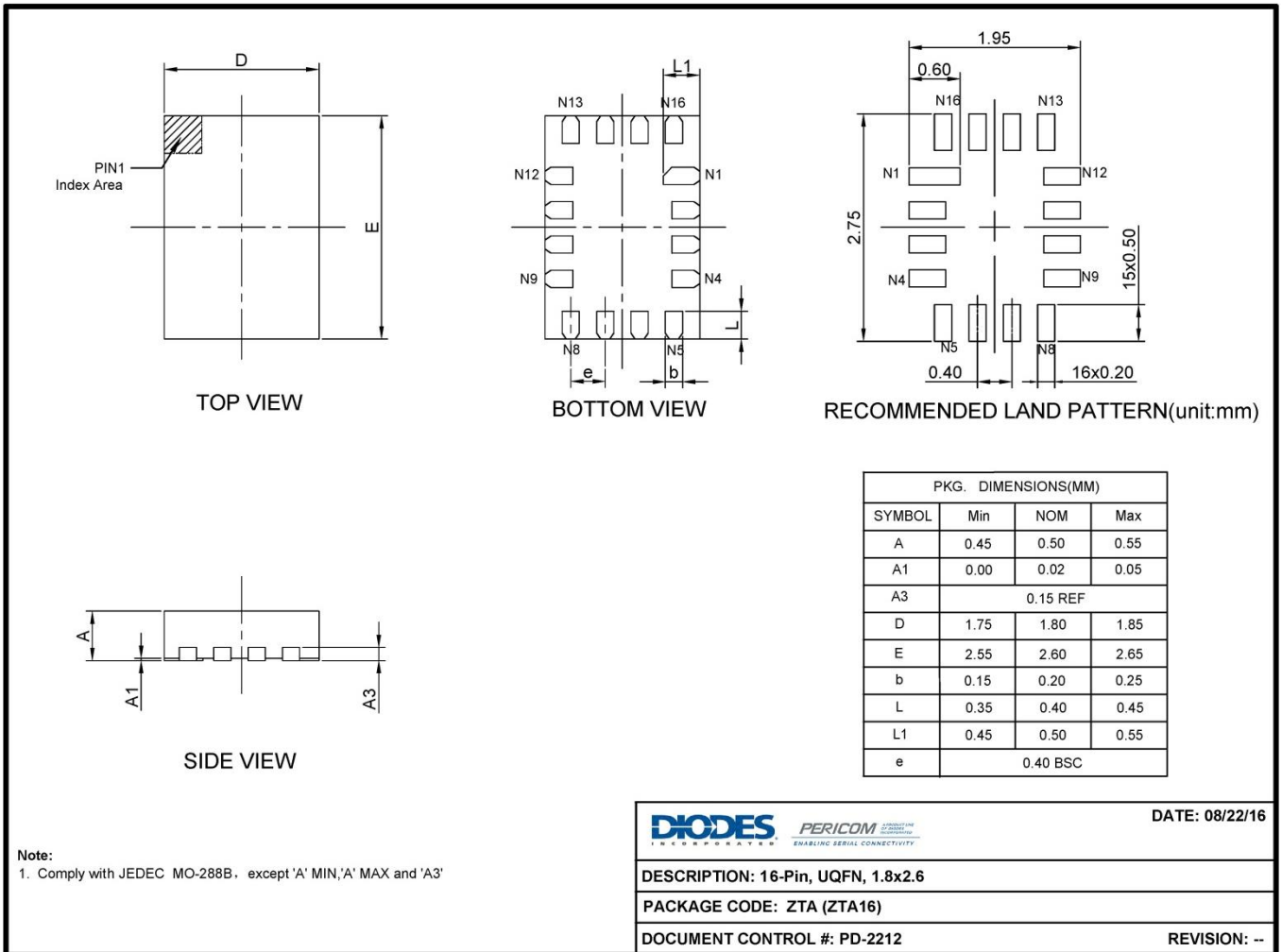
ZTA Packaging



Y: Year

W: Workweek

Packaging Mechanical
16-UQFN (ZTA)



16-0164

For latest package info.

please check: <http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/>

Ordering Information

| Part No. | Package Code | Package |
|-------------------|--------------|------------------------|
| PI4IOE5V6408ZTAEX | ZTA | 16-Pin, 1.8x2.6 (UQFN) |

- Notes:**
- EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3). Compliant. All applicable RoHS exemptions applied.
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