MCP6541/1R/1U/2/3/4

Push-Pull Output Sub-Microamp Comparators

Features

- Low Quiescent Current: 600 nA/comparator (typ.)
- Rail-to-Rail Input: V_{SS} - 0.3V to V_{DD} + 0.3V
- CMOS/TTL-Compatible Output
- Propagation Delay: 4 µs (typ., 100 mV Overdrive)
- Wide Supply Voltage Range: 1.6V to 5.5V
- Available in Single, Dual and Quad
- Single available in SOT-23-5, SC-70-5 * packages
- Chip Select ($\overline{CS}$) with MCP6543
- Low Switching Current
- Internal Hysteresis: 3.3 mV (typ.)
- Temperature Ranges:
  - Industrial: -40°C to +85°C
  - Extended: -40°C to +125°C

Typical Applications

- Laptop Computers
- Mobile Phones
- Metering Systems
- Hand-held Electronics
- RC Timers
- Alarm and Monitoring Circuits
- Windowed Comparators
- Multi-vibrators

Related Devices

- Open-Drain Output: MCP6546/7/8/9

Description

The Microchip Technology Inc. MCP6541/1R/1U/2/3/4 family of comparators is offered in single (MCP6541, MCP6541R, MCP6541U), single with Chip Select ($\overline{CS}$) (MCP6543), dual (MCP6542) and quad (MCP6544) configurations. The outputs are push-pull (CMOS/TTL-compatible) and are capable of driving heavy DC or capacitive loads.

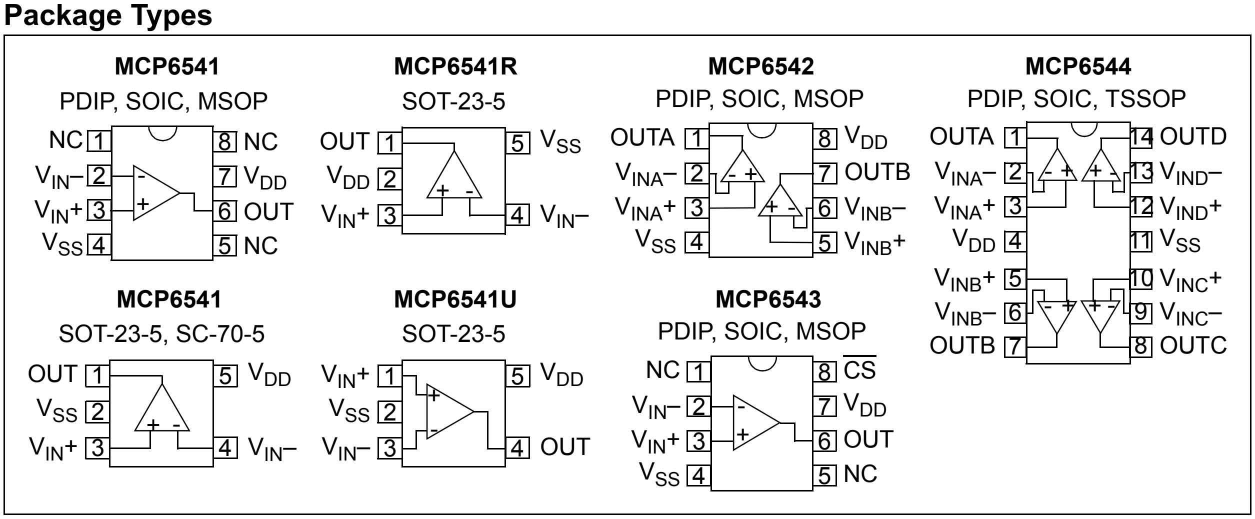
These comparators are optimized for low power, single-supply operation with greater than rail-to-rail input operation. The push-pull output of the MCP6541/1R/1U/2/3/4 family supports rail-to-rail output swing and interfaces with TTL/CMOS logic. The internal input hysteresis eliminates output switching due to internal input noise voltage, reducing current draw. The output limits supply current surges and dynamic power consumption while switching. This product family operates with a single-supply voltage as low as 1.6V and draws less than 1 µA/comparator of quiescent current.

The related MCP6546/7/8/9 family of comparators from Microchip has an open-drain output. Used with a pull-up resistor, these devices can be used as level-shifters for any desired voltage up to 10V and in wired-OR logic.

* SC-70-5 E-Temp parts not available at this release of the data sheet.

MCP6541U SOT-23-5 is E-Temp only.

Package Types



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

V_{DD} - V_{SS} 7.0V
Current at Analog Input Pin (V_{IN}+, V_{IN}-........................±2 mA
Analog Input (V_{IN}) †† .... V_{SS} - 1.0V to V_{DD} + 1.0V
All other Inputs and Outputs........... V_{SS} - 0.3V to V_{DD} + 0.3V
Difference Input voltage .... $|V_{DD} - V_{SS}|$
Output Short-Circuit Current ....continuous
Current at Input Pins ....±2 mA
Current at Output and Supply Pins ....±30 mA
Storage temperature ....-65°C to +150°C
Maximum Junction Temperature (T_J).......................... +150°C
ESD protection on all pins (HBM;MM) ....4 kV; 400V

† Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

†† See **Section 4.1.2 "Input Voltage and Current Limits"**

DC CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, V_{DD} = +1.6V to +5.5V, V_{SS} = GND, T_A = +25°C, V_{IN}+ = V_{DD}/2, V_{IN-} = V_{SS}, and R_L = 100 kΩ to V_{DD}/2 (Refer to Figure 1-3).

Parameters	Sym	Min	Typ	Max	Units	Conditions
Power Supply						
Supply Voltage	V_{DD}	1.6	—	5.5	V	
Quiescent Current per comparator	I_Q	0.3	0.6	1.0	µA	I_{OUT} = 0
Input						
Input Voltage Range	V_{CMR}	V_{SS}–0.3	—	V_{DD}+0.3	V	
Common Mode Rejection Ratio	CMRR	55	70	—	dB	V_{DD} = 5V, V_{CM} = -0.3V to 5.3V
Common Mode Rejection Ratio	CMRR	50	65	—	dB	V_{DD} = 5V, V_{CM} = 2.5V to 5.3V
Common Mode Rejection Ratio	CMRR	55	70	—	dB	V_{DD} = 5V, V_{CM} = -0.3V to 2.5V
Power Supply Rejection Ratio	PSRR	63	80	—	dB	V_{CM} = V_{SS}
Input Offset Voltage	V_{OS}	-7.0	±1.5	+7.0	mV	V_{CM} = V_{SS} **(Note 1)**
Drift with Temperature	$\Delta V_{OS}/\Delta T_A$	—	±3	—	µV/°C	T_A = -40°C to +125°C, V_{CM} = V_{SS}
Input Hysteresis Voltage	V_{HYST}	1.5	3.3	6.5	mV	V_{CM} = V_{SS} **(Note 1)**
Linear Temp. Co. **(Note 2)**	TC_1	—	6.7	—	µV/°C	T_A = -40°C to +125°C, V_{CM} = V_{SS}
Quadratic Temp. Co. **(Note 2)**	TC_2	—	-0.035	—	µV/°C²	T_A = -40°C to +125°C, V_{CM} = V_{SS}
Input Bias Current	I_B	—	1	—	pA	V_{CM} = V_{SS}
At Temperature (I-Temp parts)	I_B	—	25	100	pA	T_A = +85°C, V_{CM} = V_{SS} **(Note 3)**
At Temperature (E-Temp parts)	I_B	—	1200	5000	pA	T_A = +125°C, V_{CM} = V_{SS} **(Note 3)**
Input Offset Current	I_{OS}	—	±1	—	pA	V_{CM} = V_{SS}
Common Mode Input Impedance	Z_{CM}	—	10^{13}‖4	—	Ω‖pF	
Differential Input Impedance	Z_{DIFF}	—	10^{13}‖2	—	Ω‖pF	

Note 1: The input offset voltage is the center (average) of the input-referred trip points. The input hysteresis is the difference between the input-referred trip points.
2: V_{HYST} at different temperatures is estimated using $V_{HYST}(T_A) = V_{HYST} + (T_A - 25°C)\,TC_1 + (T_A - 25°C)^2\,TC_2$.
3: Input bias current at temperature is not tested for SC-70-5 package.
4: Limit the output current to Absolute Maximum Rating of 30 mA.

DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise indicated, V_{DD} = +1.6V to +5.5V, V_{SS} = GND, T_A = +25°C, $V_{IN}+$ = $V_{DD}/2$, $V_{IN}-$ = V_{SS}, and R_L = 100 kΩ to $V_{DD}/2$ (Refer to Figure 1-3).

Parameters	Sym	Min	Typ	Max	Units	Conditions
Push-Pull Output						
High-Level Output Voltage	V_{OH}	V_{DD}–0.2	—	—	V	I_{OUT} = -2 mA, V_{DD} = 5V
Low-Level Output Voltage	V_{OL}	—	—	V_{SS}+0.2	V	I_{OUT} = 2 mA, V_{DD} = 5V
Short-Circuit Current	I_{SC}	—	-2.5, +1.5	—	mA	V_{DD} = 1.6V (**Note 4**)
	I_{SC}	—	±30	—	mA	V_{DD} = 5.5V (**Note 4**)

Note 1: The input offset voltage is the center (average) of the input-referred trip points. The input hysteresis is the difference between the input-referred trip points.

2: V_{HYST} at different temperatures is estimated using $V_{HYST}(T_A) = V_{HYST} + (T_A - 25°C)\,TC_1 + (T_A - 25°C)^2\,TC_2$.

3: Input bias current at temperature is not tested for SC-70-5 package.

4: Limit the output current to Absolute Maximum Rating of 30 mA.

AC CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, V_{DD} = +1.6V to +5.5V, V_{SS} = GND, T_A = +25°C, $V_{IN}+$ = $V_{DD}/2$, Step = 200 mV, Overdrive = 100 mV, and C_L = 36 pF (Refer to Figure 1-2 and Figure 1-3).

Parameters	Sym	Min	Typ	Max	Units	Conditions
Rise Time	t_R	—	0.85	—	µs	
Fall Time	t_F	—	0.85	—	µs	
Propagation Delay (High-to-Low)	t_{PHL}	—	4	8	µs	
Propagation Delay (Low-to-High)	t_{PLH}	—	4	8	µs	
Propagation Delay Skew	t_{PDS}	—	±0.2	—	µs	**(Note 1)**
Maximum Toggle Frequency	f_{MAX}	—	160	—	kHz	V_{DD} = 1.6V
	f_{MAX}	—	120	—	kHz	V_{DD} = 5.5V
Input Noise Voltage	E_{ni}	—	200	—	μV_{P-P}	10 Hz to 100 kHz

Note 1: Propagation Delay Skew is defined as: $t_{PDS} = t_{PLH} - t_{PHL}$.

MCP6543 CHIP SELECT ($\overline{CS}$) CHARACTERISTICS

Parameters	Sym	Min	Typ	Max	Units	Conditions
Electrical Specifications: Unless otherwise indicated, V_{DD} = +1.6V to +5.5V, V_{SS} = GND, T_A = +25°C, $V_{IN}+$ = $V_{DD}/2$, $V_{IN}–$ = V_{SS}, and C_L= 36 pF (Refer to Figures 1-1 and 1-3).						
$\overline{CS}$ Low Specifications						
$\overline{CS}$ Logic Threshold, Low	V_{IL}	V_{SS}	—	0.2 V_{DD}	V	
$\overline{CS}$ Input Current, Low	I_{CSL}	—	5.0	—	pA	$\overline{CS}$ = V_{SS}
$\overline{CS}$ High Specifications						
$\overline{CS}$ Logic Threshold, High	V_{IH}	0.8 V_{DD}	—	V_{DD}	V	
$\overline{CS}$ Input Current, High	I_{CSH}	—	1	—	pA	$\overline{CS}$ = V_{DD}
$\overline{CS}$ Input High, V_{DD} Current	I_{DD}	—	18	—	pA	$\overline{CS}$ = V_{DD}
$\overline{CS}$ Input High, GND Current	I_{SS}	—	–20	—	pA	$\overline{CS}$ = V_{DD}
Comparator Output Leakage	$I_{O(LEAK)}$	—	1	—	pA	V_{OUT} = V_{DD}, $\overline{CS}$ = V_{DD}
$\overline{CS}$ Dynamic Specifications						
$\overline{CS}$ Low to Comparator Output Low Turn-on Time	t_{ON}	—	2	50	ms	$\overline{CS}$ = 0.2 V_{DD} to V_{OUT} = $V_{DD}/2$, $V_{IN}–$ = V_{DD}
$\overline{CS}$ High to Comparator Output High Z Turn-off Time	t_{OFF}	—	10	—	µs	$\overline{CS}$ = 0.8 V_{DD} to V_{OUT} = $V_{DD}/2$, $V_{IN}–$ = V_{DD}
$\overline{CS}$ Hysteresis	V_{CS_HYST}	—	0.6	—	V	V_{DD} = 5V

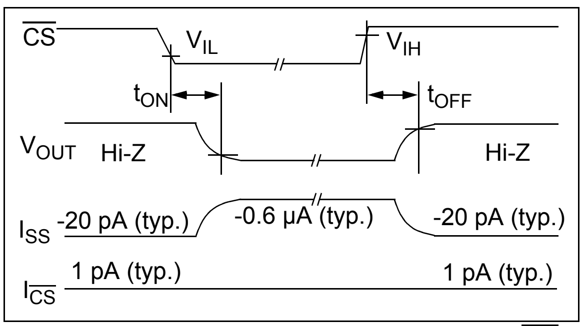


FIGURE 1-1: *Timing Diagram for the $\overline{CS}$ Pin on the MCP6543.*

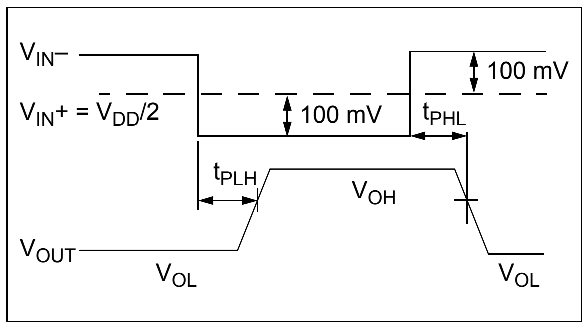


FIGURE 1-2: *Propagation Delay Timing Diagram.*

TEMPERATURE CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, V_{DD} = +1.6V to +5.5V and V_{SS} = GND.						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+85	°C	
Operating Temperature Range	T_A	-40	—	+125	°C	**Note**
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 5L-SC-70	θ_{JA}	—	331	—	°C/W	
Thermal Resistance, 5L-SOT-23	θ_{JA}	—	256	—	°C/W	
Thermal Resistance, 8L-PDIP	θ_{JA}	—	85	—	°C/W	
Thermal Resistance, 8L-SOIC	θ_{JA}	—	163	—	°C/W	
Thermal Resistance, 8L-MSOP	θ_{JA}	—	206	—	°C/W	
Thermal Resistance, 14L-PDIP	θ_{JA}	—	70	—	°C/W	
Thermal Resistance, 14L-SOIC	θ_{JA}	—	120	—	°C/W	
Thermal Resistance, 14L-TSSOP	θ_{JA}	—	100	—	°C/W	

Note: The MCP6541/1R/1U/2/3/4 I-Temp parts operate over this extended temperature range, but with reduced performance. In any case, the Junction Temperature (T_J) must not exceed the Absolute Maximum specification of +150°C.

1.1 Test Circuit Configuration

This test circuit configuration is used to determine the AC and DC specifications.

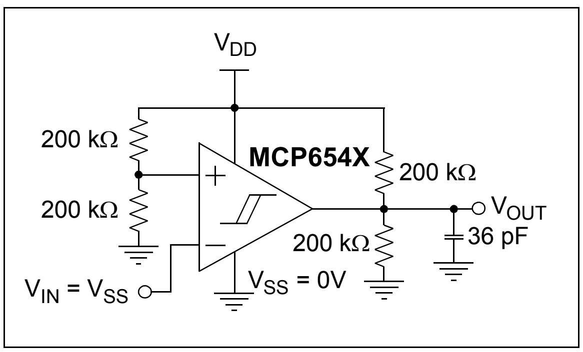


FIGURE 1-3: *AC and DC Test Circuit for the Push-Pull Output Comparators.*

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, V_{DD} = +1.6V to +5.5V, V_{SS} = GND, T_A = +25°C, $V_{IN}+$ = $V_{DD}/2$, V_{IN-} = GND, R_L = 100 kΩ to $V_{DD}/2$, and C_L = 36 pF.

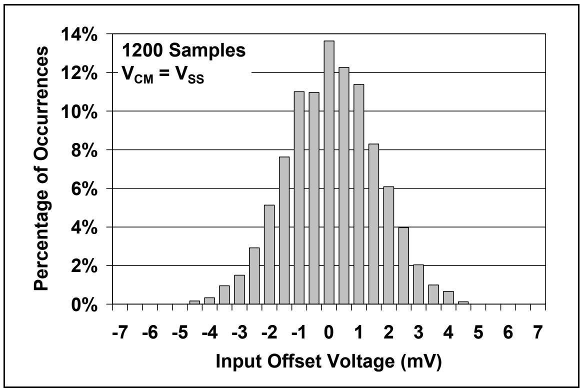


FIGURE 2-1: *Input Offset Voltage at $V_{CM} = V_{SS}$.*

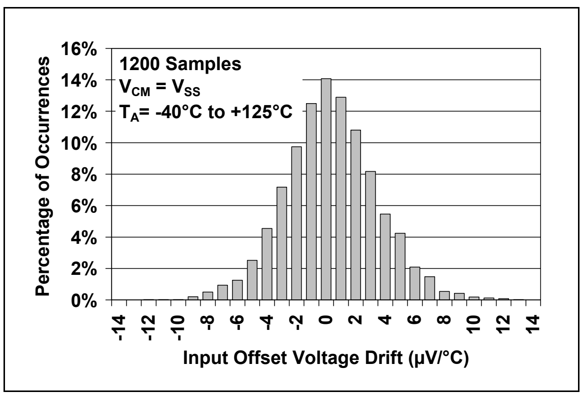


FIGURE 2-2: *Input Offset Voltage Drift at $V_{CM} = V_{SS}$.*

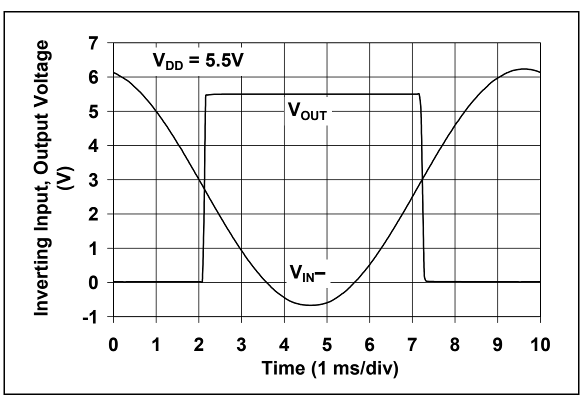


FIGURE 2-3: *The MCP6541/1R/1U/2/3/4 comparators show no phase reversal.*

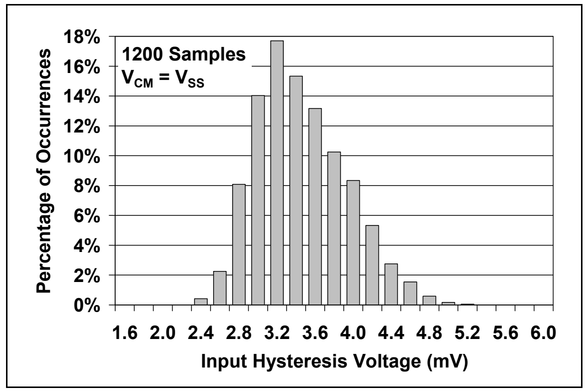


FIGURE 2-4: *Input Hysteresis Voltage at $V_{CM} = V_{SS}$.*

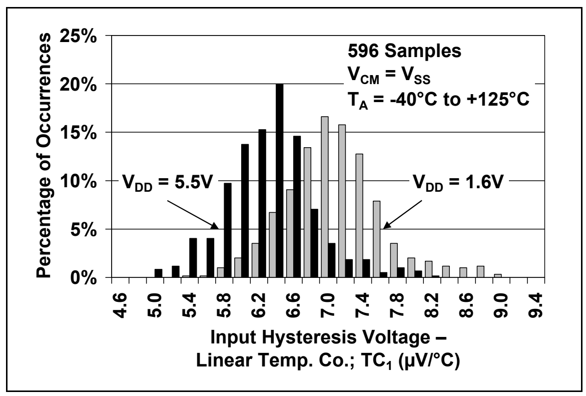


FIGURE 2-5: *Input Hysteresis Voltage Linear Temp. Co. (TC_1) at $V_{CM} = V_{SS}$.*

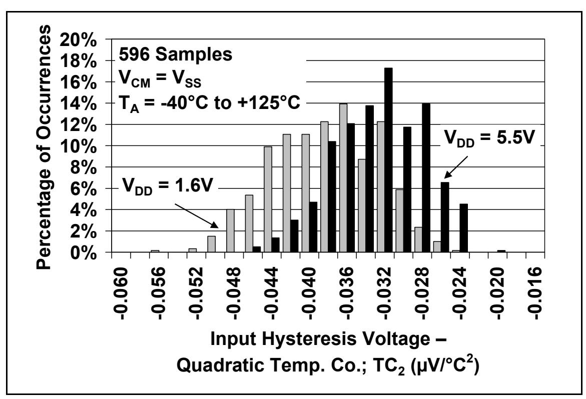


FIGURE 2-6: *Input Hysteresis Voltage Quadratic Temp. Co. (TC_2) at $V_{CM} = V_{SS}$.*

Note: Unless otherwise indicated, V_{DD} = +1.6V to +5.5V, V_{SS} = GND, T_A = 25°C, V_{IN}+ = V_{DD}/2, V_{IN}– = GND, R_L = 100 kΩ to V_{DD}/2, and C_L = 36 pF.

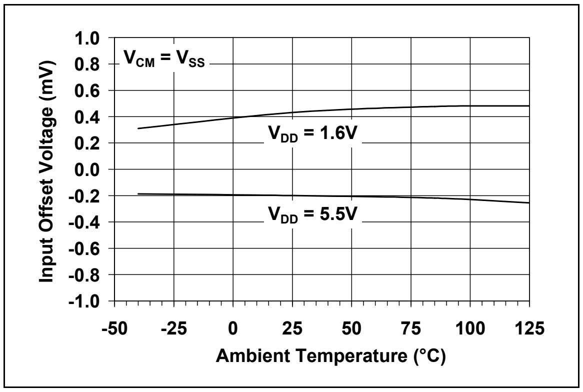


FIGURE 2-7: *Input Offset Voltage vs. Ambient Temperature at V_{CM} = V_{SS}.*

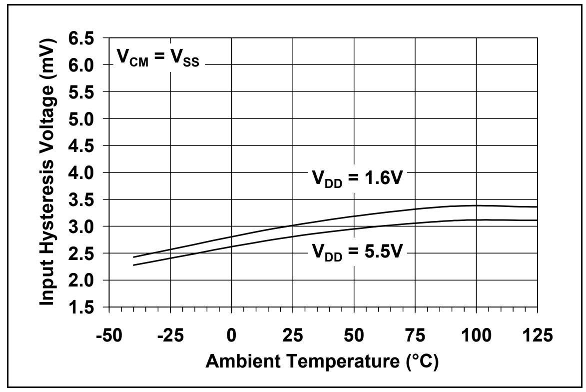


FIGURE 2-10: *Input Hysteresis Voltage vs. Ambient Temperature at V_{CM} = V_{SS}.*

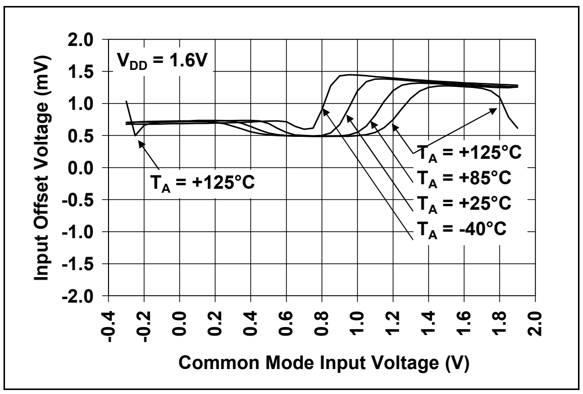


FIGURE 2-8: *Input Offset Voltage vs. Common Mode Input Voltage at V_{DD} = 1.6V.*

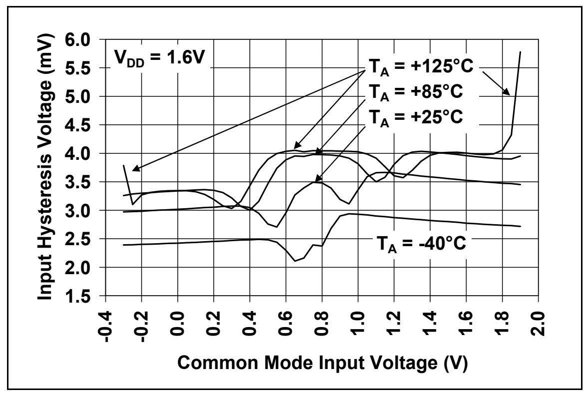


FIGURE 2-11: *Input Hysteresis Voltage vs. Common Mode Input Voltage at V_{DD} = 1.6V.*

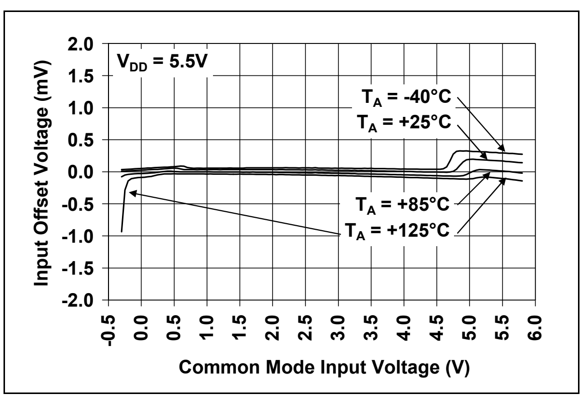


FIGURE 2-9: *Input Offset Voltage vs. Common Mode Input Voltage at V_{DD} = 5.5V.*

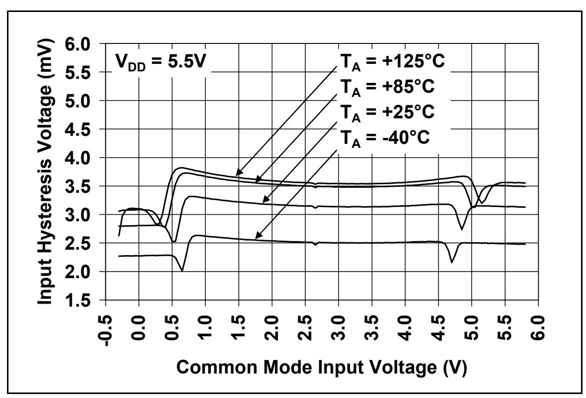


FIGURE 2-12: *Input Hysteresis Voltage vs. Common Mode Input Voltage at V_{DD} = 5.5V.*

Note: Unless otherwise indicated, V_{DD} = +1.6V to +5.5V, V_{SS} = GND, T_A = 25°C, $V_{IN}+ = V_{DD}/2$, $V_{IN}–$ = GND, R_L = 100 kΩ to $V_{DD}/2$, and C_L = 36 pF.

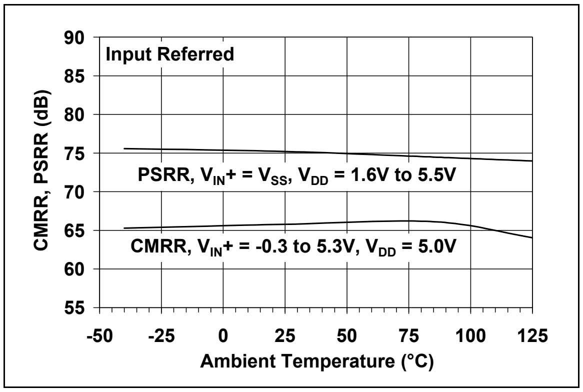


FIGURE 2-13: *CMRR,PSRR vs. Ambient Temperature.*

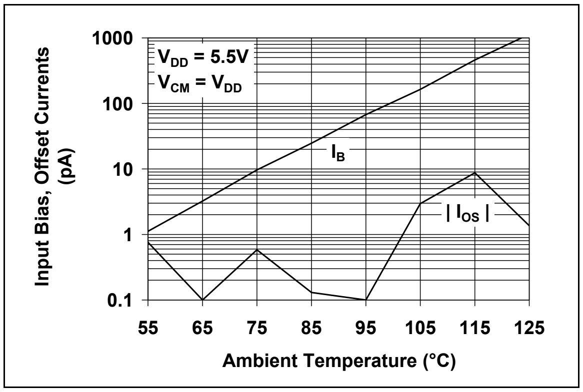


FIGURE 2-14: *Input Bias Current, Input Offset Current vs. Ambient Temperature.*

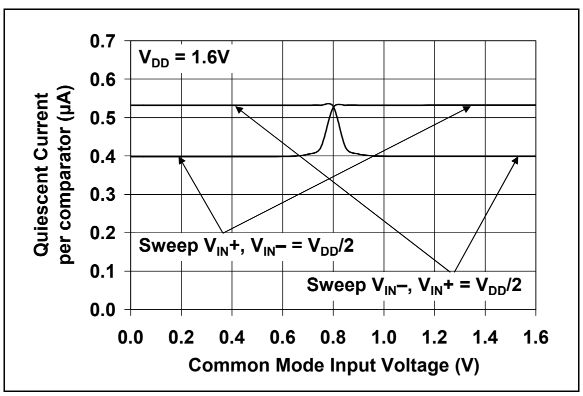


FIGURE 2-15: *Quiescent Current vs. Common Mode Input Voltage at V_{DD} = 1.6V.*

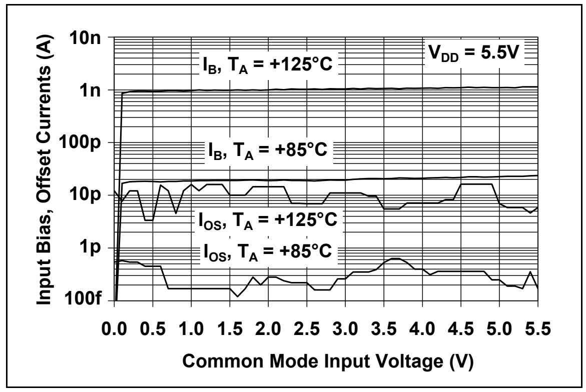


FIGURE 2-16: *Input Bias Current, Input Offset Current vs. Common Mode Input Voltage.*

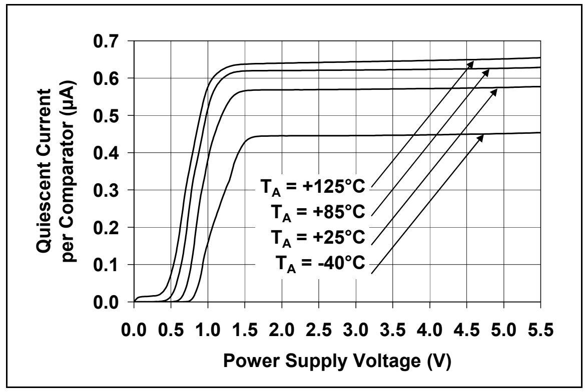


FIGURE 2-17: *Quiescent Current vs. Power Supply Voltage.*

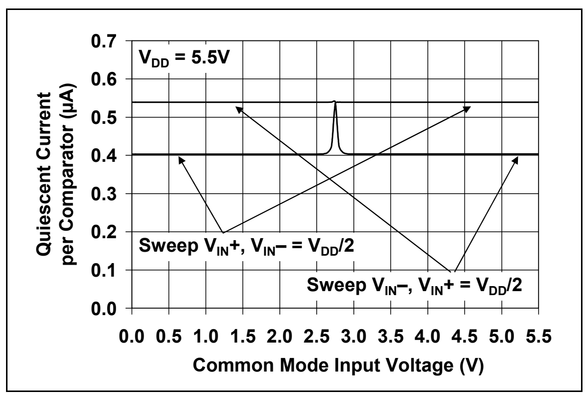


FIGURE 2-18: *Quiescent Current vs. Common Mode Input Voltage at V_{DD} = 5.5V.*

Note: Unless otherwise indicated, V_{DD} = +1.6V to +5.5V, V_{SS} = GND, T_A = 25°C, V_{IN}+ = V_{DD}/2, V_{IN}– = GND, R_L = 100 kΩ to V_{DD}/2, and C_L = 36 pF.

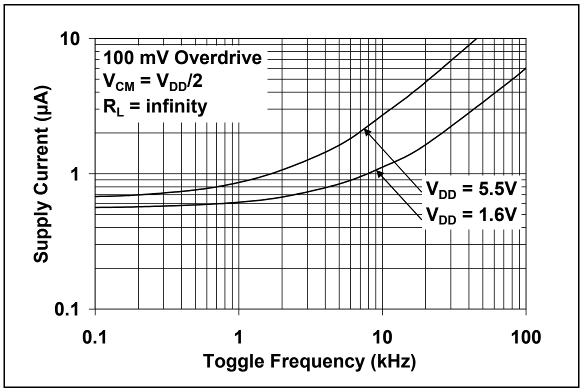


FIGURE 2-19: Supply Current vs. Toggle Frequency.

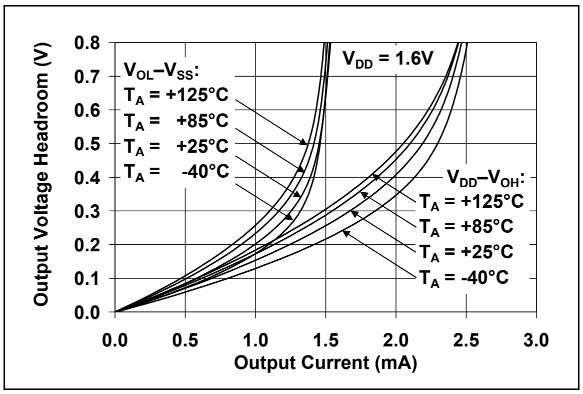


FIGURE 2-20: Output Voltage Headroom vs. Output Current at V_{DD} = 1.6V.

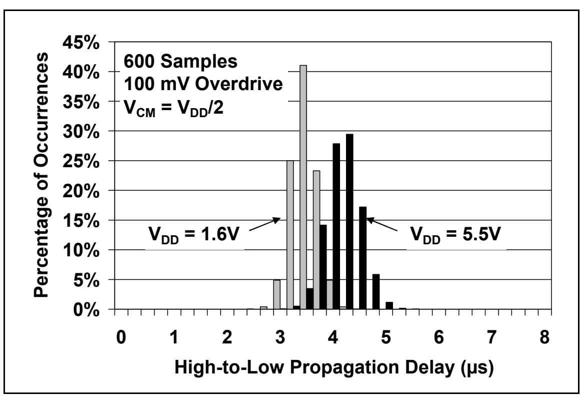


FIGURE 2-21: High-to-Low Propagation Delay.

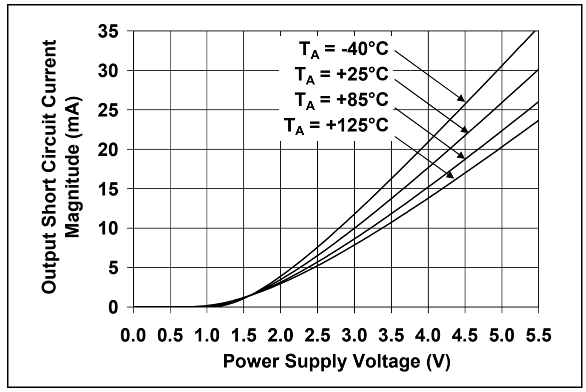


FIGURE 2-22: Output Short Circuit Current Magnitude vs. Power Supply Voltage.

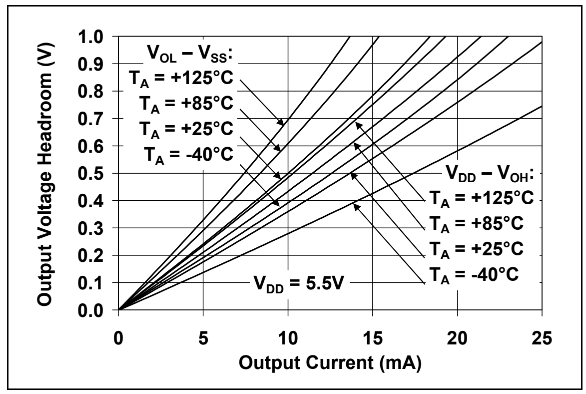


FIGURE 2-23: Output Voltage Headroom vs. Output Current at V_{DD} = 5.5V.

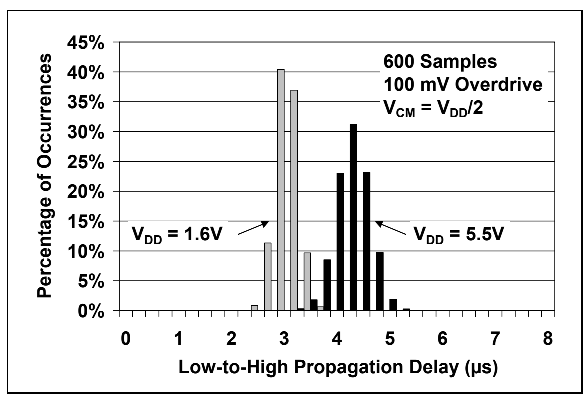


FIGURE 2-24: Low-to-High Propagation Delay.

Note: Unless otherwise indicated, V_{DD} = +1.6V to +5.5V, V_{SS} = GND, T_A = 25°C, $V_{IN}+ = V_{DD}/2$, $V_{IN}-$ = GND, R_L = 100 kΩ to $V_{DD}/2$, and C_L = 36 pF.

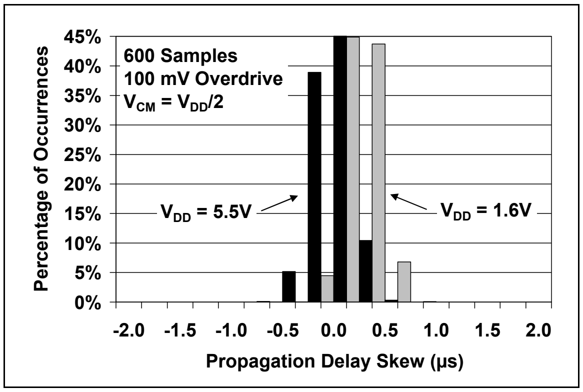


FIGURE 2-25: *Propagation Delay Skew.*

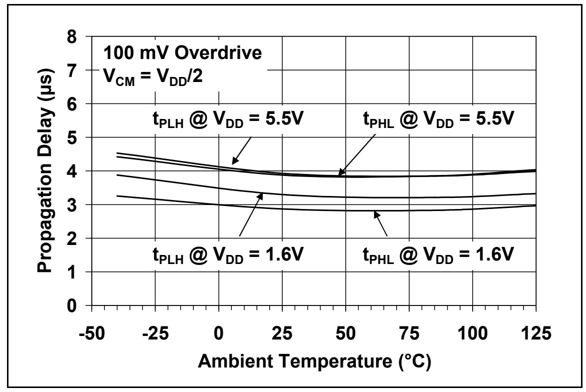


FIGURE 2-28: *Propagation Delay vs. Ambient Temperature.*

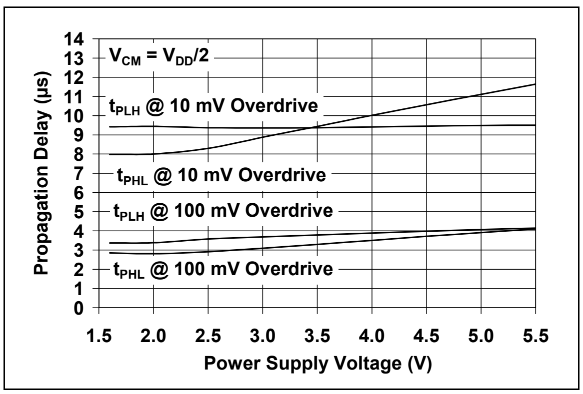


FIGURE 2-26: *Propagation Delay vs. Power Supply Voltage.*

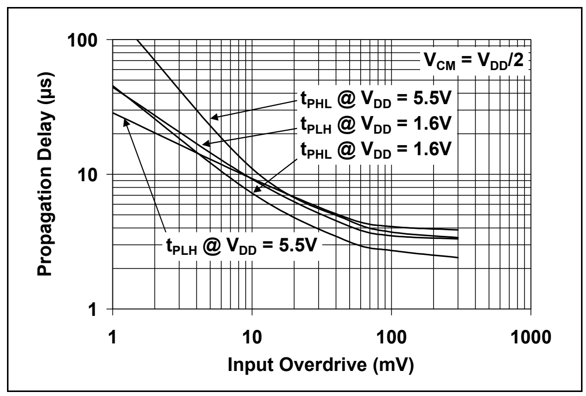


FIGURE 2-29: *Propagation Delay vs. Input Overdrive.*

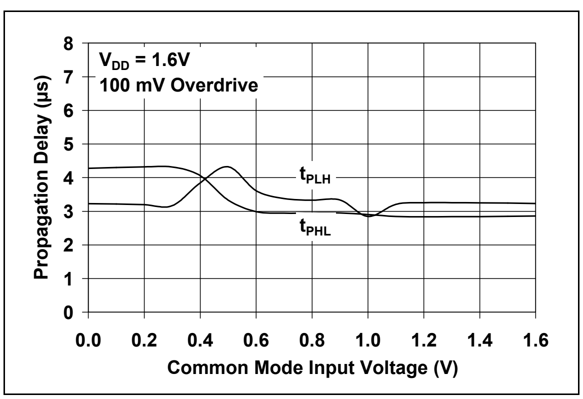


FIGURE 2-27: *Propagation Delay vs. Common Mode Input Voltage at V_{DD} = 1.6V.*

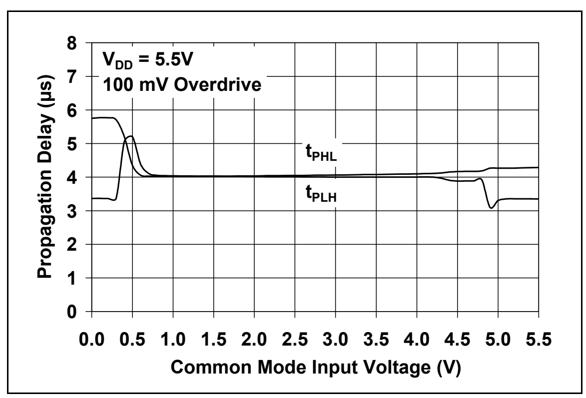


FIGURE 2-30: *Propagation Delay vs. Common Mode Input Voltage at V_{DD} = 5.5V.*

Note: Unless otherwise indicated, V_{DD} = +1.6V to +5.5V, V_{SS} = GND, T_A = 25°C, V_{IN}+ = V_{DD}/2, V_{IN}– = GND, R_L = 100 kΩ to V_{DD}/2, and C_L = 36 pF.

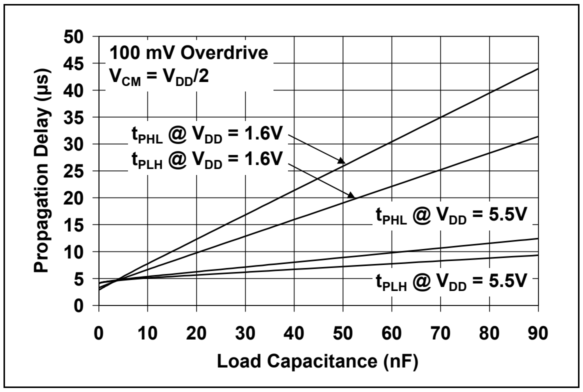


FIGURE 2-31: *Propagation Delay vs. Load Capacitance.*

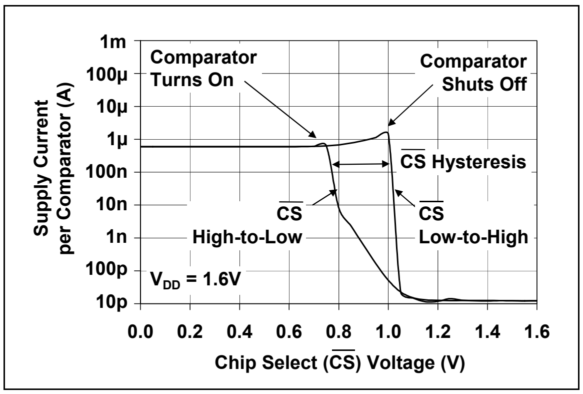


FIGURE 2-32: *Supply Current (shoot through current) vs. Chip Select ($\overline{CS}$) Voltage at V_{DD} = 1.6V (MCP6543 only).*

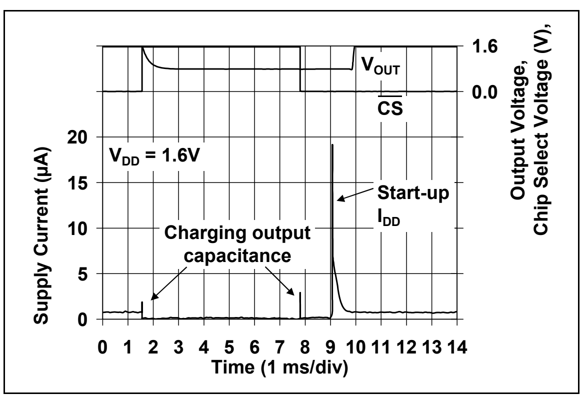


FIGURE 2-33: *Supply Current (charging current) vs. Chip Select ($\overline{CS}$) pulse at V_{DD} = 1.6V (MCP6543 only).*

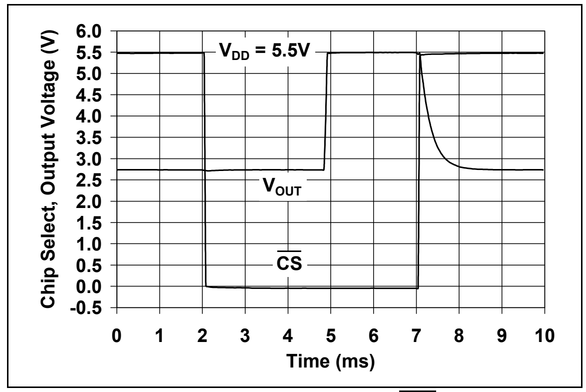


FIGURE 2-34: *Chip Select ($\overline{CS}$) Step Response (MCP6543 only).*

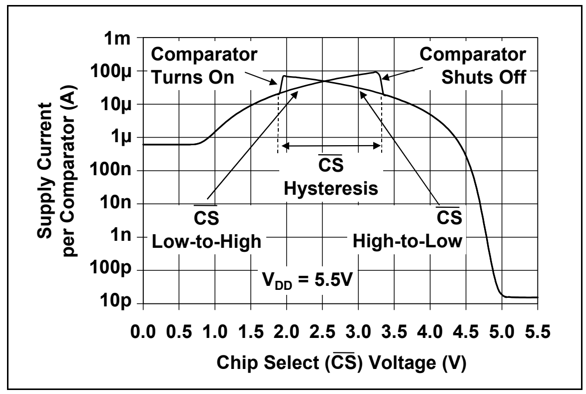


FIGURE 2-35: *Supply Current (shoot through current) vs. Chip Select ($\overline{CS}$) Voltage at V_{DD} = 5.5V (MCP6543 only).*

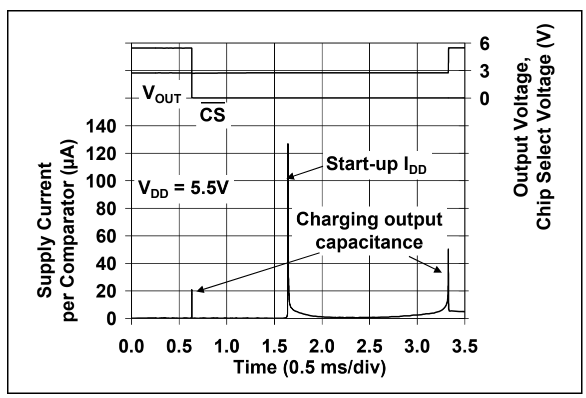


FIGURE 2-36: *Supply Current (charging current) vs. Chip Select ($\overline{CS}$) pulse at V_{DD} = 5.5V (MCP6543 only).*

Note: Unless otherwise indicated, V_{DD} = +1.6V to +5.5V, V_{SS} = GND, T_A = 25°C, $V_{IN}+ = V_{DD}/2$, $V_{IN}–$ = GND, R_L = 100 kΩ to $V_{DD}/2$, and C_L = 36 pF.

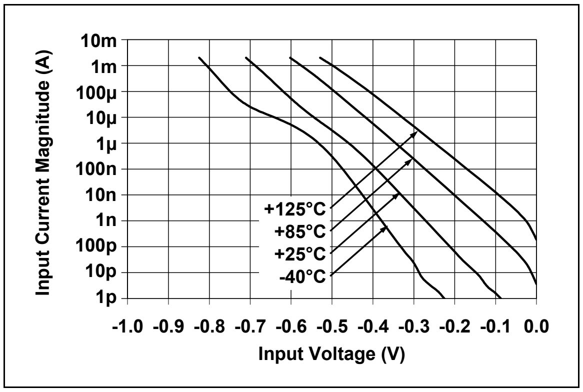


FIGURE 2-37: *Input Bias Current vs. Input Voltage.*

3.0 PIN DESCRIPTIONS

Descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

MCP6541 PDIP, SOIC, MSOP	**MCP6541** SOT-23-5, SC-70-5	**MCP6541R**	**MCP6541U**	**MCP6542**	**MCP6543**	**MCP6544**	**Symbol**	**Description**
6	1	1	4	1	6	1	OUT, OUTA	Digital Output (comparator A)
2	4	4	3	2	2	2	V_{IN}–, V_{INA}–	Inverting Input (comparator A)
3	3	3	1	3	3	3	V_{IN}+, V_{INA}+	Non-inverting Input (comparator A)
7	5	2	5	8	7	4	V_{DD}	Positive Power Supply
—	—	—	—	5	—	5	V_{INB}+	Non-inverting Input (comparator B)
—	—	—	—	6	—	6	V_{INB}–	Inverting Input (comparator B)
—	—	—	—	7	—	7	OUTB	Digital Output (comparator B)
—	—	—	—	—	—	8	OUTC	Digital Output (comparator C)
—	—	—	—	—	—	9	V_{INC}–	Inverting Input (comparator C)
—	—	—	—	—	—	10	V_{INC}+	Non-inverting Input (comparator C)
4	2	5	2	4	4	11	V_{SS}	Negative Power Supply
—	—	—	—	—	—	12	V_{IND}+	Non-inverting Input (comparator D)
—	—	—	—	—	—	13	V_{IND}–	Inverting Input (comparator D)
—	—	—	—	—	—	14	OUTD	Digital Output (comparator D)
—	—	—	—	—	8	—	$\overline{CS}$	Chip Select
1, 5, 8	—	—	—	—	1, 5	—	NC	No Internal Connection

3.1 Analog Inputs

The comparator non-inverting and inverting inputs are high-impedance CMOS inputs with low bias currents.

3.2 $\overline{CS}$ Digital Input

This is a CMOS, Schmitt-triggered input that places the part into a low power mode of operation.

3.3 Digital Outputs

The comparator outputs are CMOS, push-pull digital outputs. They are designed to be compatible with CMOS and TTL logic and are capable of driving heavy DC or capacitive loads.

3.4 Power Supply (V_{SS} and V_{DD})

The positive power supply pin (V_{DD}) is 1.6V to 5.5V higher than the negative power supply pin (V_{SS}). For normal operation, the other pins are at voltages between V_{SS} and V_{DD}.

Typically, these parts are used in a single (positive) supply configuration. In this case, V_{SS} is connected to ground and V_{DD} is connected to the supply. V_{DD} will need a local bypass capacitor (typically 0.01 µF to 0.1 µF) within 2 mm of the V_{DD} pin. These can share a bulk capacitor with nearby analog parts (within 100 mm), but it is not required.

4.0 APPLICATIONS INFORMATION

The MCP6541/1R/1U/2/3/4 family of push-pull output comparators are fabricated on Microchip's state-of-the-art CMOS process. They are suitable for a wide range of applications requiring very low power consumption.

4.1 Comparator Inputs

4.1.1 PHASE REVERSAL

The MCP6541/1R/1U/2/3/4 comparator family uses CMOS transistors at the input. They are designed to prevent phase inversion when the input pins exceed the supply voltages. Figure 2-3 shows an input voltage exceeding both supplies with no resulting phase inversion.

4.1.2 INPUT VOLTAGE AND CURRENT LIMITS

The ESD protection on the inputs can be depicted as shown in Figure 4-1. This structure was chosen to protect the input transistors, and to minimize input bias current (IB). The input ESD diodes clamp the inputs when they try to go more than one diode drop below V_{SS}. They also clamp any voltages that go too far above V_{DD}; their breakdown voltage is high enough to allow normal operation, and low enough to bypass ESD events within the specified limits.

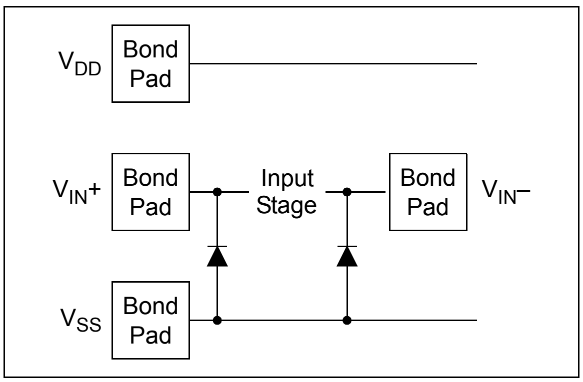
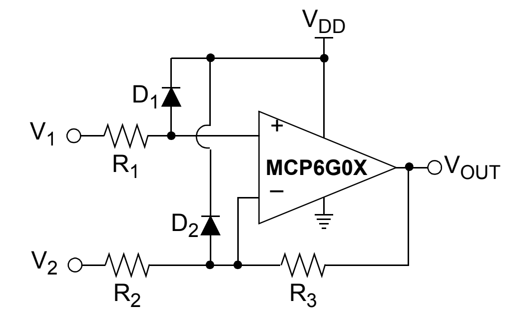


FIGURE 4-1: *Simplified Analog Input ESD Structures.*

In order to prevent damage and/or improper operation of these amplifiers, the circuits they are in must limit the currents (and voltages) at the V_{IN}+ and V_{IN}– pins (see Absolute Maximum Ratings † at the beginning of **Section 1.0 "Electrical Characteristics"**). Figure 4-3 shows the recommended approach to protecting these inputs. The internal ESD diodes prevent the input pins (V_{IN}+ and V_{IN}–) from going too far below ground, and the resistors R_1 and R_2 limit the possible current drawn out of the input pin. Diodes D_1 and D_2 prevent the input pin (V_{IN}+ and V_{IN}–) from going too far above V_{DD}. When implemented as shown, resistors R_1 and R_2 also limit the current through D_1 and D_2.



$$R_1 \geq \frac{V_{SS} - (\text{minimum expected } V_1)}{2\ mA}$$

$$R_2 \geq \frac{V_{SS} - (\text{minimum expected } V_2)}{2\ mA}$$

FIGURE 4-2: *Protecting the Analog Inputs.*

It is also possible to connect the diodes to the left of the resistors R_1 and R_2. In this case, the currents through the diodes D_1 and D_2 need to be limited by some other mechanism. The resistor then serves as in-rush current limiter; the DC current into the input pins (V_{IN}+ and V_{IN}–) should be very small.

A significant amount of current can flow out of the inputs when the common mode voltage (V_{CM}) is below ground (V_{SS}); see Figure 2-37. Applications that are high impedance may need to limit the useable voltage range.

4.1.3 NORMAL OPERATION

The input stage of this family of devices uses two differential input stages in parallel: one operates at low input voltages and the other at high input voltages. With this topology, the input voltage is 0.3V above V_{DD} and 0.3V below V_{SS}. Therefore, the input offset voltage is measured at both V_{SS} - 0.3V and V_{DD} + 0.3V to ensure proper operation.

The MCP6541/1R/1U/2/3/4 family has internally-set hysteresis that is small enough to maintain input offset accuracy (<7 mV) and large enough to eliminate output chattering caused by the comparator's own input noise voltage (200 μV_{p-p}). Figure 4-3 depicts this behavior.

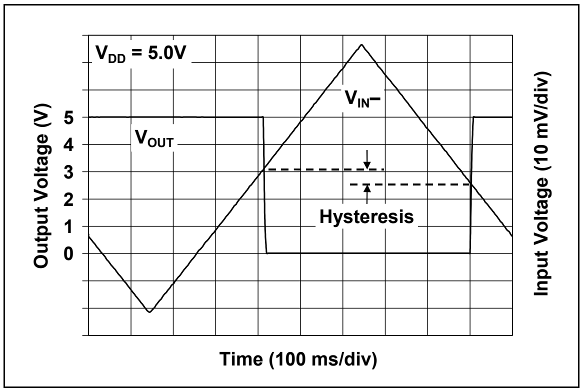


FIGURE 4-3: The MCP6541/1R/1U/2/3/4 comparators' internal hysteresis eliminates output chatter caused by input noise voltage.

4.2 Push-Pull Output

The push-pull output is designed to be compatible with CMOS and TTL logic, while the output transistors are configured to give rail-to-rail output performance. They are driven with circuitry that minimizes any switching current (shoot-through current from supply-to-supply) when the output is transitioned from high-to-low, or from low-to-high (see Figures 2-15, 2-18, 2-32 through 2-36 for more information).

4.3 MCP6543 Chip Select ($\overline{CS}$)

The MCP6543 is a single comparator with Chip Select ($\overline{CS}$). When $\overline{CS}$ is pulled high, the total current consumption drops to 20 pA (typ.); 1 pA (typ.) flows through the $\overline{CS}$ pin, 1 pA (typ.) flows through the output pin and 18 pA (typ.) flows through the V_{DD} pin, as shown in Figure 1-1. When this happens, the comparator output is put into a high-impedance state. By pulling $\overline{CS}$ low, the comparator is enabled. If the $\overline{CS}$ pin is left floating, the comparator will not operate properly. Figure 1-1 shows the output voltage and supply current response to a $\overline{CS}$ pulse.

The internal $\overline{CS}$ circuitry is designed to minimize glitches when cycling the $\overline{CS}$ pin. This helps conserve power, which is especially important in battery-powered applications.

4.4 Externally Set Hysteresis

Greater flexibility in selecting hysteresis (or input trip points) is achieved by using external resistors.

Input offset voltage (V_{OS}) is the center (average) of the (input-referred) low-high and high-low trip points. Input hysteresis voltage (V_{HYST}) is the difference between the same trip points. Hysteresis reduces output chattering when one input is slowly moving past the other and thus reduces dynamic supply current. It also helps in systems where it is best not to cycle between states too frequently (e.g., air conditioner thermostatic control).

4.4.1 NON-INVERTING CIRCUIT

Figure 4-4 shows a non-inverting circuit for single-supply applications using just two resistors. The resulting hysteresis diagram is shown in Figure 4-5.

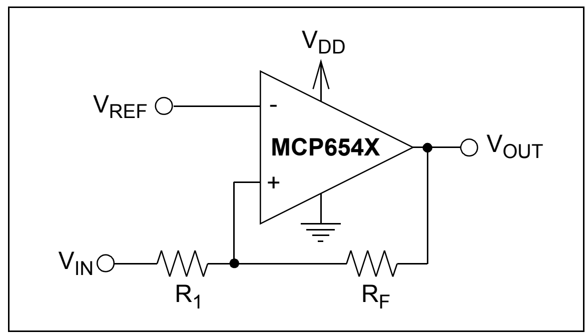


FIGURE 4-4: Non-inverting circuit with hysteresis for single-supply.

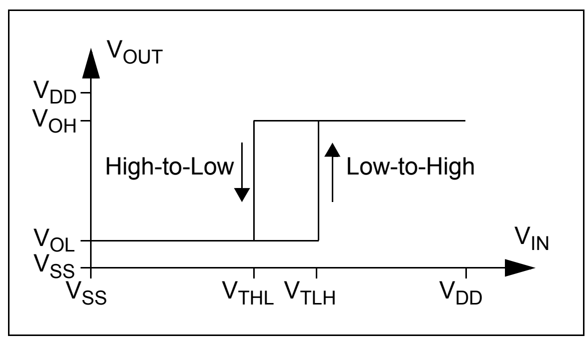


FIGURE 4-5: Hysteresis Diagram for the Non-Inverting Circuit.

The trip points for Figures 4-4 and 4-5 are:

EQUATION 4-1:

$$V_{TLH} = V_{REF}\left(1 + \frac{R_1}{R_F}\right) - V_{OL}\left(\frac{R_1}{R_F}\right)$$

$$V_{THL} = V_{REF}\left(1 + \frac{R_1}{R_F}\right) - V_{OH}\left(\frac{R_1}{R_F}\right)$$

V_{TLH} = trip voltage from low to high

V_{THL} = trip voltage from high to low

4.4.2 INVERTING CIRCUIT

Figure 4-6 shows an inverting circuit for single-supply using three resistors. The resulting hysteresis diagram is shown in Figure 4-7.

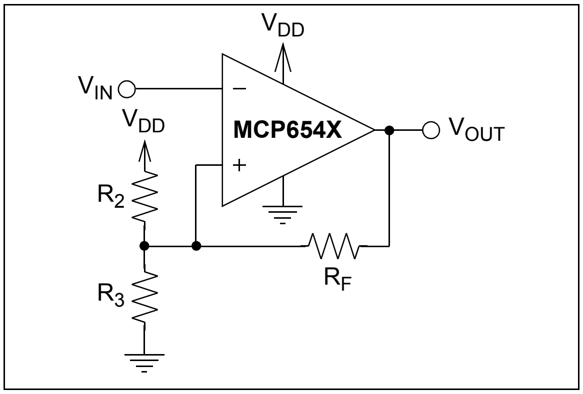


FIGURE 4-6: *Inverting Circuit With Hysteresis.*

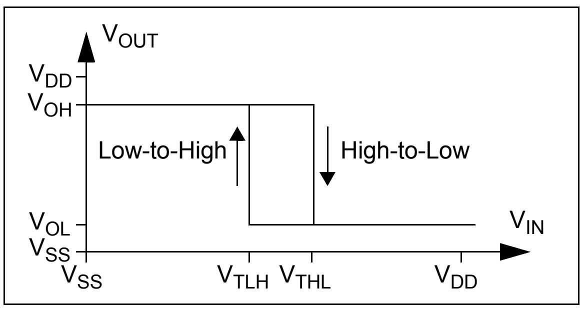


FIGURE 4-7: *Hysteresis Diagram for the Inverting Circuit.*

In order to determine the trip voltages (V_{THL} and V_{TLH}) for the circuit shown in Figure 4-6, R_2 and R_3 can be simplified to the Thevenin equivalent circuit with respect to V_{DD}, as shown in Figure 4-8.

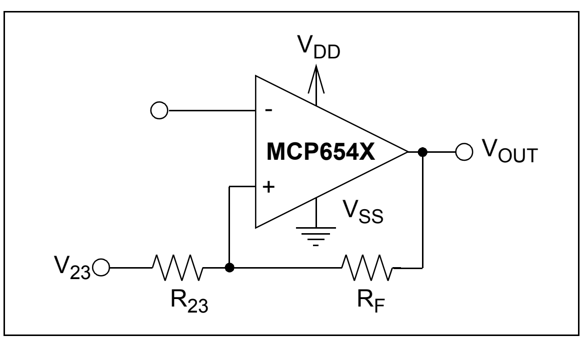


FIGURE 4-8: *Thevenin Equivalent Circuit.*

Where:

$$R_{23} = \frac{R_2 R_3}{R_2 + R_3}$$

$$V_{23} = \frac{R_3}{R_2 + R_3} \times V_{DD}$$

Using this simplified circuit, the trip voltage can be calculated using the following equation:

EQUATION 4-2:

$$V_{THL} = V_{OH}\left(\frac{R_{23}}{R_{23} + R_F}\right) + V_{23}\left(\frac{R_F}{R_{23} + R_F}\right)$$

$$V_{TLH} = V_{OL}\left(\frac{R_{23}}{R_{23} + R_F}\right) + V_{23}\left(\frac{R_F}{R_{23} + R_F}\right)$$

V_{TLH} = trip voltage from low to high

V_{THL} = trip voltage from high to low

Figure 2-20 and Figure 2-23 can be used to determine typical values for V_{OH} and V_{OL}.

4.5 Bypass Capacitors

With this family of comparators, the power supply pin (V_{DD} for single supply) should have a local bypass capacitor (i.e., 0.01 µF to 0.1 µF) within 2 mm for good edge rate performance.

4.6 Capacitive Loads

Reasonable capacitive loads (e.g., logic gates) have little impact on propagation delay (see Figure 2-31). The supply current increases with increasing toggle frequency (Figure 2-19), especially with higher capacitive loads.

4.7 Battery Life

In order to maximize battery life in portable applications, use large resistors and small capacitive loads. Avoid toggling the output more than necessary. Do not use Chip Select ($\overline{CS}$) frequently to conserve start-up power. Capacitive loads will draw additional power at start-up.

4.8 PCB Surface Leakage

In applications where low input bias current is critical, PCB (Printed Circuit Board) surface leakage effects need to be considered. Surface leakage is caused by humidity, dust or other contamination on the board. Under low humidity conditions, a typical resistance between nearby traces is $10^{12}\Omega$. A 5V difference would cause 5 pA of current to flow. This is greater than the MCP6541/1R/1U/2/3/4 family's bias current at 25°C (1 pA, typ.).

The easiest way to reduce surface leakage is to use a guard ring around sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin. An example of this type of layout is shown in Figure 4-9.

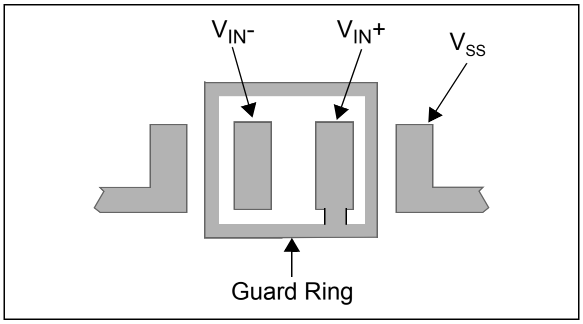


FIGURE 4-9: *Example Guard Ring Layout for Inverting Circuit.*

1. Inverting Configuration (Figures 4-6 and 4-9):
   a. Connect the guard ring to the non-inverting input pin (V_{IN}+). This biases the guard ring to the same reference voltage as the comparator (e.g., V_{DD}/2 or ground).
   b. Connect the inverting pin (V_{IN}–) to the input pad without touching the guard ring.
2. Non-inverting Configuration (Figure 4-4):
   a. Connect the non-inverting pin (V_{IN}+) to the input pad without touching the guard ring.
   b. Connect the guard ring to the inverting input pin (V_{IN}–).

4.9 Unused Comparators

An unused amplifier in a quad package (MCP6544) should be configured as shown in Figure 4-10. This circuit prevents the output from toggling and causing crosstalk. It uses the minimum number of components and draws minimal current (see Figure 2-15 and Figure 2-18).

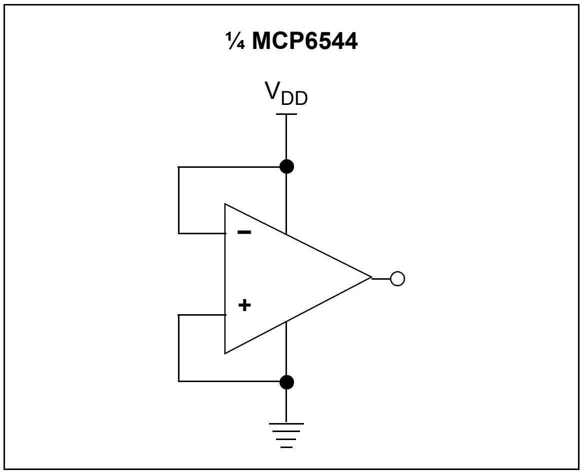


FIGURE 4-10: *Unused Comparators.*

4.10 Typical Applications

4.10.1 PRECISE COMPARATOR

Some applications require higher DC precision. An easy way to solve this problem is to use an amplifier (such as the MCP6041) to gain-up the input signal before it reaches the comparator. Figure 4-11 shows an example of this approach.

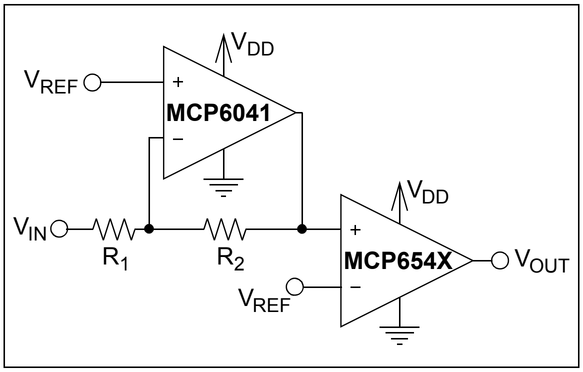


FIGURE 4-11: *Precise Inverting Comparator.*

4.10.2 WINDOWED COMPARATOR

Figure 4-12 shows one approach to designing a windowed comparator. The AND gate produces a logic '1' when the input voltage is between V_{RB} and V_{RT} (where $V_{RT} > V_{RB}$).

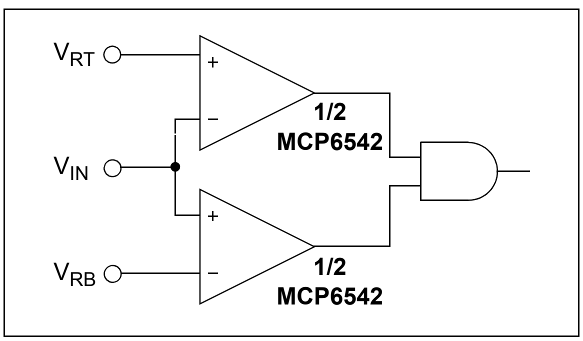


FIGURE 4-12: *Windowed Comparator.*

4.10.3 BISTABLE MULTI-VIBRATOR

A simple bistable multi-vibrator design is shown in Figure 4-13. V_{REF} needs to be between the power supplies (V_{SS} = GND and V_{DD}) to achieve oscillation. The output duty cycle changes with V_{REF}.

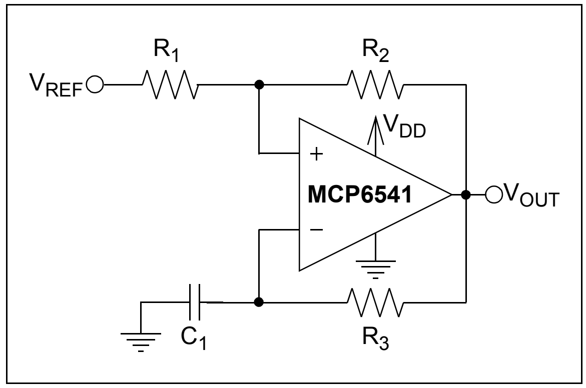
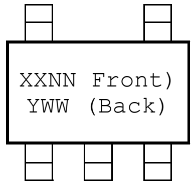


FIGURE 4-13: *Bistable Multi-vibrator.*

5.0 PACKAGING INFORMATION

5.1 Package Marking Information

5-Lead SC-70 (**MCP6541**)

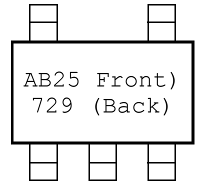


Device	I-Temp Code	E-Temp Code
MCP6541U	ABNN	**Note 2**

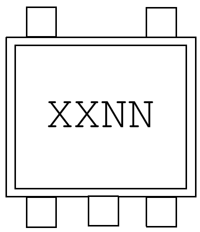
Note 1: I-Temp parts prior to March 2005 are marked “ABN”

2: SC-70-5 E-Temp parts not available at this release of this data sheet.

Example:



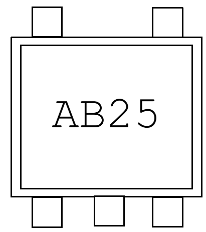
5-Lead SOT-23 (**MCP6541, MCP6541R, MCP6541U**)



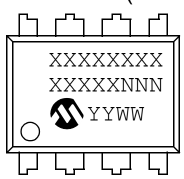
Device	I-Temp Code	E-Temp Code
MCP6541	ABNN	GTNN
MCP6541R	AGNN	GUNN
MCP6541U	—	ATNN

Note: Applies to 5-Lead SOT-23

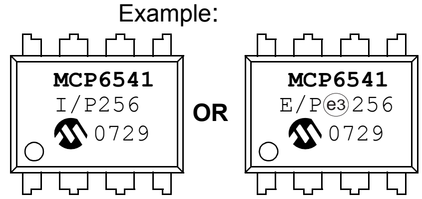
Example:



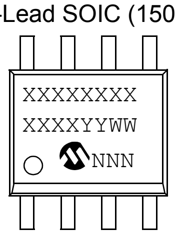
8-Lead PDIP (300 mil)



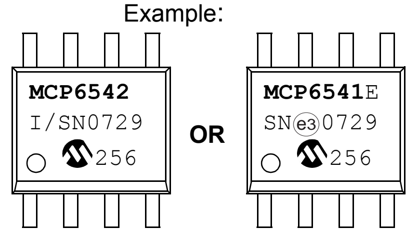
Example:



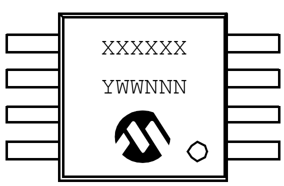
8-Lead SOIC (150 mil)



Example:



8-Lead MSOP



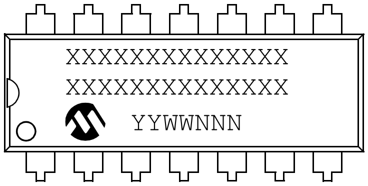
Example:

Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

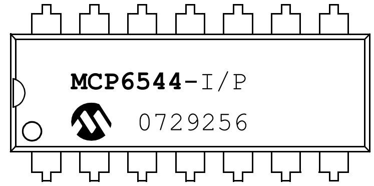
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

Package Marking Information (Continued)

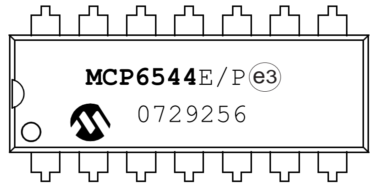
14-Lead PDIP (300 mil) **(MCP6544)**



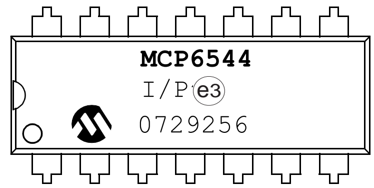
Example:



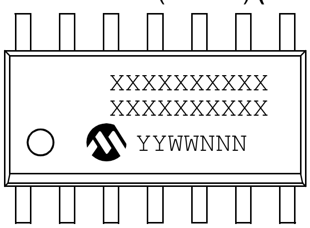
OR



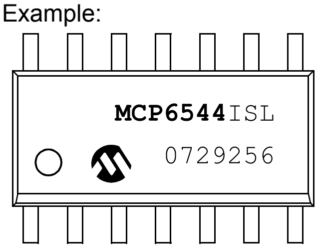
OR



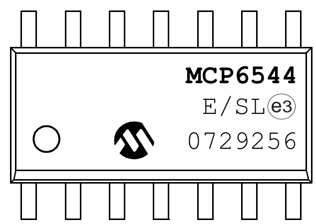
14-Lead SOIC (150 mil) **(MCP6544)**



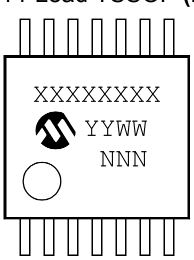
Example:



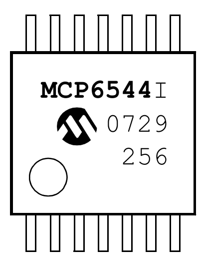
OR



14-Lead TSSOP **(MCP6544)**

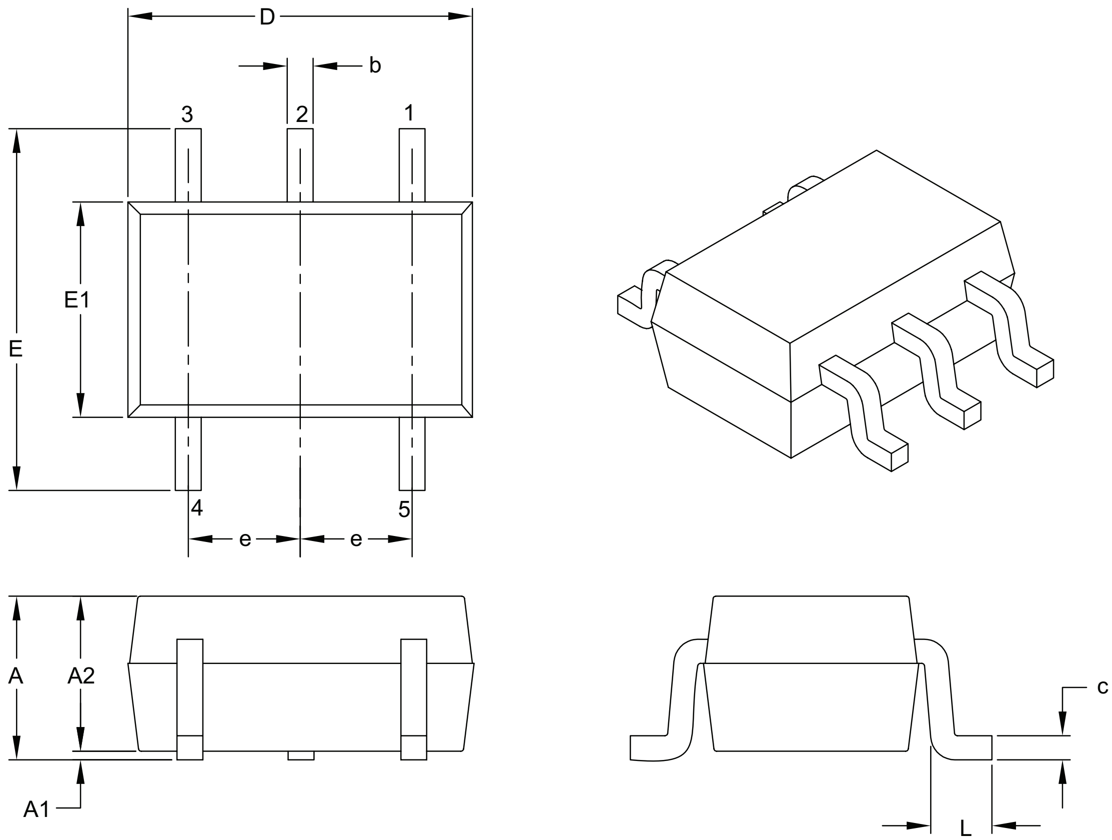


Example:



5-Lead Plastic Small Outline Transistor (LT) [SC70]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		5	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	–	1.10
Molded Package Thickness	A2	0.80	–	1.00
Standoff	A1	0.00	–	0.10
Overall Width	E	1.80	2.10	2.40
Molded Package Width	E1	1.15	1.25	1.35
Overall Length	D	1.80	2.00	2.25
Foot Length	L	0.10	0.20	0.46
Lead Thickness	c	0.08	–	0.26
Lead Width	b	0.15	–	0.40

Notes:

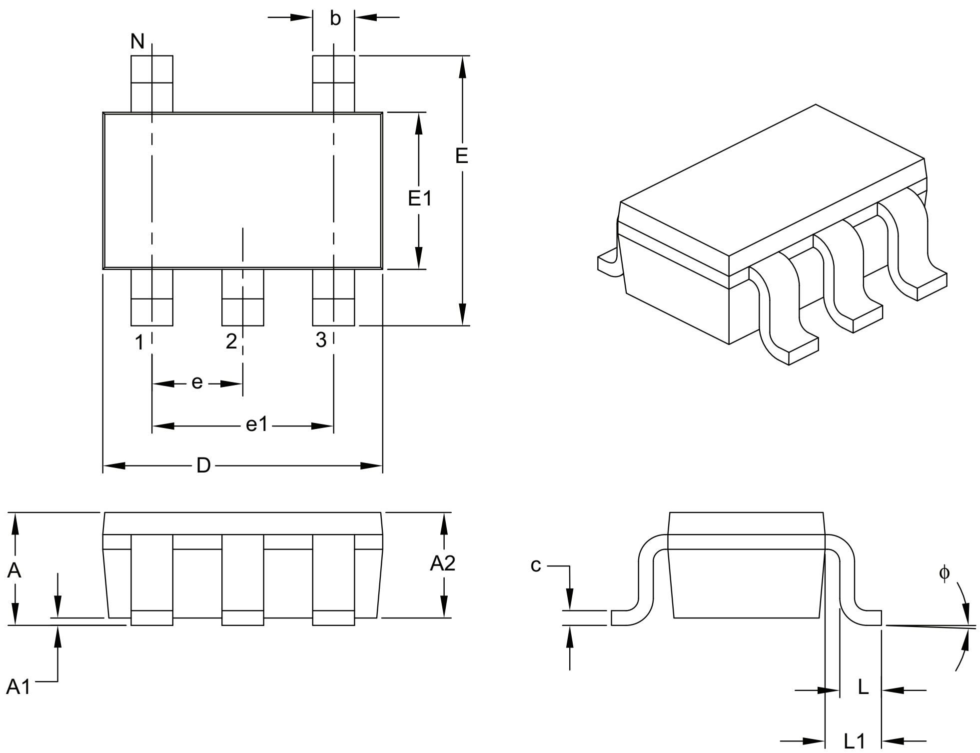
1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-061B

5-Lead Plastic Small Outline Transistor (OT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		5	
Lead Pitch	e		0.95 BSC	
Outside Lead Pitch	e1		1.90 BSC	
Overall Height	A	0.90	–	1.45
Molded Package Thickness	A2	0.89	–	1.30
Standoff	A1	0.00	–	0.15
Overall Width	E	2.20	–	3.20
Molded Package Width	E1	1.30	–	1.80
Overall Length	D	2.70	–	3.10
Foot Length	L	0.10	–	0.60
Footprint	L1	0.35	–	0.80
Foot Angle	ϕ	0°	–	30°
Lead Thickness	c	0.08	–	0.26
Lead Width	b	0.20	–	0.51

Notes:

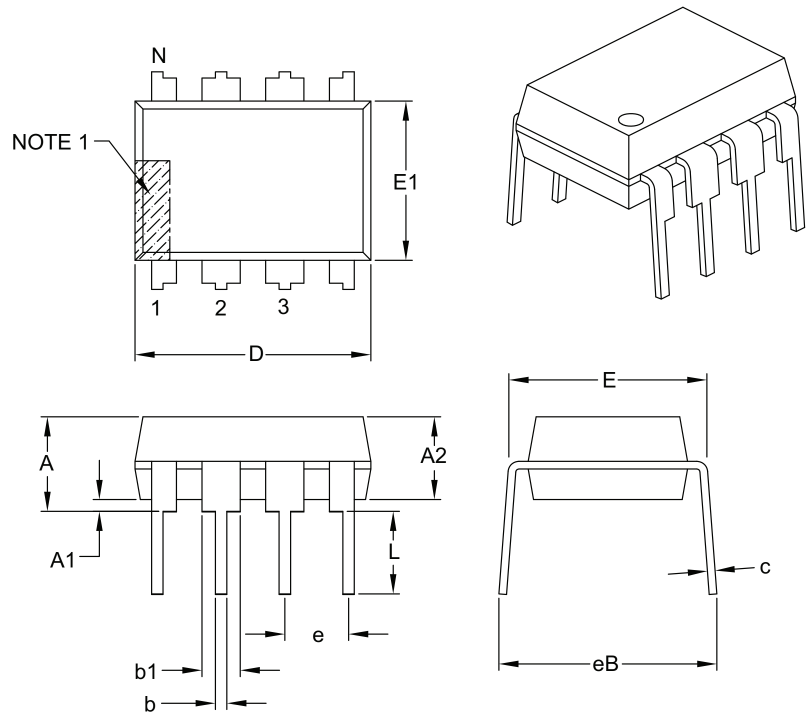
1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-091B

8-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	INCHES		
	Dimension Limits	MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	.100 BSC		
Top to Seating Plane	A	–	–	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.348	.365	.400
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

Notes:

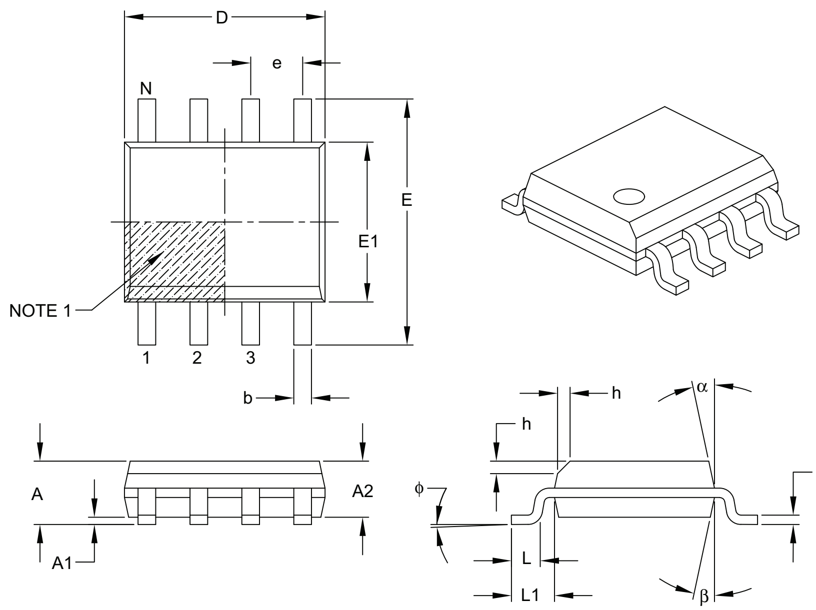
1. Pin 1 visual index feature may vary, but must be located with the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-018B

8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



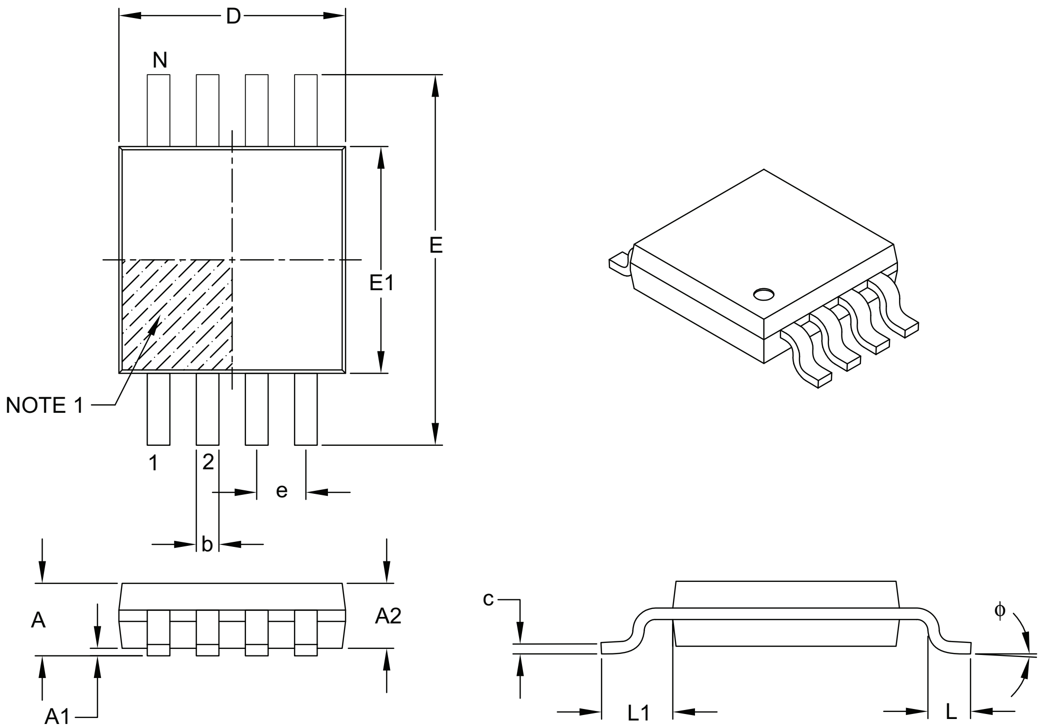
Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	1.27 BSC		
Overall Height	A	–	–	1.75
Molded Package Thickness	A2	1.25	–	–
Standoff §	A1	0.10	–	0.25
Overall Width	E	6.00 BSC		
Molded Package Width	E1	3.90 BSC		
Overall Length	D	4.90 BSC		
Chamfer (optional)	h	0.25	–	0.50
Foot Length	L	0.40	–	1.27
Footprint	L1	1.04 REF		
Foot Angle	φ	0°	–	8°
Lead Thickness	c	0.17	–	0.25
Lead Width	b	0.31	–	0.51
Mold Draft Angle Top	α	5°	–	15°
Mold Draft Angle Bottom	β	5°	–	15°

Notes:
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-057B

8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



		Units	MILLIMETERS		
		Dimension Limits	MIN	NOM	MAX
Number of Pins		N		8	
Pitch		e		0.65 BSC	
Overall Height		A	–	–	1.10
Molded Package Thickness		A2	0.75	0.85	0.95
Standoff		A1	0.00	–	0.15
Overall Width		E		4.90 BSC	
Molded Package Width		E1		3.00 BSC	
Overall Length		D		3.00 BSC	
Foot Length		L	0.40	0.60	0.80
Footprint		L1		0.95 REF	
Foot Angle		φ	0°	–	8°
Lead Thickness		c	0.08	–	0.23
Lead Width		b	0.22	–	0.40

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

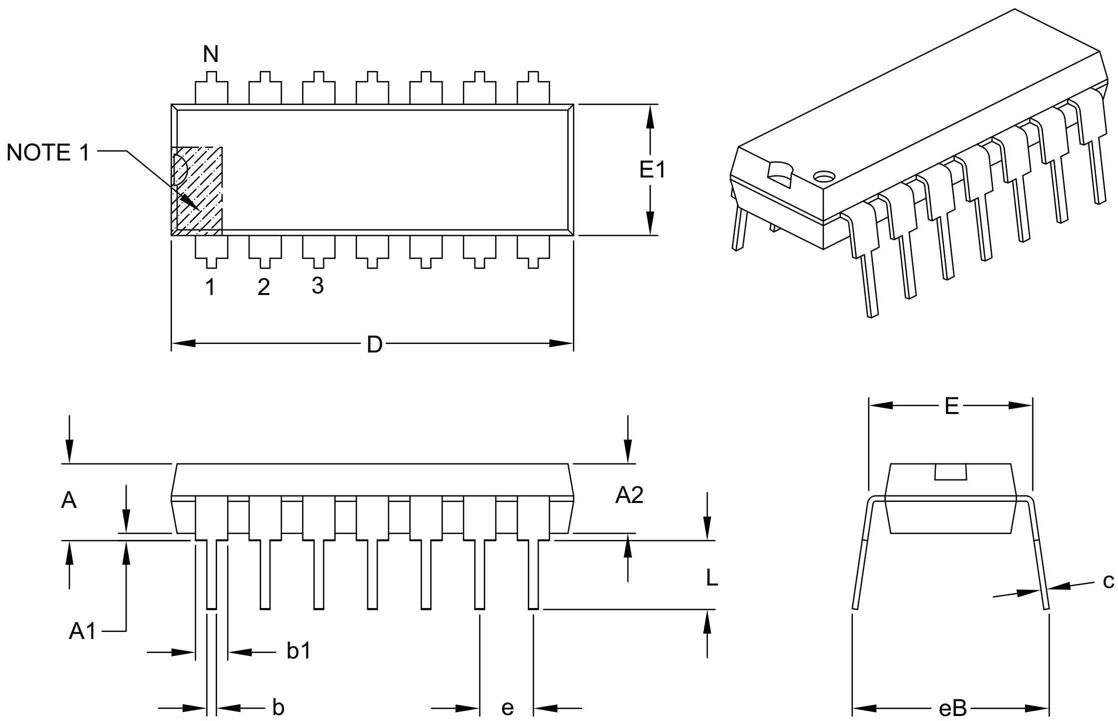
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-111B

14-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	14		
Pitch	e	.100 BSC		
Top to Seating Plane	A	–	–	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.735	.750	.775
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.045	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

Notes:

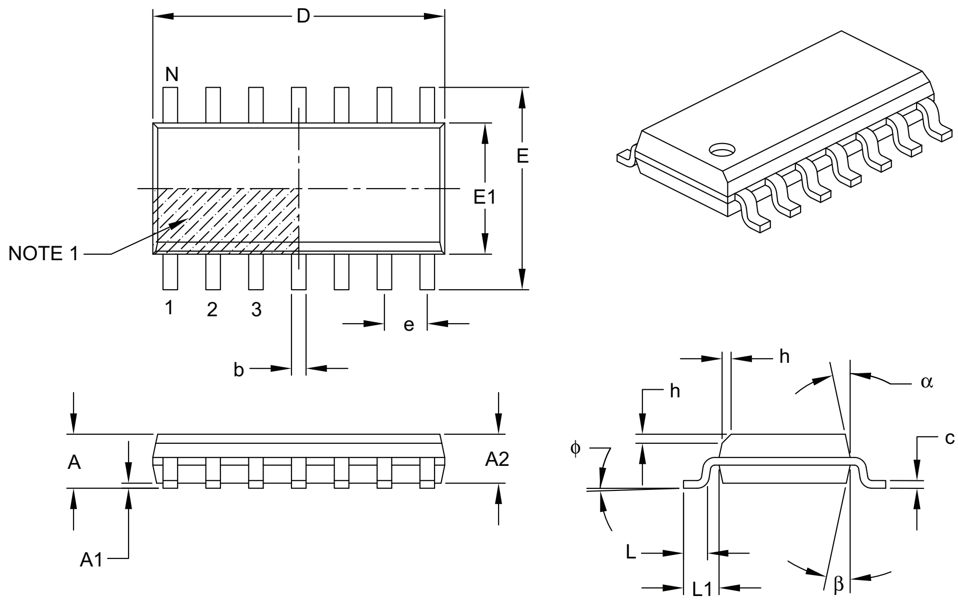
1. Pin 1 visual index feature may vary, but must be located with the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-005B

14-Lead Plastic Small Outline (SL) – Narrow, 3.90 mm Body [SOIC]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Number of Pins	N	14		
Pitch	e	1.27 BSC		
Overall Height	A	–	–	1.75
Molded Package Thickness	A2	1.25	–	–
Standoff §	A1	0.10	–	0.25
Overall Width	E	6.00 BSC		
Molded Package Width	E1	3.90 BSC		
Overall Length	D	8.65 BSC		
Chamfer (optional)	h	0.25	–	0.50
Foot Length	L	0.40	–	1.27
Footprint	L1	1.04 REF		
Foot Angle	ϕ	0°	–	8°
Lead Thickness	c	0.17	–	0.25
Lead Width	b	0.31	–	0.51
Mold Draft Angle Top	α	5°	–	15°
Mold Draft Angle Bottom	β	5°	–	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

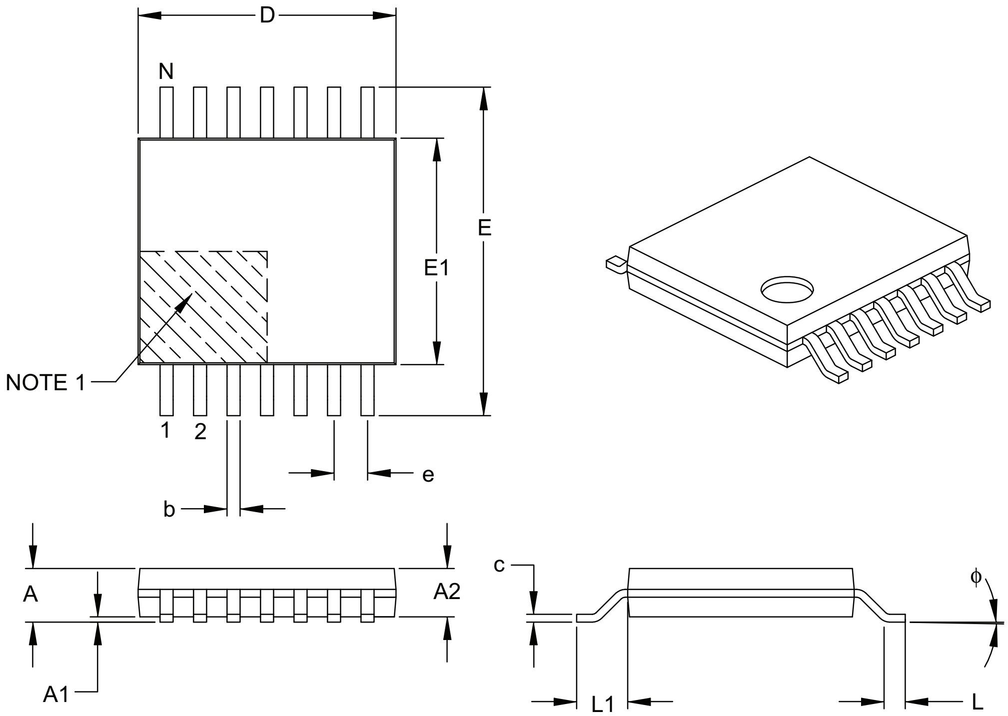
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-065B

14-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		14	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.80	1.00	1.05
Standoff	A1	0.05	–	0.15
Overall Width	E		6.40 BSC	
Molded Package Width	E1	4.30	4.40	4.50
Molded Package Length	D	4.90	5.00	5.10
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	ϕ	0°	–	8°
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.19	–	0.30

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-087B

APPENDIX A: REVISION HISTORY

Revision F (September 2007)

1. Corrected polarity of MCP6541U SOT-23-5 pin out diagram on front page.
2. **Section 5.1 "Package Marking Information"**: Updated package outline drawings per marcom.

Revision E (September 2006)

The following is the list of modifications:

1. Added MCP6541U pinout for the SOT-23-5 package.
2. Clarified Absolute Maximum Analog Input Voltage and Current Specifications.
3. Added applications writeups on unused comparators.
4. Added disclaimer to package outline drawings.

Revision D (May 2006)

The following is the list of modifications:

1. Added E-temp parts.
2. Changed V_{HYST} temperature specification to linear and quadratic temperature coefficients.
3. Changed specifications and plots for E-Temp.
4. Added Section 3.0 Pin Descriptions
5. Corrected package marking (See **Section 5.1 "Package Marking Information"**)
6. Added Appendix A: Revision History.

Revision C (September 2003)

Revision B (November 2002)

Revision A (March 2002)

- Original Release of this Document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	-X	/XX
Device	Temperature Range	Package

Device:	MCP6541:	Single Comparator
	MCP6541T:	Single Comparator (Tape and Reel) (SC-70, SOT-23, SOIC, MSOP)
	MCP6541RT:	Single Comparator (Rotated - Tape and Reel) (SOT-23 only)
	MCP6541UT:	Single Comparator (Tape and Reel) **(SOT-23-5 is E-Temp only)**
	MCP6542:	Dual Comparator
	MCP6542T:	Dual Comparator (Tape and Reel for SOIC and MSOP)
	MCP6543:	Single Comparator with $\overline{CS}$
	MCP6543T:	Single Comparator with $\overline{CS}$ (Tape and Reel for SOIC and MSOP)
	MCP6544:	Quad Comparator
	MCP6544T:	Quad Comparator (Tape and Reel for SOIC and TSSOP)
Temperature Range:	I =	-40°C to +85°C
	E * =	-40°C to +125°C
		* SC-70-5 E-Temp parts not available at this release of the data sheet.
Package:	LT =	Plastic Package (SC-70), 5-lead
	OT =	Plastic Small Outline Transistor (SOT-23), 5-lead
	MS =	Plastic MSOP, 8-lead
	P =	Plastic DIP (300 mil Body), 8-lead, 14-lead
	SN =	Plastic SOIC (150 mil Body), 8-lead
	SL =	Plastic SOIC (150 mil Body), 14-lead (MCP6544)
	ST =	Plastic TSSOP (4.4mm Body), 14-lead (MCP6544)

Examples:

a) MCP6541T-I/LT: Tape and Reel, Industrial Temperature, 5LD SC-70.
b) MCP6541T-I/OT: Tape and Reel, Industrial Temperature, 5LD SOT-23.
c) MCP6541-E/P: Extended Temperature, 8LD PDIP.
d) MCP6541RT-I/OT: Tape and Reel, Industrial Temperature, 5LD SOT23.
e) MCP6541-E/SN: Extended Temperature, 8LD SOIC.
f) MCP6541UT-E/OT: Tape and Reel, Extended Temperature, 5LD SOT23.

a) MCP6542-I/MS: Industrial Temperature, 8LD MSOP.
b) MCP6542T-I/MS: Tape and Reel, Industrial Temperature, 8LD MSOP.
c) MCP6542-I/P: Industrial Temperature, 8LD PDIP.
d) MCP6542-E/SN: Extended Temperature, 8LD SOIC.

a) MCP6543-I/SN: Industrial Temperature, 8LD SOIC.
b) MCP6543T-I/SN: Tape and Reel, Industrial Temperature, 8LD SOIC.
c) MCP6543-I/P: Industrial Temperature, 8LD PDIP.
d) MCP6543-E/SN: Extended Temperature, 8LD SOIC.

a) MCP6544T-I/SL: Tape and Reel, Industrial Temperature, 14LD SOIC.
b) MCP6544T-E/SL: Tape and Reel, Extended Temperature, 14LD SOIC.
c) MCP6544-I/P: Industrial Temperature, 14LD PDIP.
d) MCP6544T-E/ST: Tape and Reel, Extended Temperature, 14LD TSSOP.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
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Общество с ограниченной ответственностью «МосЧип» ИНН 7719860671 / КПП 771901001
Адрес: 105318, г.Москва, ул.Щербаковская д.3, офис 1107

Данный компонент на территории Российской Федерации

Вы можете приобрести в компании MosChip.

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http://moschip.ru/get-element

Вы можете разместить у нас заказ для любого Вашего проекта, будь то серийное производство или разработка единичного прибора.

В нашем ассортименте представлены ведущие мировые производители активных и пассивных электронных компонентов.

Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

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