

CDB43L22

Evaluation Board for CS43L22

Features

- Analog Passthrough Input
 - Four Stereo Line Input Jacks
 - Channel Mixer
- Analog Output
 - Stereo Headphone Jack w/ HP Detect Capability
 - Speaker Output via Differential Stereo PWM Terminals and Audio Jacks
- ♦ 8- to 96-kHz S/PDIF Interface
 - Optical and RCA S/PDIF Input Jacks
 - CS8416 Digital Audio Receiver
- ♦ I/O Stake Headers
 - External Control Port Accessibility
 - External DSP Serial Audio I/O Accessibility
- Multiple Power Supply options via Battery or External Power Supplies.
- ♦ 1.8 V to 3.3 V Logic Interface
- FlexGUI S/W Control Windows[®] Compatible
 Pre-Defined & User-Configurable Scripts

Description

Using the CDB43L22 evaluation board is an ideal way to evaluate the CS43L22. Use of the board requires an analog/digital signal source, an analyzer and power supplies. A Windows PC-compatible computer is also required in order to configure the CDB43L22.

System timing can be provided by the CS8416, by the CS43L22 with supplied master clock, or via an I/O stake header with a DSP connected. 1/8th inch audio jacks are provided for the analog passthrough inputs and HP/Line outputs. Two pairs of banana jacks and an additional pair of 1/8th inch audio jacks are provided to monitor the stereo differential speaker PWM output from the CS43L22. Digital input connections are via RCA phono or optical connectors to the CS8416 (S/PDIF Rx).

The Windows-based software GUI provided makes configuring the CDB43L22 easy. The software communicates through the PC's USB port to configure the board and FPGA registers so that all features of the CS43L22 can be evaluated. The evaluation board may also be configured to accept external timing and data signals for operation in a user application during system development.

ORDERING INFORMATION

CDB43L22

Evaluation Board







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1. SYSTEM OVERVIEW

The CDB43L22 platform provides analog and digital interfaces to the CS43L22 and allows for external DSP and $I^2C^{\mbox{\sc B}}$ interconnects. On-board power regulators are provided so that an external power supply upto +5 V can be used to provide power for the digital and analog cores of the CS43L22. On-board peripherals are powered from the USB connection which also serves as an interface to a PC. The CDB43L22 is configured using Cirrus Logic's Windows-compatible FlexGUI software to read/write to device registers.

This section describes the various components on the CDB43L22 and how they are used. Section 2 on page 7 is a simplified quick connect guide provided for user convenience and can be used to set up the board quickly with the CS43L22 in its startup default configuration. Section 3 on page 8 describes the various configuration options in which the board can be used. Section 4 "Software Mode Control" on page 11 provides further configuration details and describes software functionality. The CDB43L22 schematic set is shown in Figures 7 through 18. Section 5 on page 17 provides a description of all stake headers and connectors, including the default factory settings for all jumpers.

1.1 Power

Power is supplied to the evaluation board via the USB connection or by applying +5.0 V to TP2. Jumper J34 allows the user to select the power source. Power (VP) and ground (GND) for the CS43L22 is supplied via binding posts J35 and J4 (respectively) or by standard AAA batteries in locations BT1, BT2 and BT3. The voltage provided to the binding posts can be in the range of +2.7 V to +5.25 V. On-board regulators and jumpers allow the user to connect the CS43L22's supplies to +1.8 V, 2.5 V or +3.3 V for VL and +1.8 V or 2.5 V for VD, VA and VA_HP. All voltage inputs are referenced to ground using the black binding post J4.

Stake headers J47, J52, J53 and J74 provide a convenient way to measure supply currents to the CS43L22 for VA_HP, VL, VD and VA supplies respectively. The current can be easily calculated by measuring the voltage drop across the parallel resistors with its associated jumper removed.

NOTE: Stake headers J47, J48, J52, J53 and J74 must be shunted with the supplied jumpers during normal operation.

WARNING: Please refer to the CS43L22 data sheet for allowable voltage levels.

1.2 Grounding and Power Supply Decoupling

The CS43L22 requires careful attention to power supply and grounding arrangements to optimize performance. The CDB43L22 demonstrates these optimal arrangements. Figure 9 on page 19 provides an overview of the connections to the CS43L22. Figure 14 on page 24 shows the component placement, Figure 15 on page 25 shows the top layout, and Figure 18 on page 28 shows the bottom layout. Power supply decoupling capacitors are located as close as possible to the CS43L22. Extensive use of ground plane fill helps reduce radiated noise.

1.3 FPGA

The FPGA controls digital signal routing between the CS43L22, CS8416, SRC, PLL and the I/O stake header. It also provides routing control of the system master clock from an on-board oscillator and the CS8416. The Cirrus FlexGUI software provides full control of the FPGA's routing and configuration options. Section 4 "Software Mode Control" on page 11 provides configuration details.

1.4 CS43L22

A complete description of the CS43L22 can be found in the CS43L22 product data sheet.



The CS43L22 is configured using the Cirrus FlexGUI. The device configuration registers are accessible via the "Register Maps" tab of the Cirrus FlexGUI software. This tab provides low-level control of each bit. For easier configuration, additional tabs provide high-level control. Section 4 "Software Mode Control" on page 11 provides configuration details.

1.5 CS8416 Digital Audio Receiver

A complete description of the CS8416 receiver and a discussion of the digital audio interface can be found in the CS8416 data sheet.

The CS8416 converts the input S/PDIF data stream from the optical or RCA connector into PCM data that is input to the CS43L22.

Selections are made by using the "Board Configuration" tab of the Cirrus FlexGUI software. Section 4 "Software Mode Control" on page 11 provides configuration details.

1.6 Oscillator

The socketed on-board oscillator can be selected as the system master clock source by using the selections on the "Board Configuration" tab of the Cirrus FlexGUI. Section 4 "Software Mode Control" on page 11 provides configuration details.

The oscillator is mounted in pin sockets, allowing easy removal or replacement. The device footprint on the board will accommodate full- or half-can-sized oscillators.

1.7 I/O Stake Headers

The evaluation board has been designed to allow interfacing with external systems via a serial port header (reference designation J8) and a control port header (reference designation J109). The serial port header provides access to the serial audio signals required to interface with a DSP (Figure 10 on page 20).

The control port header provides bidirectional access to the I²C control port signals by simply removing all the shunt jumpers from the "USB" position. The user may then connect a ribbon cable connector to the "Ext Sys Connect" pins for external control of board functions. A single row of "GND" pins are provided to maintain signal ground integrity. Two unpopulated pull-up resistors are also available should the user choose to use the CDB43L22 logic supply (VL) externally.

1.8 Analog Inputs

Four stereo jack connectors can be used to supply AC coupled line-level analog inputs to the CS43L22 for testing the device in passthrough mode.

Figure 10 on page 20 illustrates how the analog passthrough inputs are connected and routed. Table 5 on page 18 details the jumper selections. The CS43L22 data sheet specifies the allowed full scale input voltage level.

1.9 Analog Outputs

The CDB43L22 has a stereo headphone/line output jack (J40) and a dedicated stereo headphone (HP) output jack (J21) to monitor the CS43L22's ground centered analog output. The dedicated HP jack (J21) has circuitry that drives the SPKR/HP pin low when a stereo jack is inserted thereby allowing users to test the CS43L22's HP detect capability. Stake headers (J3 and J9) are provided to allow the user to select either a 16 Ω or a 32 Ω load for the headphone amplifier output. Stake headers(J1 and J2) are also provided to allow one to filter HP/Line outputs from the board. HP jack J21 can be used to connect a real headphone to provide an actual headphone load while performance measurements are taken on HP jack J40. When con-



necting headphones to either output jack, the on-board resistive load should be disconnected by removing the jumpers on each stake header(J3 and J9).

The CDB43L22 also has A/B speaker output banana jacks (2 per A or B channel) and 1/8" jack outputs (1 per A or B channel). Stake headers J15 and J19 allow one to short the differential outputs of Channel A and B together, in order to monitor MONO PWM output from the CS43L22. The red banana jacks designate the positive speaker terminal connection and the black jacks designate the negative terminal connection.

1.10 Control Port Connectors

The graphical user interface for the CDB43L22 (Cirrus Logic Flex GUI) allows the user to configure the CS43L22 registers and other component registers via the on-board I²C control bus. The GUI interfaces with the CDB via the USB connection to a PC. Section 4 "Software Mode Control" on page 11 provides a description of the Graphical User Interface (GUI).

1.11 USB Connector

Connecting a USB port cable from a PC to the USB connector on the board and launching the Cirrus FlexGUI software enables one to use the CDB43L22. Note: The USB port connection also provides DC power to the board (except for VP). The minimum current required is approximately 300 mA. It may, therefore, be necessary to connect the CDB43L22 directly to the USB port on the PC as opposed to a hub or keyboard port where current may be limited.



2. QUICK START GUIDE

The following figure is a simplified quick start up guide made for user convenience. The following start up guide configures the board with a 1.8 V power supply to VL, VA, VA_HP and VD. The user may choose from steps 9 through 13 depending on the desired measurement. Refer to Section 3 on page 8 for details on how the various components on the board interface with each other in different board configuration modes. Refer to Section 4 on page 11 for descriptions on control settings in the Cirrus FlexGUI software.





3. CONFIGURATION OPTIONS

In order to configure the CDB43L22 for making performance measurements, one needs to use Cirrus Logic's Windows compatible FlexGUI software to program the various components on the board. This section serves to give a deeper understanding of the on-board circuitry and the digital clock and data signal routing involved in the different configuration modes of the CDB43L22. The section also has the expected performance characteristics which are observed when using the board in the respective configuration mode.

3.1 SPDIF In to Headphone or Line Out

The CS43L22's stereo headphone/line output performance can be tested by loading the "**SPDIF In to Headphone or Line Out**" quick setup file provided with the software package. The script configures the digital clock and data signal routing on the board as shown in Figure 1.

Stereo audio outputs can be monitored on the 1/8" jacks J21 or J40. HP jack J21 can be used to connect a real headphone to provide an actual headphone load while performance measurements are taken on HP jack J40. Digital S/PDIF input can be provided on the optical (OPT2) or RCA (J68) jacks. Jumpers J8 and J9 can be used to select output loads and jumpers J1 and J2 can be used to select filtered or unfiltered outputs. Refer to Section 4 on page 11 for details on software configuration.



Figure 1. SPDIF In to Headphone or Line Out

Table 1 shows the expected performance characteristics one should expect when using the CDB43L22 for SPDIF In to Headphone or Line Out measurements.

Plot	Location
FFT - S/PDIF Input to HP Output @ -1dBFS	Figure 19 on page 29
FFT - S/PDIF Input to HP Output @ -60dBFS	Figure 20 on page 29
THD+N vs. HP Output Power	Figure 21 on page 29
Frequency Response- S/PDIF Input to HP Output @ 0dBFS	Figure 22 on page 29
THD+N - S/PDIF Input to HP Output	Figure 23 on page 29
Dynamic Range- S/PDIF Input to HP Output @ -60dBFS	Figure 24 on page 29



3.2 SPDIF In to Stereo Speaker Out

The CS43L22's stereo differential PWM speaker output performance can be tested by loading the "**SPDIF In to Stereo Speaker Out**" quick setup file provided with the software package. The script configures the digital clock and data signal routing on the board as shown in Figure 2.

Stereo output jacks J6 and J18 can be used to monitor filtered PWM output for measurement purposes. The figure shows how a real speaker or a speaker model should attach to the binding posts during performace tests. Digital S/PDIF input can be provided on the optical (OPT2) or RCA (J68) jacks. Refer to Section 4 on page 11 for details on software configuration.



Figure 2. SPDIF In to Stereo Speaker Out

Table 2 shows the expected performance characteristics one should expect when using the CDB43L22 for SPDIF In to Stereo Speaker Out measurements.

Plot	Location
FFT - S/PDIF In to Speaker Out @ 0 dBFS	Figure 25 on page 30
FFT - S/PDIF In to Speaker Out @ -60 dBFS	Figure 26 on page 30
Frequency Response- S/PDIF In to Speaker Out	Figure 27 on page 30
THD+N - S/PDIF In to Speaker Out	Figure 28 on page 30
THD+N vs. Output Power- S/PDIF In to Speaker Out	Figure 29 on page 30

Table 2. SPDIF In to Stereo Speaker Out Performance Plots



3.3 SPDIF In to Mono Speaker Out

The CS43L22's mono differential PWM speaker output performance can be tested by loading the "**SPDIF In to Mono Speaker Out**" quick setup file provided with the software package. The script configures the digital clock and data signal routing on the board as shown in Figure 2.

Stereo output jacks J6 and J18 can be used to monitor filtered PWM output for measurement purposes. The figure shows how a real speaker or a speaker model should attach to the binding posts during performace tests. Please note how ONLY the tip from the stereo jacks is used to attach the mono differential channel to the measurement device. Digital S/PDIF input can be provided on the optical (OPT2) or RCA (J68) jacks. Refer to Section 4 on page 11 for details on software configuration.



Figure 3. SPDIF In to Mono Speaker Out

 Table 3 shows the expected performance characteristics one should expect when using the CDB43L22

 for SPDIF In to Mono Speaker Out measurements.

Plot	Location
THD+N vs. Output Power- S/PDIF In to Speaker Out	Figure 30 on page 30

Table 3. SPDIF In to Mono Speaker Out Performance Plots



4. SOFTWARE MODE CONTROL

The CDB43L22 may be used with the Microsoft Windows[®]-based FlexGUI graphical user interface, allowing software control of the CS43L22, FPGA and CS8416 registers. The latest control software may be downloaded from www.cirrus.com/msasoftware. Step-by-step instructions for setting up the FlexGUI are provided as follows:

- 1. Download and install the FlexGUI software as instructed on the Website.
- 2. Connect and apply power to the +5.0 VP binding post.
- 3. Connect the CDB to the host PC using a USB cable.
- 4. Launch the Cirrus FlexGUI. Once the GUI is launched successfully, all registers are set to their default reset state.
- 5. Refresh the GUI by clicking on the "Update" button. The default state of all registers are now visible.

For standard set-up:

- 6. Set up the signal routing in the "Board Configuration" tab as desired.
- 7. Set up the CS43L22 in the "Passthrough, Power and Serial Audio Interface Configuration", "DSP Engine" and "Analog and PWM Output Volume" tab as desired.
- 8. Begin evaluating the CS43L22.

For quick set-up, the CDB43L22 may, alternatively, be configured by loading a predefined sample script file:

Cirrus FlexGUI System DEMO MODE		
File	Options Help	
Sa	ave Board Registers	
R	estore Board Registers	Power and Serial Au
E)	kit	
	- Quick-Setups	

- 9. On the File menu, click "Restore Board Registers..."
- 10. Browse to Boards\CDB43L22\Scripts\.
- 11. Choose any one of the provided scripts to begin evaluation.

To create personal scripts files:

Cirrus FlexGUI System DEMO MODE				
File	Options Help			
Sa	ave Board Registers			
Restore Board Registers Power and Serial				
E:	kit			
	Quick-Setups	,		

- 12. On the File menu, click "Save Board Registers..."
- 13. Enter any name that sufficiently describes the created setup.
- 14. Choose the desired location and save the script.
- 15. To load this script, follow the instructions from step 9 above.



4.1 Board Configuration Tab

The "Board Configuration" tab provides high-level control of signal routing on the CDB43L22. This tab also includes basic controls that allow "quick setup" in a number of simple board configurations. Status text detailing the CS43L22's specific configuration appears directly below the associated control. This text may change depending on the setting of the associated control. A description of each control group is outlined below:

CS43L22 Basic Configuration - Includes controls for configuring the interface format, clocking functions and analog input signal routing in the CS43L22. See Section 4.2 through Section 4.4 for more controls in the CS43L22.

CS8416 S/PDIF Receiver Control - Register controls for setting up the CS8416.

Clock Source and Routing Selection - Includes controls used to configure the value and source of the master, frame and bit clocks which are sent to the CS43L22.

Update - Reads all registers in the FPGA, CS43L22 and the CS8416 and shows the current values in the GUI.

Reset - Resets FPGA to default routing configuration.

ard Configuratio	Passthru,Power and Seri	al Audio Interface Configuration DSP E	ngine Analog and PWM Ou	tput Volume Register M	1aps	
Quick-Set	ups			CS8421 SRC Cont	rol	
				SRC In/SRC Out:	N/A	•
	Make Selection		-	Input Format:	N/A	•
				Output Format:	Left-Justified 32-bit	•
On-board	d Oscillator (Y6) a MCLK to CODEC by 2 ar Down PLL . Osc.(Y6)->Derive SCLK and Basic Configuration	CS8416 S. Enable Devic ILRCK(Fs): RMCK Free	/PDIF Receiver Control	▼ ▼	CS43L22 Bouting for	
CS43L22	Power Status	✓ Auto-Detect Speed Speed setting ignored	Speed: Single (4 kHz - 50 kHz)		So following for.	•
Initial Po	ower State	🦳 Fs = 8 kHz, 16 kHz or 32 kHz	Internal MCLK/LRCK Ra 128	atio:		
DAC Dig	ital Interface Format:	Master Clock ÷2 MCLK is 27 MHz SCLK = MCLK=12.0000 MHz (mother mode ONLY)	, Serial Port Master LRCK and SCLK are inp Quick-Setup (Input MCL)	outs K, Fs):		

Figure 4. Board Configuration Tab



4.2 Passthrough, Power and Serial Audio Interface Configuration Tab

The "Passthrough, Power and Serial Audio Interface Configuration" Tab provides high-level control of the CS43L22 passthrough, power control and serial port register settings. Status text detailing the CS43L22's specific configuration is shown in parenthesis or appears directly below the associated control. This text will change depending on the setting of the associated control. A description of each group is outlined below. See the CS43L22 data sheet for complete register descriptions.

Power Control - Register controls for powering down each section within the CS43L22.

Analog Passthrough Configuration - Controls for the input mixer (summing amp) and analog passthrough settings.

Serial Port Configuration - Controls for all settings related to the serial I/O data and clocks on the board.

Update - Reads all registers in the CS43L22 and reflects the current values in the GUI.

Reset - Resets the CS43L22.

ower and Serial Audio Interface Configuration $\Big _{DSF}$	P Engine Analog and PWM Output Vol	ume Register Maps
wer Control CS43L22 Power Status Initial Power State	Headphone Ch. A is S ON when pin 31 is LC V Headphone Ch. B is S ON when pin 31 is LC V	peaker Ch. A is DN when pin 31 is HI ▼ Switch, pin 31, L0 ipeaker Ch. B is DN when pin 31 is HI▼
onfiguration		
Passthru A		Passthru B
Changes □ Mute □ Mute □ 0.0 dB □ Soft Ramp □ Zero-Cross	 ✓ AIN1 ✓ AIN2 ✓ AIN3 ✓ AIN4 Passthrough Gain cha without a soft ramp on zero crossings 	nges
		1
Speed (Allowed Sample Rates): Single (4 kHz - 50 kHz)	Internal MCLK/LRCK Ratio:	DAC Digital Interface Format:
I Auto-Detect Speed Speed setting ignored I Fs = 8 kHz, 16 kHz or 32 kHz	MCLK is 27 MHz Master Clock ÷2 SCLK = MCLK= 12.0000 MHz (master mode ONLY) Invert SCLK	Left-Justified 24-bit or DSP DSP Mode bit depth is-32 (DSP Mode)24 (RJ-DAC) Update Beset
	ver Control CS43L22 Power Status Initial Power State fect immediately onfiguration Passthru A 0.0 dB Soft Ramp Zero-Cross Passthrough Channel A is disabled Mute Speed (Allowed Sample Rates): Single (4 kHz - 50 kHz) X Auto-Detect Speed Speed setting ignored Fs = 8 kHz, 16 kHz or 32 kHz	ver Control Headphone Ch. A is S CS43L22 Power Status ON when pin 31 is LC I Initial Power State Initial Power State Initial Power State I fect immediately Gang channels B to A ON when pin 31 is LC I fect immediately Gang channels B to A I IIII IIIIIIIIIIIIIIIIIIIIIIIIIIIIIIII

Figure 5. Passthrough, Power and Serial Audio Interface Configuration Tab



4.3 DSP Engine Tab

The "DSP Engine" tab provides high-level control of the SDIN (PCM) data volume level, the PCM mix volume level and the overall DAC/PWM channel volume level. DAC/PWM channel Limiter, Tone Control and Beep Generator control functions are also provided. Status text detailing the CS43L22's specific configuration is shown in parenthesis or inside the control group of the affected control. This text will change depending on the setting of the associated control. A description of each control group is outlined below. See the CS43L22 datasheet for complete register descriptions.

Digital Volume Control - Digital volume controls and adjustments for the SDIN data and overall channel volume. Mute, gang, invert and de-emphasis functions are also available.

Limiter - Configuration settings for the Limiter.

Tone Control - Bass and treble volume controls and filter corner frequencies.

Beep Generator - On/Off time, frequency, volume, mix and repeat beep functions.

Update - Reads all registers in the CS43L22 and reflects the current values in the GUI.

Reset - Resets the CS43L22.

Cirrus FlexGUI System DEMO MODE Elle Options Help Board Configuration Passthru, Power and Serial Audio Interface Configuration	SP Engine Analog and PWM Output Volume Regist	er Maps
Digital Volume Control Master AOUTA 0.0 dB 0.0 dB Image: Status: Mute Mute Mute PCM A Mix Image: Status: Image: Status: <td>Limiter Max Min Max Min OdB OdB OdB OdB OdB OdB IIIII Attack Rate: (Slow) Release Rate: (Slow) BEEP Generator Repeat Volume OdB Disable Mix w/Digital Input OFF Time IIIIII Short) Chord Disable Mix w/Digital Input OFF Time IIIIIII Chord Disable Mix w/Digital Input OFF Time IIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIII</td> <td>Tone Control Bass 0.0 dB II III Frequency: 50 Hz SKH2 DSP Status Ch. A: No Clipping No Clipping Vo Clipping</td>	Limiter Max Min Max Min OdB OdB OdB OdB OdB OdB IIIII Attack Rate: (Slow) Release Rate: (Slow) BEEP Generator Repeat Volume OdB Disable Mix w/Digital Input OFF Time IIIIII Short) Chord Disable Mix w/Digital Input OFF Time IIIIIII Chord Disable Mix w/Digital Input OFF Time IIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIII	Tone Control Bass 0.0 dB II III Frequency: 50 Hz SKH2 DSP Status Ch. A: No Clipping No Clipping Vo Clipping

Figure 6. DSP Engine Tab



4.4 Analog and PWM Output Volume Tab

The "Analog and PWM Output Volume" tab provides high-level control of the CS43L22 PWM outputs, HP/Line output volume levels and charge pump frequency. This tab also provides controls for the PWM output including speaker volume and PWM gain. Temperature and Battery monitoring controls for the PWM/Speaker outputs are also on this tab. Status text detailing the CS43L22's specific configuration is shown in read-only edit boxes, in parenthesis or appears directly below the associated control. This text will change depending on the setting of the associated control. A description of each control group is outlined below. See the CS43L22 datasheet for complete register descriptions.

Headphone/Line Analog Output - Volume controls and adjustments for the DAC channel (outside of the DSP). The modulation index and gain settings make up the parameters that determine the full scale headphone/line output level.

PWM Output - Volume, mute, power down and other functional controls for the PWM speaker outputs.

Temperature and Battery Monitor/Control - Battery Compensation, Thermal Foldback, Temperature Shutdown and Battery Monitor for the PWM/Speaker outputs.

Board Configuration Passthru,Power and Serial Audio Interface Configuration DSP Engine Analog and PWM Output Volume Register Maps PWM Output Temperature and Battery Monitor/Control Speaker A Speaker B Shut down speakers when die temperature exceeds safe operating levels(error status). RELEASE Build output Image: Status of the status o
Board Configuration Passthru, Power and Serial Audio Interface Configuration DSP Engine Analog and PWM Output Volume Register Maps PWM Output Speaker A Speaker B Speaker B Shut down speakers when die temperature exceeds safe operating levels(error status). RELEASE SHUTDOWN (Die temperature is still within safe levels.) . . . Thermal Foldback Battery Compensation . .
PwM Output Temperature and Battery Monitor/Control Speaker A Speaker B 0.0 dB 0.0 dB 0.1 dB 0.0 dB 0.0 dB
Image: Status: Gang channels B to A Mute with 50/50 duty cycle when die temperature approaches thermal error. Image: Status: Alt digital volume changes: when die temperature approaches thermal error. Image: Status: Image: Status: Status: Image: Status: Image:

Figure 7. Analog and PWM Output Volume Tab



4.5 Register Maps Tab

The Register Maps tabs provide low-level control of the CS43L22, CS8416, CS8421, FPGA and GPIO register settings. Register values can be modified bit-wise or byte-wise. "Left-clicking" on a particular register accesses that register and shows its contents at the bottom. The user can change the register contents by using the push-buttons, by selecting a particular bit and typing in the new bit value or by selecting the register in the map and typing in a new hex value.

otions																			_
	Help																		
rd Coofi	Figuration	Deceth	Dru Dowe	ar and Sa	riəl Ölüdir	o Interfa	ce Confi	auration		aine Ì àr	nalog ap	d DWM (Subout V	duma F	Register I	Mans			
	nyuracion	r Fassu	110,0000			o Incena	ce com	yuracion	I DOF LI		nalog an	u F WING	Jacpac vi	June .					
CS43		CS8416	6 - S/PE	DIF Rx	CS84	121 - S	RC	PGA	GPIO									1	
	00	01	02	03	04	05	06	07	08	09	0A	OB	0C	0D	0E	OF	1		
00	00	00	00		05	AO	00	00	81	81	A5		00	60	02	00	1		
10					00	00					00	00	00	00	00	88			
20	00	00	00	00	00	00	00	00	7F	C0					00	00			
30	00	00	ЗB	00	5F	00	08	08	68	14	C8	B7	BF	FF	FA	66			
40	60	40	D8	34	33	07	30	10	00	00	00	5D	15	00	A8	60			
50	04	E7	00	00	00	EO	00	00	00	00									
Reg	g: 00 A	ACCESS																	
Reg	g: 00 A	Access													00		-		
Reg	g: 00 A rec07	Access	; req06	1	reg05	1	regO	4	reg	03	re		1	reg01	00	reg00	-		
Reg	g: 00 A reg07	Access	reg06		reg05]	regO	4]	reg	13	re	:gO2	J	reg01		reg00	- -		
Reg Grid La	g: 00 A reg07 egend — Read/Wi	ACCESS	regO6		reg05 Only Rea		reg0	4	reg	03	re m Mode	gO2 Select:		reg01 Rese	00 et All	reg00	• Register		
Reg Grid La	g: 00 A reg07 	ACCESS	: reg06 ;ter <mark>0</mark>	0 Read	reg05 Only Reg] gister	reg0	4	regi Register	03 Com	re m Mode ²C	gO2 Select:		reg01 Reset I	00 et All Device	reg00	Register Device		
Reg Grid Ld	g: 00 A reg07 	xccess	reg06 ster 0		reg05 Only Ret] gister	reg0	4	regi Register)3 Com	re m Mode ²C	:gO2 Select:	J	reg01 Reset Release	00 et All Device d Reset	reg00 Update Update	Register Device		
Reg Grid La	g: 00 A reg07 	ACCESS	: reg06 :ter 0		reg05 Only Ret		reg0	4	regi Register	03 	re m Mode ²⊂	g02 Select:		reg01 Rese Reset I Release	00 et All Device d Reset	reg00 Update	Register Device		
Reg Grid La	g: 00 A reg07 	ACCESS	regO6	l	reg05 Only Ret] gister	reg0	4	regi Register	03 Com 	re ım Mode ²⊂	gO2 Select:		reg01 Reset Reset I Release	00 et All Device d Reset	reg00 Update Update	Register		

Figure 8. Register Maps Tab - CS43L22



5. SYSTEM CONNECTIONS AND JUMPERS

CONNECTOR	REF	INPUT/OUTPUT	SIGNAL PRESENT
VP	J35	Input	+2.7 V to +5.25 V Power Supply.
GND	J4	Input	Ground Reference.
USB	J94	Input/Output	USB connection to PC for I ² C control port signals.
S/PDIF OPTICAL IN	OPT3	Input	CS8416 digital audio input via optical cable.
S/PDIF COAX IN	J61	Input	CS8416 digital audio input via coaxial cable.
I/O Header	J8	Input/Output	I/O for Clocks & Data directly to/from the CS43L22.
S/W CONTROL	J109	Input/Output	I/O for external I ² C control port signals.
MICRO JTAG	J110	Input/Output	I/O for programming the micro controller (U84).
FPGA JTAG	J75	Input/Output	I/O for programming the FPGA (U5).
MICRO RESET	S4	Input	Reset for the micro controller (U84).
FPGA PROGRAM	S2	Input	Reload Xilinx program into the FPGA from Flash (U14).
H/W BOARD RESET	S1	Input	Reset for the CS43L22(U1).
AIN1	J33	Input	1/8" audio jacks for analog passthrough input signal to CS43L22.
AIN2	J37	Input	
AIN3	J45	Input	1/8" audio jacks for Line or MIC analog passthrough input signals to
AIN4	J50	Input	CS43L22.
A(RC LPF)	J6	Output	30 kHz LPF version of the signal on speaker binding posts (Used for mea-
	510	Output	Sulenient pulposes only).
SPEAKER A-	J60	Output	Full Bridge speaker outputs.
	J59 1101	Output	
SPEAKER B+	.199	Output	
HP/Line Output	140	Output	Stereo 1/8" jack for line outputs. When headphones are plugged in to HP
	540	Output	Connect (on .121) this output may be used for performance measure-
			ment.
HP Connect	J21	Output	Stereo headphone jack for Headphone outputs.
I/O HDR	J78	Input/Output	I/O for clocks and input for DAC SDIN. Signals are passed through the
			FPGA for muxing with the S/PDIF input.

Table 4. System Connections



6. JUMPER SETTINGS

JMP	LABEL	PURPOSE	POSITION	FUNCTION SELECTED
			*+1.8V	Voltage source is +1.8 V regulator.
J31	VL	Selects source of voltage for the	+2.5V	Voltage source is +2.5 V regulator.
			+3.3V	Voltage source is +3.3 V regulator.
		Selects source of voltage for the	*+1.8V	Voltage source is +1.8 V regulator.
130	VA_HP	VA_HP supply	+2.5V	Voltage source is +2.5 V regulator.
105		Selects source of voltage for the	*+1.8V	Voltage source is +1.8 V regulator.
J25 VA		VA supply	+2.5V	Voltage source is +2.5 V regulator.
100		Selects source of voltage for the	*+1.8V	Voltage source is +1.8 V regulator.
J20	VD	VD supply	+2.5V	Voltage source is +2.5 V regulator.
J52	VL		*SHUNTED	1 Ω series resistor is shorted.
J47 J74 J53	+VA_HP VA VD	Current Measurement	OPEN	1 Ω series resistor in power supply path.
J48	VP	Current measurement	*SHUNTED	VP supply to CS43L22 is selected.
J13		Applies a filtered or a non-filtered	*1 - 2	SPKOUTA- output routed to J60.
J14	[No Label]	version of the SPKA- signal to J60	2 - 3	SPKOUTA- output not routed to J60.
J16		Applies a filtered or a non-filtered	*1 - 2	SPKOUTA+ output routed to J59.
J17	[No Label]	version of the SPKA+ signal to J59	2 - 3	SPKOUTA+ output not routed to J59.
144		Applies a filtered or a non-filtered	*1 - 2	SPKOUTB- output routed to J101.
J12	[No Label]	version of the SPKB- signal to J101	2 - 3	SPKOUTB- output not routed to J101.
J20		Applies a filtered or a non-filtered	*1 - 2	SPKOUTB+ output routed to J99.
J23		version of the SPKA- signal to J99	2 - 3	SPKOUTB+ output not routed to J99.
J15	MONO	Applies a short between SPKOUT A+ and A (Used only <u>after</u>	*OPEN	Channel A+ and A- to J59 and J60 respec- tively.
0.0		MONO function is enabled in the CS43L22)	SHUNTED	Channel + to J59 and J60 respectively.
J19	MONO	Applies a short between SPKOUT B+ and B (Used only <u>after</u>	*OPEN	Channel B+ and B- to J99 and J101 respec- tively.
		MONO function is enabled in the CS43L22)	SHUNTED	Channel - to J99 and J101 respectively.
.13		Selects 32 or 16 Ω load for	1 - 2	16 Ω load selected.
00		HP/LINE_OUTB (DAC out)	2 - 3	32 Ω load selected.
.19		Selects 32 or 16 Ω load for	1 - 2	16 Ω load selected.
		HP/LINE_OUTA (DAC out)	2 - 3	32 Ω load selected.
		Selects between a filtered or non	1 - 2	Non-filtered HP/LINE_OUTA to HP/Line Jack.
J1	LEFT CH	filtered version of the HP/LINE_OUTA signal.	*2 - 3	Filtered HP/LINE_OUTA to HP/Line Jack.
10		Selects between a filtered or non	1 - 2	Non-filtered HP/LINE_OUTA to HP/Line Jack.
JZ	RIGHT CH	HP/LINE_OUTB signal.	*2 - 3	Filtered HP/LINE_OUTA to HP/Line Jack.
J22	HP DETECT	Selects the control source for the	1 - 2	FPGA.
	221201	SPKR/HP pin	*2 - 3	HP Jack.
10.1		Selects either USB or External	1 - 2	External +5 V power.
J34	Board Power	+5 V power for the board	*2 - 3	USB generated +5 V power. (USB hub must be capable of greater than 300 mA)
		Selects either External or Battery	*1 - 2	External from J35.
J5	VP	power for VP and for the buck reg- ulators that powers VA, VA_HP and VD	2 - 3	Battery from BT1-BT3 (bottom side)

Table 5. Jumper Settings

7. CDB43L22 BLOCK DIAGRAM





Figure 9. Block Diagram

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8 | 8. CDB43L22 SCHEMATICS



Figure 10. CS43L22 & Analog I/O (Schematic Sheet 1)

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DS792DB1





Figure 11. S/PDIF & Digital Interface (Schematic Sheet 2)

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Figure 12. Micro & FPGA Control (Schematic Sheet 3)

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DS792DB1





Figure 13. Power (Schematic Sheet 4)

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♀ | 9. CDB43L22 LAYOUT



Figure 14. Silk Screen

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Figure 15. Top-Side Layer

CDB43L22

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Figure 16. GND (Layer 2)



Figure 17. Power (Layer 3)

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Figure 18. Bottom-Side Layer



CDB43L22



10.PERFORMANCE PLOTS

Test conditions (unless otherwise specified): Measurement bandwidth is 20 Hz to 20 kHz (unweighted); VA=VD=VA_HP=1.8V; Sample Frequency = 48 kHz; HP test load: R_1 = 16 Ω .



Figure 19. FFT - S/PDIF Input to HP Output @ -1 dBFS



Figure 21. THD+N vs. HP Output Power





Figure 20. FFT - S/PDIF Input to HP Output @ -60 dBFS



Figure 22. Freq. Resp. - S/PDIF Input to HP Output









Figure 25. FFT - S/PDIF In to Speaker Out @ 0 dBFS



Figure 27. Frequency Response - S/PDIF In to Speaker Out



Figure 29. THD+N vs. Output Power (Stereo)



Figure 26. FFT - S/PDIF In to Speaker Out @ -60 dBFS



%

Figure 28. THD+N - S/PDIF In to Speaker Out



Figure 30. THD+N vs. Output Power (Mono)



11.REVISION HISTORY

Revision	Changes
DB1	Initial Release

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative. To find the one nearest you, go to www.cirrus.com.

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