Automotive Serial EEPROMs

125℃ SPI BUS ICs

BR35□□□□ Family

BR35H□□□-WC Series

No.11001ECT09

●Description

BR35H□□□-WC Series is a SPI BUS interface method serial EEPROM.

●Features

1) High speed clock operation up to 5MHz(Max.)
2) 2.5V to 5.5V single power source operation most suitable for battery use.
3) Page write mode useful for initial value at factory shipment.
4) Highly reliable connection by Au pad and Au wire.
5) For SPI bus interface (CPOL,CPHA)=(0,0),(1,1)
6) Auto erase and auto end function at data rewrite.
7) Low operating current
   At write operation (5V): 0.6mA(Typ.)
   At read operation (5V): 1.3mA(Typ.)
   At standby operation (5V): 0.1μA(Typ.)
8) Address auto increment function at read operation.
9) Write mistake prevention function
   Write prohibition at power on.
   Write prohibition by command code (WRDI)
   Write mistake prevention function at low voltage.
10) MSOP8 / TSSOP-B8 / SOP8 / SOP-J8 Package.
11) Data at shipment Memory array:FFh.
12) Data Retention : 20 years(Ta≦125℃)
13) Endurance : 300,000 cycles(Ta≦125℃)

●Page Write

Number of pages	32Byte	64Byte
Product number	BR35H160-WC BR35H320-WC BR35H640-WC	BR35H128-WC

●BR35H□□□ Series

Capacity	Bit Format	Product Name	Supply Voltage	MSOP8	TSSOP-B8	SOP8	SOP-J8
16Kbit	2K×8	BR35H160-WC	2.5～5.5V	●	●	●	●
32Kbit	4K×8	BR35H320-WC	2.5～5.5V	●	●	●	●
64Kbit	8K×8	BR35H640-WC	2.5～5.5V	−	●	●	●
128Kbit	16Kx8	BR35H128-WC	2.5～5.5V	−	−	●	●

●Absolute Maximum Ratings (Ta=25℃)

Parameter	Symbol	Limits	Unit
Impressed Voltage	Vcc	-0.3 to +6.5	V
Permissible Dissipation	Pd	560(SOP8) *1	mW
		560(SOP-J8) *2	
		410(TSSOP-B8) *3	
		380(MSOP8) *4	
Storage Temperature Range	Tstg	-65 to +150	℃
Operating Temperature Range	Topr	-40 to +125	℃
Terminal Voltage	-	-0.3 toVcc+0.3	V

∗ When using at Ta=25℃ or higher, 4.5mW (*1,*2), 3.3mW (*3) , 3.1 mW (*4)to be reduced per 1℃

●Recommended Operating Conditions

Parameter	Symbol	Limits	Unit
Supply Voltage	Vcc	2.5 to 5.5	V
Input Voltage	Vin	0 to Vcc	

●Memory Cell Characteristics (Vcc=2.5V to 5.5V)

Parameter	Limits			Unit	Condition
	Min.	Typ.	Max.		
Endurance *5	1,000,000	-	-	Cycles	Ta≦85℃
	500,000	-	-	Cycles	Ta≦105℃
	300,000	-	-	Cycles	Ta≦125℃
Data Retention *5	40	-	-	Years	Ta≦25℃
	25	-	-	Years	Ta≦105℃
	20	-	-	Years	Ta≦125℃

*5:Not 100% TESTED

●Input / Output Capacitance (Ta=25℃, frequency=5MHz)

Parameter	Symbol	Conditions	Min.	Max.	Unit
Input Capacitance *6	C_{IN}	V_{IN}=GND	—	8	pF
Output Capacitance *6	C_{OUT}	V_{OUT}=GND	—	8	

*6:Not 100% TESTED

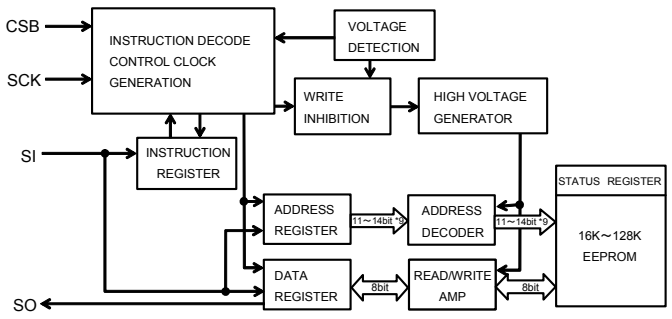
●Electrical Characteristics (Unless otherwise specified, Ta=-40 to +125℃, Vcc=2.5 to 5.5V)

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
“H” Input Voltage	VIH	0.7xVcc	—	Vcc+0.3	V	2.5V≦Vcc≦5.5V
“L” Input Voltage	VIL	-0.3	—	0.3xVcc	V	2.5V≦Vcc≦5.5V
“L” Output Voltage	VOL	0	—	0.4	V	IOL=2.1mA
“H” Output Voltage	VOH	Vcc-0.5	—	Vcc	V	IOH=-0.4mA
Input Leakage Current	ILI	-10	—	10	μA	VIN=0V to Vcc
Output Leakage Current	ILO	-10	—	10	μA	VOUT=0V to Vcc, CSB=Vcc
Operating Current (Write)	ICC1	—	—	2.0 *7	mA	Vcc=2.5V,fSCK=5MHz, tE/W=5ms, VIH/VIL=0.9Vcc/0.1Vcc, SO=OPEN Byte Wrte, Page Write
				2.5 *8		
	ICC2	—	—	3.0 *7	mA	Vcc=5.5V,fSCK=5MHz, tE/W=5ms, VIH/VIL=0.9Vcc/0.1Vcc, SO=OPEN Byte Wirte, Page Write
				5.5 *8		
Operating Current (Read)	ICC3	—	—	1.5	mA	Vcc=2.5V,fSCK=5MHz, VIH/VIL=0.9Vcc/0.1Vcc SO=OPEN, Read, Read Status Register
	ICC4	—	—	2.0	mA	Vcc=5.5V,fSCK=5MHz, VIH/VIL=0.9Vcc/0.1Vcc SO=OPEN, Read, Read Status Register
Standby Current	ISB	—	—	10	μA	Vcc=5.5V CSB=Vcc, SCK=SI=Vcc or GND, SO=OPEN

* This product is not designed for protection against radioactive rays.

*7 BR35H160/320-WC *8 BR35H640/128-WC

●Block Diagram



*9 11bit: BR35H160-WC
12bit: BR35H320-WC
13bit: BR35H640-WC
14bit: BR35H128-WC

Fig.1 Block Diagram

●Pin Assignment and Description

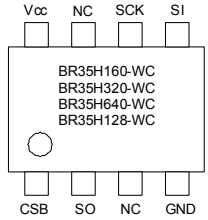


Fig.2 Pin Assignment Diagram

Terminal Name	Input/Output	Function
Vcc	–	Power Supply to be connected
GND	–	All input / output reference voltage, 0V
CSB	Input	Chip select input
SCK	Input	Serial clock input
SI	Input	Start bit, ope code, address, and serial data input
SO	Output	Serial data output
NC	–	Non connection

●Operating Timing Characteristics

(Ta=-40℃ to +125℃, unless otherwise specified, load capacitance C_{L1}=100pF)

Parameter	Symbol	2.5≦Vcc≦5.5V			Unit
		Min.	Typ.	Max.	
SCK frequency	fSCK	-	-	5	MHz
SCK high time	tSCKWH	85	-	-	ns
SCK low time	tSCKWL	85	-	-	ns
CSB high time	tCS	85	-	-	ns
CSB setup time	tCSS	90	-	-	ns
CSB hold time	tCSH	85	-	-	ns
SCK setup time	tSCKS	90	-	-	ns
SCK hold time	tSCKH	90	-	-	ns
SI setup time	tDIS	20	-	-	ns
SI hold time	tDIH	30	-	-	ns
Data output delay time1	tPD1	-	-	70	ns
Data output delay time2 (C_{L2}=30pF)	tPD2	-	-	55	ns
Output hold time	tOH	0	-	-	ns
Output disable time	tOZ	-	-	100	ns
SCK rise time	tRC	-	-	1	μs
SCK fall time *1	tFC	-	-	1	μs
OUTPUT rise time	tRO	-	-	50	ns
OUTPUT fall time	tFO	-	-	50	ns
Write time	tE/W	-	-	5	ms

*1 NOT 100% TESTED

●Sync data input / output timing

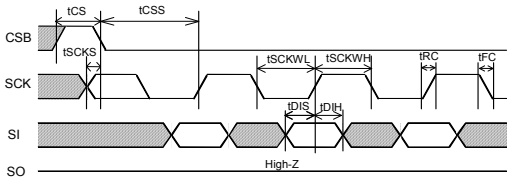


Fig.3 Input timing

Data through SI enters the IC in sync with the data rise edge of SCK. Please input address and data starting from the most significant bit MSB.

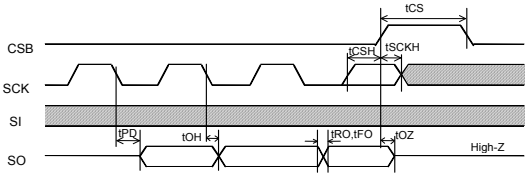


Fig.4 Input / Output timing

Data through SO is output in sync with the data fall edge of SCK. Data is output starting from the most significant bit MSB.

●AC measurement conditions

Parameter	Symbol	Limits			Unit
		Min.	Typ.	Max.	
Load capacitance 1	C_{L1}	-	-	100	pF
Load capacitance 2	C_{L2}	-	-	30	pF
Input rise time	-	-	-	50	ns
Input fall time	-	-	-	50	ns
Input voltage	-	0.2Vcc / 0.8Vcc			V
Input / Output judgment voltage	-	0.3Vcc / 0.7Vcc			V

●tOZ measurement condition

IL is the load current that changes the SO voltage to 0.5×Vcc. IL = ±1mA.

After CSB starts to rise, the time needed for SO to change to High-Z is defined with 10% changing point from SO=High or SO=Low.

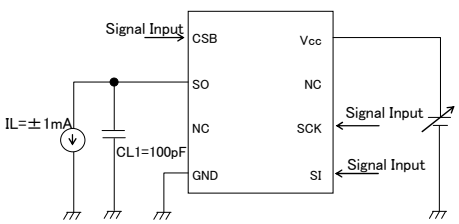


Fig.5 tOZ measurement circuit

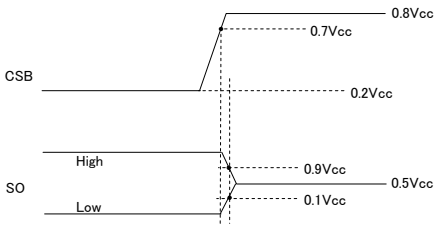


Fig.6 tOZ measurement timing

●Characteristics Data

(The following characteristic data are Typ. value.)

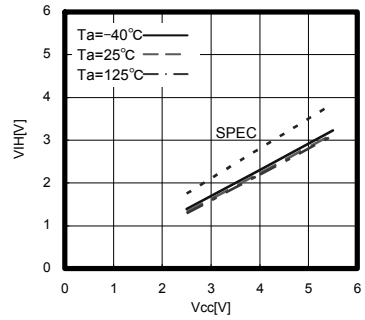


Fig.7 "H" input voltage VIH(CSB,SCK,SI)

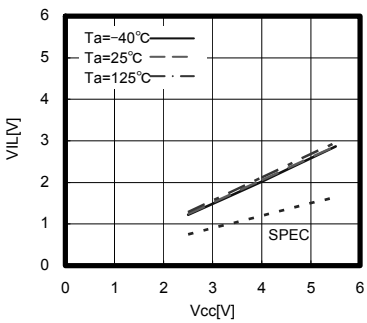


Fig.8 "L" input voltage VIL(CSB,SCK,SI)

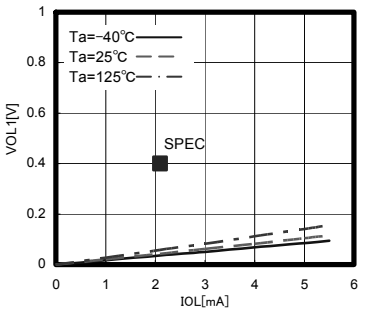


Fig.9 "L" output voltage VOL1 (Vcc=2.5V)

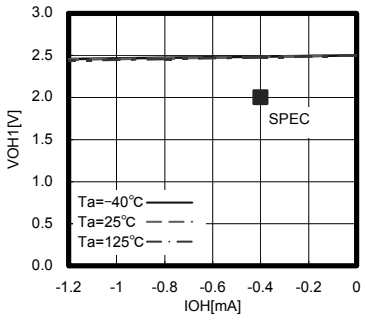


Fig.10 "H" output voltage VOH1 (Vcc=2.5V)

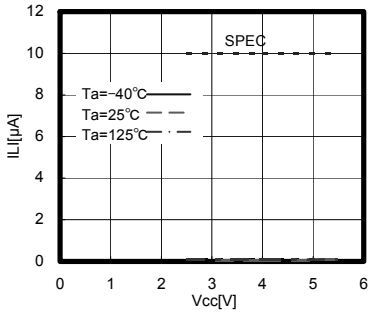


Fig.11 Input leak current ILI(CSB,SCK,SI)

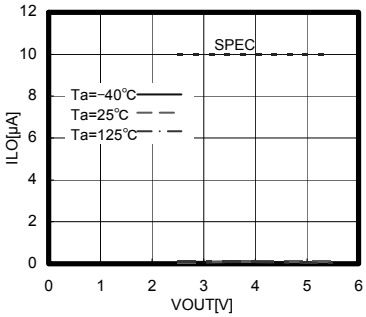


Fig.12 Output leak current ILO(SO)

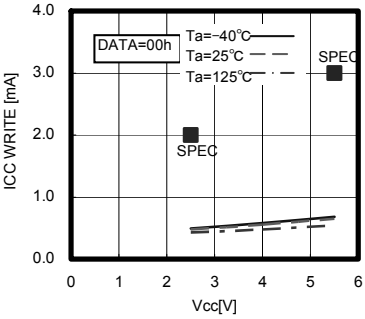


Fig.13 Operating Current (WRITE) ICC1,2
(BR35H160/320-WC)

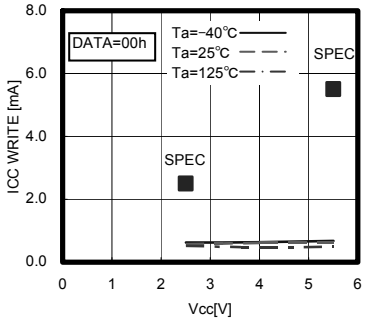


Fig.14 Operating Current (WRITE) ICC1,2
(BR35H640/128-WC)

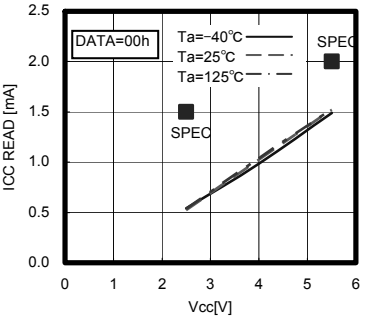


Fig.15 Operating Current (READ) ICC3,4

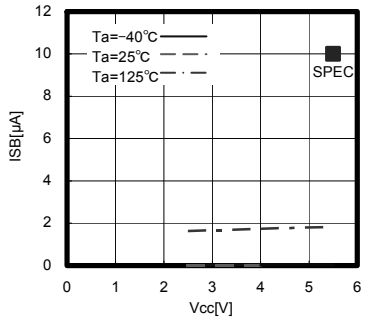


Fig.16 Standby Current ISB

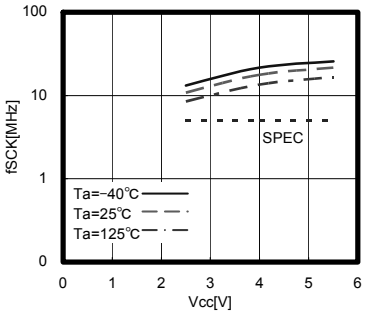


Fig.17 SCK frequency fSCK

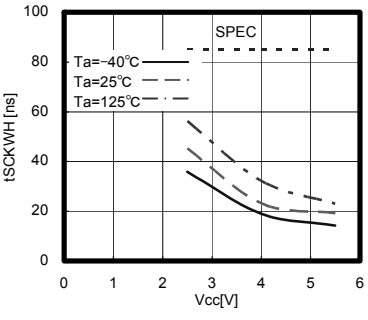


Fig.18 SCK high time tSCKWH

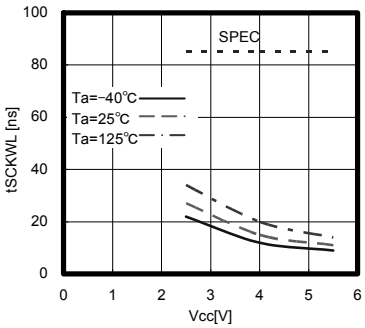


Fig.19 SCK low time tSCKWL

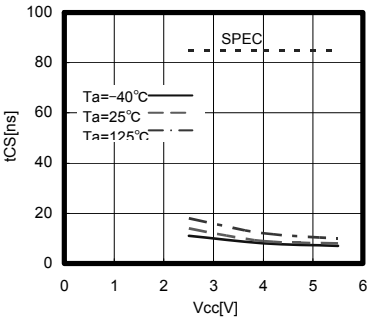


Fig.20 CSB high time tCS

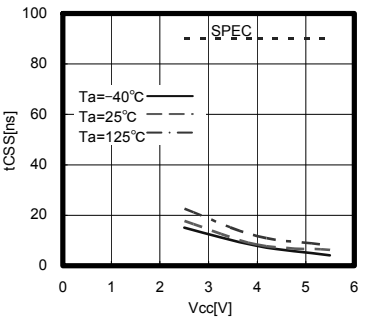


Fig.21 CSB setup time tCSS

●Characteristics Data

(The following characteristic data are Typ. value.)

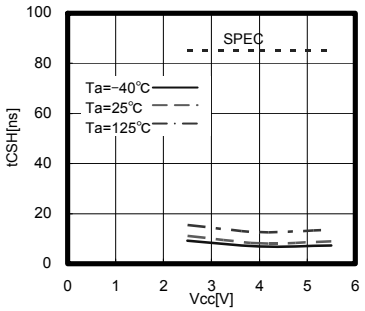


Fig.22 CSB hold time tCSH

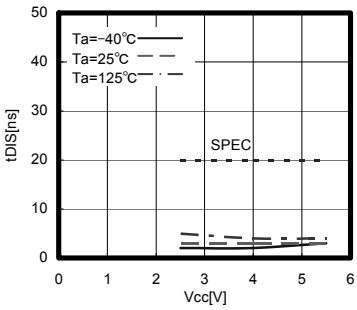


Fig.23 SI setup time tDIS

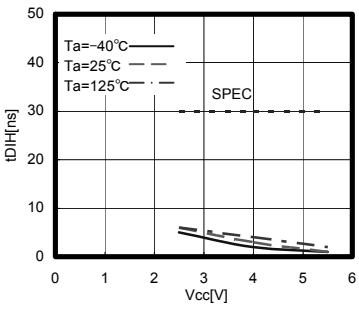


Fig.24 SI hold time tDIH

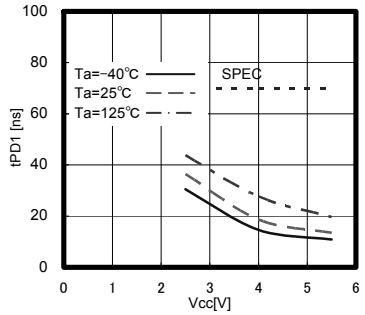


Fig.25 Data output delay time tPD1 (CL=100pF)

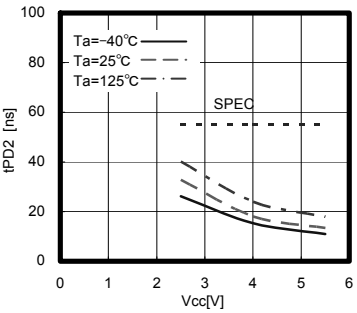


Fig.26 Data utput delay time tPD2

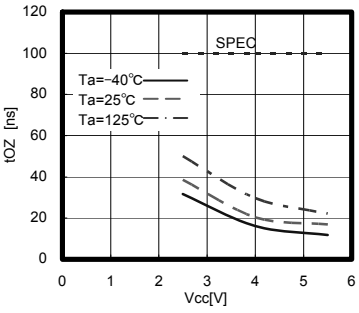


Fig.27 Output disable time tOZ

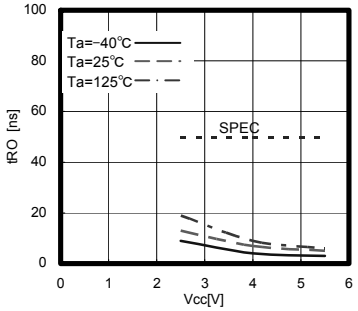


Fig.28 Output rise time tRO

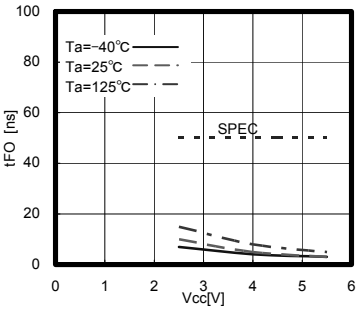


Fig.29 Output fall time tFO

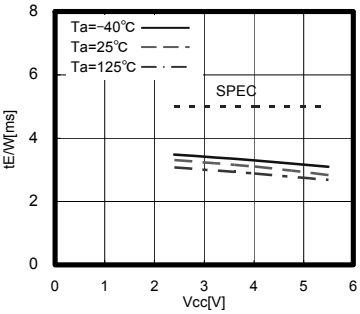


Fig.30 Write cycle time tE/W

●Features

○Status registers

This IC has status registers. The status register has 8 bits and expresses the following parameters.
WEN is set by the write enable command and write disable command. WEN goes into the write disable status when the power source is turned off. The $\overline{R}$/B bit is for write confirmation and therefore cannot be set externally.
The status register value can be read by use of the read status command.

●Status registers

Product Number	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
BR35H160-WC	0	0	0	0	0	0	WEN	$\overline{R}$/B
BR35H320-WC								
BR35H640-WC								
BR35H128-WC								

bit	Memory location	Function
WEN	Register	Write and write status register write enable / disable status confirmation bit WEN=0=prohibited WEN=1=permitted
$\overline{R}$/B	Register	Write cycle status (READY / BUSY) status confirmation bit $\overline{R}$/B=0=READY $\overline{R}$/B=1=BUSY

●Command mode

Command		Contents	Ope code	
			BR35H160-WC BR35H320-WC BR35H640-WC BR35H128-WC	
WREN	Write enable	Write enable command	0000	0110
WRDI	Write disable	Write disable command	0000	0100
READ	Read	Read command	0000	0011
WRITE	Write	Write command	0000	0010
RDSR	Read status register	Status register read command	0000	0101

●Timing chart

1. Write enable (WREN) / disable (WRDI) cycle

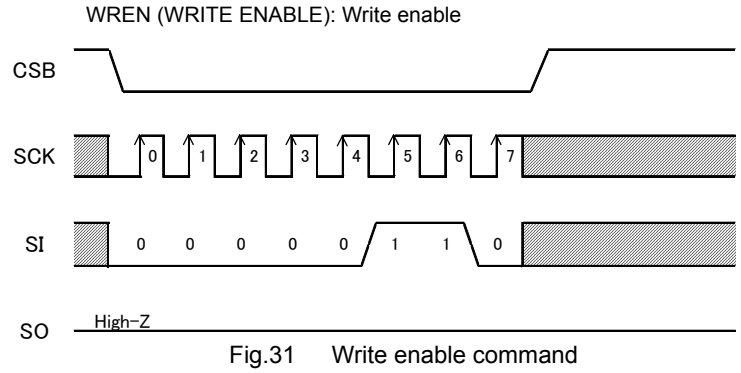


Fig.31 Write enable command

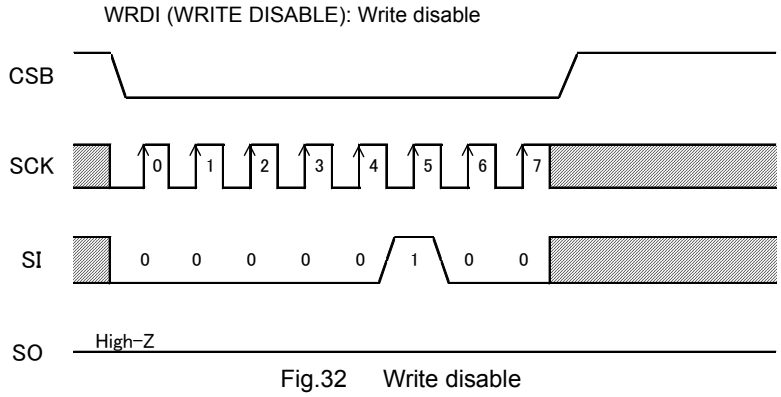
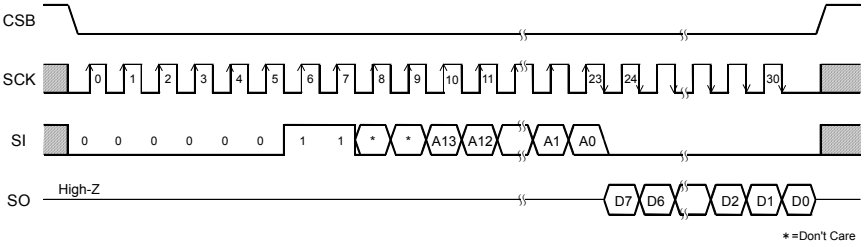


Fig.32 Write disable

○This IC has a write enable status and a write disable status. Write enable status is achieved by the write enable command and write disable status is achieved by the write disable command. As for these commands, set CSB to LOW and then input the respective ope codes. The respective commands are accepted at the 7-th clock rise. The command is also valid with Inputs over 7 clocks.
In order to perform a write command it is necessary to use the write enable command to set the IC to the write enable status. If a write command is input during write disable status the command will be cancelled. After a write command is input during write enable status the IC will return to the write disable status. When turning on the power the IC will be in write disable status.

2. Read command (READ)

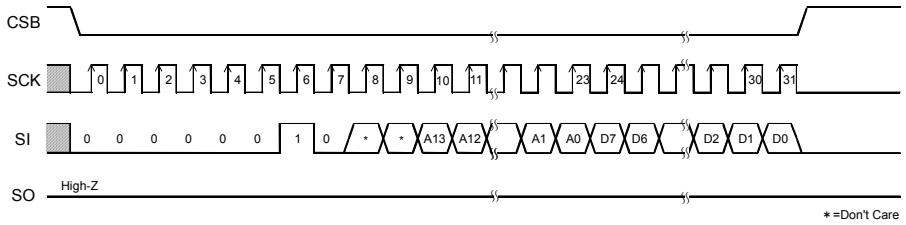


Product number	Address Length
BR35H160-WC	A10-A0
BR35H320-WC	A11-A0
BR35H640-WC	A12-A0
BR35H128-WC	A13-A0

Fig.33 Read command (BR35H160/320/640/128-WC)

By use of the read command, the data of the EEPROM can be read. As for this command, set CSB to LOW, then input the address after the read ope code. EEPROM starts data output of the designated address. Data output is started from the SCK fall of 23 clock and from D7 to D0 sequentially. The IC features an increment read function. After the output of 1 byte (8bits) of data, by continuing input of SCK the next data addresses can be read. Increment read can read all addresses of the EEPROM. After reading the data of the most the significant address, by continuing with the increment read the data of the most insignificant address is read.

3. Write command (WRITE)



Product number	Address Length
BR35H160-WC	A10-A0
BR35H320-WC	A11-A0
BR35H640-WC	A12-A0
BR35H128-WC	A13-A0

Fig.34 Write command (BR35H160/320/640/128-WC)

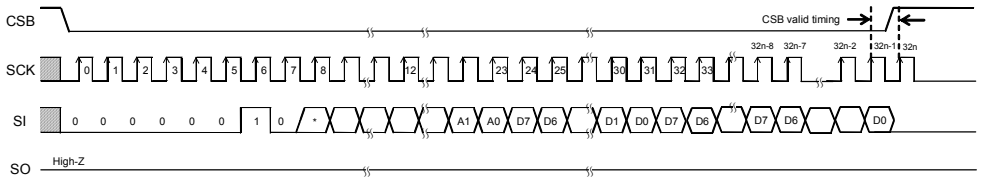


Fig.35 N Byte page write command (BR35H160/320/640-WC)

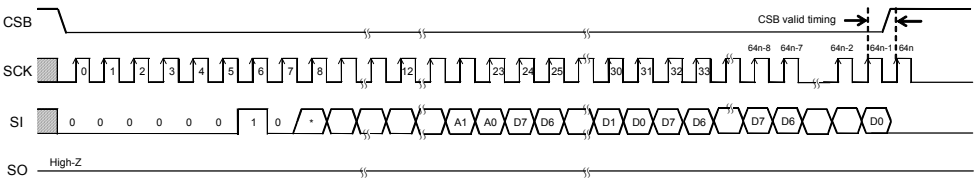


Fig.36 N Byte page write command (BR35H128-WC)

With the write command data can be written to the EEPROM. As for this command, set CSB to LOW, then input address and data after inputting the write ope code. Then, by making CSB HIGH, the EEPROM starts writing. The write time of EEPROM requires time of tE/W (Max 5ms). During tE/W, commands other than the status read command are not accepted. Start CSB after taking the last data (D0) and before the next SCK clock starts. At other timings the write command will not be executed and will be cancelled. The IC has page write functionality. After input 1 byte (8bits) of data, by continuing data input without starting CSB, data up to 32/64[*1] bytes can be written in one tE/W. In page write, the insignificant 5/6[*2] bit of the designated address is incremented internally every time 1 byte of data is input, and data is written to the respective addresses. When data larger then the maximum bytes is input the address rolls over and previously input data is overwritten.

Write command is executed when CSB rises between the SCK clock rising edge to recognize the 8th bit's of data input and the next SCK rising edge. At other timings the write command is not executed and cancelled (Fig.42 valid timing c). In page write, the CSB valid timing is every 8 bits. If CSB rises at other timings page write is cancelled together with the write command and the input data is reset.

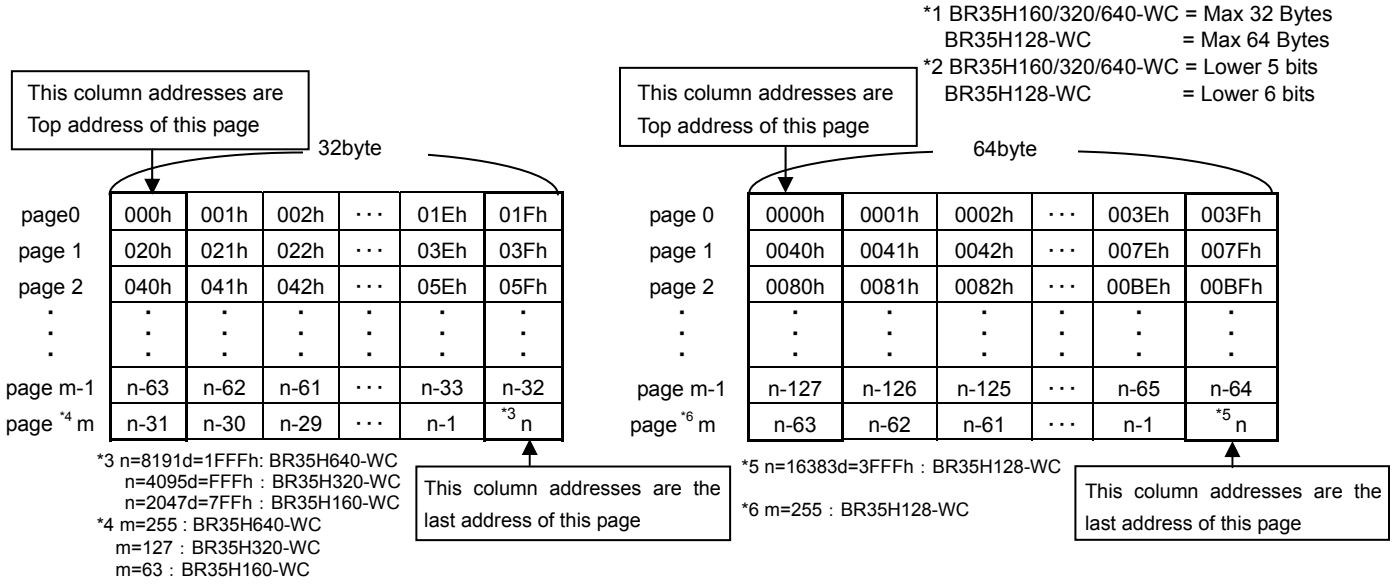


Fig.37 EEPROM physical address for Page write command (32/64Byte)

●**Example of Page write command**

No.	Addresses of Page0	000h	001h	002h	····	01Eh	01Fh
①	Previous data	00h	01h	02h	····	1Eh	1Fh
②	2 bytes input data	AAh	55h	-	····	-	-
③	After No.②	AAh	55h	02h	····	1Eh	1Fh
④	34 byte input data	AAh	55h	AAh	····	AAh	55h
		FFh	00h	-	····	-	-
⑤	After No.④	FFh	00h	AAh	····	AAh	55h

a : In case of input the data of No.② which is 2 bytes page write command for the data of No.①, EEPROM data changes like No.③.

b : In case of input the data of No.④ which is 34 bytes page write command for the data of No.①, EEPROM data changes like No.⑤.

c : In case of a or b, when write command is cancelled, EEPROM data keep No.①.

In page write command, when data is set to the last address of a page (e.g. address "03Fh" of page 1), the next data will be set to the top address of the same page (e.g. address "020h" of page 1). This is why page write address increment is available in the same page. As a reference, if of 32 bytes, page write command is executed for 2 bytes the data of the other 30 bytes without addresses will not be changed.

4.Status register read command

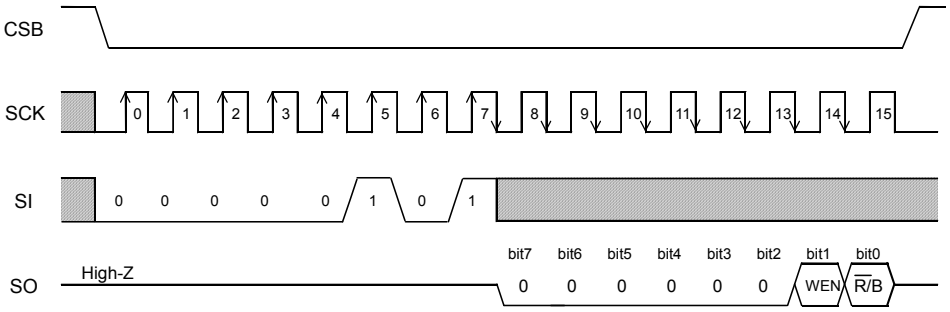


Fig.38 Status register read command (BR35H160/320/640/128-WC)

The EEPROM status can be read by use of the status register read command. For this command set CSB to Low then input the ope code of the status register read command followed by the clock input as shown above. The data of status register will then be read out. This command features increment functionality. When clock input is continued during CSB=Low, 8 bytes of status register data will be continuously read out. When this command is executed from the start of write programming to the end of write programming, the end of write programming can be confirmed by checking the following changes: WEN=Low followed by $\overline{R}$/B=Low. After confirming the end of write programming, before inputting the next command CSB first needs to be High and then put back to Low.

●At standby

○Current at standby

Set CSB “H”, and be sure to set SCK, SI input “L” or “H”. Do not input intermediate electric potantial.

○Timing

As shown in Fig.39, at standby, when SCK is “H”, even if CSB falls, SI status is not read at fall edge. SI status is read at SCK rise edge after fall of CSB. At standby and at power ON/OFF, set CSB “H” status

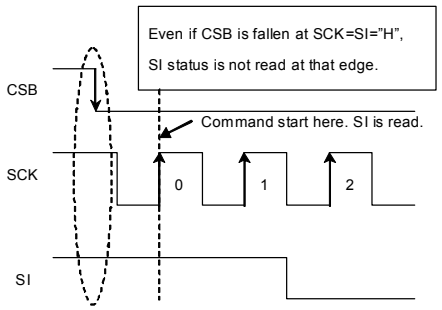


Fig.39 Operating timing

●Method to cancel each command

○READ

・Cancellation method: cancel by CSB = “H”

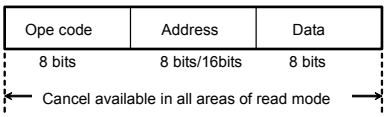


Fig.40 READ cancel valid timing

○RDSR

・Cancellation method: cancel by CSB = “H”

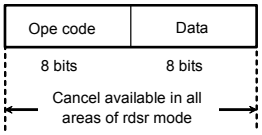


Fig.41 RDSR cancel valid timing

○WRITE, PAGE WRITE

a : Ope code, address input area.
Cancellation possible by CSB=”H”
b : Data input area (D7~D1 input area)
Cancellation possible by CSB=”H”
c : Data input area (D0 area)
Write starts after CSB rise.
After CSB rise, cancellation is no longer possible.
d : tE/W area.
Cancellation is possible by CSB = “H”. However, when write starts (CSB rise) in area c, cancellation is no longer possible. Also, cancellation is not possible by continues inputting of SCK clock. In page write mode, there is a write enable area at every 8 clocks.

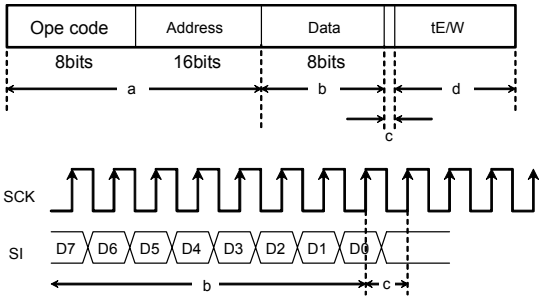


Fig.42 WRITE cancel valid timing

Note 1) If Vcc is set to OFF during execution of write the data of the designated address is not guaranteed. Please execute write again.
Note 2) If CSB rises at the same timing as that the SCK rises, write execution / cancel will become unstable. Therefore, it is recommended to let CSB rise in the SCK = “L” area. As for SCK rise, ensure a timing of tCSS / tCSH or higher.

○WREN/WRDI

a : From ope code to 7-th clock rise, cancel by CSB = “H”.
b : Cancellation is not possible when CSB rises after the 7-th clock.

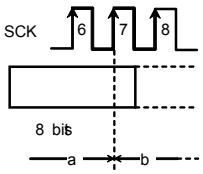


Fig.43 WREN/WRDI cancel valid timing

●High speed operations

In order to realize stable high speed operations, pay attention to the following input / output pin conditions.

○Input pin pull up, pull down resistance

When attaching pull up, pull down resistance to the EEPROM input pin, select an appropriate value for the microcontroller VOL, IOL from the VIL characteristics of this IC.

○Pull up resistance

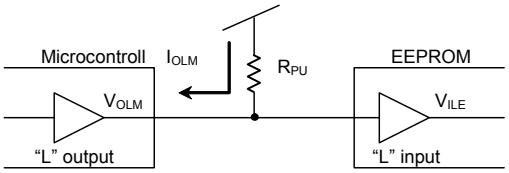


Fig.44 Pull up resistance

$$R_{PU} \geq \frac{V_{CC}-V_{OLM}}{I_{OLM}} \quad \cdots ①$$

$$V_{OLM} \leq V_{ILE} \quad \cdots ②$$

Example) When Vcc=5V, V_{ILE}=1.5V, V_{OLM}=0.4V, I_{OLM}=2mA, from the equation ①,

$$R_{PU} \geqq \frac{5-0.4}{2\times10^{-3}}$$

$$\therefore R_{PU} \geqq 2.3[k\Omega]$$

With the value of Rpu to satisfy the above equation, V_{OLM} becomes 0.4V or lower, and with V_{ILE} (=1.5V), the equation ② is also satisfied.

- V_{ILE} :EEPROM V_{IL} specifications
- V_{OLM} :Microcontroller V_{OL} specifications
- I_{OLM} :Microcontroller I_{OL} specifications

Also, in order to prevent malfunction or erroneous write at power ON/OFF, be sure to make CSB pull up.

○Pull down resistance

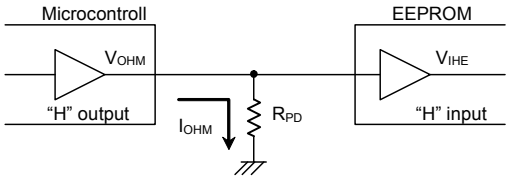


Fig.45 Pull down resistance

$$R_{PD} \geqq \frac{V_{OHM}}{I_{OHM}} \quad \cdots ③$$

$$V_{OHM} \geqq V_{IHE} \quad \cdots ④$$

Example) When V_{CC}=5V, V_{OHM}=V_{CC}-0.5V, I_{OHM}=0.4mA, V_{IHE}=V_{CC}×0.7V, from the equation③,

$$R_{PD} \geqq \frac{5-0.5}{0.4\times10^{-3}}$$

$$\therefore R_{PU} \geqq 11.3[k\Omega]$$

The operations speed changes according to the amplitude VIHE, VILE of the signals input to the EEPROM. More stable high speed operations can be realized by inputting signals with Vcc / GND levels of amplitude. On the contrary, when signals with an amplitude of 0.8Vcc / 0.2Vcc are input, operation speed slows down.[*1]

In order to realize more stable high speed operation, it is recommended to set the values of R_{PU}, R_{PD} as large as possible, and to have the amplitude of the signals input to the EEPROM close to the Vcc / GND amplitude level.
([*]1 In this case, the guaranteed value of operating timing is guaranteed.)

○SO load capacitance condition

The load capacitance of the SO output pin affects the SO output delay characteristic. (Data output delay time, time from HOLDB to High-Z, output rise time, output fall time.). Make the SO load capacitance small to improve the output delay characteristic.

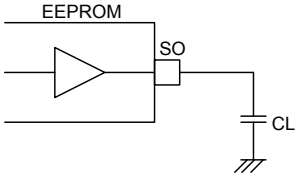


Fig.46 SO load dependency of data output delay time tPD

○Other cautions

Make all wires from the microcontroller to EEPROM input pin the same length. This in order to prevent setup / hold violation to the EEPROM.

●Equivalent circuit

○Output circuit

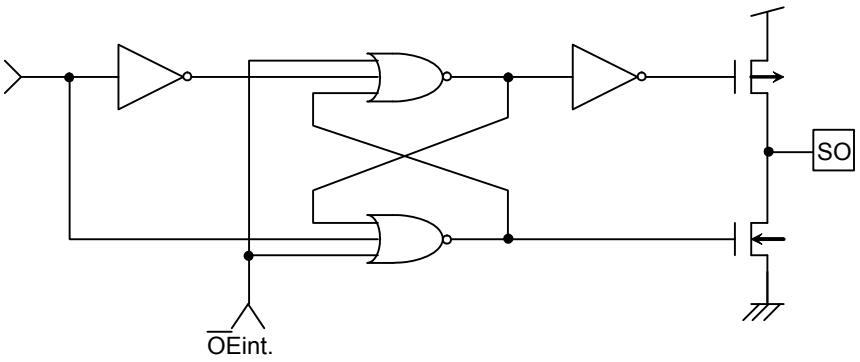


Fig.47 SO output equivalent circuit

○Input circuit

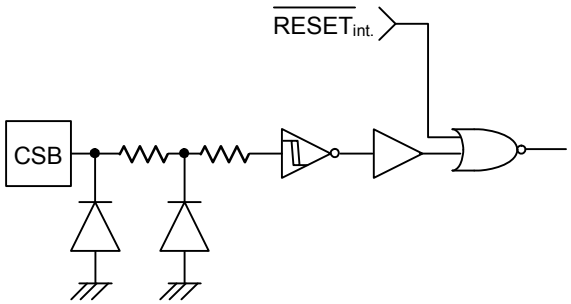


Fig.48 CSB input equivalent circuit

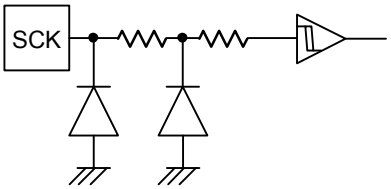


Fig.49 SCK input equivalent circuit

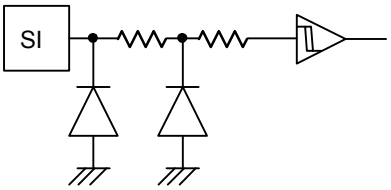


Fig.50 SI input equivalent circuit

●Notes on power ON/OFF

○At power ON/OFF set CSB="H" (=Vcc).

When CSB is "L", the IC goes into input accept status (active). If power is turned on in this status noises, etc. may cause malfunction or erroneous write. To prevent this, set CSB to "H" at power ON. (When CSB is in "H" status, all inputs are canceled.)

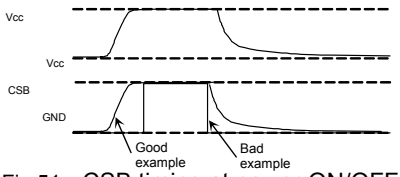


Fig.51 CSB timing at power ON/OFF

(Good example) CSB terminal is pulled up to Vcc.

After turning power off allow for 10ms or more before turning power on again. If power is turned on without observing this condition, the IC internal circuit may not be reset.

(Bad example) CSB terminal is "L" at power ON/OFF.

In this case, CSB always becomes "L" (active status), and the EEPROM may malfunction or perform an erroneous write due to noises, etc.

This can even occur when CSB input is High-Z.

○LVCC circuit

LVCC (Vcc-Lockout) circuit prevents data rewrite action at low power and prevents erroneous write.

At LVCC voltage (Typ. =1.9V) or below, it prevents data rewrite.

○P.O.R. circuit

This IC has a POR (Power On Reset) circuit as countermeasure against erroneous write. After the POR operation is performed, write disable status is entered. The POR circuit is only valid when power is ON and does not work when power is OFF. When power is ON and the following recommended tR, tOFF, Vbot conditions are not satisfied, write enable status might be entered due to noise etc.

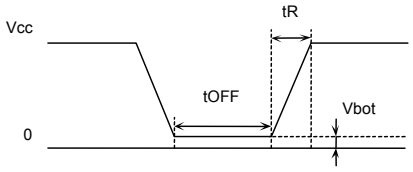


Fig.52 Rise waveform

Recommended conditions for t_R, t_{OFF}, Vbot

tR	tOFF	Vbot
10ms or below	10ms or higher	0.3V or below
100ms or below	10ms or higher	0.2V or below

●Noise countermeasures

○Vcc noise (bypass capacitor)

When noise or surge gets in the power source line, malfunction may occur. To prevent this, it is recommended to attach a bypass capacitor (0.1μF) between IC Vcc and GND, as close to IC as possible.

It is also recommended to attach a bypass capacitor between the board Vcc and GND.

○SCK noise

When the rise time of SCK (tRC) is long and a there is a certain degree of noise, malfunction may occur due to clock bit displacement. To avoid this, a Schmitt trigger circuit is built in the SCK input. The hysteresis width of this circuit is set to about 0.2V. If noises exist at the SCK input set the noise amplitude to 0.2Vp-p or below. Also, it is recommended to set the rise time of SCK (tRC) to 100ns or below. In case the rise time is 100ns or higher, sufficient noise countermeasures are needed. Clock rise, fall time should be as small as possible.

●Notes for use

(1) Described numeric values and data are design representative values and not guaranteed.

(2) We believe that the application circuit examples are recommendable. However, in actual use, please sufficiently further characteristics. When changing the fixed number of external parts, make your decision with sufficient margin, in consideration of static characteristics, transition characteristics and fluctuations of external parts and our LSI.

(3) Absolute maximum ratings
If the absolute maximum ratings such as impressed voltage, operating temperature range, etc. are exceeded, the LSI might be damaged. Please do not impress voltage or temperature exceeding the absolute maximum ratings. In case of fear of exceeding the absolute maximum ratings please take physical safety countermeasures such as fuses and see to it that conditions exceeding the absolute maximum ratings are impressed to LSI.

(4) GND electric potential
Set the voltage of the GND terminal as low as possible with all action conditions. Ensure that that all terminal voltages are higher than that of the GND terminal.

(5) Heat design
In consideration of permissible dissipation in actual use condition, please carry out the heat design with sufficient margin.

(6) Inter-terminal short circuit and wrong packaging
When packaging the LSI onto a board, pay sufficient attention to the LSI direction and displacement. Wrong packaging may damage LSI. Short circuit between LSI terminals, terminals and power source, terminal and GND due to foreign matters may also result in LSI damage.

(7) Use in strong electromagnetic fields may cause malfunction. Therefore, please evaluate the design sufficiently.

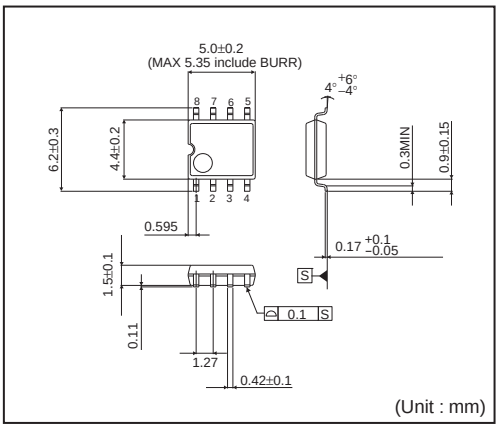
●Ordering part number

B R	3 5	H	1 6 0	F	—	W C	E 2

- Rohm type
- BUS type: 35: SPI
- Operating temperature: H:-40℃ to +125℃
- Capacity: 160=16K, 320=32K, 640=64K, 128=128K
- Package: FVM : MSOP8, FVT : TSSOP-B8, F : SOP8, FJ : SOP-J8
- Double cell
- Packaging and forming specification: E2 : Embossed tape and reel, TR : Embossed tape and reel (MSOP8 package only)

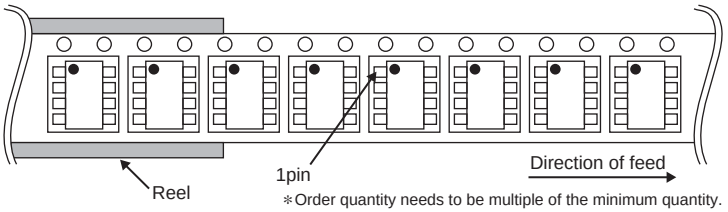
●Package specifications

SOP8



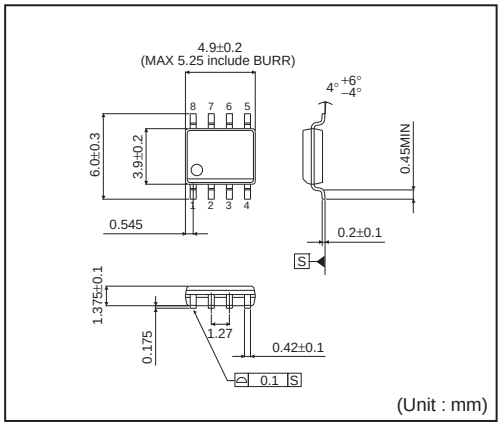
<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



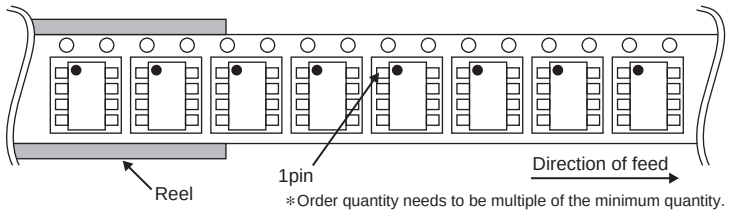
∗Order quantity needs to be multiple of the minimum quantity.

SOP-J8



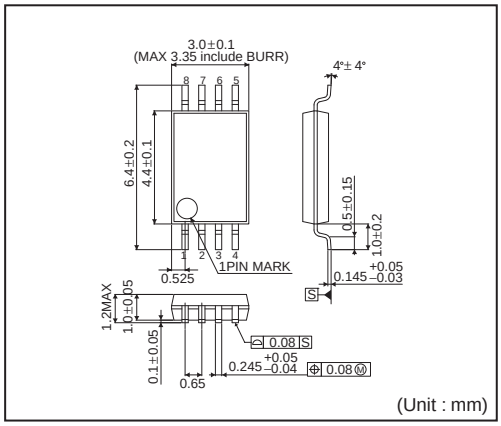
<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



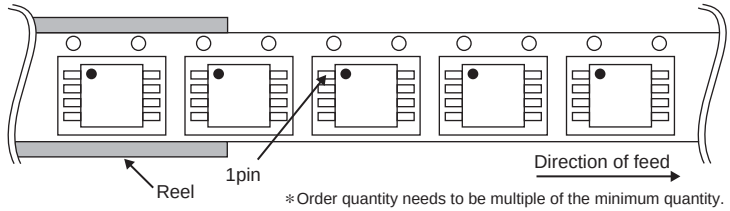
∗Order quantity needs to be multiple of the minimum quantity.

TSSOP-B8



<Tape and Reel information>

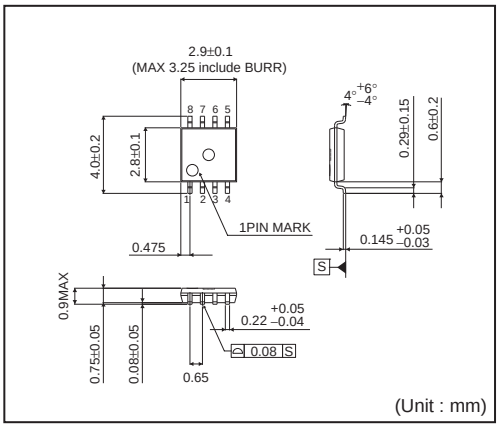
Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

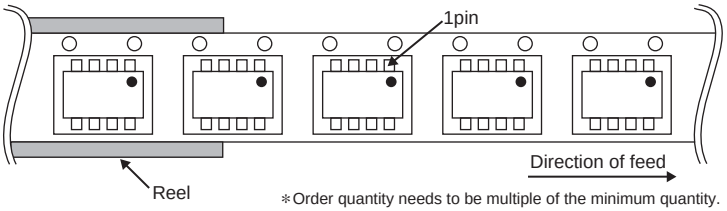
●Package specifications (Continue)

MSOP8



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	TR (The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

Notes

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The Products are not designed or manufactured to be used with any equipment, device or system which requires an extremely high level of reliability the failure or malfunction of which may result in a direct threat to human life or create a risk of human injury (such as a medical instrument, transportation equipment, aerospace machinery, nuclear-reactor controller, fuel-controller or other safety device). ROHM shall bear no responsibility in any way for use of any of the Products for the above special purposes. If a Product is intended to be used for any such special purpose, please contact a ROHM sales representative before purchasing.

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ROHM SEMICONDUCTOR

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More detail product informations and catalogs are available, please contact us.

ROHM Customer Support System

http://www.rohm.com/contact/

Общество с ограниченной ответственностью «МосЧип» ИНН 7719860671 / КПП 771901001
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Данный компонент на территории Российской Федерации

Вы можете приобрести в компании MosChip.

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http://moschip.ru/get-element

Вы можете разместить у нас заказ для любого Вашего проекта, будь то серийное производство или разработка единичного прибора.

В нашем ассортименте представлены ведущие мировые производители активных и пассивных электронных компонентов.

Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

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