4K/8K 2.5V CMOS Serial EEPROMs

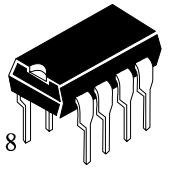
IN24LC04B/08B

DESCRIPTION

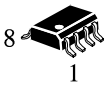
IN24LC04B/08B is a 4K-or 8K-bit Electrically Erasable PROM. The device is organized as two or four blocks of 256 x 8 bit memory with a two wire serial interface. Low voltage design permits operation down to 2.5 volts with standby and active currents of only 5μA and 1mA respectively. The IN24LC04B/08B also has a page-write capability for up to 16 bytes of data. The IN24LC04B/08B is available in the standard 8-pin DIP.

FEATURES

- Single supply with operation down to 2.5V
- Low power CMOS technology
  - 1 mA active current typical
  - 10 μA standby current typical at 5.5V
  - 5 μA standby current typical at 3.0V
- Organized as two or four blocks of 256 bytes (2x256x8) and (4x256x8)
- Two wire serial interface bus, I^2C compatible
- Schmitt trigger, filtered inputs for noise suppression
- Output slope control to eliminate ground bounce
- 100 kHz (2.5V) and 400 kHz (5V) compatibility
- Self-timed write cycle (including auto-erase)
- Page-write buffer for up to 16 bytes
- 2 ms typical write cycle time for page-write
- Hardware write protect for entire memory
- Can be operated as a serial ROM
- Factory programming (QTP) available
- ESD protection > 4,000V
- 1,000,000 ERASE/WRITE cycles guaranteed*
- Data retention > 200 years
- 8-pin DIP
- Temperature range -40 to +85 °C



N SUFFIX
PLASTIC



D SUFFIX
SOIC

PACKAGE
T_A = -40 ... +85 °C

PINNING

Name	Function
Vss	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
WP	Write Protect Input
VCC	+2.5V to 5.5V Power Supply
AO, A1, A2	No Internal Connection

Pin Connection

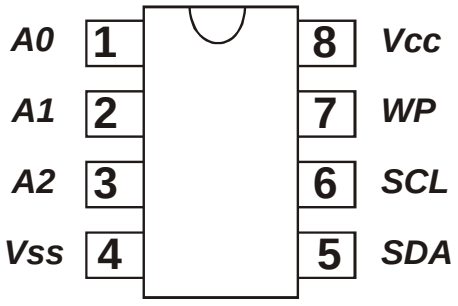
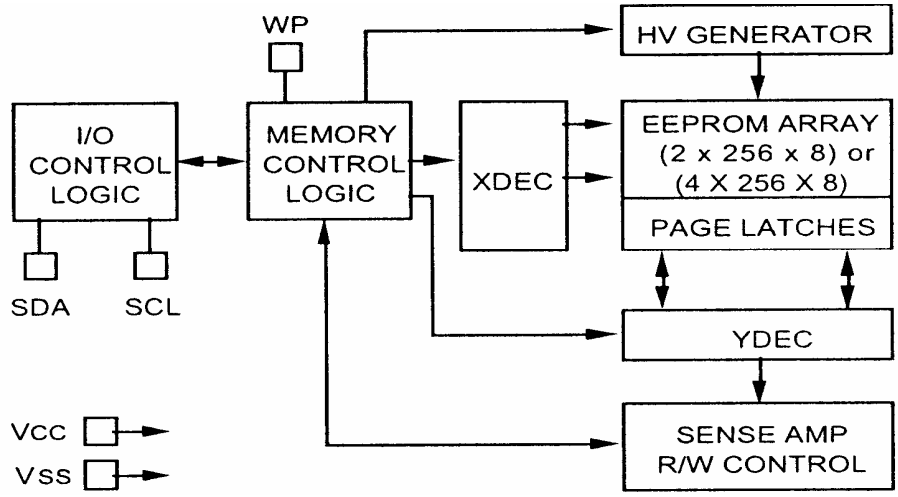


Figure 1. Representative Block Diagram



ELECTRICAL CHARACTERISTICS

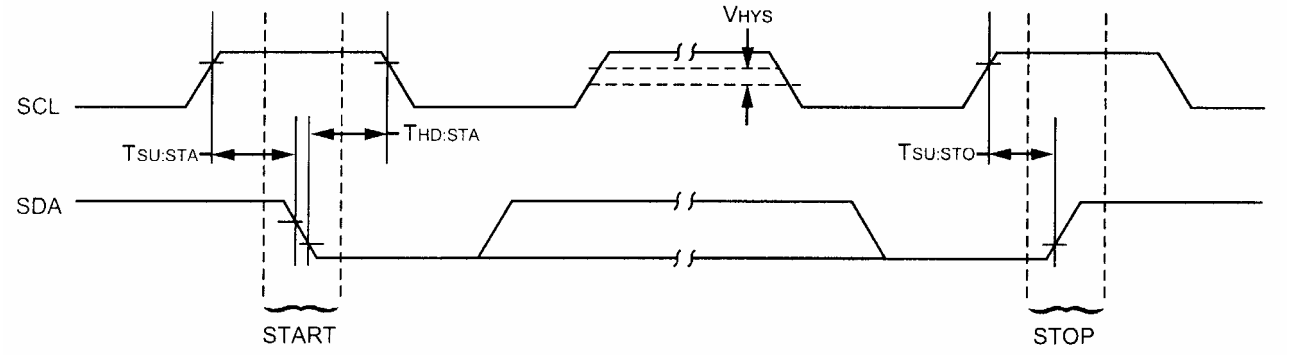
Maximum Ratings*

Parameter	**Value**
V_{CC}	7.0 V
All inputs and outputs w.r.t.Vss	-0.3V to Vcc + 1.0V
Storage temperature	-65°C to +150°C
Ambient temp. with power applied	-40 to +85°C
Soldering temperature of leads (10 seconds)	+300°C
ESD protection on all pins	> 4 kV

DC CHARACTERISTICS

Vcc = +2.5V to +5.5V Commercial: Tamb = -40to +85					
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Mode**
WP, SCL and SDA pins: High level input voltage Low level input voltage Hysteresis of Schmitt trigger inputs Low level output voltage	 V_{IH} V_{IL} V_{HYS} V_{OL}	 $0.7V_{CC}$ - $0.05V_{CC}$ -	 - $0.3V_{CC}$ - 0.40	 V V V V	 Note 1 I_{OL} = 3.0mA, V_{CC} = 2.5V
Input leakage current	I_{LI}	-10	10	µA	V_{IN}=0.1V to V_{CC}
Output leakage current	I_{LO}	-10	10	µA	V_{OUT}=0.1V to V_{CC}
Pin capacitance (all inputs/outputs)	C_{IN} C_{OUT}	-	10	pF	V_{CC} = 5.0V (Note 1) Tamb =25°C, Fclk =1MHz
Operating current	I_{CC} WRITE I_{CC}READ	- -	3 1	mA mA	V_{CC} = 5.5V SCL = 400kHz
Standby current	I_{CCS}	- -	30 100	µA µA	SDA=SCL=V_{CC}=3.0V, SDA=SCL=V_{CC}=5.5V

Figure 2. Bus timing Start/Stop



AC CHARACTERISTICS

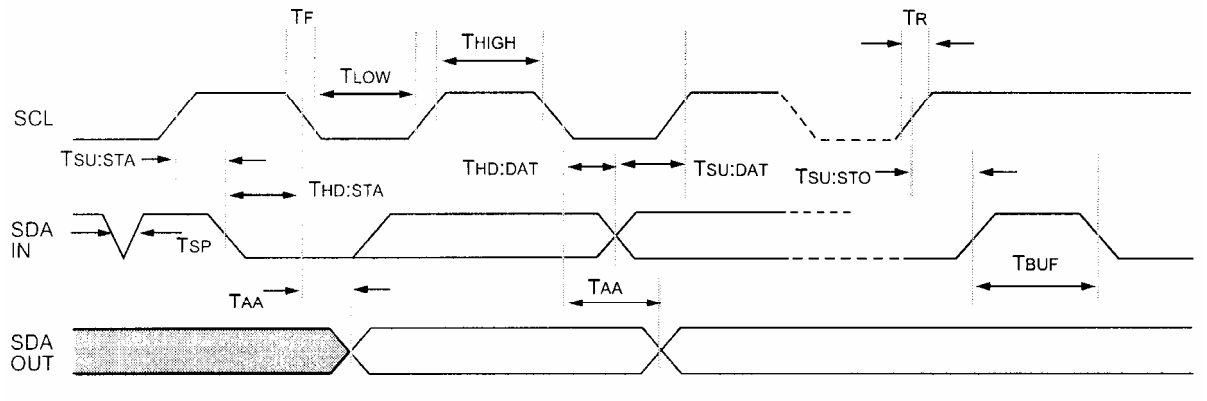
Parameter	Symbol	STANDARD MODE		Vcc = 4.5 - 5.5V FAST MODE		Units	Remarks
		Min	Max	Min	Max		
Clock frequency	F_{CLK}	-	100	-	400	kHz	
Clock high time	T_{HIGH}	4000	-	600	-	ns	
Clock low time	T_{LOW}	4700	-	1300	-	ns	
SDA and SCL rise time	T_R	-	1000	-	300	ns	Note 2
SDA and SCL fall time	T_F	-	300	-	300	ns	Note 2
START condition hold time	$T_{HD:STA}$	4000	-	600	-	ns	After this period the first clock pulse is generated
START condition setup time	$T_{SU:STA}$	4700	-	600	-	ns	Only relevant for repeated START condition
Data input hold time	$T_{HD:DAT}$	0	-	0	-	ns	
Data input setup time	$T_{SU:DAT}$	250	-	100	-	ns	
STOP condition setup time	$T_{SU:STO}$	4000	-	600	-	ns	
Output valid from clock	T_{AA}	-	3500	-	900	ns	Note 1
Bus free time	T_{BUF}	4700	-	1300	-	ns	Time the bus must be free before a new transmission can start
Output fall time from V_{IH} min to V_{IL} max	T_{OF}	-	250	$20+0.1C_B$	250	ns	Note2, $C_B \leq 100pF$
Input filter spike suppres-sion (SDA & SCL pins)	T_{SP}	-	50	-	50	ns	Note 3
Write cycle time	T_{WR}	-	10	-	10	ms	Byte or Page mode

Note 1: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

Note 2: Not 100% tested. C_B = total capacitance of one bus line in pF.

Note 3: The combined T_{SP} and V_{HYS} specifications are due to new Schmitt trigger inputs which provide improved noise and spike suppression. This eliminates the need for a Ti specification for standard operation.

Figure 3. Bus timing Data



FUNCTIONAL DESCRIPTION

The IN24LC04B/08B supports a bidirectional two wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the IN24LC04B/08B works as slave. Both, master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

BUS CHARACTERISTICS

The following bus protocol has been defined:

Data transfer may be initiated only when the bus is not busy.

During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition. Accordingly, the following bus conditions have been defined (see Figure 4).

Bus not Busy (A)

Both data and clock lines remain HIGH.

Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited, although only the last sixteen will be stored when doing a write operation. When an overwrite does occur it will replace data in a first in first out fashion.

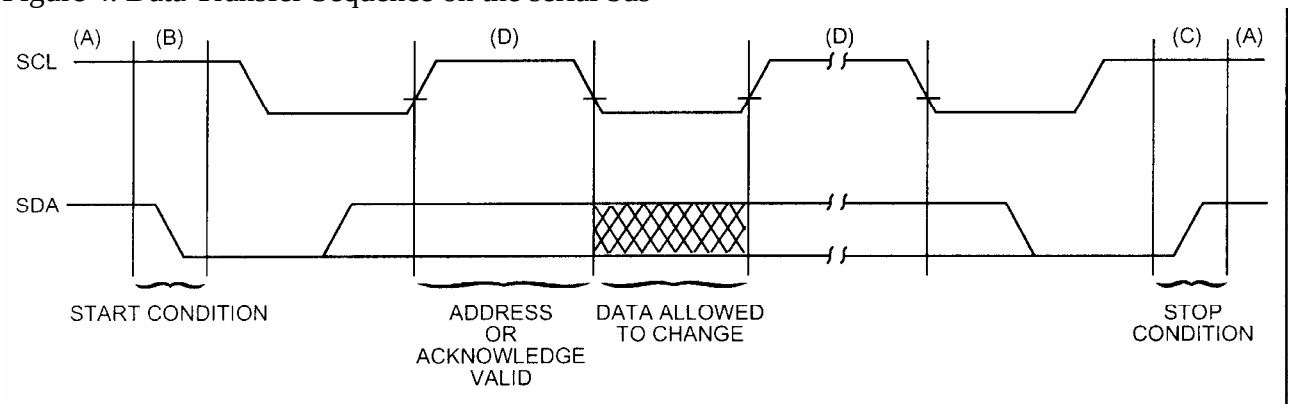
Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note: The IN24LC04B/08B does not generate any acknowledge bits if an internal programming cycle is in progress

The device that acknowledges, has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

Figure 4. Data Transfer Sequence on the serial bus



BUS CHARACTERISTICS

Device Addressing and Operation

A control byte is the first byte received following the start condition from the master device. The control byte consists of a four bit control code, for the IN24LC04B/08B this is set as 1010 binary for read and write operations. The next three bits of the control byte are the block select bits (B2, B1, BO). B2 is a don't care for both the IN24LC04B and IN24LC08B; B1 is a don't care for the IN24LC04B. They are used by the master device to select which of the two or four 256 word blocks of memory are to be accessed. These bits are in effect the most significant bits of the word address. The last bit of the control byte defines the operation to be performed. When set to one a read operation is selected, when set to zero a write operation is selected. Following the start condition, the IN24LC04B/08B monitors the SDA bus checking the device type identifier being transmitted, upon a 1010 code the slave device outputs an acknowledge signal on the SDA line. Depending on the state of the R/W bit, the IN24LC04B/ 08B will select a read or write operation.

Operation	Control Code	Block Select	R/W
Read	1010	Block Address	1
Write	1010	Block Address	0

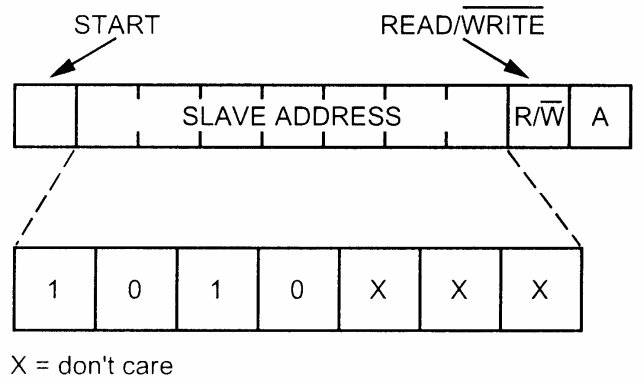


Figure 5. Control Byte Allocation

WRITE OPERATION

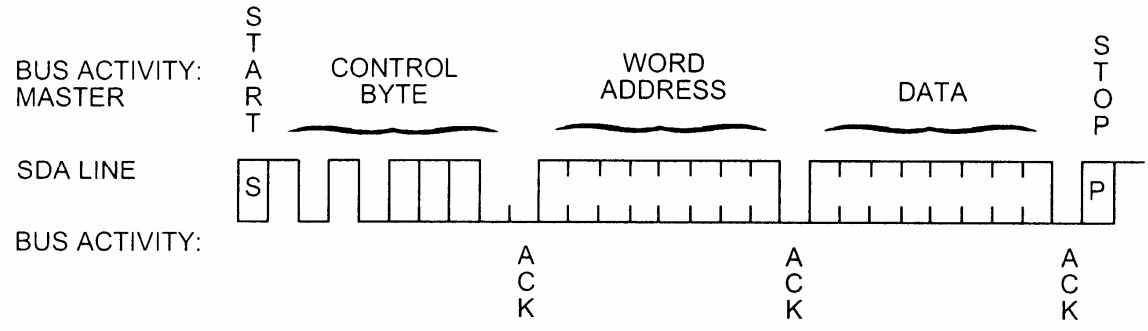
Byte Write

Following the start condition from the master, the device code (4 bits), the block address (3 bits), and the R/W bit which is a logic low is placed onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore the next byte transmitted by the master is the word address and will be written into the address pointer of the IN24LC04B/08B. After receiving another acknowledge signal from the IN24LC04B/08B the master device will transmit the data word to be written into the addressed memory location. The IN24LC04B/08B acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time the IN24LC04B/08B will not generate acknowledge signals (see Figure 6).

Page Write

The write control byte, word address and the first data byte are transmitted to the IN24LC04B/08B in the same way as in a byte write. But instead of generating a stop condition the master transmits up to sixteen data bytes to the IN24LC04B/08B which are temporarily stored in the on-chip page buffer and will be written into the memory after the master has transmitted a stop condition. After the receipt of each word, the four lower order address pointer bits are internally incremented by one. The higher order seven bits of the word address remains constant. If the master should transmit more than sixteen words prior to generating the stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the stop condition is received an internal write cycle will begin (see Figure 8).

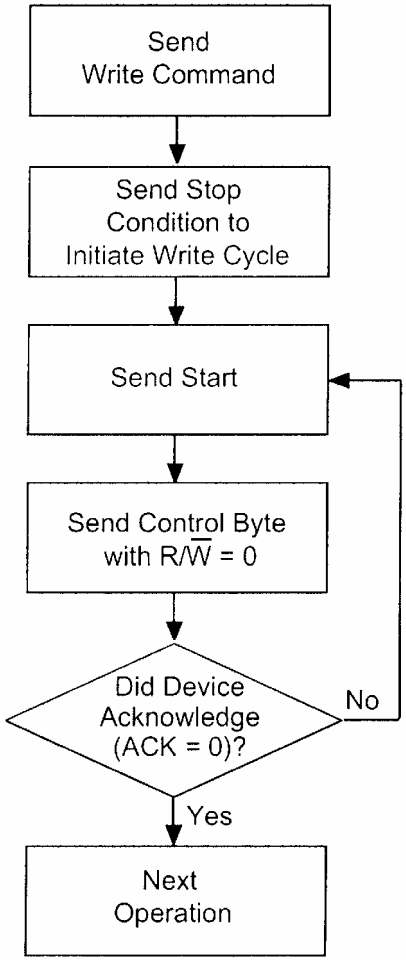
Figure 6. Byte Write



ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle, ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command (R/W =0). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 7 for flow diagram**.**

Figure 7. Acknowledge Polling Flow



WRITE PROTECTION

The IN24LC04B/08B can be used as a serial ROM when the WP pin is connected to Vcc. Programming will be inhibited and the entire memory will be write-protected.

READ OPERATION

Read operations are initiated in the same way as write operations with the exception that the R/W bit of the slave address is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

Current Address Read

The IN24LC04B/08B contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n, the next current address read operation would access data from address n + 1. Upon receipt of the slave address with R/W bit set to one, the IN24LC04B/08B issues an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the IN24LC04/08 discontinues transmission (see Figure 9).

Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the IN24LC04B/08B as part of a write operation. After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the R/W bit set to a one. The IN24LC04B/08B will then issue an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the IN24LC04B/08B discontinues transmission (see Figure 10).

Figure 8. Page Write

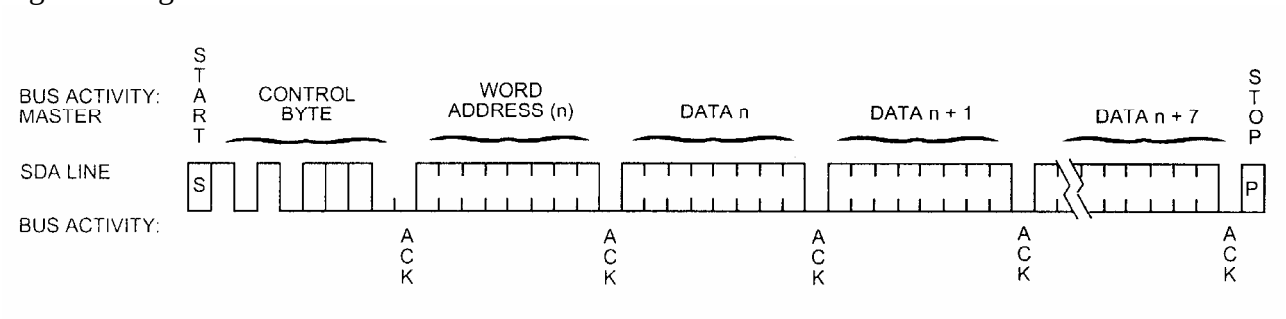


Figure 9. Current Address Read

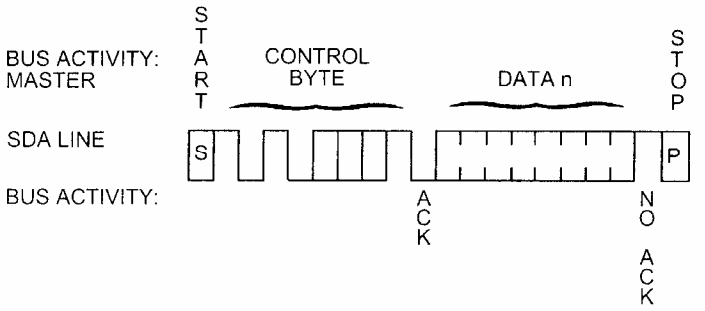
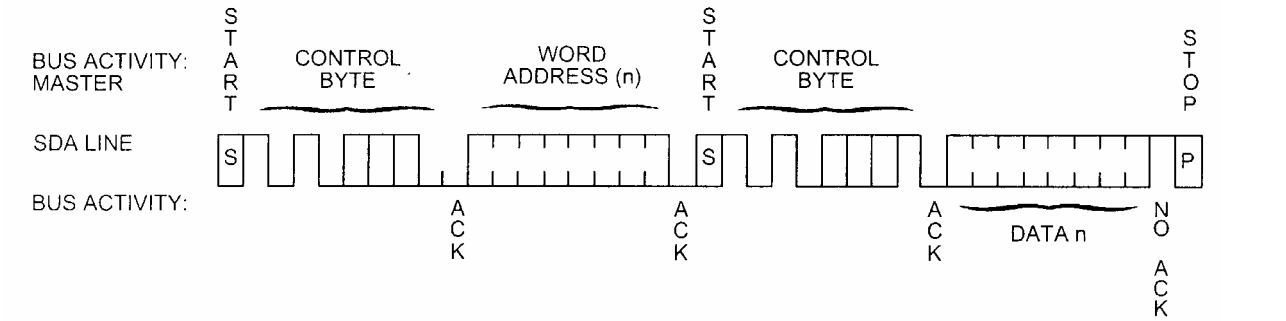


Figure 10. Random Read



Sequential Read

Sequential reads are initiated in the same way as a random read except that after the IN24LC04B/08B transmits the first data byte, the master issues an acknowledge as opposed to a stop condition in a random read. This directs the IN24LC04B/08B to transmit the next sequentially addressed 8 bit word (see Figure 11).

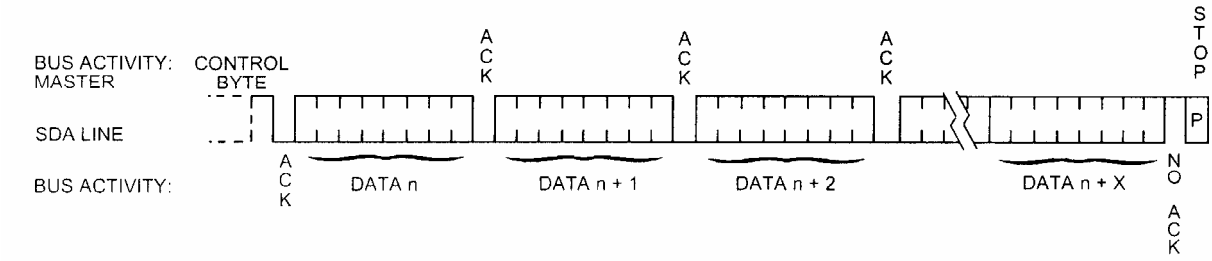
To provide sequential reads the IN24LC04B/08B contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation.

Noise Protection

The IN24LC04B/08B employs a Vcc threshold detector circuit which disables the internal erase/write logic if the Vcc is below 1,5 volts at nominal conditions.

The SCL and SDA inputs have Schmitt trigger and filter circuits which suppress noise spikes to assure proper device operation even on a noisy bus.

Figure 11. Sequential read



PIN DESCRIPTIONS

SPA Serial Address/Data Input/Output

This is a bidirectional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal, therefore the SDA bus requires a puliup resistor to Vcc (typical 10KΩ for 100 kHz, 1 KΩ for 400 kHz**).**

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

WP

This pin must be connected to either Vss or Vcc.

If tied to Vss, normal memory operation is enabled (read/write the entire memory).

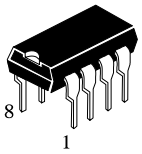
If tied to Vcc, WRITE operations are inhibited. The entire memory will be write-protected. Read operations are not affected.

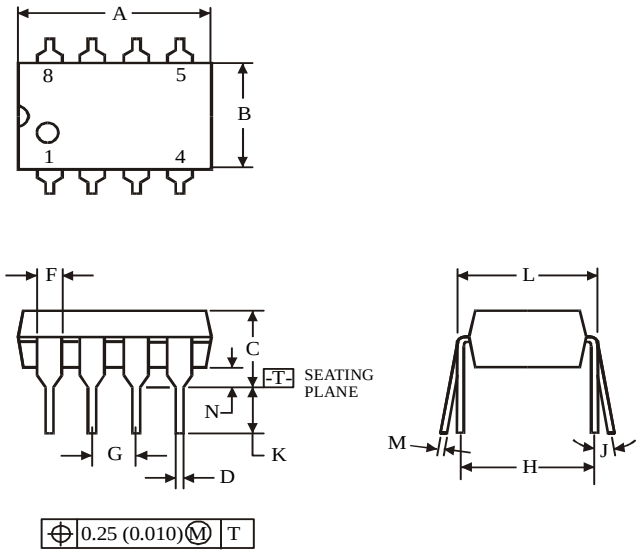
This feature allows the user to use the IN24LC04B/08B as a serial ROM when WP is enabled (tied to Vcc).

A0,A1,A2

These pins are not used by the IN24LC04B/08B. They may be left floating or tied to either Vss or Vcc.

N SUFFIX PLASTIC DIP
(MS – 001BA)



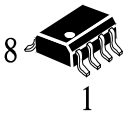


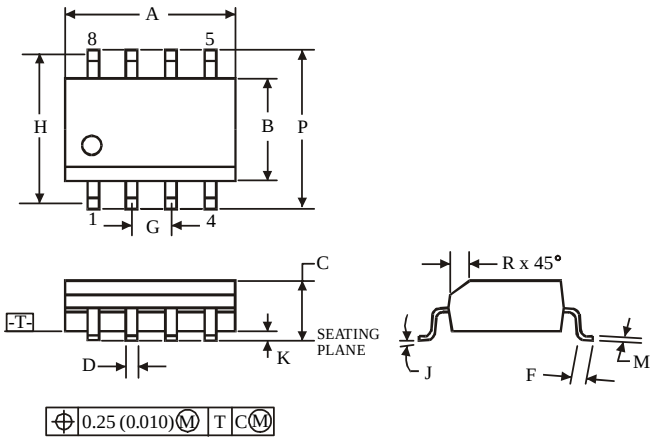
	Dimension, mm	
Symbol	**MIN**	**MAX**
A	8.51	10.16
B	6.1	7.11
C		5.33
D	0.36	0.56
F	1.14	1.78
G	2.54	
H	7.62	
J	0°	10°
K	2.92	3.81
L	7.62	8.26
M	0.2	0.36
N	0.38	

NOTES:

1. Dimensions “A”, “B” do not include mold flash or protrusions.
   Maximum mold flash or protrusions 0.25 mm (0.010) per side.

D SUFFIX SOIC
(MS - 012AA)





	Dimension, mm	
Symbol	**MIN**	**MAX**
A	4.8	5
B	3.8	4
C	1.35	1.75
D	0.33	0.51
F	0.4	1.27
G	1.27	
H	5.72	
J	0°	8°
K	0.1	0.25
M	0.19	0.25
P	5.8	6.2
R	0.25	0.5

NOTES:

1. Dimensions A and B do not include mold flash or protrusion.
2. Maximum mold flash or protrusion 0.15 mm (0.006) per side for A; for B – 0.25 mm (0.010) per side.

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Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

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Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

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