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FDC6301N Dual N-Channel , Digital FET

General Description

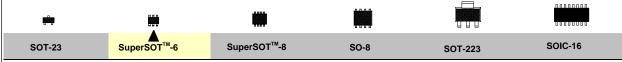
These dual N-Channel logic level enhancement mode field effect transistors are produced using Fairchild 's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance. This device has been designed especially for low voltage applications as a replacement for digital transistors. Since bias resistors are not required, these N-Channel FET's can replace several digital transistors, with a variety of bias resistors.

Features

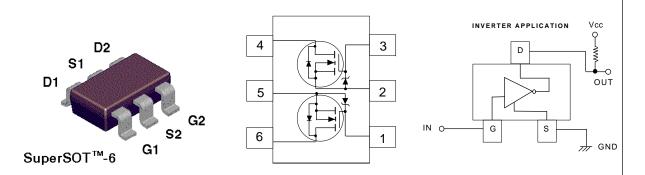
■ 25 V, 0.22 A continuous, 0.5 A Peak.

$$\begin{aligned} \mathsf{R}_{\mathsf{DS(ON)}} &= 5~\Omega~@~\mathsf{V}_{\mathsf{GS}} \\ \mathsf{R}_{\mathsf{DS(ON)}} &= 4~\Omega~@~\mathsf{V}_{\mathsf{GS}} \\ \end{aligned}$$

- Very low level gate drive requirements allowing direct operation in 3V circuits. V_{GS(th)} < 1.5V.
- Gate-Source Zener for ESD ruggedness.
 >6kV Human Body Model.



Mark: .301



Absolute Maximum Ratings $T_A = 25^{\circ}C$ unless other wise noted

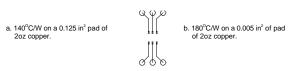
| Symbol | Parameter | | FDC6301N | Units | |
|-----------------------------------|--|------------------------|-------------|-------|--|
| V_{DSS}, V_{CC} | Drain-Source Voltage, Power Supply Voltage | | 25 | V | |
| V_{GSS}, V_{IN} | Gate-Source Voltage, V _{IN} | | - 0.5 to +8 | V | |
| l _D , l _{OUT} | Drain/Output Current - Continuous | | 0.22 | А | |
| | - Pulsed | | 0.5 | | |
| P _D | Maximum Power Dissipation | (Note 1a) (Note 1b) | 0.9 | W | |
| | | | 0.7 | | |
| T_{J},T_{STG} | Operating and Storage Temperature Ran | ge | -55 to 150 | °C | |
| ESD | Electrostatic Discharge Rating MIL-STD-883D Human Body Model (100pf / 1500 Ohm) | | 6.0 | kV | |
| THERMA | L CHARACTERISTICS | · | | | |
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambien | t (Note 1a) | 140 | °C/W | |
| $R_{\theta JC}$ | Thermal Resistance, Junction-to-Case | (Note 1) | 60 | °C/W | |

| Symbol | Parameter | Conditions | | Min | Тур | Max | Units |
|----------------------------------|---|--|--|------|------|-----|--------|
| OFF CHAR | ACTERISTICS | • | | , | | ı | |
| BV _{DSS} | Drain-Source Breakdown Voltage | $V_{GS} = 0 \text{ V}, I_{D} = 250 \mu\text{A}$ | | 25 | | | V |
| $\Delta BV_{DSS}/\Delta T_{J}$ | Breakdown Voltage Temp. Coefficient | I _D = 250 μA, Referenced to 25 °C | | | 25 | | mV /°C |
| I _{DSS} | Zero Gate Voltage Drain Current | $V_{DS} = 20 \text{ V}, \ V_{GS} = 0 \text{ V}$ | | | | 1 | μΑ |
| | | | $T_J = 55^{\circ}C$ | | | 10 | μA |
| I _{GSS} | Gate - Body Leakage Current | $V_{GS} = 8 \text{ V}, \ V_{DS} = 0 \text{ V}$ | 1 | | | 100 | nA |
| ON CHARA | CTERISTICS (Note 2) | <u>.</u> | | | | | • |
| $\Delta V_{GS(th)}/\Delta T_{J}$ | Gate Threshold Voltage Temp.Coefficient | $I_D = 250 \mu\text{A}$, Referenced to | I _D = 250 μA, Referenced to 25 °C | | -2.1 | | mV /°C |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS} = V_{GS}, I_{D} = 250 \mu\text{A}$ | | 0.65 | 0.85 | 1.5 | V |
| R _{DS(ON)} | Static Drain-Source On-Resistance | $V_{GS} = 2.7 \text{ V}, I_D = 0.2 \text{ A}$ | | | 3.8 | 5 | Ω |
| | | | T _J =125°C | | 6.3 | 9 | |
| | | $V_{GS} = 4.5 \text{ V}, I_D = 0.4 \text{ A}$ | • | | 3.1 | 4 | |
| I _{D(ON)} | On-State Drain Current | $V_{GS} = 2.7 \text{ V}, \ V_{DS} = 5 \text{ V}$ | | 0.2 | | | Α |
| g _{FS} | Forward Transconductance | $V_{DS} = 5 \text{ V}, I_{D} = 0.4 \text{ A}$ | | | 0.25 | | S |
| DYNAMIC (| CHARACTERISTICS | • | | • | | | • |
| C _{iss} | Input Capacitance | $V_{DS} = 10 \text{ V}, \ V_{GS} = 0 \text{ V},$ $f = 1.0 \text{ MHz}$ | | | 9.5 | | pF |
| C _{oss} | Output Capacitance | | | | 6 | | pF |
| C _{rss} | Reverse Transfer Capacitance | | | | 1.3 | | pF |
| SWITCHING | CHARACTERISTICS (Note 2) | | | | | | |
| t _{D(on)} | Turn - On Delay Time | $V_{DD} = 6 \text{ V}, \ I_{D} = 0.5 \text{ A},$ $V_{GS} = 4.5 \text{ V}, \ R_{GEN} = 50 \Omega$ | | | 5 | 10 | ns |
| t _r | Turn - On Rise Time | | | | 4.5 | 10 | ns |
| t _{D(off)} | Turn - Off Delay Time | | | | 4 | 8 | ns |
| t, | Turn - Off Fall Time | | | | 3.2 | 7 | ns |
| Q_g | Total Gate Charge | $V_{DS} = 5 \text{ V}, I_{D} = 0.2 \text{ A},$ $V_{GS} = 4.5 \text{ V}$ | | | 0.49 | 0.7 | nC |
| Q_{gs} | Gate-Source Charge | | | | 0.22 | | nC |
| Q_{gd} | Gate-Drain Charge | | | | 0.07 | | nC |
| Inverte | Electrical Characteristics (T | A = 25°C unless other | wise noted) | | | | |
| I _{O (off)} | Zero Input Voltage Output Current | $V_{CC} = 20 \text{ V}, \ V_{I} = 0 \text{ V}$ | | | | 1 | μA |
| V _{I (off)} | Input Voltage | $V_{CC} = 5 \text{ V}, I_{O} = 10 \mu\text{A}$ | | | | 0.5 | V |
| V _{I (on)} | | $V_0 = 0.3 \text{ V}, I_0 = 0.005 \text{ A}$ | | 1 | | | V |
| R _{O (on)} | Output to Ground Resistance | $V_1 = 2.7 \text{ V}, \ I_0 = 0.2 \text{ A}$ | | | 3.8 | 5 | Ω |

Notes:

1. R_{B,M} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{B,C} is guaranteed by design while R_{eca} is determined by the user's board design. R_{gus} shown below for single device operation on FR-4 in still air.





2. Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2.0%.

Typical Electrical Characteristics

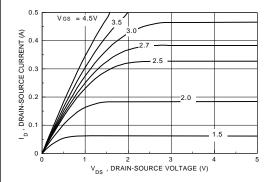


Figure 1. On-Region Characteristics.

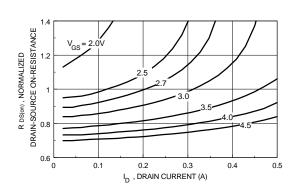


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

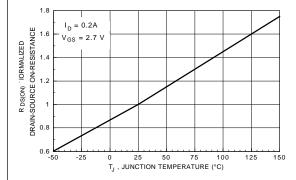


Figure 3. On-Resistance Variation with Temperature.

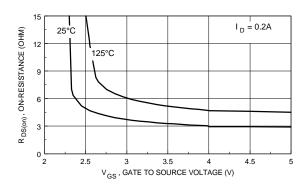


Figure 4. On Resistance Variation with Gate-To- Source Voltage.

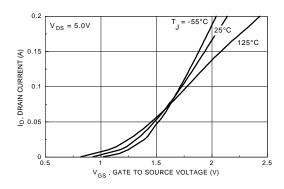


Figure 5. Transfer Characteristics.

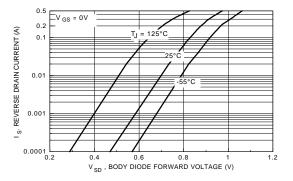
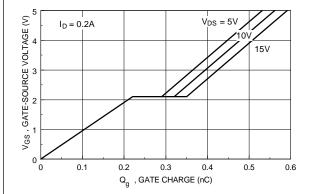


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Electrical Characteristics (continued)



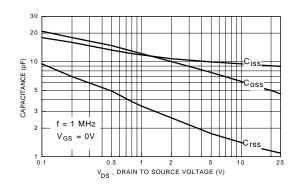


Figure 7. Gate Charge Characteristics.

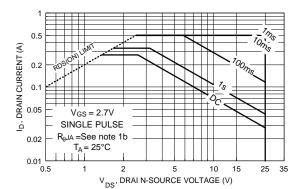


Figure 8. Capacitance Characteristics.

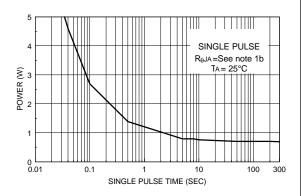
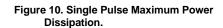


Figure 9. Maximum Safe Operating Area.



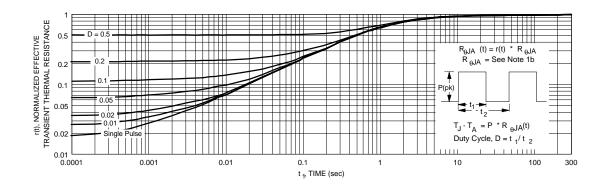


Figure 11. Transient Thermal Response Curve.

Note: Thermal characterization performed using the conditions described in note 1b.Transient thermal response will change depending on the circuit board design.

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