

BUK9610-100B

N-channel TrenchMOS logic level FET Rev. 03 — 31 January 2011

Product data sheet

1. **Product profile**

1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in automotive critical applications.

1.2 Features and benefits

- AEC Q101 compliant
- Low conduction losses due to low on-state resistance
- Suitable for logic level gate drive sources
- Suitable for thermally demanding environments due to 175 °C rating

1.3 Applications

- 12 V, 24 V and 42 V loads
- Automotive systems

- General purpose power switching
- Motors, lamps and solenoids

1.4 Quick reference data

Quick reference data Table 1.

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V_{DS}	drain-source voltage	$T_j \ge 25 ^{\circ}\text{C}; T_j \le 175 ^{\circ}\text{C}$		-	-	100	V
I _D	drain current	$V_{GS} = 5 \text{ V; } T_{mb} = 25 \text{ °C;}$ see <u>Figure 1</u> ; see <u>Figure 3</u>	1]	-	-	75	Α
P _{tot}	total power dissipation	T _{mb} = 25 °C; see <u>Figure 2</u>		-	-	300	W
Static chara	Static characteristics						
R _{DSon}	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 ^{\circ}\text{C}$		-	8.3	9.7	mΩ
		$V_{GS} = 5 \text{ V}; I_D = 25 \text{ A}; T_j = 25 ^{\circ}\text{C};$ see Figure 11; see Figure 12		-	8.6	10	mΩ



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Table 1. Quick reference data ...continued

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Avalanche	ruggedness					
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	$I_D = 75 \text{ A}; V_{\text{sup}} \le 100 \text{ V};$ $R_{\text{GS}} = 50 \Omega; V_{\text{GS}} = 5 \text{ V};$ $T_{j(\text{init})} = 25 ^{\circ}\text{C}; \text{ unclamped}$	-	-	629	mJ
Dynamic cl	haracteristics					
Q_{GD}	gate-drain charge	$V_{GS} = 5 \text{ V}; I_D = 25 \text{ A};$ $V_{DS} = 80 \text{ V}; T_j = 25 \text{ °C};$ see Figure 13	-	32	-	nC

^[1] Continuous current is limited by package.

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		_
2	D	drain[1]	mb	D
3	S	source		
mb	D	mounting base; connected to drain	1 3	mbb076 S
			SOT404 (D2PAK)	

^[1] It is not possible to make a connection to pin 2.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK9610-100B	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

		,				
Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C		-	100	V
V_{DGR}	drain-gate voltage	$R_{GS} = 20 \text{ k}\Omega$		-	100	V
V_{GS}	gate-source voltage			-15	15	V
I _D	drain current	$T_{mb} = 25 \text{ °C}; V_{GS} = 5 \text{ V}; \text{ see } \frac{\text{Figure 1}}{\text{Figure 1}};$	<u>[1]</u>	-	110	Α
		see Figure 3	[2]	-	75	Α
		$T_{mb} = 100 ^{\circ}C; V_{GS} = 5 V; see \underline{Figure 1}$	[2]	-	75	Α
I _{DM}	peak drain current	T_{mb} = 25 °C; pulsed; $t_p \le 10 \mu s$; see Figure 3		-	438	Α
P _{tot}	total power dissipation	T _{mb} = 25 °C; see <u>Figure 2</u>		-	300	W
T _{stg}	storage temperature			-55	175	°C
Tj	junction temperature			-55	175	°C
Source-drai	n diode					
Is	source current	T _{mb} = 25 °C	<u>[1]</u>	-	110	Α
			[2]	-	75	Α
I _{SM}	peak source current	pulsed; $t_p \le 10 \ \mu s$; $T_{mb} = 25 \ ^{\circ}C$		-	438	Α
Avalanche i	ruggedness					
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I_D = 75 A; $V_{sup} \le 100$ V; R_{GS} = 50 Ω; V_{GS} = 5 V; $T_{j(init)}$ = 25 °C; unclamped		-	629	mJ
		* *				

- [1] Current is limited by power dissipation chip rating.
- [2] Continuous current is limited by package.

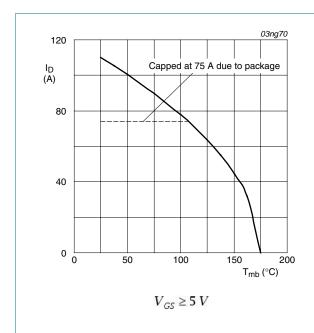


Fig 1. Normalized continuous drain current as a function of mounting base temperature

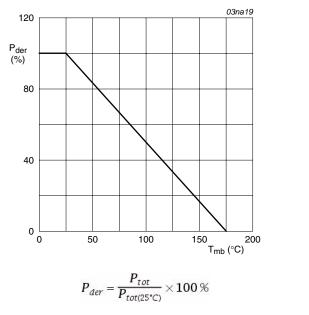


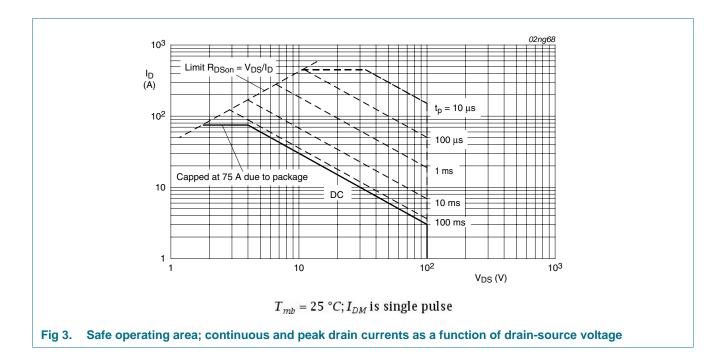
Fig 2. Normalized total power dissipation as a function of mounting base temperature

BUK9610-100B

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5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	-	0.5	K/W
R _{th(j-a)}	thermal resistance from junction to ambient	mounted on a printed-circuit board; minimum footprint	-	50	-	K/W

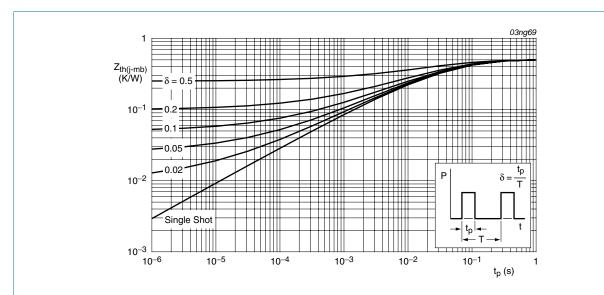


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

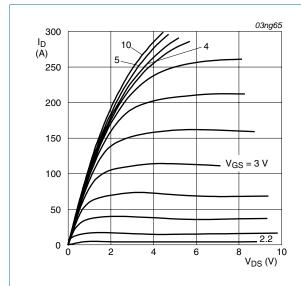
6. Characteristics

Table 6. Characteristics

Table 6.	Characteristics					
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static cha	racteristics					
$V_{(BR)DSS}$	drain-source breakdown	$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C}$	100	-	-	V
	voltage	$I_D = 0.25$ mA; $V_{GS} = 0$ V; $T_j = -55$ °C	89	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1$ mA; $V_{DS} = V_{GS}$; $T_j = 25$ °C; see <u>Figure 10</u>	1.1	1.5	2	V
		I_D = 1 mA; V_{DS} = V_{GS} ; T_j = 175 °C; see <u>Figure 10</u>	0.5	-	-	V
		I_D = 1 mA; V_{DS} = V_{GS} ; T_j = -55 °C; see <u>Figure 10</u>	-	-	2.3	V
I _{DSS}	drain leakage current	$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	0.02	1	μΑ
		$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ °C}$	-	-	500	μΑ
I _{GSS}	gate leakage current	$V_{GS} = 15 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	2	100	nΑ
		V_{GS} = -15 V; V_{DS} = 0 V; T_j = 25 °C	-	2	100	nΑ
R _{DSon}	drain-source on-state resistance	V_{GS} = 5 V; I_D = 25 A; T_j = 175 °C; see <u>Figure 11</u> ; see <u>Figure 12</u>	-	-	25	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ °C}$	-	8.3	9.7	mΩ
		$V_{GS} = 4.5 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ °C}$	-	-	11	mΩ
		$V_{GS} = 5 \text{ V}; I_D = 25 \text{ A}; T_j = 25 ^{\circ}\text{C};$ see <u>Figure 11</u> ; see <u>Figure 12</u>	-	8.6	10	mΩ
Dynamic (characteristics					
$Q_{G(tot)}$	total gate charge	$I_D = 25 \text{ A}; V_{DS} = 80 \text{ V}; V_{GS} = 5 \text{ V};$	-	86	-	nC
Q_{GS}	gate-source charge	T _j = 25 °C; see <u>Figure 13</u>	-	16	-	nC
Q_{GD}	gate-drain charge		-	32	-	nC
C _{iss}	input capacitance	$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}; f = 1 \text{ MHz};$	-	8284	11045	pF
C _{oss}	output capacitance	T _j = 25 °C; see <u>Figure 14</u>	-	676	811	pF
C_{rss}	reverse transfer capacitance		-	237	325	pF
t _{d(on)}	turn-on delay time	$V_{DS} = 30 \text{ V}; R_L = 1.2 \Omega; V_{GS} = 5 \text{ V};$	-	60	-	ns
t _r	rise time	$R_{G(ext)} = 10 \Omega; T_j = 25 ^{\circ}C$	-	110	-	ns
$t_{d(off)}$	turn-off delay time		-	250	-	ns
t _f	fall time	V_{DS} = 30 V; R_L = 1.2 Ω ; V_{GS} 5 V; $R_{G(ext)}$ = 10 Ω ; T_j = 25 °C	-	94	-	ns
L _D	internal drain inductance	from drain lead 6 mm from package to centre of die; $T_j = 25$ °C	-	4.5	-	nΗ
		from upper edge of drain mounting base to centre of die ; $T_j = 25 ^{\circ}\text{C}$	-	2.5	-	nΗ
L _S	internal source inductance	from source lead to source bond pad ; $T_j = 25 ^{\circ}\text{C}$	-	7.5	-	nΗ

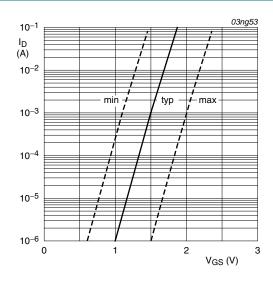
Table 6. Characteristics ... continued

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Source-dra	in diode					
V_{SD}	source-drain voltage	$I_S = 40 \text{ A}$; $V_{GS} = 0 \text{ V}$; $T_j = 25 \text{ °C}$; see Figure 15	-	0.85	1.2	V
t _{rr}	reverse recovery time	$I_S = 20 \text{ A}$; $dI_S/dt = -100 \text{ A/}\mu\text{s}$;	-	78	-	ns
Q _r	recovered charge	$V_{GS} = -10 \text{ V}; V_{DS} = 30 \text{ V}; T_j = 25 \text{ °C}$	-	268	-	nC



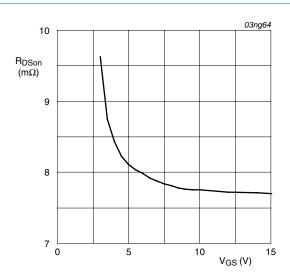
 $T_j = 25^{\circ}C; t_p = 300\mu s$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



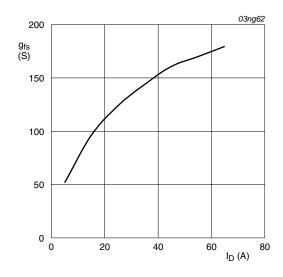
 $T_j = 25 \,^{\circ}C; V_{DS} = V_{GS}$

Fig 7. Sub-threshold drain current as a function of gate-source voltage



$$T_j = 25^{\circ}C; I_D = 25A$$

Fig 6. Drain-source on-state resistance as a function of gate-source voltage; typical values



 $T_j=25^{\circ}C; V_{DS}=25V$

Fig 8. Forward transconductance as a function of drain current; typical values

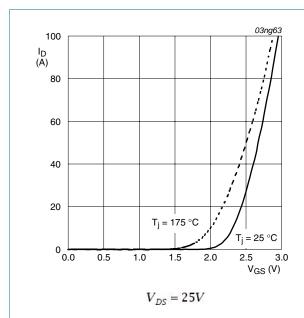


Fig 9. Transfer characteristics: drain current as a function of gate-source voltage; typical values

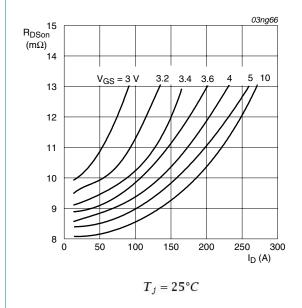
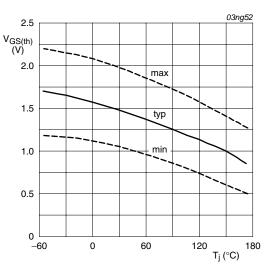


Fig 11. Drain-source on-state resistance as a function of drain current; typical values



 $I_D = 1mA; V_{DS} = V_{GS}$

Fig 10. Gate-source threshold voltage as a function of junction temperature

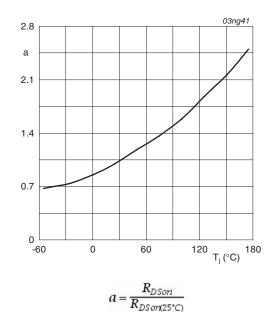


Fig 12. Normalized drain-source on-state resistance factor as a function of junction temperature

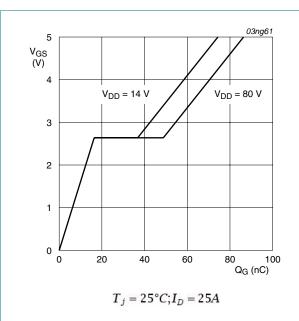
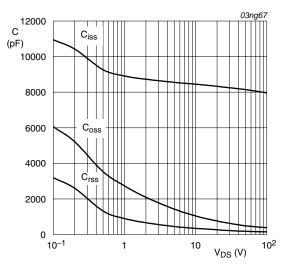


Fig 13. Gate-source voltage as a function of turn-on gate charge; typical values



 $V_{GS} = 0V; f = 1MHz$

Fig 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

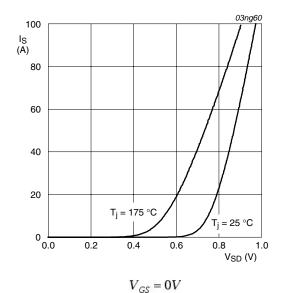


Fig 15. Reverse diode current as a function of reverse diode voltage; typical values

7. Package outline

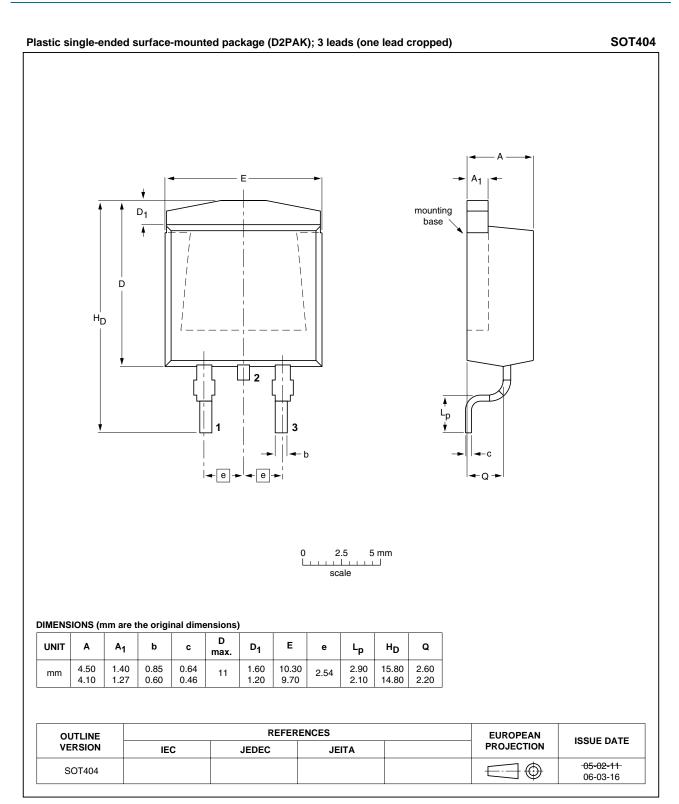


Fig 16. Package outline SOT404 (D2PAK)

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8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK9610-100B v.3	20110131	Product data sheet	-	BUK95_9610_100B v.2
Modifications:	 The format of thi of NXP Semicor 		designed to comply v	vith the new identity guidelines
	 Legal texts have 	been adapted to the nev	v company name wh	nere appropriate.
	 Type number Bl 	JK9610-100B separated t	rom data sheet BUI	(95_9610_100B v.2.
BUK95_9610_100B v.2	20021008	Product data	-	BUK95_9610-100B v.1

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9.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions"
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