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September 2016

## FDD9410L\_F085

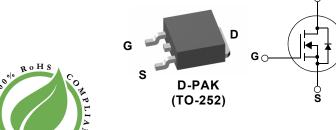
# N-Channel Logic Level PowerTrench $^{(\!R\!)}$ MOSFET 40 V, 50 A, 4.2 m $\Omega$

#### **Features**

- Typical  $R_{DS(on)}$  = 3.3 m $\Omega$  at  $V_{GS}$  = 10V,  $I_D$  = 50 A
- Typical  $Q_{q(tot)}$  = 29 nC at  $V_{GS}$  = 10V,  $I_D$  = 50 A
- UIS Capability
- RoHS Compliant
- Qualified to AEC Q101

## **Applications**

- Automotive Engine Control
- PowerTrain Management
- Solenoid and Motor Drivers
- Electronic Steering
- Integrated Starter/Alternator
- Distributed Power Architectures and VRM
- Primary Switch for 12V Systems



For current package drawing, please refer to the Fairchild website at http://www.fairchildsemi.com/package-drawings/TO/TO252A03.ndf.

## **MOSFET Maximum Ratings** T<sub>J</sub> = 25°C unless otherwise noted.

Symbol	Parameter		Ratings	Units
$V_{DSS}$	Drain-to-Source Voltage		40	V
$V_{GS}$	Gate-to-Source Voltage		±20	V
	Drain Current - Continuous (V <sub>GS</sub> =10) (Note 1)	T <sub>C</sub> = 25°C	50	Α
ID	Pulsed Drain Current	T <sub>C</sub> = 25°C	See Figure 4	A
E <sub>AS</sub>	Single Pulse Avalanche Energy	(Note 2)	24	mJ
D	Power Dissipation		75	W
$P_{D}$	Derate Above 25°C		0.5	W/°C
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature		-55 to + 175	°C
$R_{\theta JC}$	Thermal Resistance, Junction to Case		2	°C/W
$R_{\theta JA}$	Maximum Thermal Resistance, Junction to Ambient	(Note 3)	52	°C/W

#### Notes

- 1: Current is limited by bondwire configuration.
- 2: Starting  $T_J$  = 25°C, L = 30 $\mu$ H,  $I_{AS}$  = 40A,  $V_{DD}$  = 40V during inductor charging and  $V_{DD}$  = 0V during time in avalanche.
- 3: R<sub>0,JA</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. R<sub>0,JC</sub> is guaranteed by design, while R<sub>0,JA</sub> is determined by the board design. The maximum rating presented here is based on mounting on a 1 in<sup>2</sup> pad of 2oz copper.

### **Package Marking and Ordering Information**

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDD9410L	FDD9410L_F085	D-PAK(TO-252)	13"	16mm	2500units

Units

Max.

Тур.

## **Electrical Characteristics** $T_J = 25^{\circ}C$ unless otherwise noted.

**Parameter** 

Off Ch	Off Characteristics						
B <sub>VDSS</sub>	Drain-to-Source Breakdown Voltage	$I_D = 250 \mu A$	V <sub>GS</sub> = 0V	40	-	-	V
I Proin to Co	Drain-to-Source Leakage Current	V <sub>DS</sub> =40V,	$T_J = 25^{\circ}C$	-	-	1	μΑ
I <sub>DSS</sub> Drain-to-Source Leakage Current		$V_{GS} = 0V$	$T_J = 175^{\circ}C \text{ (Note 4)}$	-	-	1	mA
I <sub>GSS</sub>	Gate-to-Source Leakage Current	V <sub>GS</sub> = ±20V		-	-	±100	nA

**Test Conditions** 

Min.

### On Characteristics

Symbol

V <sub>GS(th)</sub>	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = 250 \mu A$		1.0	1.8	3.0	V
		$I_D = 50A, V_{GS}$	<sub>S</sub> = 4.5V	-	5.0	6.5	mΩ
R <sub>DS(on)</sub>	Drain to Source On Resistance	I <sub>D</sub> = 50A,	$T_J = 25^{\circ}C$	-	3.3	4.2	mΩ
		V <sub>GS</sub> = 10V	$T_J = 175^{\circ}C \text{ (Note 4)}$	-	6.0	7.6	mΩ

## **Dynamic Characteristics**

C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 20V, V <sub>GS</sub> = 0V, f = 1MHz		-	1960	-	pF
C <sub>oss</sub>	Output Capacitance			-	615	-	pF
C <sub>rss</sub>	Reverse Transfer Capacitance			-	41	-	pF
$R_g$	Gate Resistance	f = 1MHz		-	1.9	-	Ω
$Q_{g(ToT)}$	Total Gate Charge	V <sub>GS</sub> = 0 to 10V	V <sub>DD</sub> = 32V	-	29	43	nC
$Q_{g(th)}$	Threshold Gate Charge	$V_{GS} = 0$ to 2V	I <sub>D</sub> = 50A	-	4	-	nC
Q <sub>gs</sub>	Gate-to-Source Gate Charge		_	-	6	-	nC
$Q_{gd}$	Gate-to-Drain "Miller" Charge			-	5	-	nC

## **Switching Characteristics**

t <sub>on</sub>	Turn-On Time		-	-	22	ns
t <sub>d(on)</sub>	Turn-On Delay		-	8	-	ns
t <sub>r</sub>	Rise Time	V <sub>DD</sub> = 20V, I <sub>D</sub> = 50A,	-	7	-	ns
t <sub>d(off)</sub>	Turn-Off Delay	$V_{GS} = 10V, R_{GEN} = 6\Omega$	-	25	-	ns
t <sub>f</sub>	Fall Time		-	5	-	ns
t <sub>off</sub>	Turn-Off Time		-	-	45	ns

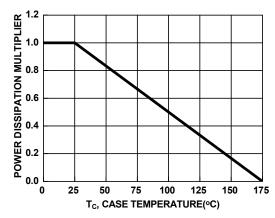
## **Drain-Source Diode Characteristics**

V	Source-to-Drain Diode Voltage	I <sub>SD</sub> =50A, V <sub>GS</sub> = 0V		1.25	V	
$V_{SD}$	Source-to-Drain blode voltage	$I_{SD}$ = 25A, $V_{GS}$ = 0V	1	-	1.2	V
t <sub>rr</sub>	Reverse-Recovery Time	I <sub>F</sub> = 50A, dI <sub>SD</sub> /dt = 100A/μs	-	47	71	ns
Q <sub>rr</sub>	Reverse-Recovery Charge	V <sub>DD</sub> = 32V	-	36	71	nC

#### Note:

4: The maximum value is specified by design at  $T_J$  = 175°C. Product is not tested to this condition in production.

## **Typical Characteristics**



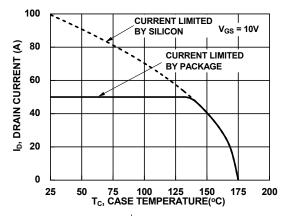


Figure 1. Normalized Power Dissipation vs. Case Temperature

Figure 2. Maximum Continuous Drain Current vs.

Case Temperature

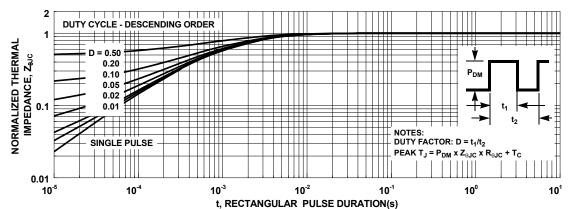


Figure 3. Normalized Maximum Transient Thermal Impedance

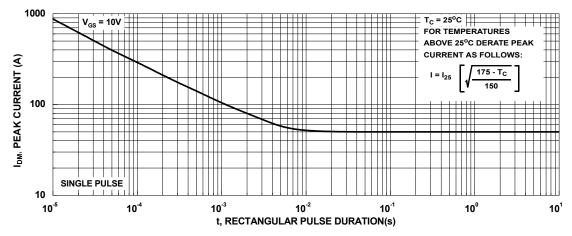


Figure 4. Peak Current Capability

## **Typical Characteristics**

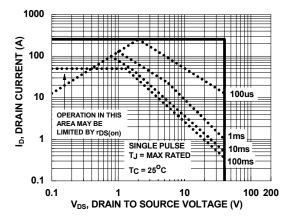
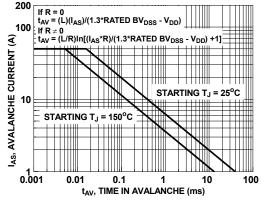


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to Fairchild Application Notes AN7514 and AN7515

Figure 6. Unclamped Inductive Switching

Capability

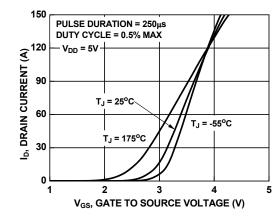


Figure 7. Transfer Characteristics

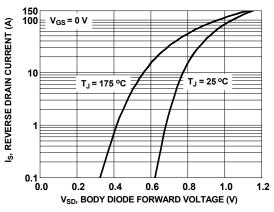


Figure 8. Forward Diode Characteristics

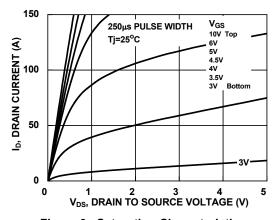


Figure 9. Saturation Characteristics

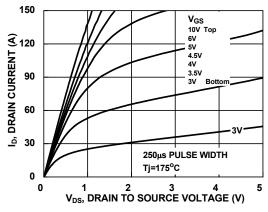


Figure 10. Saturation Characteristics

## **Typical Characteristics**

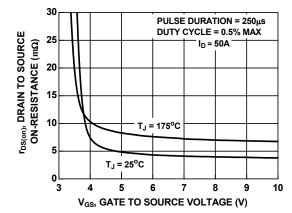


Figure 11. R<sub>DSON</sub> vs. Gate Voltage

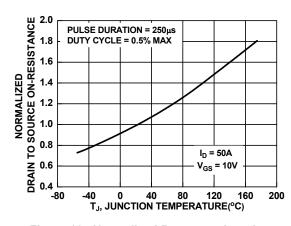


Figure 12. Normalized R<sub>DSON</sub> vs. Junction Temperature

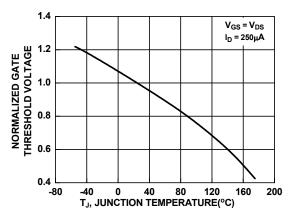


Figure 13. Normalized Gate Threshold Voltage vs. Temperature

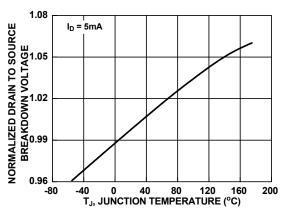


Figure 14. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

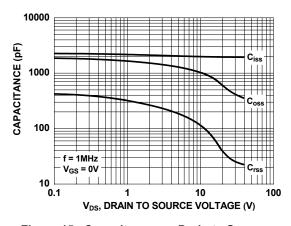


Figure 15. Capacitance vs. Drain to Source Voltage

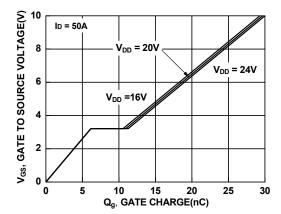


Figure 16. Gate Charge vs. Gate to Source Voltage





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