ISL84514, ISL84515

Low-Voltage, Single Supply, SPST, Analog Switches

FN6025
Rev 5.00
June 9, 2014

The Intersil ISL84514 and ISL84515 devices are precision, analog switches designed to operate from a single +2.4V to +12V supply. Targeted applications include battery powered equipment that benefit from the devices' low power consumption (5µW), and low leakage currents (1nA). Low r_{ON} and fast switching speeds over a wide operating supply range make these switches ideal for use in industrial equipment, portable instruments, and as input signal multiplexers for new generation, low supply voltage data converters. Some of the smallest packages available alleviate board space limitations, and make Intersil's newest line of low-voltage switches an ideal solution for space constrained products.

The ISL8451x are single-pole/single-throw (SPST) switches, with the ISL84514 being normally open (NO), and the ISL84515 being normally closed (NC).

Table 1 summarizes the performance of this family. For higher performance, pin compatible versions, see the ISL43110, ISL43111 data sheet. For ±5V supply versions, see the ISL84516, ISL84517 data sheet.

TABLE 1. FEATURES AT A GLANCE

DESCRIPTION	ISL84514	ISL84515
Number of Switches	1	1
Configuration	NO	NC
3.3V r_{ON}	20Ω	20Ω
3.3V t_{ON}/t_{OFF}	60ns/30ns	60ns/30ns
5V r_{ON}	12Ω	12Ω
5V t_{ON}/t_{OFF}	45ns/25ns	45ns/25ns
12V r_{ON}	8Ω	8Ω
12V t_{ON}/t_{OFF}	40ns/25ns	40ns/25ns
Packages	8 Ld SOIC, 5 Ld SOT-23	

Related Literature

- Technical Brief TB363 "Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)"
- Application Note AN557 "Recommended Test Procedures for Analog Switches"

Features

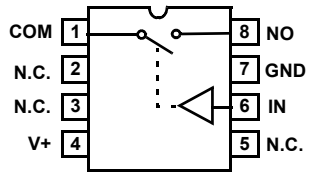
- Drop-in replacements for MAX4514 and MAX4515
- Available in SOT-23 and SOIC packaging
- Fully specified for 5V and 12V supplies
- Single supply operation . . . . . +2.4V to +12V
- ON-resistance (r_{ON} max) . . . . . 20Ω (V+ = 5V)
  10Ω (V+ = 12V)
- r_{ON} flatness (max) 3Ω
- Charge injection (max) 10pC
- Low power consumption (P_D) . . . . . <5µW
- Low leakage current (max at +85°C) . . 20nA (off leakage)
  40nA (on leakage)
- Fast switching action
  - t_{ON} (max) 150ns
  - t_{OFF} (max) 100ns
- Minimum 2000V ESD protection per method 3015.7
- TTL, CMOS compatible
- Pb-free (RoHS compliant)

Applications

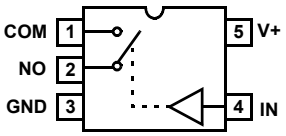
- Battery powered, handheld, and portable equipment
- Communications systems
  - Radios
  - Telecom infrastructure
- Test equipment
  - Logic and spectrum analyzers
  - Portable meters
- Medical equipment
  - Ultrasound and MRI
  - Electrocardiograph
- Audio and video switching
- General purpose circuits
  - +3V/+5V DACs and ADCs
  - Sample and hold circuits
  - Digital filters
  - Operational amplifier gain switching networks
  - High frequency analog switching
  - High-speed multiplexing
  - Integrator reset circuits

Pinouts (Note 1))

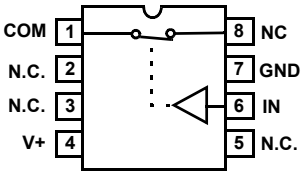
ISL84514
(8 LD SOIC)
TOP VIEW



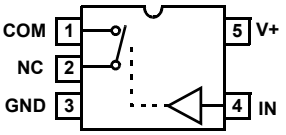
ISL84514
(5 LD SOT-23)
TOP VIEW



ISL84515
(8 LD SOIC)
TOP VIEW



ISL84515
(5 LD SOT-23)
TOP VIEW



NOTE:

1. Switches Shown for Logic “0” Input.

Truth Table

LOGIC	ISL84514	ISL84515
0	OFF	ON
1	ON	OFF

NOTE: Logic “0” ≤ 0.8V. Logic “1” ≥ 2.4V.

Pin Description

PIN	FUNCTION
V+	System Power Supply Input (+2.4V to +12V)
GND	Ground Connection
IN	Digital Control Input
COM	Analog Switch Common Pin
NO	Analog Switch Normally Open Pin
NC	Analog Switch Normally Closed Pin
N.C.	No Internal Connection

Ordering Information

PART NUMBER (Notes 3, 4)	PART MARKING	TEMP RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL84514IBZ	84514 IBZ	-40 to +85	8 Ld SOIC	M8.15
ISL84514IBZ-T (Note 2)	84514 IBZ	-40 to +85	8 Ld SOIC Tape and Reel	M8.15
ISL84514IHZ-T (Note 2)	514Z (Note 5)	-40 to +85	5 Ld SOT-23, Tape and Reel	P5.064
ISL84515IBZ	84515 IBZ	-40 to +85	8 Ld SOIC	M8.15
ISL84515IBZ-T (Note 2)	84515 IBZ	-40 to +85	8 Ld SOIC Tape and Reel	M8.15
ISL84515IHZ-T (Note 2)	515Z (Note 5)	-40 to +85	5 Ld SOT-23, Tape and Reel	P5.064

NOTES:

2. Please refer to TB347 for details on reel specifications.
3. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
4. For Moisture Sensitivity Level (MSL), please see product information page for ISL84514, ISL85415. For more information on MSL, please see tech brief TB363.
5. The part marking is located on the bottom of the part.

Absolute Maximum Ratings

V+ to GND . . . . . -0.3 to 15V
Input Voltages
IN (Note 6) . . . . . -0.3 to ((V+) + 0.3V)
NO, NC (Note 6). . . . . -0.3 to ((V+) + 0.3V)
Output Voltages
COM (Note 6). . . . . -0.3 to ((V+) + 0.3V)
Continuous Current (Any Terminal) 20mA
Peak Current NO, NC, or COM
(Pulsed 1ms, 10% Duty Cycle, Max) 30mA
ESD Rating
Human Body Model (Per MIL-STD-883 Method 3015) 2.5kV
Machine Model 100V

Thermal Information

Thermal Resistance (Typical, Note 7)	θ_{JA} (°C/W)
5 Ld SOT-23 Package	225
8 Ld SOIC Package	170

Maximum Junction Temperature (Plastic Package). . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Pb-Free Reflow Profile. . . . . see TB493

Operating Conditions

Temperature Range . . . . . -40°C to +85°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

6. Signals on NO, NC, COM, or IN exceeding V+ or GND are clamped by internal diodes. Limit forward diode current to maximum current ratings.
7. θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications

Test Conditions: V+ = +4.5V to +5.5V, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V (Note 8), unless otherwise specified. Boldface limits apply across the operating temperature range, -40°C to +85°C.

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 9, 11)	TYP	MAX (Notes 9, 11)	UNITS
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}		Full	**0**	-	**V+**	V
ON-resistance, r_{ON}	V+ = 4.5V, I_{COM} = 1.0mA, V_{COM} = 3.5V, (see Figure 4)	+25	-	-	20	Ω
		Full	-	-	**25**	Ω
r_{ON} Flatness, $R_{FLAT(ON)}$	V+ = 4.5V, I_{COM} = 1.0mA, V_{COM} = 1V, 2V, 3V	+25	-	-	3	Ω
		Full	-	-	**5**	Ω
NO or NC OFF Leakage Current, $I_{NO(OFF)}$ or $I_{NC(OFF)}$	V+ = 5.5V, V_{COM} = 1V, 4.5V, V_{NO} or V_{NC} = 4.5V, 1V, (Note 10)	+25	-1	0.01	1	nA
		Full	**-20**	-	**20**	nA
COM OFF Leakage Current, $I_{COM(OFF)}$	V+ = 5.5V, V_{COM} = 4.5V, 1V, V_{NO} or V_{NC} = 1V, 4.5V, (Note 10)	+25	-1	0.01	1	nA
		Full	**-20**	-	**20**	nA
COM ON Leakage Current, $I_{COM(ON)}$	V+ = 5.5V, V_{COM} = 1V, 4.5V, or V_{NO} or V_{NC} = 1V, 4.5V, (Note 10)	+25	-2	0.01	2	nA
		Full	**-40**	-	**40**	nA
DIGITAL INPUT CHARACTERISTICS						
Input Voltage High, V_{INH}		Full	**2.4**	-	**V+**	V
Input Voltage Low, V_{INL}		Full	**0**	-	**0.8**	V
Input Current, I_{INH}, I_{INL}	V+ = 5.5V, V_{IN} = 0V or V+	Full	**-1**	-	**1**	µA
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	V_{NO} or V_{NC} = 3V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3V, (see Figure 1)	+25	-	-	150	ns
		Full	-	-	**240**	ns
Turn-OFF Time, t_{OFF}	V_{NO} or V_{NC} = 3V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3V, (see Figure 1)	+25	-	-	100	ns
		Full	-	-	**150**	ns
Charge Injection, Q	C_L = 1.0nF, V_G = 0V, R_G = 0Ω, (see Figure 2)	+25	-	2	10	pC
OFF-isolation	R_L = 50Ω, C_L = 15pF, f = 100kHz, (see Figure 3)	+25	-	>90	-	dB
NO or NC OFF Capacitance, C_{OFF}	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V, (see Figure 5)	+25	-	14	-	pF

Electrical Specifications Test Conditions: V+ = +4.5V to +5.5V, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V (Note 8), unless otherwise specified. Boldface limits apply across the operating temperature range, -40°C to +85°C. **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 9, 11)	TYP	MAX (Notes 9, 11)	UNITS
COM OFF Capacitance, $C_{COM(OFF)}$	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V, (see Figure 5)	+25	-	14	-	pF
COM ON Capacitance, $C_{COM(ON)}$	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V, (see Figure 5)	+25	-	30	-	pF
POWER SUPPLY CHARACTERISTICS						
Positive Supply Current, I+	V+ = 5.5V, V_{IN} = 0V or V+, Switch On or Off	+25	-1	0.0001	1	µA
		Full	**-10**	-	**10**	µA

Electrical Specifications - 12V Supply Test Conditions: V+ = +10.8V to +13.2V, GND = 0V, V_{INH} = 5V, V_{INL} = 0.8V (Note 8), unless otherwise specified. **Boldface limits apply across the operating temperature range, -40°C to +85°C.**

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 9, 11)	TYP	MAX (Notes 9, 11)	UNITS
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}		Full	**0**	-	**V+**	V
ON-resistance, r_{ON}	V+ = 10.8V, I_{COM} = 1.0mA, V_{COM} = 10V	+25	-	-	10	Ω
		Full	-	-	**15**	Ω
r_{ON} Flatness, $R_{FLAT(ON)}$	V+ = 12V, I_{COM} = 1.0mA, V_{COM} = 3V, 6V, 9V	+25	-	-	3	Ω
		Full	-	-	**5**	Ω
NO or NC OFF Leakage Current, $I_{NO(OFF)}$ or $I_{NC(OFF)}$	V+ = 13.2V, V_{COM} = 1V, 10V, V_{NO} or V_{NC} = 10V, 1V, (Note 10)	+25	-2	-	2	nA
		Full	**-50**	-	**50**	nA
COM OFF Leakage Current, $I_{COM(OFF)}$	V+ = 13.2V, V_{COM} = 10V, 1V, V_{NO} or V_{NC} = 1V, 10V, (Note 10)	+25	-2	-	2	nA
		Full	**-50**	-	**50**	nA
COM ON Leakage Current, $I_{COM(ON)}$	V+ = 13.2V, V_{COM} = 1V, 10V, or V_{NO} or V_{NC} = 1V, 10V, (Note 10)	+25	-4	-	4	nA
		Full	**-100**	-	**100**	nA
DIGITAL INPUT CHARACTERISTICS						
Input Voltage High, V_{INH}		Full	**5**	3	**V+**	V
Input Voltage Low, V_{INL}		Full	**0**	-	**0.8**	V
Input Current, I_{INH}, I_{INL}	V+ = 13.2V, V_{IN} = 0V or V+	Full	**-1**	-	**1**	µA
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	V_{NO} or V_{NC} = 10V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 5V, (see Figure 1)	+25	-	-	150	ns
		Full	-	-	**240**	ns
Turn-OFF Time, t_{OFF}	V_{NO} or V_{NC} = 10V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 5V, (see Figure 1)	+25	-	-	100	ns
		Full	-	-	**150**	ns
Charge Injection, Q	C_L = 1.0nF, V_G = 0V, R_G = 0Ω, (see Figure 2)	+25	-	8	20	pC
OFF-isolation	R_L = 50Ω, C_L = 15pF, f = 100kHz, (see Figure 3)	+25	-	>90	-	dB
NO or NC OFF Capacitance, C_{OFF}	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V, (see Figure 5)	+25	-	14	-	pF
COM OFF Capacitance, $C_{COM(OFF)}$	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V, (see Figure 5)	+25	-	14	-	pF
COM ON Capacitance, $C_{COM(ON)}$	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V, (see Figure 5)	+25	-	30	-	pF
POWER SUPPLY CHARACTERISTICS						
Positive Supply Current, I+	V+ = 13.2V, V_{IN} = 0V or V+, Switch On or Off	+25	-2	-	2	µA
		Full	**-20**	-	**20**	µA

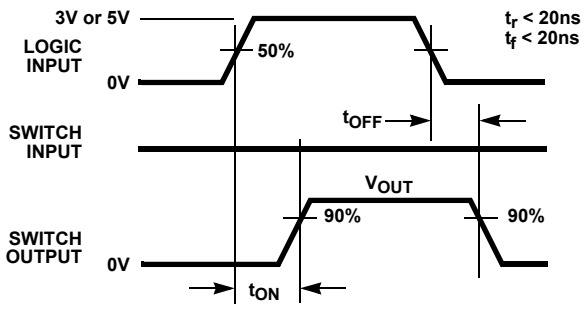
Electrical Specifications - 3.3V Supply Test Conditions: V+ = +3.0V to +3.6V, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V (Note 8), Unless Otherwise Specified. **Boldface limits apply across the operating temperature range, -40°C to +85°C.**

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 9, 11)	TYP	MAX (Notes 9, 11)	UNITS
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}		Full	**0**	-	**V+**	V
ON-resistance, r_{ON}	V+ = 3V, I_{COM} = 1.0mA, V_{COM} = 1.5V	+25	-	-	50	Ω
		Full	-	-	**75**	Ω
r_{ON} Flatness, $R_{FLAT(ON)}$	I_{COM} = 1.0mA, V_{COM} = 0.5V, 1V, 1.5V	+25	-	-	5.5	Ω
		Full	-	-	**7.0**	Ω
NO or NC OFF Leakage Current, $I_{NO(OFF)}$ or $I_{NC(OFF)}$	V+ = 3.6V, V_{COM} = 3V, 1V, V_{NO} or V_{NC} = 1V, 3V, (Note 10)	+25	-1	0.01	1	nA
		Full	**-20**	-	**20**	nA
COM OFF Leakage Current, $I_{COM(OFF)}$	V+ = 3.6V, V_{COM} = 3V, 1V, V_{NO} or V_{NC} = 1V, 3V, (Note 10)	+25	-1	0.01	1	nA
		Full	**-20**	-	**20**	nA
COM ON Leakage Current, $I_{COM(ON)}$	V+ = 3.6V, V_{COM} = 1V, 3V, or V_{NO} or V_{NC} = 1V, 3V, (Note 10)	+25	-2	0.01	2	nA
		Full	**-40**	-	**40**	nA
DIGITAL INPUT CHARACTERISTICS						
Input Voltage High, V_{INH}		Full	**2.4**	-	**V+**	V
Input Voltage Low, V_{INL}		Full	**0**	-	**0.8**	V
Input Current, I_{INH}, I_{INL}	V+ = 3.6V, V_{IN} = 0V or V+	Full	**-1**	-	**1**	µA
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	V_{NO} or V_{NC} = 1.5V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3V	+25	-	-	150	ns
		Full	-	-	**240**	ns
Turn-OFF Time, t_{OFF}	V_{NO} or V_{NC} = 1.5V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3V	+25	-	-	100	ns
		Full	-	-	**150**	ns
Charge Injection, Q	C_L = 1.0nF, V_G = 0V, R_G = 0Ω	+25	-	4	10	pC
POWER SUPPLY CHARACTERISTICS						
Positive Supply Current, I+	V+ = 3.6V, V_{IN} = 0V or V+, Switch On or Off	+25	-1	-	1	µA
		Full	**-10**	-	**10**	µA

NOTES:

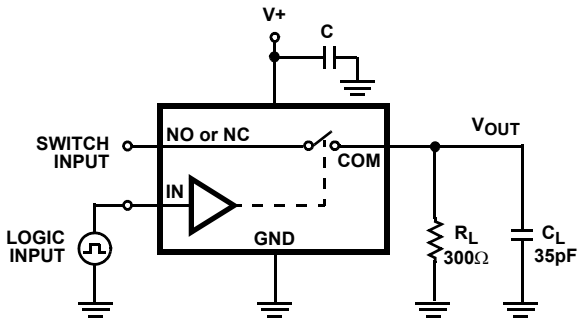
8. V_{IN} = input voltage to perform proper function.
9. The algebraic convention, whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
10. Leakage parameter is 100% tested at high temp, and guaranteed by correlation at +25°C.
11. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

Test Circuits and Waveforms



Logic input waveform is inverted for switches that have the opposite logic sense.

FIGURE 1A. MEASUREMENT POINTS



C_L includes fixture and stray capacitance.

$$V_{OUT} = V_{(NO\ or\ NC)} \frac{R_L}{R_L + r_{ON}}$$

FIGURE 1B. TEST CIRCUIT

FIGURE 1. SWITCHING TIMES

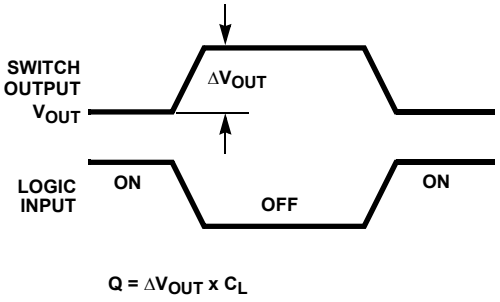


FIGURE 2A. MEASUREMENT POINTS

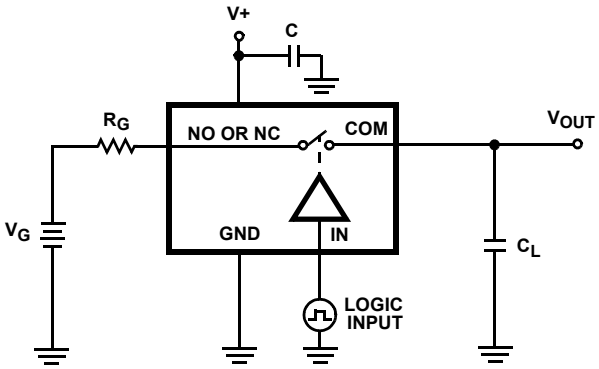


FIGURE 2B. TEST CIRCUIT

FIGURE 2. CHARGE INJECTION

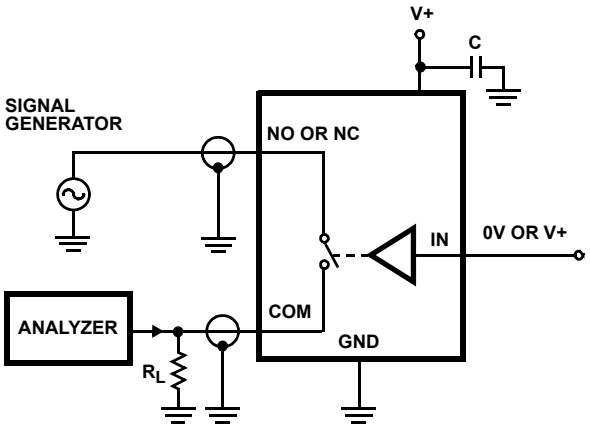


FIGURE 3. OFF-ISOLATION TEST CIRCUIT

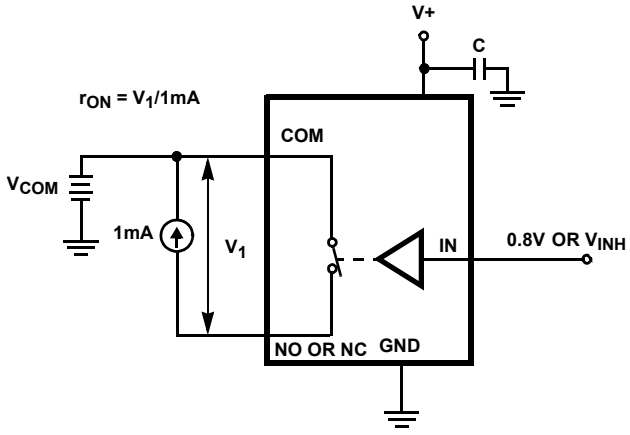


FIGURE 4. r_{ON} TEST CIRCUIT

Test Circuits and Waveforms (Continued)

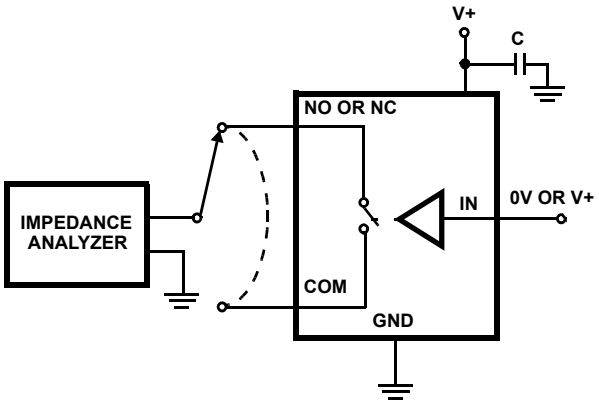


FIGURE 5. CAPACITANCE TEST CIRCUIT

Detailed Description

The ISL84514 and ISL84515 analog switches offer precise switching capability from a single 2.4V to 12V supply with low ON-resistance, and high-speed operation. The devices are especially well suited to portable battery powered equipment thanks to the low operating supply voltage (2.4V), low power consumption (5µW), low leakage currents (2nA max), and the tiny SOT-23 packaging. High frequency applications also benefit from the wide bandwidth, and the very high off-isolation.

Supply Sequencing and Overvoltage Protection

With any CMOS device, proper power supply sequencing is required to protect the device from excessive input currents, which might permanently damage the IC. All I/O pins contain ESD protection diodes from the pin to V+ and to GND (see Figure 6). To prevent forward biasing these diodes, V+ must be applied before any input signals, and input signal voltages must remain between V+ and GND. If these conditions cannot be guaranteed, then one of the following two protection methods should be employed.

Logic inputs can easily be protected by adding a 1kΩ resistor in series with the input (see Figure 6). The resistor limits the input current below the threshold that produces permanent damage, and the sub-microamp input current produces an insignificant voltage drop during normal operation.

Adding a series resistor to the switch input defeats the purpose of using a low r_{ON} switch, so two small signal diodes can be added in series with the supply pins to provide overvoltage protection for all pins (see Figure 6). These additional diodes limit the analog signal from 1V below V+ to 1V above GND. The low leakage current performance is unaffected by this approach, but the switch resistance may increase, especially at low supply voltages

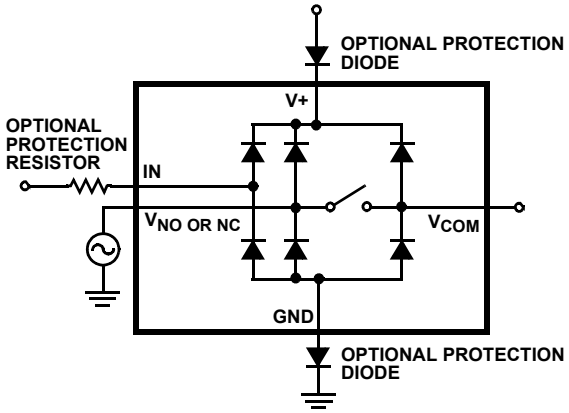


FIGURE 6. OVERVOLTAGE PROTECTION

Power-Supply Considerations

The ISL8451x construction is typical of most CMOS analog switches, except that there are only two supply pins: V+ and GND. Unlike switches with a 13V maximum supply voltage, the ISL8451x 15V maximum supply voltage provides plenty of room for the 10% tolerance of 12V supplies, as well as margin for overshoot and noise spikes.

The minimum recommended supply voltage is 2.4V. It is important to note that the input signal range, switching times, and ON-resistance degrade at lower supply voltages. Refer to the “Electrical Specifications” tables beginning on page 3 and “Typical Performance Curves” beginning on page 9 for details.

V+ and GND power the internal CMOS switches and set their analog voltage limits. These supplies also power the internal logic and level shifters. The level shifters convert the input logic levels to switched V+ and GND signals to drive the analog switch gate terminals.

This family of switches cannot be operated with bipolar supplies, because the input switching point becomes negative in this configuration. For a ±5V single SPST switch, see the ISL84516, ISL84517 data sheet.

Logic-Level Thresholds

This switch family is TTL compatible (0.8V and 2.4V) over a supply range of 3V to 11V, and the full temperature range (see Figure 10). At 12V the low temperature V_{IH} level is about 2.5V. This is still below the TTL guaranteed high output minimum level of 2.8V, but noise margin is reduced. For best results with a 12V supply, use a logic family that provides a V_{OH} greater than 3V.

The digital input stages draw supply current whenever the digital input voltage is not at one of the supply rails. Driving the digital input signals from GND to V+ with a fast transition time minimizes power dissipation.

High-Frequency Performance

In 50Ω systems, signal response is reasonably flat to 20MHz, with a -3dB bandwidth exceeding 200MHz (see Figure 13). Figure 13 also illustrates that the frequency response is very consistent over a wide V+ range, and for varying analog signal levels.

An OFF switch acts like a capacitor and passes higher frequencies with less attenuation, resulting in signal feed-through from a switch's input to its output. Off-isolation is the resistance to this feed-through. Figure 14 details the high off-isolation provided by this family. At 10MHz, off-isolation is about 50dB in 50Ω systems, decreasing approximately 20dB per decade as frequency increases. Higher load impedances decrease off-isolation due to the voltage divider action of the switch OFF impedance and the load impedance.

Leakage Considerations

Reverse ESD protection diodes are internally connected between each analog-signal pin and both V+ and GND. One of these diodes conducts if any analog signal exceeds V+ or GND.

Virtually, all the analog leakage current comes from the ESD diodes to V+ or GND. Although the ESD diodes on a given signal pin are identical and therefore fairly well balanced, they are reverse biased differently. Each is biased by either V+ or GND and the analog signal. This means their leakages will vary as the signal varies. The difference in the two diode leakages to the V+ and GND pins constitutes the analog-signal-path leakage current. All analog leakage current flows between each pin and one of the supply terminals, not to the other switch terminal. This is why both sides of a given switch can show leakage currents of the same or opposite polarity. There is no connection between the analog-signal paths and V+ or GND.

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified

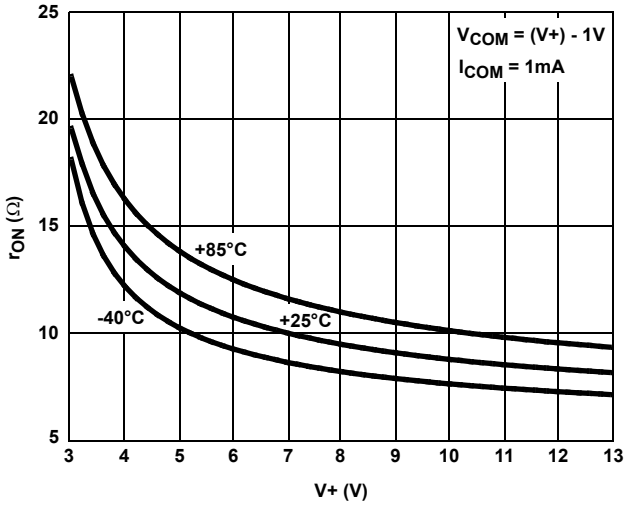


FIGURE 7. ON-RESISTANCE vs SUPPLY VOLTAGE

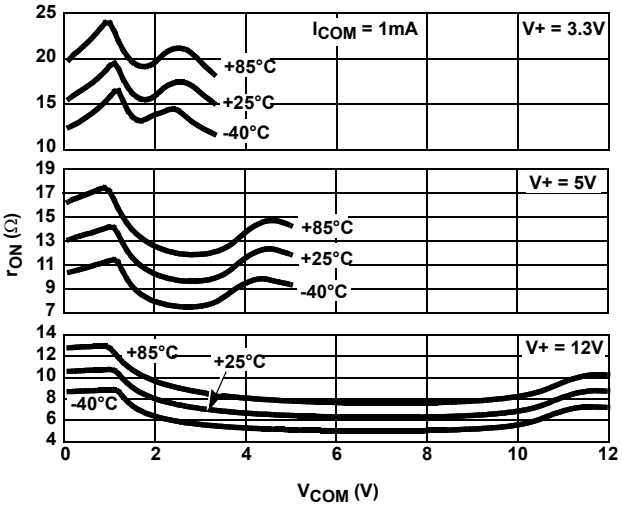


FIGURE 8. ON-RESISTANCE vs SWITCH VOLTAGE

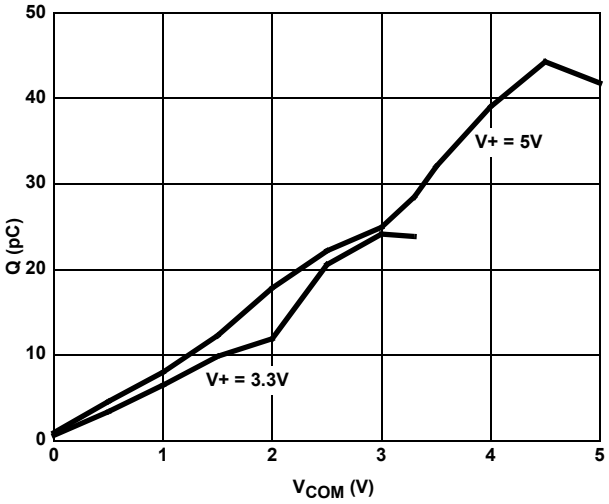


FIGURE 9. CHARGE INJECTION vs SWITCH VOLTAGE

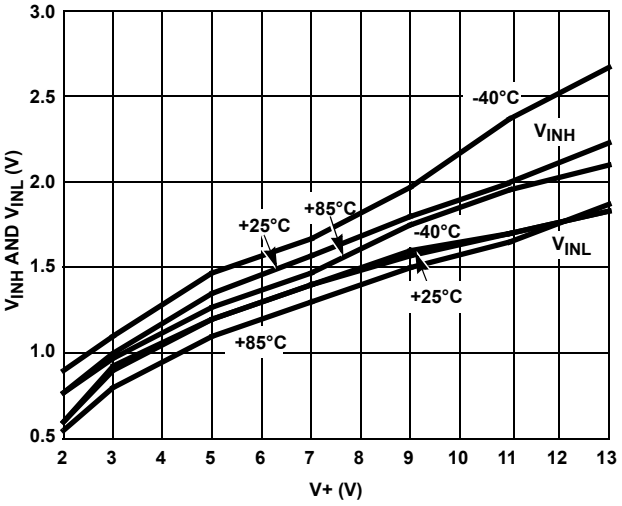


FIGURE 10. DIGITAL SWITCHING POINT vs SUPPLY VOLTAGE

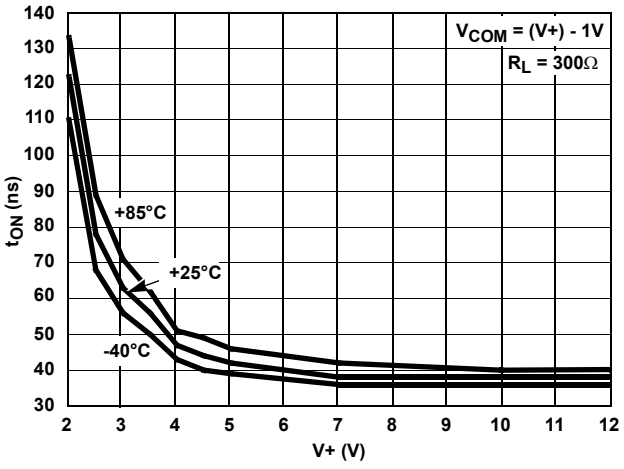


FIGURE 11. TURN-ON TIME vs SUPPLY VOLTAGE

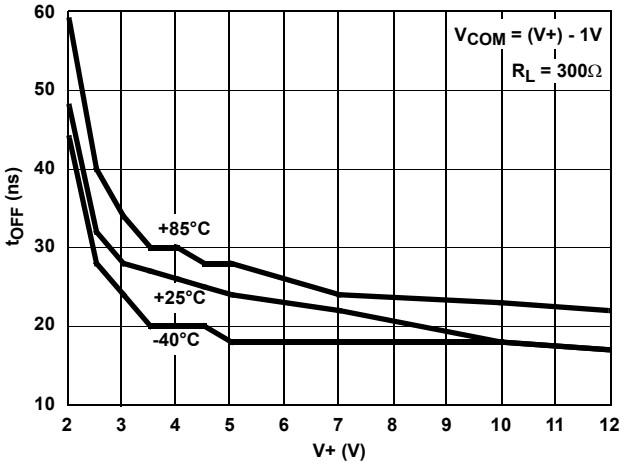


FIGURE 12. TURN-OFF TIME vs SUPPLY VOLTAGE

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified **(Continued)**

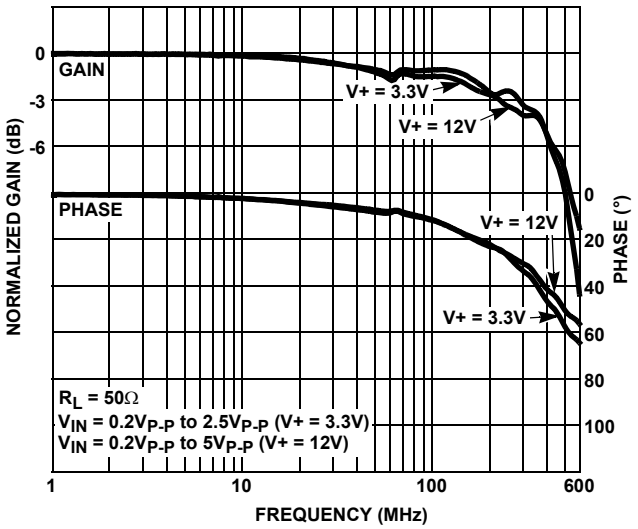


FIGURE 13. FREQUENCY RESPONSE

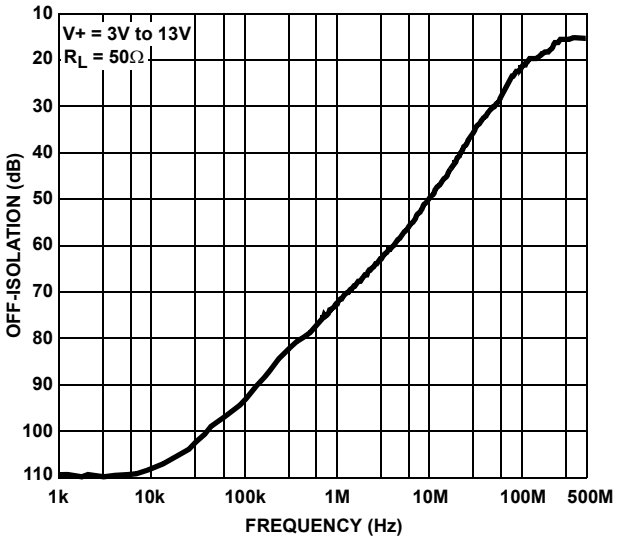


FIGURE 14. OFF-ISOLATION

Die Characteristics

SUBSTRATE POTENTIAL (POWERED UP):

GND

TRANSISTOR COUNT:

ISL84514: 40
ISL84515: 40

PROCESS:

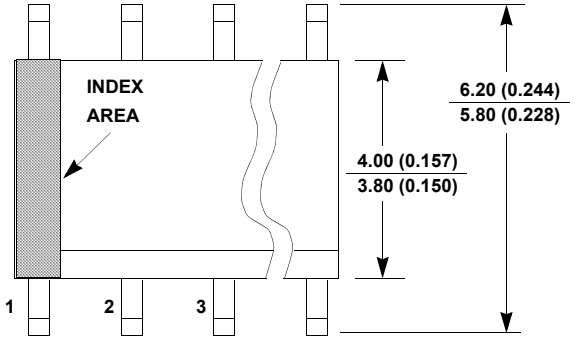
Si Gate CMOS

Package Outline Drawing

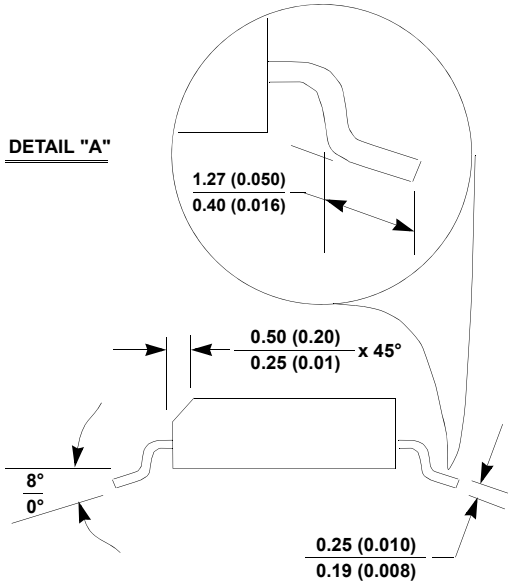
M8.15

8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

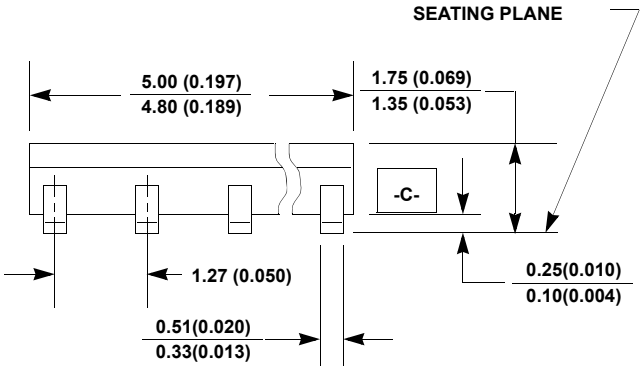
Rev 4, 1/12



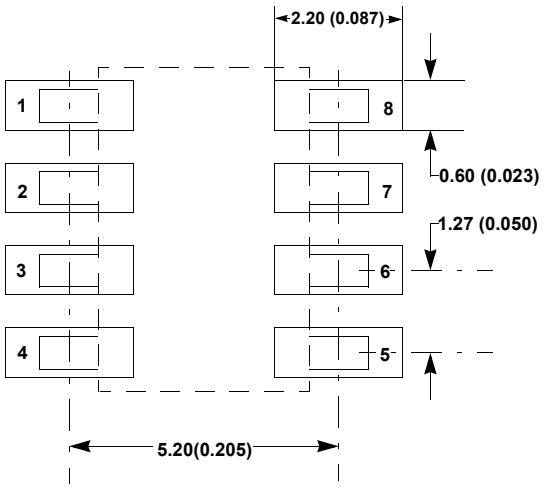
TOP VIEW



SIDE VIEW "B"



SIDE VIEW "A"



TYPICAL RECOMMENDED LAND PATTERN

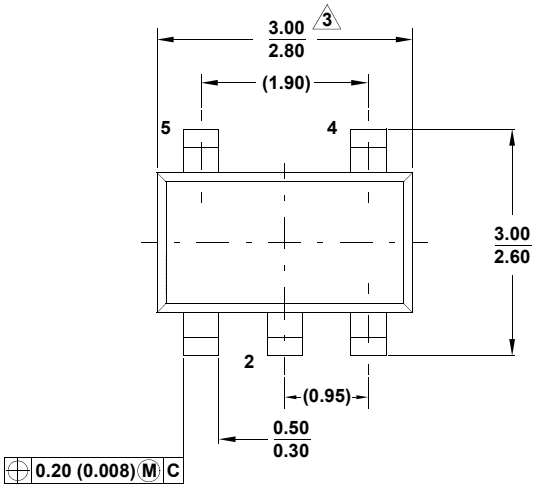
NOTES:

1. Dimensioning and tolerancing per ANSI Y14.5M-1994.
2. Package length does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
3. Package width does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
5. Terminal numbers are shown for reference only.
6. The lead width as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
7. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
8. This outline conforms to JEDEC publication MS-012-AA ISSUE C.

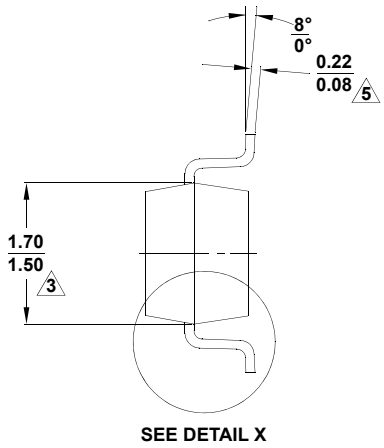
Package Outline Drawing

P5.064

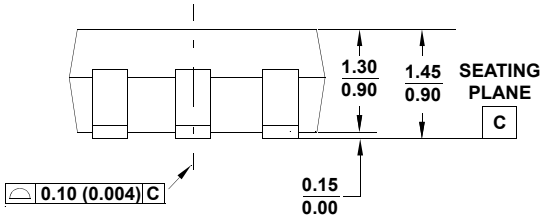
5 LEAD SMALL OUTLINE TRANSISTOR PLASTIC PACKAGE
Rev 3, 4/11



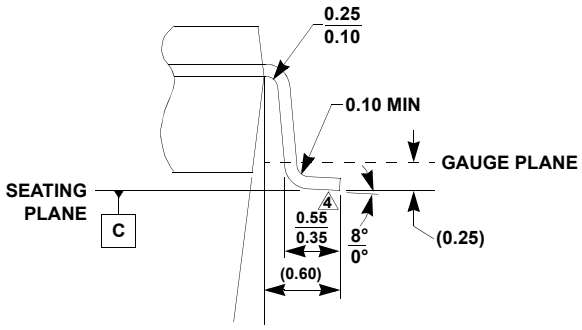
TOP VIEW



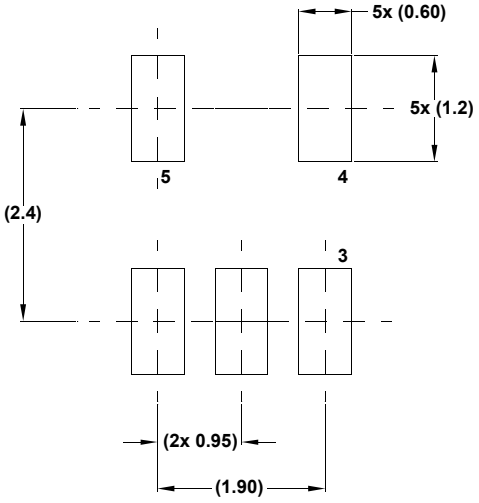
END VIEW



SIDE VIEW



DETAIL "X"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensioning and tolerance per ASME Y14.5M-1994.
2. Package conforms to EIAJ SC-74 and JEDEC MO178AA.
3. Package length and width are exclusive of mold flash, protrusions, or gate burrs.
4. Footlength measured at reference to gauge plane.
5. Lead thickness applies to the flat section of the lead between 0.08mm and 0.15mm from the lead tip.
6. Controlling dimension: MILLIMETER. Dimensions in ( ) for reference only.

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Адрес: 105318, г.Москва, ул.Щербаковская д.3, офис 1107

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