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FDMC008N08C

N-Channel Shielded Gate PowerTrench® MOSFET 80 V, 60 A, 7.8 m Ω

Features

- Shielded Gate MOSFET Technology
- Max $r_{DS(on)}$ = 7.8 m Ω at V_{GS} = 10 V, I_D =21 A
- Max $r_{DS(on)}$ = 19.3 m Ω at V_{GS} = 6 V, I_D = 10 A
- 50% lower Qrr than other MOSFET suppliers
- Lowers switching noise/EMI
- MSL1 robust package design
- 100% UIL tested
- RoHS Compliant

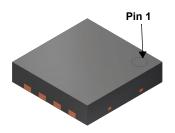


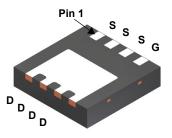
General Description

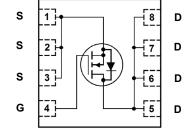
This N-Channel MV MOSFET is produced using ON Semiconductor's advanced PowerTrench® process that incorporates Shielded Gate technology. This process has been optimized to minimise on-state resistance and yet maintain superior switching performance with best in class soft body diode.

Applications

- Primary DC-DC MOSFET
- Synchronous Rectifier in DC-DC and AC-DC
- Motor Drive
- Solar







Top Power 33 Bottom

MOSFET Maximum Ratings $T_A = 25$ °C unless otherwise noted.

Symbol	Paramete	r		Ratings	Units
V _{DS}	Drain to Source Voltage			80	V
V_{GS}	Gate to Source Voltage			±20	V
	Drain Current -Continuous	T _C = 25 °C	(Note 5)	60	
	-Continuous	T _C = 100 °C	(Note 5)	38	A
I _D	-Continuous	T _A = 25 °C	(Note 1a)	12	_ ^
	-Pulsed		(Note 4)	273	
E _{AS}	Single Pulse Avalanche Energy		(Note 3)	150	mJ
P _D	Power Dissipation	T _C = 25 °C		57	W
	Power Dissipation	T _A = 25 °C	(Note 1a)	2.3	VV
T _J , T _{STG}	Operating and Storage Junction Temperature	e Range		-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	2.2	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	53	C/VV

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
008N08C	FDMC008N08C	Power 33	13 "	12 mm	3000 units

Electrical Characteristics T_J = 25 °C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Units	
Off Characteristics							
BV_{DSS}	Drain to Source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0 V	80			V	
$\frac{\Delta BV_{DSS}}{\Delta T_{J}}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C		51		mV/°C	
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 64 V, V _{GS} = 0 V			1	μА	
I _{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$			100	nA	

On Characteristics

V _{GS(th)}	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 120 \mu A$	2.0	3.0	4.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I _D = 120 μA, referenced to 25 °C		-8.4		mV/°C
r _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = 10 V, I _D = 21 A		6.3	7.8	
		V _{GS} = 6 V, I _D = 10 A		9.6	19.3	mΩ
		$V_{GS} = 10 \text{ V}, I_D = 21 \text{ A}, T_J = 125 ^{\circ}\text{C}$		10.7	13.5	
9 _{FS}	Forward Transconductance	V _{DS} = 5 V, I _D = 21 A		50		S

Dynamic Characteristics

C _{iss}	Input Capacitance	V - 40 V V - 0 V		1535	2150	pF
C _{oss}	Output Capacitance	V _{DS} = 40 V, V _{GS} = 0 V, f = 1 MHz		517	730	pF
C _{rss}	Reverse Transfer Capacitance	1 - 1 1011 12		19	30	pF
R_q	Gate Resistance		0.1	0.4	0.8	Ω

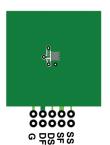
Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time		12	22	ns
t _r	Rise Time	V _{DD} = 40 V, I _D = 21 A,	3	10	ns
t _{d(off)}	Turn-Off Delay Time	V_{GS} = 10 V, R_{GEN} = 6 Ω	18	32	ns
t _f	Fall Time		3	10	ns
Q_g	Total Gate Charge	V _{GS} = 0 V to 10 V	21	29	nC
Q_g	Total Gate Charge	$V_{GS} = 0 \text{ V to 6 V}$ $V_{DD} = 40 \text{ V},$	13	18	nC
Q_{gs}	Gate to Source Charge	I _D = 21 A	6.7		nC
Q_{gd}	Gate to Drain "Miller" Charge		3.8		nC
Q _{oss}	Output Charge	V _{DD} = 40 V, V _{GS} = 0 V	28		nC
Q _{sync}	Total Gate Charge Sync.	V _{DS} = 0 V, I _D = 21 A	18		nC

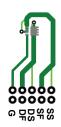
Drain-Source Diode Characteristics

V _{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_S = 2 \text{ A}$ (Note 2)	0.7	1.2	V
	Source to Drain blode Forward Voltage	$V_{GS} = 0 \text{ V}, I_{S} = 21 \text{ A}$ (Note 2)	0.8	1.3	V
t _{rr}	Reverse Recovery Time	I _F = 10 A, di/dt = 300 A/μs	19	30	ns
Q _{rr}	Reverse Recovery Charge	-1 _F = 10 A, α//αι = 300 A/μs	27	44	nC
t _{rr}	Reverse Recovery Time	I _E = 10 A, di/dt = 1000 A/μs	15	23	ns
Q _{rr}	Reverse Recovery Charge	- 1 _F - 10 A, αι/αι - 1000 A/μs	65	105	nC

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in 2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta CA}$ is determined by the user's board design.



a. 53 °C/W when mounted on a 1 in² pad of 2 oz



b. 125 $^{\circ}\text{C/W}$ when mounted on a minimum pad of 2 oz

^{2.} Pulse Test: Pulse Width < $300 \, \mu s$, Duty cycle < 2.0%.
3. E_{AS} of 150 mJ is based on starting T_J = $25 \, ^{\circ}C$, L = 3 mH, I_{AS} = $10 \, A$, V_{DD} = $10 \, V$, V_{GS} = $80 \, V$, 100% test at L = $0.1 \, \text{mH}$, I_{AS} = $33 \, A$.
4. Pulsed Id please refer to Fig 11 SOA graph for more details.
5. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

Typical Characteristics T_J = 25 °C unless otherwise noted.

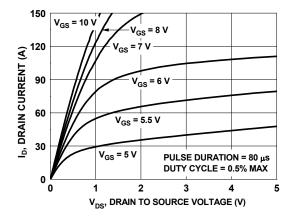


Figure 1. On Region Characteristics

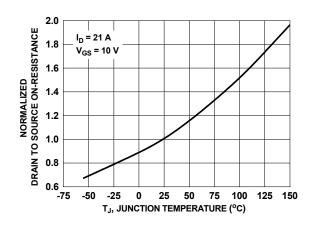


Figure 3. Normalized On Resistance vs. Junction Temperature

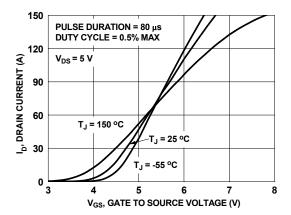


Figure 5. Transfer Characteristics

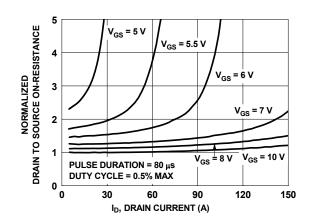


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

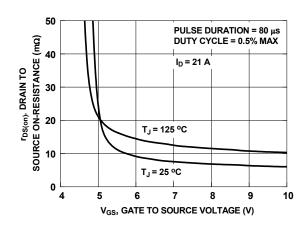


Figure 4. On-Resistance vs. Gate to Source Voltage

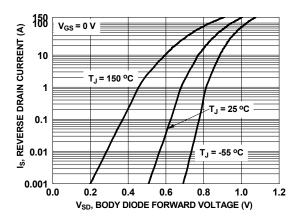


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

Typical Characteristics $T_J = 25$ °C unless otherwise noted.

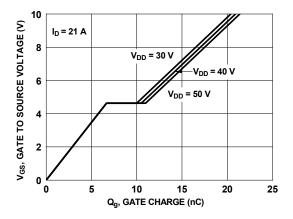


Figure 7. Gate Charge Characteristics

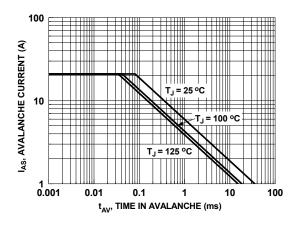


Figure 9. Unclamped Inductive Switching Capability

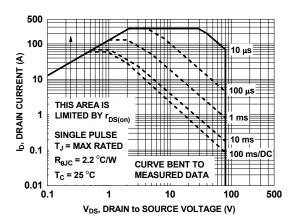


Figure 11. Forward Bias Safe Operating Area

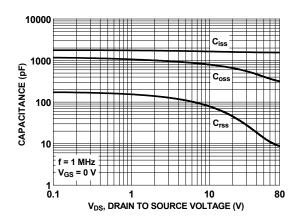


Figure 8. Capacitance vs. Drain to Source Voltage

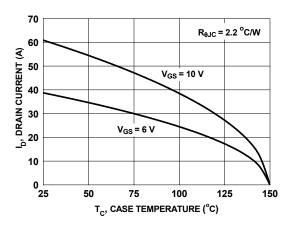


Figure 10. Maximum Continuous Drain Current vs Case Temperature

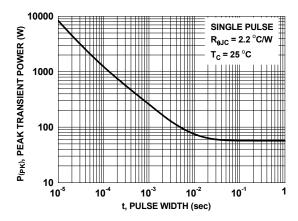


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics T_J = 25 °C unless otherwise noted.

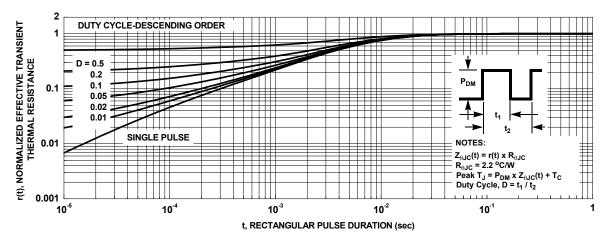
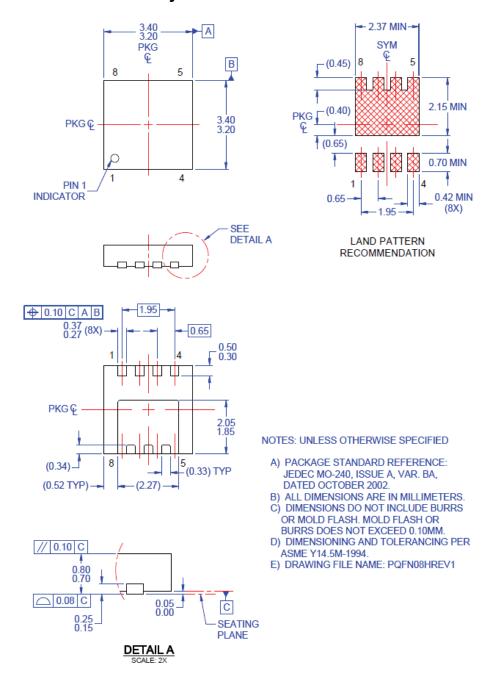


Figure 13. Junction-to-Case Transient Thermal Response Curve

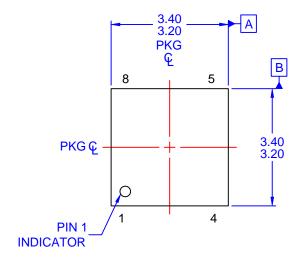
Dimensional Outline and Pad Layout

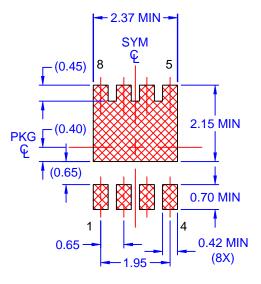


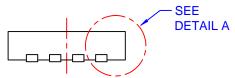
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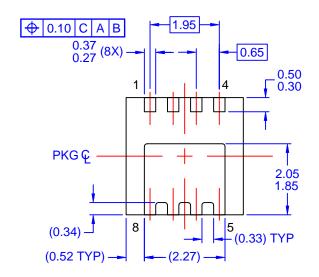
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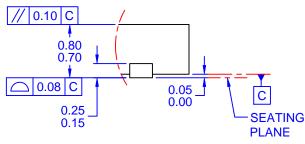


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