FAIRCHILD SEMICONDUCTOR™

April 1988
Revised August 2000

# 74F32
# Quad 2-Input OR Gate

## General Description

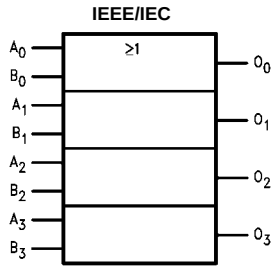
This device contains four independent gates, each of which performs the logic OR function.

## Ordering Code:

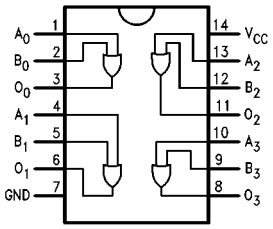
| Order Number | Package Number | Package Description |
|---|---|---|
| 74F32SC | M14A | 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow |
| 74F32SJ | M14D | 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| 74F32MTC | MTC14 | 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide |
| 74F32PC | N14A | 14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide |

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

## Logic Symbol




## Connection Diagram




## Unit Loading/Fan Out

| Pin Names | Description | U.L. HIGH/LOW | Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$ |
|---|---|---|---|
| $A_n$, $B_n$ | Inputs | 1.0/1.0 | 20 µA/−0.6 mA |
| $O_n$ | Outputs | 50/33.3 | −1 mA/20 mA |

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## Absolute Maximum Ratings(Note 1)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Ambient Temperature under Bias | −55°C to +125°C |
| Junction Temperature under Bias | −55°C to +150°C |
| $V_{CC}$ Pin Potential to Ground Pin | −0.5V to +7.0V |
| Input Voltage (Note 2) | −0.5V to +7.0V |
| Input Current (Note 2) | −30 mA to +5.0 mA |
| Voltage Applied to Output | |
| in HIGH State (with $V_{CC}$ = 0V) | |
| Standard Output | −0.5V to $V_{CC}$ |
| 3-STATE Output | −0.5V to +5.5V |
| Current Applied to Output | |
| in LOW State (Max) | twice the rated $I_{OL}$ (mA) |
| ESD Last Passing Voltage (Min) | 4000V |

## Recommended Operating Conditions

| | |
|---|---|
| Free Air Ambient Temperature | 0°C to +70°C |
| Supply Voltage | +4.5V to +5.5V |

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

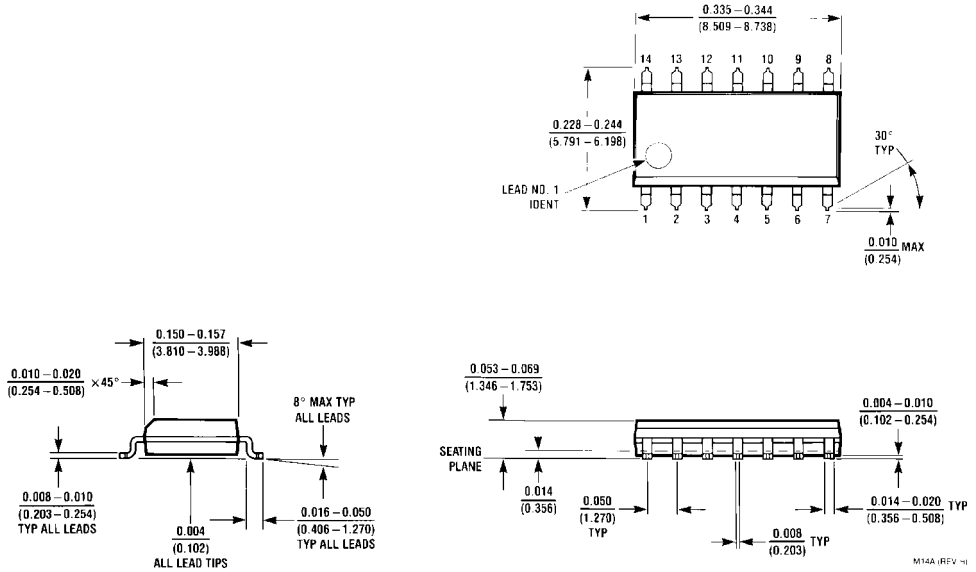
## DC Electrical Characteristics

| Symbol | Parameter | | Min | Typ | Max | Units | $V_{CC}$ | Conditions |
|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage | | 2.0 | | | V | | Recognized as a HIGH Signal |
| $V_{IL}$ | Input LOW Voltage | | | | 0.8 | V | | Recognized as a LOW Signal |
| $V_{CD}$ | Input Clamp Diode Voltage | | | | −1.2 | V | Min | $I_{IN}$ = −18 mA |
| $V_{OH}$ | Output HIGH | 10% $V_{CC}$ | 2.5 | | | V | Min | $I_{OH}$ = −1 mA |
| | Voltage | 5% $V_{CC}$ | 2.7 | | | | | $I_{OH}$ = −1 mA |
| $V_{OL}$ | Output LOW | 10% $V_{CC}$ | | | 0.5 | V | Min | $I_{OL}$ = 20 mA |
| | Voltage | | | | | | | |
| $I_{IH}$ | Input HIGH | | | | 5.0 | µA | Max | $V_{IN}$ = 2.7V |
| | Current | | | | | | | |
| $I_{BVI}$ | Input HIGH Current | | | | 7.0 | µA | Max | $V_{IN}$ = 7.0V |
| | Breakdown Test | | | | | | | |
| $I_{CEX}$ | Output HIGH | | | | 50 | µA | Max | $V_{OUT}$ = $V_{CC}$ |
| | Leakage Current | | | | | | | |
| $V_{ID}$ | Input Leakage | | 4.75 | | | V | 0.0 | $I_{ID}$ = 1.9 µA |
| | Test | | | | | | | All Other Pins Grounded |
| $I_{OD}$ | Output Leakage | | | | 3.75 | µA | 0.0 | $V_{IOD}$ = 150 mV |
| | Circuit Current | | | | | | | All Other Pins Grounded |
| $I_{IL}$ | Input LOW Current | | | | −0.6 | mA | Max | $V_{IN}$ = 0.5V |
| $I_{OS}$ | Output Short-Circuit Current | | −60 | | −150 | mA | Max | $V_{OUT}$ = 0V |
| $I_{CCH}$ | Power Supply Current | | | 6.1 | 9.2 | mA | Max | $V_O$ = HIGH |
| $I_{CCL}$ | Power Supply Current | | | 10.3 | 15.5 | mA | Max | $V_O$ = LOW |

## AC Electrical Characteristics

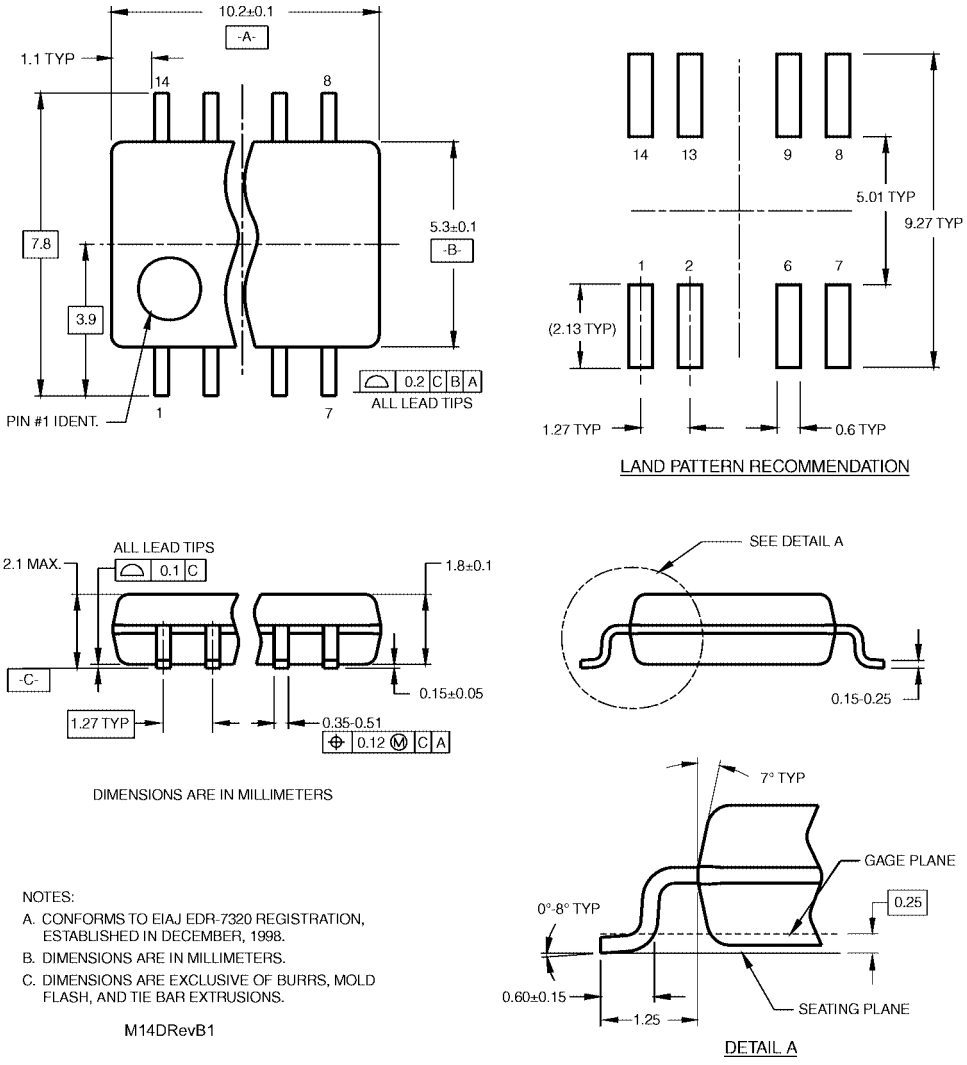
| Symbol | Parameter | $T_A$ = +25°C, $V_{CC}$ = +5.0V, $C_L$ = 50 pF | | | $T_A$ = −55°C to +125°C, $V_{CC}$ = +5.0V, $C_L$ = 50 pF | | $T_A$ = 0°C to +70°C, $V_{CC}$ = +5.0V, $C_L$ = 50 pF | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Max | Min | Max | |
| $t_{PLH}$ | Propagation Delay | 3.0 | 4.2 | 5.6 | 3.0 | 7.5 | 3.0 | 6.6 | ns |
| $t_{PHL}$ | $A_n$, $B_n$ to $O_n$ | 3.0 | 4.0 | 5.3 | 2.5 | 7.5 | 3.0 | 6.3 | |

## Physical Dimensions inches (millimeters) unless otherwise noted




**14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow**
**Package Number M14A**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.

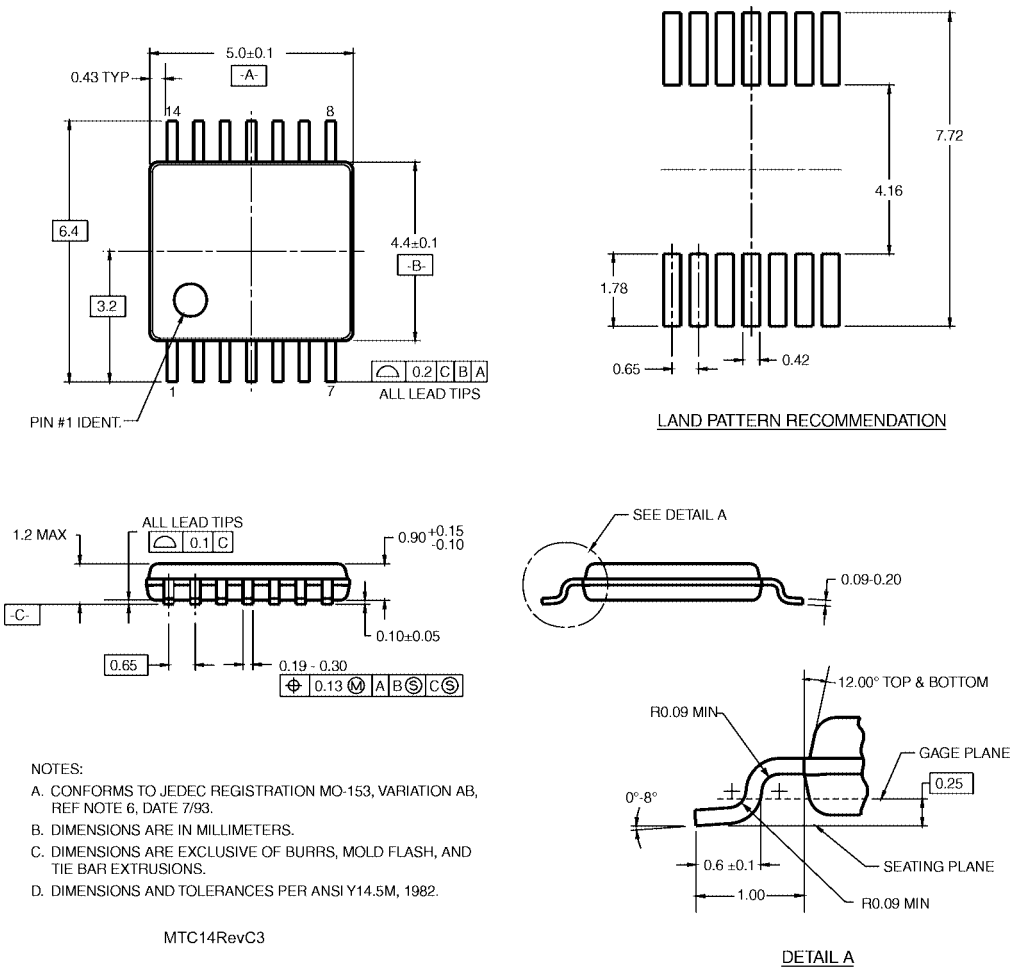
B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M14DRevB1

**14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide**
**Package Number M14D**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6, DATE 7/93.

B. DIMENSIONS ARE IN MILLIMETERS.

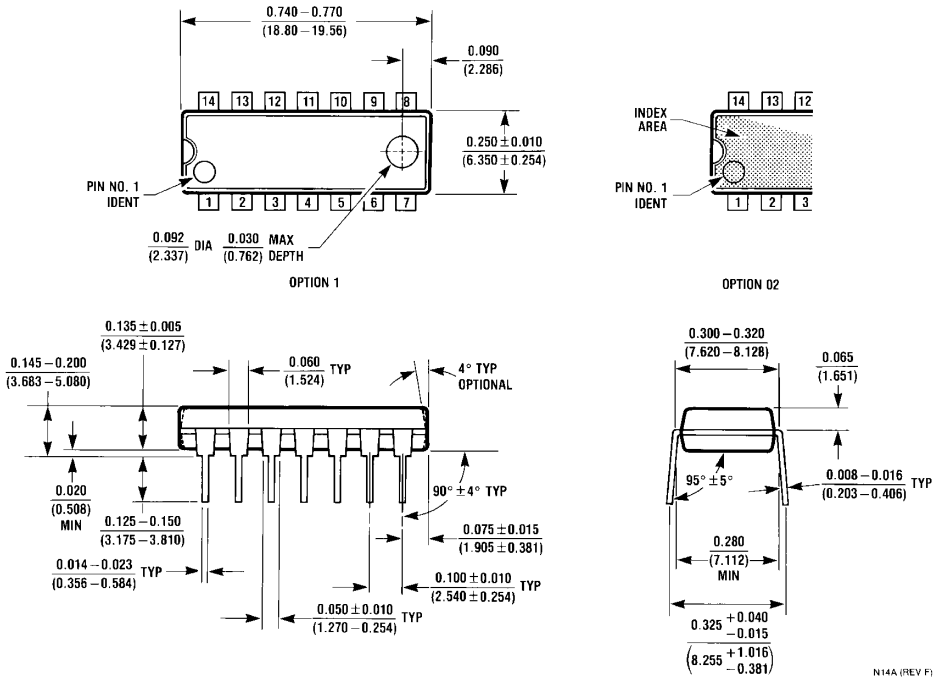
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC14RevC3

**14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide**
**Package Number MTC14**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




**14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide**
**Package Number N14A**

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