74HC4020-Q100; 74HCT4020-Q100

14-stage binary ripple counter

Rev. 1 — 23 May 2013 Product data sheet

1. General description

The 74HC4020-Q100; 74HCT4020-Q100 are 14-stage binary ripple counters with a clock input ($\overline{CP}$), an overriding asynchronous master reset input (MR) and 12 buffered parallel outputs (Q0, and Q3 to Q13). The counter advances on the HIGH-to-LOW transition of $\overline{CP}$. A HIGH on MR clears all counter stages and forces all outputs LOW, independent of the state of $\overline{CP}$. Each counter stage is a static toggle flip-flop.. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - Specified from –40 °C to +85 °C and from –40 °C to +125 °C
- Input levels:
  - For 74HC4020-Q100: CMOS level
  - For 74HCT4020-Q100: TTL level
- Complies with JEDEC standard no. 7A
- ESD protection:
  - MIL-STD-883, method 3015 exceeds 2000 V
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V (C = 200 pF, R = 0 Ω)
- Multiple package options

3. Applications

- Frequency dividing circuits
- Time delay circuits
- Control counters

nexperia

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC4020D-Q100	–40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HCT4020D-Q100				
74HC4020PW-Q100	–40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74HCT4020PW-Q100				
74HC4020BQ-Q100	–40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1
74HCT4020BQ-Q100				

5. Functional diagram

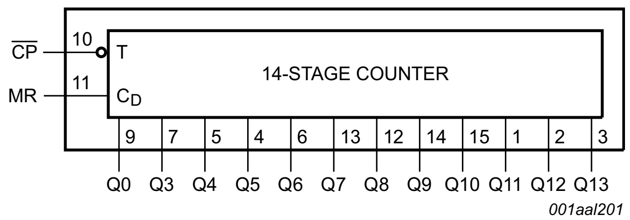


Fig 1. Functional diagram

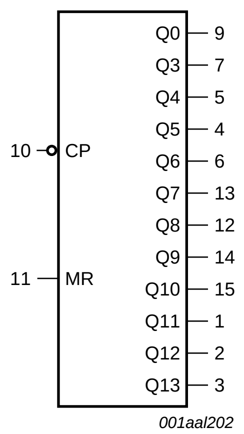


Fig 2. Logic symbol

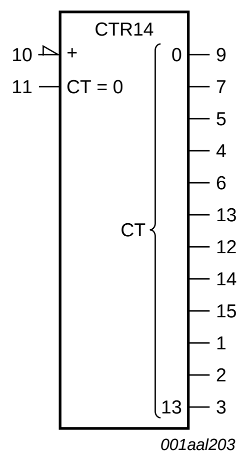


Fig 3. IEC logic symbol

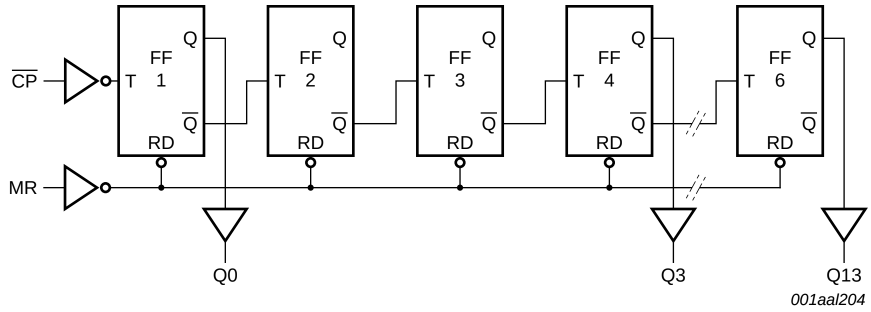


Fig 4. Logic diagram

6. Pinning information

6.1 Pinning

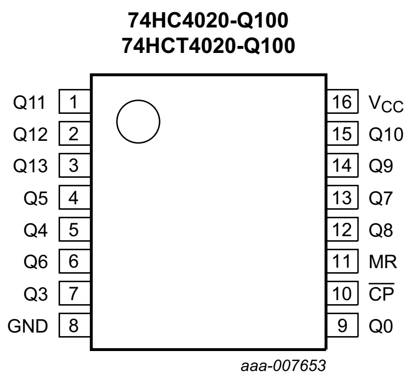
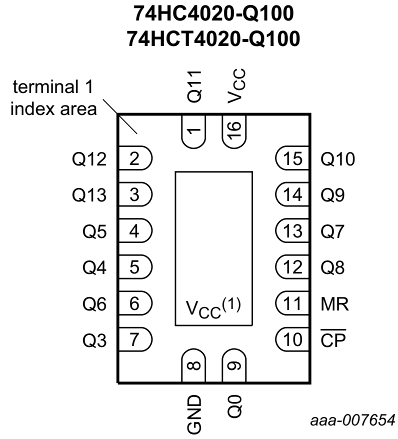


Fig 5. Pin configuration SO16 and TSSOP16



Transparent top view

(1) This is not a supply pin. The substrate is attached to this pad using conductive die attach material. There is no electrical or mechanical requirement to solder this pad. However, if it is soldered, the solder land should remain floating or be connected to V_{CC}.

Fig 6. Pin configuration DHVQFN16

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
Q0, Q3 to Q13	9, 7, 5, 4, 6, 13, 12, 14, 15, 1, 2, 3	output
GND	8	ground (0 V)
$\overline{CP}$	10	clock input (HIGH-to-LOW, edge-triggered)
MR	11	master reset input (active HIGH)
V_{CC}	16	positive supply voltage

7. Functional description

Table 3. Function table

Input		Output
$\overline{CP}$	MR	Q0, Q3 to Q13
↑	L	no change
↓	L	count
X	H	L

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; ↑ = LOW-to-HIGH clock transition; ↓ = HIGH-to-LOW clock transition.

7.1 Timing diagram

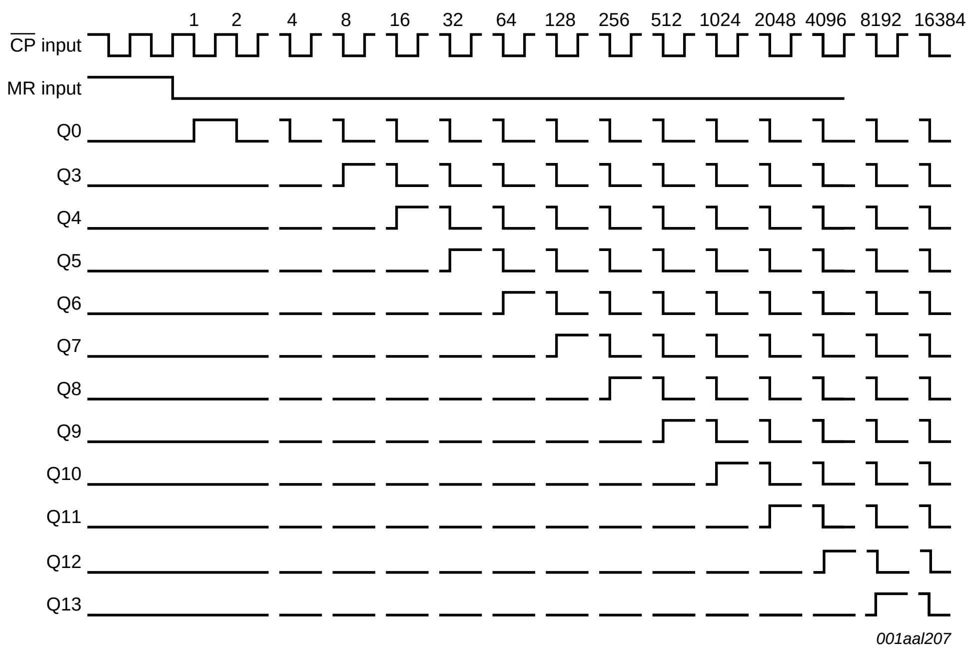


Fig 7. Timing diagram

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		–0.5	+7	V
I_{IK}	input clamping current	$V_I < –0.5$ V or $V_I > V_{CC} + 0.5$ V	-	±20	mA
I_{OK}	output clamping current	$V_I < –0.5$ V or $V_I > V_{CC} + 0.5$ V	-	±20	mA
I_O	output current	$–0.5$ V $< V_O < V_{CC} + 0.5$ V	-	±25	mA
I_{CC}	supply current		-	±50	mA
I_{GND}	ground current		-	±50	mA
T_{stg}	storage temperature		–65	+150	°C
P_{tot}	total power dissipation	T_{amb} = –40 °C to +125 °C [1]	-	500	mW

[1] For SO16 package: P_{tot} derates linearly with 8 mW/K above 70 °C.
For TSSOP16 package: P_{tot} derates linearly with 5.5 mW/K above 60 °C.
For DHVQFN16 package: P_{tot} derates linearly with 4.5 mW/K above 60 °C.

9. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	74HC4020-Q100			74HCT4020-Q100			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
$\Delta t/\Delta V$	input transition rise and fall rate	except for Schmitt trigger inputs							
		V_{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V_{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V_{CC} = 6.0 V	-	-	83	-	-	-	ns/V
T_{amb}	ambient temperature		–40	+25	+125	–40	+25	+125	°C

10. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC4020-Q100										
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V_{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V_{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V_{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V_{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}								
		I_O = −20 μA; V_{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I_O = −20 μA; V_{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = −20 μA; V_{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I_O = −4.0 mA; V_{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I_O = −5.2 mA; V_{CC} = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}								
		I_O = 20 μA; V_{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 20 μA; V_{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 20 μA; V_{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 4.0 mA; V_{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 6.0 V	-	-	±0.1	-	±1	-	±1	μA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	8.0	-	80	-	160	μA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF
74HCT4020-Q100										
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V								
		I_O = −20 μA	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = −4.0 mA	3.98	4.32	-	3.84	-	3.7	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V								
		I_O = 20 μA; V_{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 4.0 mA; V_{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 5.5 V	-	-	±0.1	-	±1	-	±1	μA

Table 6. Static characteristics *...continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
I_{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5$ V	-	-	8.0	-	80	-	160	μA
ΔI_{CC}	additional supply current	$V_I = V_{CC} - 2.1$ V; $I_O = 0$ A; other inputs at V_{CC} or GND; $V_{CC} = 4.5$ V to 5.5 V								
		pin MR	-	110	396	-	495	-	539	μA
		pin $\overline{CP}$	-	85	306	-	383	-	417	μA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF

11. Dynamic characteristics

Table 7. Dynamic characteristics

GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit, see Figure 10

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC4020-Q100										
t_{pd}	propagation delay	$\overline{CP}$ to Q0; see Figure 8 [1]								
		$V_{CC} = 2.0$ V; $C_L = 50$ pF	-	39	140	-	175	-	210	ns
		$V_{CC} = 4.5$ V; $C_L = 50$ pF	-	14	28	-	35	-	42	ns
		$V_{CC} = 5.0$ V; $C_L = 15$ pF	-	11	-	-	-	-	-	ns
		$V_{CC} = 6.0$ V; $C_L = 50$ pF	-	11	24	-	30	-	36	ns
		Qn to Qn+1; see Figure 9								
		$V_{CC} = 2.0$ V; $C_L = 50$ pF	-	22	75	-	95	-	110	ns
		$V_{CC} = 4.5$ V; $C_L = 50$ pF	-	8	15	-	19	-	22	ns
		$V_{CC} = 5.0$ V; $C_L = 15$ pF	-	6	-	-	-	-	-	ns
		$V_{CC} = 6.0$ V; $C_L = 50$ pF	-	6	13	-	16	-	19	ns
t_{PHL}	HIGH to LOW propagation delay	MR to Qn; see Figure 8								
		$V_{CC} = 2.0$ V; $C_L = 50$ pF	-	55	170	-	215	-	225	ns
		$V_{CC} = 4.5$ V; $C_L = 50$ pF	-	20	34	-	43	-	51	ns
		$V_{CC} = 5.0$ V; $C_L = 15$ pF	-	17	-	-	-	-	-	ns
		$V_{CC} = 6.0$ V; $C_L = 50$ pF	-	16	29	-	37	-	43	ns
t_t	transition time	Qn; see Figure 8 [2]								
		$V_{CC} = 2.0$ V; $C_L = 50$ pF	-	19	75	-	95	-	110	ns
		$V_{CC} = 4.5$ V; $C_L = 50$ pF	-	7	15	-	19	-	22	ns
		$V_{CC} = 6.0$ V; $C_L = 50$ pF	-	6	13	-	16	-	19	ns

Table 7. Dynamic characteristics *...continued*

GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit, see Figure 10

Symbol	Parameter	Conditions		25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
t_W	pulse width	$\overline{CP}$ HIGH or LOW; see Figure 8									
		V_{CC} = 2.0 V; C_L = 50 pF		80	14	-	100	-	120	-	ns
		V_{CC} = 4.5 V; C_L = 50 pF		16	4	-	20	-	24	-	ns
		V_{CC} = 6.0 V; C_L = 50 pF		14	3	-	17	-	20	-	ns
		MR HIGH; see Figure 8									
		V_{CC} = 2.0 V; C_L = 50 pF		80	17	-	100	-	120	-	ns
		V_{CC} = 4.5 V; C_L = 50 pF		16	6	-	20	-	24	-	ns
		V_{CC} = 6.0 V; C_L = 50 pF		14	5	-	17	-	20	-	ns
t_{rec}	recovery time	MR to $\overline{CP}$; see Figure 8									
		V_{CC} = 2.0 V; C_L = 50 pF		50	6	-	65	-	75	-	ns
		V_{CC} = 4.5 V; C_L = 50 pF		10	2	-	13	-	15	-	ns
		V_{CC} = 6.0 V; C_L = 50 pF		9	2	-	11	-	13	-	ns
f_{max}	maximum frequency	see Figure 8									
		V_{CC} = 2.0 V; C_L = 50 pF		6.0	30	-	4.8	-	4.0	-	MHz
		V_{CC} = 4.5 V; C_L = 50 pF		30	92	-	24	-	20	-	MHz
		V_{CC} = 5.0 V; C_L = 15 pF		-	101	-	-	-	-	-	MHz
		V_{CC} = 6.0 V; C_L = 50 pF		35	109	-	28	-	24	-	MHz
C_{PD}	power dissipation capacitance		[3]	-	19	-	-	-	-	-	pF
74HCT4020-Q100											
t_{pd}	propagation delay	$\overline{CP}$ to Q0; see Figure 8	[1]								
		V_{CC} = 4.5 V; C_L = 50 pF		-	18	36	-	45	-	54	ns
		V_{CC} = 5.0 V; C_L = 15 pF		-	15	-	-	-	-	-	ns
		Qn to Qn+1; see Figure 9									
		V_{CC} = 4.5 V; C_L = 50 pF		-	8	15	-	19	-	22	ns
		V_{CC} = 5.0 V; C_L = 15 pF		-	6	-	-	-	-	-	ns
t_{PHL}	HIGH to LOW propagation delay	MR to Qn; see Figure 8									
		V_{CC} = 4.5 V; C_L = 50 pF		-	22	45	-	56	-	68	ns
		V_{CC} = 5.0 V; C_L = 15 pF		-	19	-	-	-	-	-	ns
t_t	transition time	Qn; see Figure 8	[2]								
		V_{CC} = 4.5 V; C_L = 50 pF		-	7	15	-	19	-	22	ns
t_W	pulse width	$\overline{CP}$ HIGH or LOW; see Figure 8									
		V_{CC} = 4.5 V; C_L = 50 pF		20	7	-	25	-	30	-	ns
		MR HIGH; see Figure 8									
		V_{CC} = 4.5 V; C_L = 50 pF		20	8	-	25	-	30	-	ns
t_{rec}	recovery time	MR to $\overline{CP}$; see Figure 8									
		V_{CC} = 4.5 V; C_L = 50 pF		10	2	-	13	-	15	-	ns

Table 7. Dynamic characteristics *...continued*

GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit, see Figure 10

Symbol	Parameter	Conditions		25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
f_{max}	maximum frequency	see Figure 8									
		V_{CC} = 4.5 V; C_L = 50 pF		25	47	-	20	-	17	-	MHz
		V_{CC} = 5.0 V; C_L = 15 pF		-	52	-	-	-	-	-	MHz
C_{PD}	power dissipation capacitance		[3]	-	20	-	-	-	-	-	pF

[1] t_{pd} is the same as t_{PHL} and t_{PLH}.

[2] t_t is the same as t_{THL} and t_{TLH}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

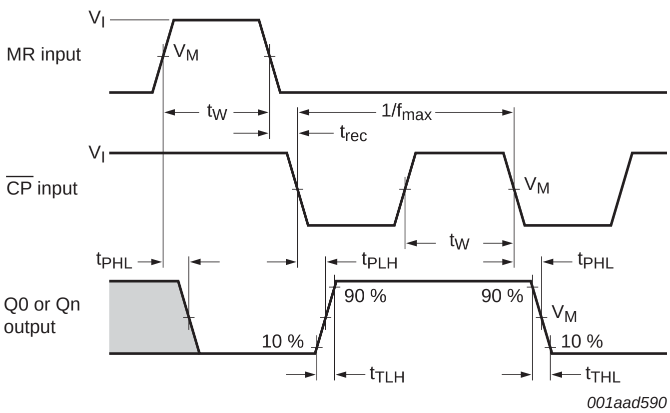
f_o = output frequency in MHz;

$\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V.

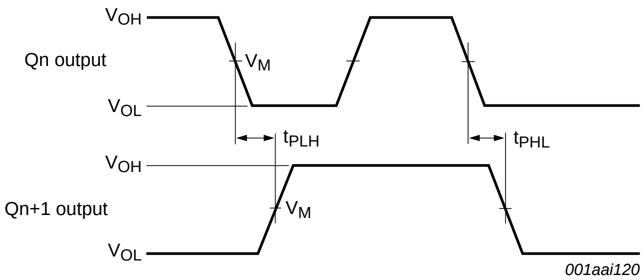
12. Waveforms



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 8. Clock timing, propagation delays, pulse widths and measurement points



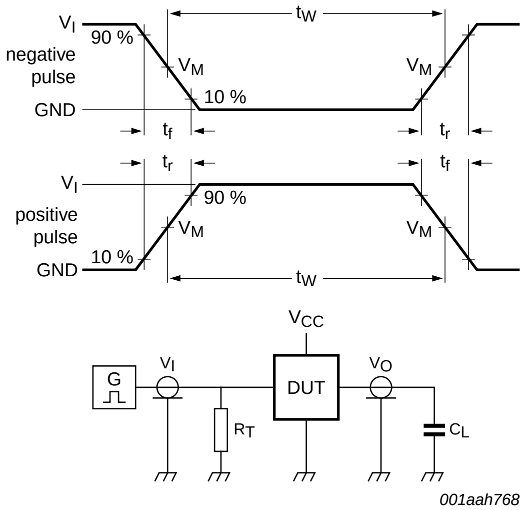
Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 9. Waveforms showing the output Qn to output Qn+1 propagation delays

Table 8. Measurement points

Type	Input	Output
	V_M	V_M
74HC4020-Q100	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
74HCT4020-Q100	1.3 V	1.3 V



Test data is given in Table 9.

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

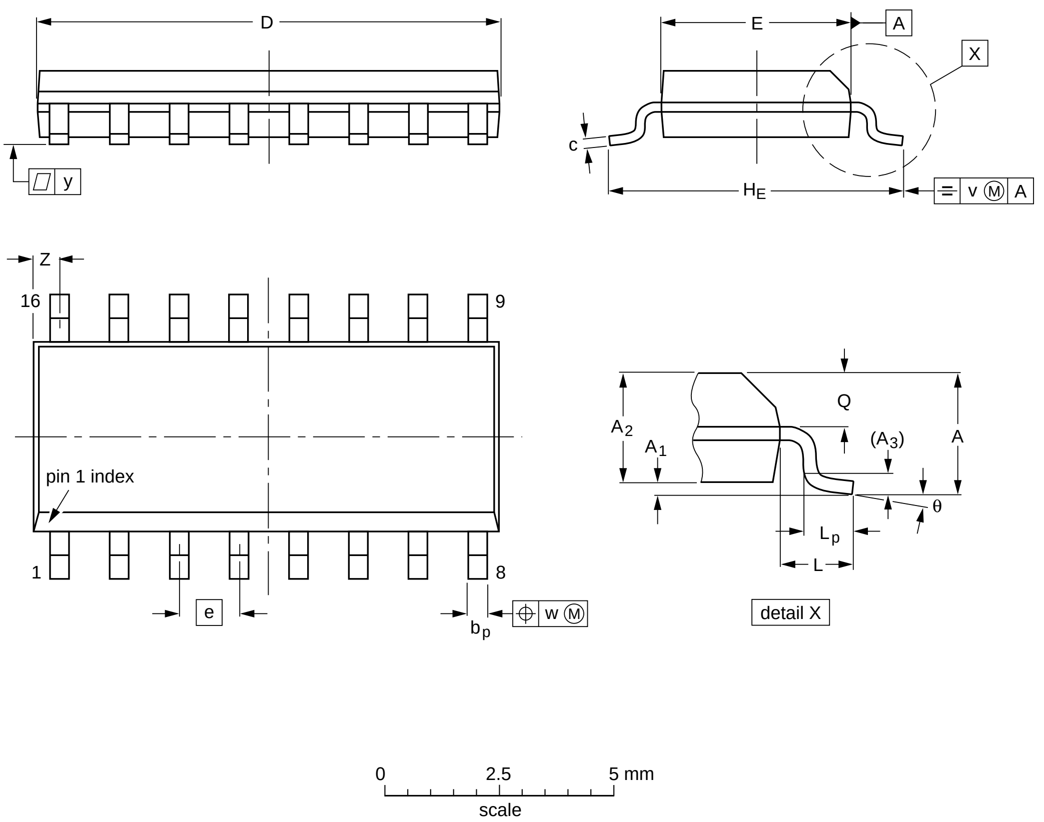
Fig 10. Test circuit for measuring switching times

Table 9. Test data

Type	Input		Load
	V_I	t_r, t_f	C_L
74HC4020-Q100	V_{CC}	6 ns	15 pF, 50 pF
74HCT4020-Q100	3 V	6 ns	15 pF, 50 pF

13. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

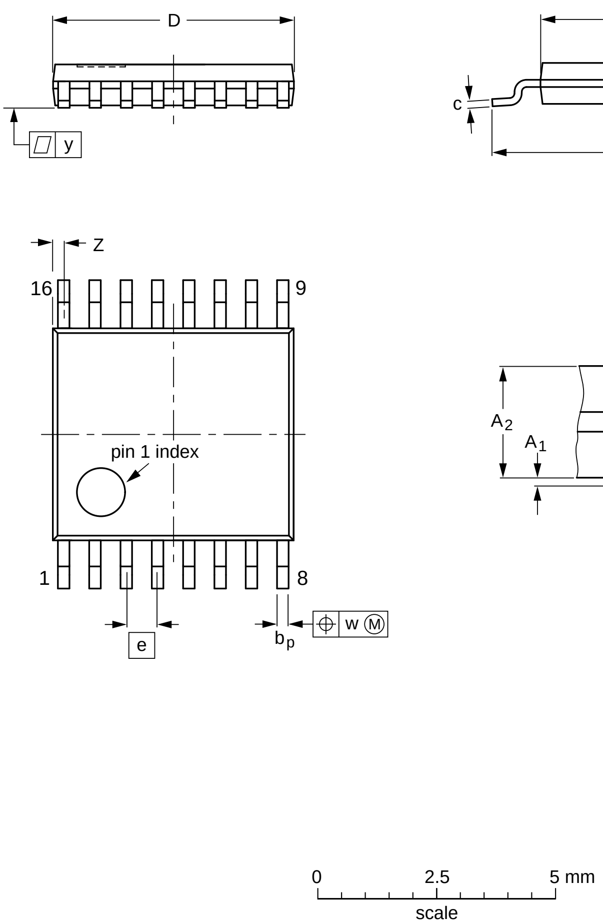
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

Fig 11. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

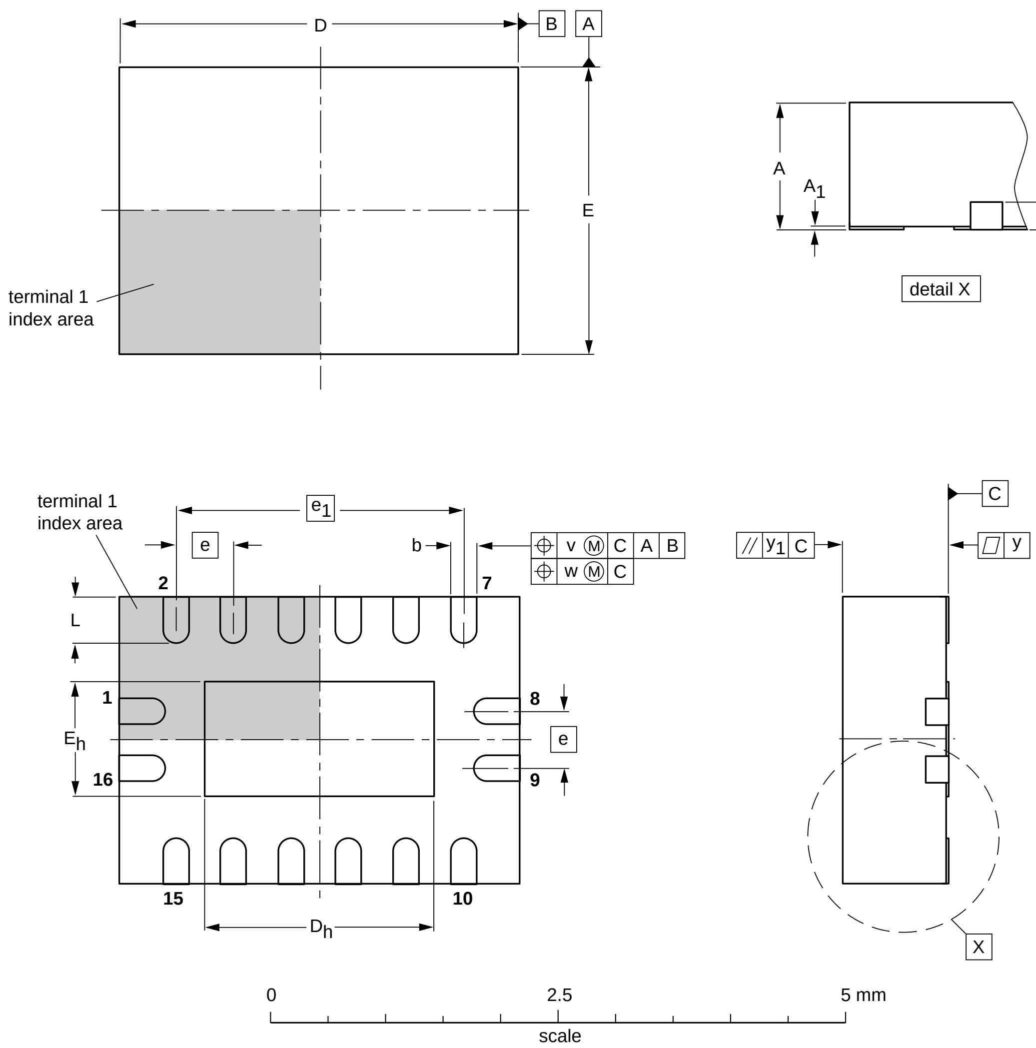
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

Fig 12. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm **SOT763-1**



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max.	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	3.6 3.4	2.15 1.85	2.6 2.4	1.15 0.85	0.5	2.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT763-1	- - -	MO-241	- - -			~~02-10-17~~ 03-01-27

Fig 13. Package outline SOT763-1 (DHVQFN16)

14. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MIL	Military
MM	Machine Model
TTL	Transistor-Transistor Logic

15. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT4020_Q100 v.1	20130523	Product data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nexperia.com.

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18. Contents

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