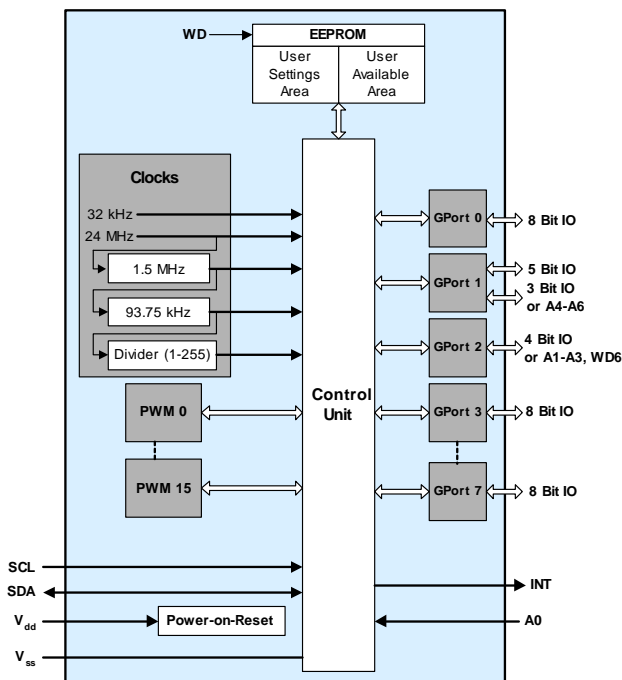


20-, 40-, and 60-Bit I/O Expander with EEPROM

Features

- I²C interface logic electrically compatible with SMBus
- Up to 20 (CY8C9520A), 40 (CY8C9540A), or 60 (CY8C9560A) I/O data pins independently configurable as inputs, outputs, Bi-directional input/outputs, or PWM outputs
- 4/8/16 PWM sources with 8-bit resolution
- Extendable soft addressing algorithm allowing flexible I²C address configuration
- Internal 3-/11-/27-Kbyte EEPROM
- User default storage, I/O port settings in internal EEPROM
- Optional EEPROM write disable (WD) input
- Interrupt output indicates input pin level changes and pulse width modulator (PWM) state changes
- Internal power on reset (POR)
- Internal configurable watchdog timer

Top Level Block Diagram



Overview

The CY8C95xxA is a multi-port I/O expander with on board user available EEPROM and several PWM outputs. All devices in this family operate identically but differ in I/O pins, number of PWMs, and internal EEPROM size.

The CY8C95xxA operates as two I²C slave devices. The first device is a multi port I/O expander (single I²C address to access all ports through registers). The second device is a serial EEPROM. Dedicated configuration registers can be used to disable the EEPROM. The EEPROM uses 2-byte addressing to support the 28 Kbyte EEPROM address space. The selected device is defined by the most significant bits of the I²C address or by specific register addressing.

The I/O expander's data pins can be independently assigned as inputs, outputs, quasi-bidirectional input/outputs or PWM outputs. The individual data pins can be configured as open drain or collector, strong drive (10 mA source, 25 mA sink), resistively pulled up or down, or high impedance. The factory default configuration is pulled up internally.

The system master writes to the I/O configuration registers through the I²C bus. Configuration and output register settings are storable as user defaults in a dedicated section of the EEPROM. If user defaults were stored in EEPROM, they are restored to the ports at power up. While this device can share the bus with SMBus devices, it can only communicate with I²C masters. The I²C slave in this device requires that the I²C master supports clock stretching.

There is one dedicated pin that is configured as an interrupt output (INT) and can be connected to the interrupt logic of the system master. This signal can inform the system master that there is incoming data on its ports or that the PWM output state was changed.

The EEPROM is byte readable and supports byte-by-byte writing. A pin can be configured as an EEPROM Write Disable (WD) input that blocks write operations when set high. The configuration registers can also disable EEPROM operations.

The CY8C95xxA has one fixed address pin (A0) and up to six additional pins (A1-A6), which allow up to 128 devices to share a common two wire I²C data bus. The Extendable Soft Addressing algorithm provides the option to choose the number of pins needed to assign the desired address. Pins not used for address bits are available as GPIO pins.

There are 4 (CY8C9520A), 8 (CY8C9540A), or 16 (CY8C9560A) independently configurable 8-bit PWMs. These PWMs are listed as PWM0-PWM15. Each PWM can be clocked by one of six available clock sources.

Errata: For information on silicon errata, see [Errata on page 30](#). Details include trigger conditions, devices affected, and proposed workaround.

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Architecture

The [Top Level Block Diagram on page 1](#) illustrates the device block diagram. The main blocks include the control unit, PWMs, EEPROM, and I/O ports. The control unit executes commands received from the I²C bus and transfers data between other bus devices and the master device.

The on chip EEPROM can be separated conventionally into two regions. The first region is designed to store data and is available for byte wide read/writes through the I²C bus. It is possible to prevent write operations by setting the WD pin to high. All EEPROM operations can be blocked by configuration register settings. The second region allows the user to store the port and PWM default settings using special commands. These defaults are automatically reloaded and processed after device power on.

The number of I/O lines and PWM sources are listed in the following table.

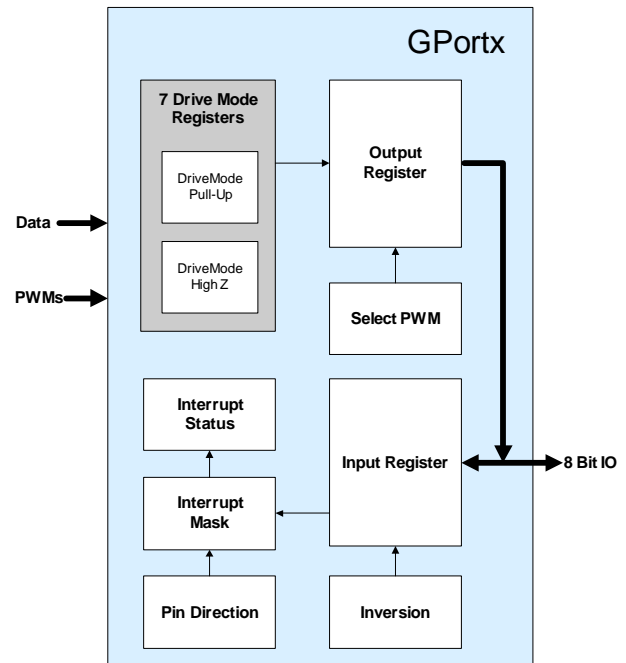
Table 1. GPIO Availability

| Port | CY8C9520A | CY8C9540A | CY8C9560A |
|---------|------------------------|-----------------------|------------------------|
| GPort 0 | 8 bit | 8 bit | 8 bit |
| GPort 1 | 5-8 bit ^[1] | 5-8bit ^[1] | 5-8 bit ^[1] |
| GPort 2 | 0-4 bit ^[1] | 0-4it ^[1] | 0-4 bit ^[1] |
| GPort 3 | – | 8 bit | 8 bit |
| GPort 4 | – | 8 bit | 8 bit |
| GPort 5 | – | 4 bit | 8 bit |
| GPort 6 | – | – | 8 bit |
| GPort 7 | – | – | 8 bit |
| PWMs | 4 | 8 | 16 |

There are four pins on GPort 2 and three on GPort 1 that can be used as general purpose I/O or EEPROM Write Disable (WD) and I²C-address input (A1-A6), depending on configuration settings.

[Figure 1](#) shows the single port logical structure. The Port Drive Mode register gives the option to select one of seven available modes for each pin separately: pulled up/down, open drain high/low, strong drive fast/slow, or high impedance. By default these configuration registers store values setting I/O pins to be pulled up. The Invert register enables inversion of the logic of the Input registers separately for each pin. The Select PWM register assigns pins as PWM outputs. All of these configuration registers are read/writable using corresponding commands in the multi-port device.

Figure 1. Logical Structure of the I/O Port



The Port Input and Output registers are separated. When the Output register is written, the data is sent to the external pins. When the Input register is read, the external pin logic levels are captured and transferred. As a result, the read data can be different from written Output register data. This enables implementation of a quasi-bidirectional input-output mode, when the corresponding binary digit is configured as pulled up/down output.

Each port has an Interrupt Mask register and an Interrupt Status register. Each high bit in the Interrupt Status register signals that there has been a change in the corresponding input line since the last read of that Interrupt Status register. The Interrupt Status register is cleared after each read. The Interrupt Mask register enables/disables activation of the INT line when input levels are changed. Each high in the Interrupt Mask register masks (disables) an interrupt generated from the corresponding input line.

Applications

Each GPIO pin can be used to monitor and control various board level devices, including LEDs and system intrusion detection devices.

The on board EEPROM can be used to store information such as error codes or board manufacturing data for read-back by application software for diagnostic purposes.

Note

1. This port contains configuration-dependant GPIO lines or A1-A6 and WD lines.

Device Access Addressing

Following a start condition, the I²C master device sends a byte to address an I²C slave. This address accesses the device in the CY8C95xx. By default there are two possible address formats in binary representation: 010000A0X and 101000A0X. The first is used to access the multi port device and the second to access the EEPROM. If additional address lines (A1-A6) are used then the Device Addressing. [Table 2](#) defines the device addresses. This addressing method uses a technique called Extendable Soft Addressing, described in the section [Extendable Soft Addressing on page 9](#).

Table 2. Device Addressing

| Multi-Port Device | | | | | | | | EEPROM Device | | | | | | | | |
|-------------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|-----|
| 01 | | 0 | 0 | 0 | 0 | A ₀ | R/W | 1 | 0 | 1 | 0 | 0 | 0 | A ₀ | R/W | |
| 0 | 1 | 0 | 0 | 0 | 0 | A ₁ | A ₀ | R/W | 1 | 0 | 1 | 0 | 0 | A ₁ | A ₀ | R/W |
| 0 | 1 | 0 | 0 | 0 | A ₂ | A ₁ | A ₀ | R/W | 1 | 0 | 1 | 0 | A ₂ | A ₁ | A ₀ | R/W |
| 0 | 1 | 0 | A ₃ | A ₂ | A ₁ | A ₀ | R/W | 1 | 0 | 1 | A ₃ | A ₂ | A ₁ | A ₀ | R/W | |
| 0 | 1 | A ₄ | A ₃ | A ₂ | A ₁ | A ₀ | R/W | 1 | 0 | A ₄ | A ₃ | A ₂ | A ₁ | A ₀ | R/W | |
| 0 | A ₅ | A ₄ | A ₃ | A ₂ | A ₁ | A ₀ | R/W | 1 | A ₅ | A ₄ | A ₃ | A ₂ | A ₁ | A ₀ | R/W | |
| A ₆ | A ₅ | A ₄ | A ₃ | A ₂ | A ₁ | A ₀ | R/W | A ₆ | A ₅ | A ₄ | A ₃ | A ₂ | A ₁ | A ₀ | R/W | |

When all address lines A1-A6 are used, the device being accessed is defined by the first byte following the address in the write transaction. If the most significant bit (MSb) of this byte is '0', this byte is treated as a command (register address) byte of the multi-port device. If the MSb is '1', this byte is the first of a 2-byte EEPROM address. In this case, the device masks the MSb to determine the EEPROM address.

Serial EEPROM Device

EEPROM reading and writing operations require 2 bytes, AHI and ALO, which indicate the memory address to use.

To read one or more bytes, the master device addresses the unit with a write cycle (= 0) to send AHI followed by ALO, readdresses the unit with a read cycle (= 1), and reads one or more data bytes. Each data byte read increments the internal address counter by one up to the end of the EEPROM address space. A read or write beyond the end of the EEPROM address space must result in a NAK response by the Port Expander.

To write data to the EEPROM, the master device performs one write cycle, with the first two bytes being AHI followed by ALO. This is followed by one or more data bytes. In the case of block writing it is advisable to set the starting address on the beginning of the 64-byte boundary, for example 01C0h or 0080h, but this is not mandatory. When a 64-byte boundary is crossed in the EEPROM, the I²C clock is stretched while the device performs an EEPROM write sequence. If the end of available EEPROM space is reached, then further writes are responded to with a NAK.

Refer to [Figure 6 on page 10](#), which illustrates memory reading and writing procedures for the EEPROM device.

Multi Port I/O Device

This device allows the user to set configurations and I/O operations through internal registers.

Each data transfer is preceded by the command byte. This byte is used as a pointer to a register that receives or transmits data. Available registers are listed in [Table 6 on page 11](#).

Pinouts

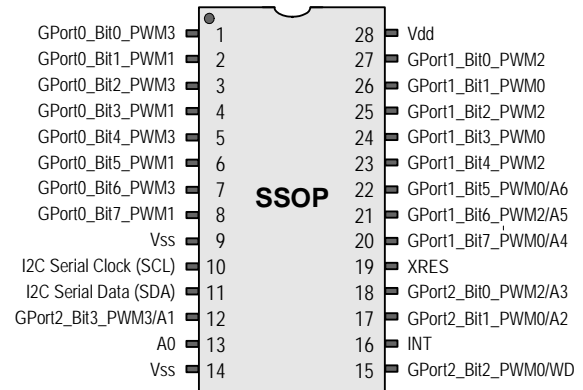
The CY8C95xxA device is available in a variety of packages, which are listed and illustrated in the following tables.

28-Pin Part Pinout

Table 3. 28-Pin Part Pinout (SSOP)

| Pin No. | Pin Name | Description |
|---------|-------------------------------------|---|
| 1 | GPort0_Bit0_PWM3 | Port 0, Bit 0, PWM 3. |
| 2 | GPort0_Bit1_PWM1 | Port 0, Bit 1, PWM 1. |
| 3 | GPort0_Bit2_PWM3 | Port 0, Bit 2, PWM 3. |
| 4 | GPort0_Bit3_PWM1 | Port 0, Bit 3, PWM 1. |
| 5 | GPort0_Bit4_PWM3 | Port 0, Bit 4, PWM 3. |
| 6 | GPort0_Bit5_PWM1 | Port 0, Bit 5, PWM 1. |
| 7 | GPort0_Bit6_PWM3 | Port 0, Bit 6, PWM 3. |
| 8 | GPort0_Bit7_PWM1 | Port 0, Bit 7, PWM 1. |
| 9 | V _{SS} | Ground connection. |
| 10 | I ² C Serial Clock (SCL) | I ² C Clock. |
| 11 | I ² C Serial Data (SDA) | I ² C Data. |
| 12 | GPort2_Bit3_PWM3/A1 | Port 2, Bit 3, PWM 3, Address 1. |
| 13 | A0 | Address 0. |
| 14 | V _{SS} | Ground connection. |
| 15 | GPort2_Bit2_PWM0/WD | Port 2, Bit 2, PWM 0, E ² Write Disable. |
| 16 | INT | |
| 17 | GPort2_Bit1_PWM0/A2 | Port 2, Bit 1, PWM 0, Address 2. |
| 18 | GPort2_Bit0_PWM2/A3 | Port 2, Bit 0, PWM 2, Address 3. |
| 19 | XRES | Active high external reset with internal pull down. |
| 20 | GPort1_Bit7_PWM0/A4 | Port 1, Bit 7, PWM 0, Address 4. |
| 21 | GPort1_Bit6_PWM2/A5 | Port 1, Bit 6, PWM 2, Address 5. |
| 22 | GPort1_Bit5_PWM0/A6 | Port 1, Bit 5, PWM 0, Address 6. |
| 23 | GPort1_Bit4_PWM2 | Port 1, Bit 4, PWM 2. |
| 24 | GPort1_Bit3_PWM0 | Port 1, Bit 3, PWM 0. |
| 25 | GPort1_Bit2_PWM2 | Port 1, Bit 2, PWM 2. |
| 26 | GPort1_Bit1_PWM0 | Port 1, Bit 1, PWM 0. |
| 27 | GPort1_Bit0_PWM2 | Port 1, Bit 0, PWM 2. |
| 28 | V _{DD} | Supply voltage. |

Figure 2. CY8C9520A 28-Pin Device

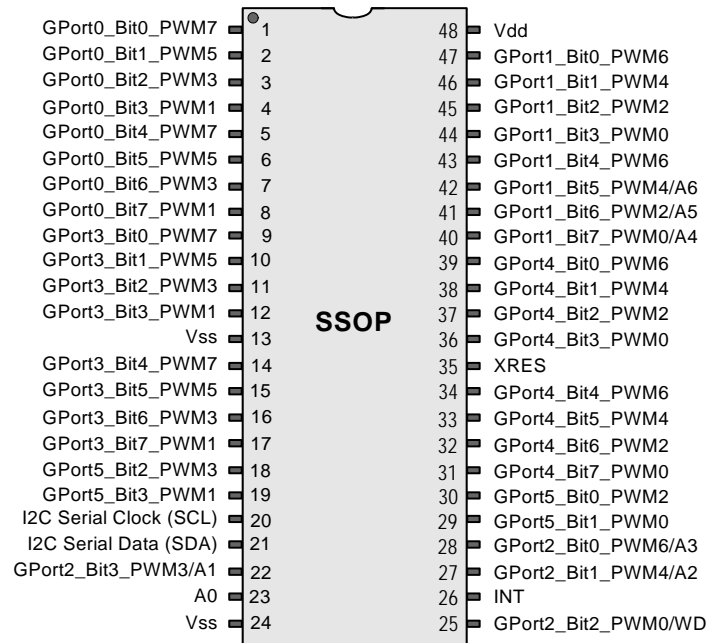


48-Pin Part Pinout

Table 4. 48-Pin Part Pinout (SSOP)

| Pin No. | Pin Name | Description |
|---------|-------------------------------------|---|
| 1 | GPort0_Bit0_PWM7 | Port 0, Bit 0, PWM 7. |
| 2 | GPort0_Bit1_PWM5 | Port 0, Bit 1, PWM 5. |
| 3 | GPort0_Bit2_PWM3 | Port 0, Bit 2, PWM 3. |
| 4 | GPort0_Bit3_PWM1 | Port 0, Bit 3, PWM 1. |
| 5 | GPort0_Bit4_PWM7 | Port 0, Bit 4, PWM 7. |
| 6 | GPort0_Bit5_PWM5 | Port 0, Bit 5, PWM 5. |
| 7 | GPort0_Bit6_PWM3 | Port 0, Bit 6, PWM 3. |
| 8 | GPort0_Bit7_PWM1 | Port 0, Bit 7, PWM 1. |
| 9 | GPort3_Bit0_PWM7 | Port 3, Bit 0, PWM 7. |
| 10 | GPort3_Bit1_PWM5 | Port 3, Bit 1, PWM 5. |
| 11 | GPort3_Bit2_PWM3 | Port 3, Bit 2, PWM 3. |
| 12 | GPort3_Bit3_PWM1 | Port 3, Bit 3, PWM 1. |
| 13 | V _{SS} | Ground connection. |
| 14 | GPort3_Bit4_PWM7 | Port 3, Bit 4, PWM 7. |
| 15 | GPort3_Bit5_PWM5 | Port 3, Bit 5, PWM 5. |
| 16 | GPort3_Bit6_PWM3 | Port 3, Bit 6, PWM 3. |
| 17 | GPort3_Bit7_PWM1 | Port 3, Bit 7, PWM 1. |
| 18 | GPort5_Bit2_PWM3 | Port 5, Bit 2, PWM 3. |
| 19 | GPort5_Bit3_PWM1 | Port 5, Bit 3, PWM 1. |
| 20 | I ² C Serial Clock (SCL) | I ² C Clock. |
| 21 | I ² C Serial Data (SDA) | I ² C Data. |
| 22 | GPort2_Bit3_PWM3/A1 | Port 2, Bit 3, PWM 3, Address 1. |
| 23 | A0 | Address 0. |
| 24 | V _{SS} | Ground connection. |
| 25 | GPort2_Bit2_PWM0/WD | Port 2, Bit 2, PWM 0, E ² Write Disable. |
| 26 | INT | |
| 27 | GPort2_Bit1_PWM4/A2 | Port 2, Bit 1, PWM 4, Address 2. |
| 28 | GPort2_Bit0_PWM6/A3 | Port 2, Bit 0, PWM 6, Address 3. |
| 29 | GPort5_Bit1_PWM0 | Port 5, Bit 1, PWM 0. |
| 30 | GPort5_Bit0_PWM2 | Port 5, Bit 0, PWM 2. |
| 31 | GPort4_Bit7_PWM0 | Port 4, Bit 7, PWM 0. |
| 32 | GPort4_Bit6_PWM2 | Port 4, Bit 6, PWM 2. |
| 33 | GPort4_Bit5_PWM4 | Port 4, Bit 5, PWM 4. |
| 34 | GPort4_Bit4_PWM6 | Port 4, Bit 4, PWM 6. |
| 35 | XRES | Active high external reset with internal pull down. |
| 36 | GPort4_Bit3_PWM0 | Port 4, Bit 3, PWM 0. |
| 37 | GPort4_Bit2_PWM2 | Port 4, Bit 2, PWM 2. |
| 38 | GPort4_Bit1_PWM4 | Port 4, Bit 1, PWM 4. |
| 39 | GPort4_Bit0_PWM6 | Port 4, Bit 0, PWM 6. |
| 40 | GPort1_Bit7_PWM0/A4 | Port 1, Bit 7, PWM 0, Address 4. |
| 41 | GPort1_Bit6_PWM2/A5 | Port 1, Bit 6, PWM 2, Address 5. |
| 42 | GPort1_Bit5_PWM4/A6 | Port 1, Bit 5, PWM 4, Address 6. |
| 43 | GPort1_Bit4_PWM6 | Port 1, Bit 4, PWM 6. |
| 44 | GPort1_Bit3_PWM0 | Port 1, Bit 3, PWM 0. |
| 45 | GPort1_Bit2_PWM2 | Port 1, Bit 2, PWM 2. |
| 46 | GPort1_Bit1_PWM4 | Port 1, Bit 1, PWM 4. |
| 47 | GPort1_Bit0_PWM6 | Port 1, Bit 0, PWM 6. |
| 48 | V _{DD} | Supply voltage. |

Figure 3. CY8C9540A 48-Pin Device

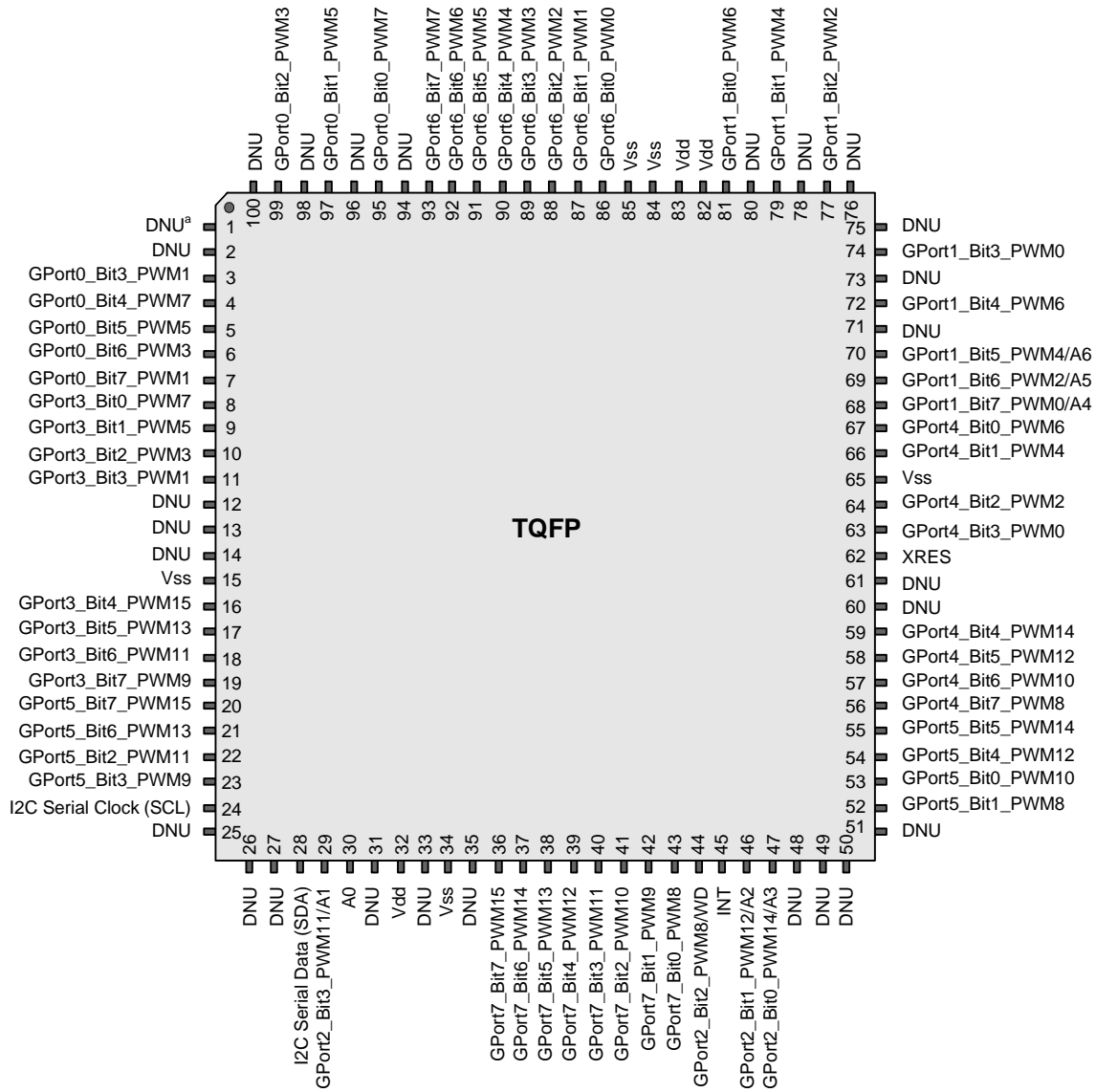


100-Pin Part Pinout

Table 5. 100-Pin Part Pinout (TQFP)

| Pin No. | Name | Description | Pin No. | Name | Description |
|---------|-------------------------------------|---|---------|---------------------|---|
| 1 | DNU | DNU = Do Not Use; leave floating. | 51 | DNU | DNU = Do Not Use; leave floating. |
| 2 | DNU | DNU = Do Not Use; leave floating. | 52 | GPort5_Bit1_PWM8 | Port 5, Bit 1, PWM 8. |
| 3 | GPort0_Bit3_PWM1 | Port 0, Bit 3, PWM 1. | 53 | GPort5_Bit0_PWM10 | Port 5, Bit 0, PWM 10. |
| 4 | GPort0_Bit4_PWM7 | Port 0, Bit 4, PWM 7. | 54 | GPort5_Bit4_PWM12 | Port 5, Bit 4, PWM 12. |
| 5 | GPort0_Bit5_PWM5 | Port 0, Bit 5, PWM 5. | 55 | GPort5_Bit5_PWM14 | Port 5, Bit 5, PWM 14. |
| 6 | GPort0_Bit6_PWM3 | Port 0, Bit 6, PWM 3. | 56 | GPort4_Bit7_PWM8 | Port 4, Bit 7, PWM 8. |
| 7 | GPort0_Bit7_PWM1 | Port 0, Bit 7, PWM 1. | 57 | GPort4_Bit6_PWM10 | Port 4, Bit 6, PWM 10. |
| 8 | GPort3_Bit0_PWM7 | Port 3, Bit 0, PWM 7. | 58 | GPort4_Bit5_PWM12 | Port 4, Bit 5, PWM 12. |
| 9 | GPort3_Bit1_PWM5 | Port 3, Bit 1, PWM 5. | 59 | GPort4_Bit4_PWM14 | Port 4, Bit 4, PWM 14. |
| 10 | GPort3_Bit2_PWM3 | Port 3, Bit 2, PWM 3. | 60 | DNU | DNU = Do Not Use; leave floating. |
| 11 | GPort3_Bit3_PWM1 | Port 3, Bit 3, PWM 1. | 61 | DNU | DNU = Do Not Use; leave floating. |
| 12 | DNU | DNU = Do Not Use; leave floating. | 62 | XRES | Active high external reset with internal pull down. |
| 13 | DNU | DNU = Do Not Use; leave floating. | 63 | GPort4_Bit3_PWM0 | Port 4, Bit 3, PWM 0. |
| 14 | DNU | DNU = Do Not Use; leave floating. | 64 | GPort4_Bit2_PWM2 | Port 4, Bit 2, PWM 2. |
| 15 | V _{SS} | Ground connection. | 65 | V _{SS} | Ground connection. |
| 16 | GPort3_Bit4_PWM15 | Port 3, Bit 4, PWM 15. | 66 | GPort4_Bit1_PWM4 | Port 4, Bit 1, PWM 4. |
| 17 | GPort3_Bit5_PWM13 | Port 3, Bit 5, PWM 13. | 67 | GPort4_Bit0_PWM6 | Port 4, Bit 0, PWM 6. |
| 18 | GPort3_Bit6_PWM11 | Port 3, Bit 6, PWM 11. | 68 | GPort1_Bit7_PWM0/A4 | Port 1, Bit 7, PWM 0, Address 4. |
| 19 | GPort3_Bit7_PWM9 | Port 3, Bit 7, PWM 9. | 69 | GPort1_Bit6_PWM2/A5 | Port 1, Bit 6, PWM 2, Address 5. |
| 20 | GPort5_Bit7_PWM15 | Port 5, Bit 7, PWM 15. | 70 | GPort1_Bit5_PWM4/A6 | Port 1, Bit 5, PWM 4, Address 6. |
| 21 | GPort5_Bit6_PWM13 | Port 5, Bit 6, PWM 13. | 71 | DNU | DNU = Do Not Use; leave floating. |
| 22 | GPort5_Bit2_PWM11 | Port 5, Bit 2, PWM 11. | 72 | GPort1_Bit4_PWM6 | Port 1, Bit 4, PWM 6. |
| 23 | GPort5_Bit3_PWM9 | Port 5, Bit 3, PWM 9. | 73 | DNU | DNU = Do Not Use; leave floating. |
| 24 | I ² C Serial Clock (SCL) | I ² C Clock. | 74 | GPort1_Bit3_PWM0 | Port 1, Bit 3, PWM 0. |
| 25 | DNU | DNU = Do Not Use; leave floating. | 75 | DNU | DNU = Do Not Use; leave floating. |
| 26 | DNU | DNU = Do Not Use; leave floating. | 76 | DNU | DNU = Do Not Use; leave floating. |
| 27 | DNU | DNU = Do Not Use; leave floating. | 77 | GPort1_Bit2_PWM2 | Port 1, Bit 2, PWM 2. |
| 28 | I ² C Serial Data (SDA) | I ² C Data. | 78 | DNU | DNU = Do Not Use; leave floating. |
| 29 | GPort2_Bit3_PWM11/A1 | Port 2, Bit 3, PWM 11, Address 1. | 79 | GPort1_Bit1_PWM4 | Port 1, Bit 1, PWM 4. |
| 30 | A0 | Address 0. | 80 | DNU | DNU = Do Not Use; leave floating. |
| 31 | DNU | DNU = Do Not Use; leave floating. | 81 | GPort1_Bit0_PWM6 | Port 1, Bit 0, PWM 6. |
| 32 | V _{dd} | Supply voltage. | 82 | V _{dd} | Supply voltage. |
| 33 | DNU | DNU = Do Not Use; leave floating. | 83 | V _{dd} | Supply voltage. |
| 34 | V _{SS} | Ground connection. | 84 | V _{SS} | Ground connection. |
| 35 | DNU | DNU = Do Not Use; leave floating. | 85 | V _{SS} | Ground connection. |
| 36 | GPort7_Bit7_PWM15 | Port 7, Bit 7, PWM 15. | 86 | GPort6_Bit0_PWM0 | Port 6, Bit 0, PWM 0. |
| 37 | GPort7_Bit6_PWM14 | Port 7, Bit 6, PWM 14. | 87 | GPort6_Bit1_PWM1 | Port 6, Bit 1, PWM 1. |
| 38 | GPort7_Bit5_PWM13 | Port 7, Bit 5, PWM 13. | 88 | GPort6_Bit2_PWM2 | Port 6, Bit 2, PWM 2. |
| 39 | GPort7_Bit4_PWM12 | Port 7, Bit 4, PWM 12. | 89 | GPort6_Bit3_PWM3 | Port 6, Bit 3, PWM 3. |
| 40 | GPort7_Bit3_PWM11 | Port 7, Bit 3, PWM 11. | 90 | GPort6_Bit4_PWM4 | Port 6, Bit 4, PWM 4. |
| 41 | GPort7_Bit2_PWM10 | Port 7, Bit 2, PWM 10. | 91 | GPort6_Bit5_PWM5 | Port 6, Bit 5, PWM 5. |
| 42 | GPort7_Bit1_PWM9 | Port 7, Bit 1, PWM 9. | 92 | GPort6_Bit6_PWM6 | Port 6, Bit 6, PWM 6. |
| 43 | GPort7_Bit0_PWM8 | Port 7, Bit 0, PWM 8. | 93 | GPort6_Bit7_PWM7 | Port 6, Bit 7, PWM 7. |
| 44 | GPort2_Bit2_PWM8/WD | Port 2, Bit 2, PWM 8, E ² Write Disable. | 94 | DNU | DNU = Do Not Use; leave floating. |
| 45 | INT | | 95 | GPort0_Bit0_PWM7 | Port 0, Bit 0, PWM 7. |
| 46 | GPort2_Bit1_PWM12/A2 | Port 2, Bit 7, PWM 0, Address 4. | 96 | DNU | DNU = Do Not Use; leave floating. |
| 47 | GPort2_Bit0_PWM14/A3 | Port 2, Bit 6, PWM 2, Address 5. | 97 | GPort0_Bit1_PWM5 | Port 0, Bit 1, PWM 5. |
| 48 | DNU | DNU = Do Not Use; leave floating. | 98 | DNU | DNU = Do Not Use; leave floating. |
| 49 | DNU | DNU = Do Not Use; leave floating. | 99 | GPort0_Bit2_PWM3 | Port 0, Bit 2, PWM 3. |
| 50 | DNU | DNU = Do Not Use; leave floating. | 100 | DNU | DNU = Do Not Use; leave floating. |

Figure 4. CY8C9560A 100-Pin Device^[2]



Note
 2. DNU = Do Not Use; leave floating.

Pin Descriptions

Extendable Soft Addressing

The A0 line defines the corresponding bit of the I²C address. This pin must be pulled up or down. If A0 is a strong pull up or a strong pull down (wired through 330 or less resistor to V_{dd} or V_{ss}), then that is the only address line being specified and the A1-A6 lines are used as GPIO. If A0 is a weak pull up or a weak pull down (connected to V_{dd} or V_{ss} through 75K- 200K ohm resistor), then A0 is not the only externally defined address bit. There is a pin assigned to be A1 if it is needed. This pin can be pulled up or pulled down strong or weak with a resistor. As with A0, the type of pull determines whether the address bit is the last externally defined address bit. Differently from A0, A1 is not dedicated as an address pin. It is only used if A0 is not the only address bit externally defined. There are also predefined pins for A2, A3, A4, A5, and A6 that is only used for addressing if needed. The last address bit in the chain is pulled strong. That way, only the number of pins needed to assign the address desired for the part are allocated as address pins, any pins not used for address bits can be used as GPIO pins. The [Table 2 on page 4](#) defines the resulting device I²C address.

Note: It is not recommended to share pull up/down resistors between multiple devices.

Interrupt Pin (INT)

The interrupt output (if enabled) is activated if one of these events occurs:

- One of the GPIO port pins changes state and the corresponding bit in the Interrupt Mask register is set low.
- When a PWM driven by the slowest clock source (367.6 Hz) and assigned to a pin changes state and the pin's corresponding bit in the Interrupt Mask register is set low.

The interrupt line is deactivated when the master device performs a read from the corresponding Interrupt Status register. The INT output is active high output and the drive mode of this pin is strong drive mode.

Write Disable Pin (WD)

If this feature is enabled, '0' allows writes to the EEPROM and '1' blocks any memory writes. This pin is checked immediately before performing any write to memory. If the EEE bit in the Enable register is not set (EEPROM disabled) or bit EERO is set (EEPROM is read-only) then WD line level is ignored.

Note that '1' on this line blocks all commands that perform operations with EEPROM (see [Table 14 on page 14](#)).

This line may be enabled/disabled by bit 1 of the Enable register (2Dh): '1' enables WD function, '0' disables.

External Reset Pin (XRES)

A full device reset is caused by pulling the XRES pin high. The XRES pin has an always-on pull down resistor, so it does not require an external pull down for operation. It can be tied directly to ground or left open. Behavior after XRES is similar to

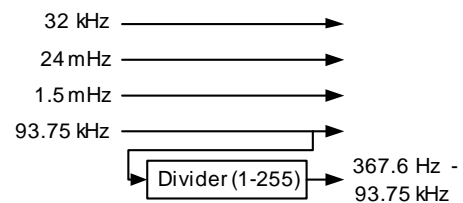
POR. When the part is held in reset, all In and Out pins are held at their default High-Z State.

Working with PWMs

There are four independent PWMs in the CY8C9520A, eight in the CY8C9540A and sixteen in the CY8C9560A. Each I/O pin can be configured as a PWM output by writing '1' to the corresponding bit of the Select PWM register (see [Table 7 on page 12](#)).

The next step of PWM configuration is clock source selection using the Config PWM registers. There are six available clock sources: 32 kHz (default), 24 MHz, 1.5 MHz, 93.75 kHz, 367.6 Hz or previous PWM output. (see [Figure 5](#))

Figure 5. Clock Sources



By default, 32 kHz is selected as the PWM clock.

PWM Period registers are used to set the output period:

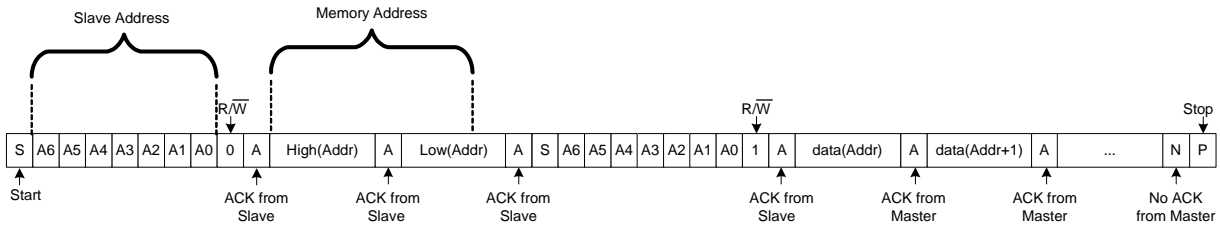
$$t_{OUT} = Period \times t_{CLK}$$

Allowed values are between 1 and FFh.

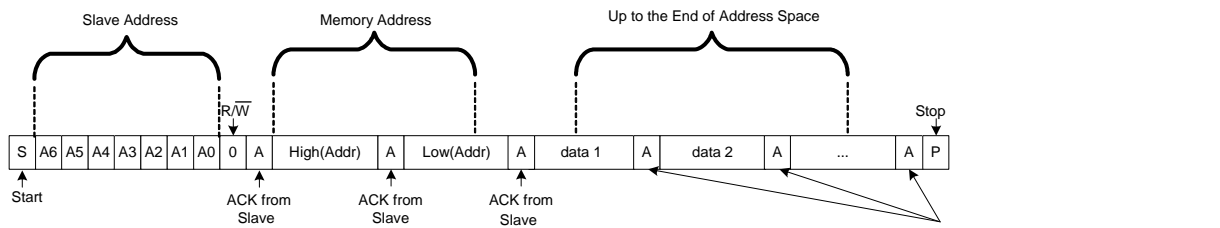
The PWM Pulse Width register sets the duration of the PWM output pulse. Allowed values are between zero and the (Period-1) value. The duty cycle ratio is computed using this equation:

$$DutyCycle = \frac{PulseWidth}{Period}$$

Figure 6. Memory Reading and Writing

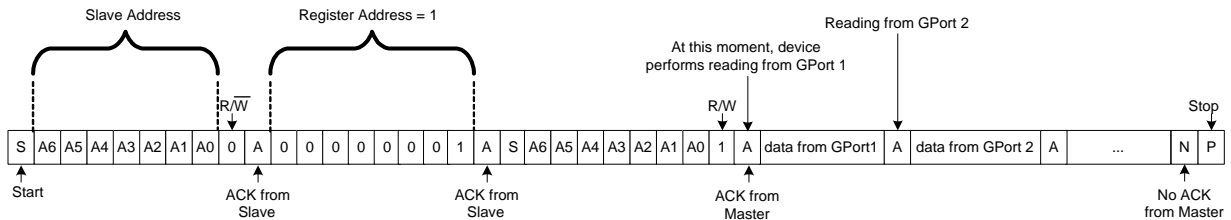


Reading from EEPROM

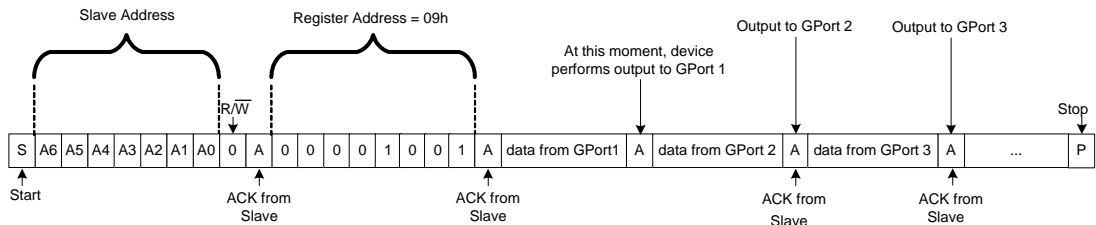


Writing to EEPROM

Figure 7. Port Reading and Writing in Multi-Port Device



Reading from GPort 1



Writing from GPort 1

Register Mapping Table

The register address is auto-incrementing. If the master device writes or reads data to or from one register and then continues data transfer in the same I²C transaction, sequential bytes are written or read to or from the following registers. For example, if the first byte is sent to the Output Port 1 register, then the next bytes are written to Output Port 2, Output Port 3, Output Port 4 etc. The first byte of each write transaction is treated as the register address.

To read data from a series of registers, the master device must write the starting register address byte then perform a start and series of read transactions. If no address was sent, reads start from address 0.

To read a specific register address, the master device must write the register address byte, then perform a start and read transaction.

See [Figure 7 on page 10](#).

The device's register mapping is listed in [Table 6](#).

Table 6. The Device Register Address Map

| Address | Register | Default Register Value |
|---------|-------------------------|------------------------|
| 00h | Input Port 0 | None |
| 01h | Input Port 1 | None |
| 02h | Input Port 2 | None |
| 03h | Input Port 3 | None |
| 04h | Input Port 4 | None |
| 05h | Input Port 5 | None |
| 06h | Input Port 6 | None |
| 07h | Input Port 7 | None |
| 08h | Output Port 0 | FFh |
| 09h | Output Port 1 | FFh |
| 0Ah | Output Port 2 | FFh |
| 0Bh | Output Port 3 | FFh |
| 0Ch | Output Port 4 | FFh |
| 0Dh | Output Port 5 | FFh |
| 0Eh | Output Port 6 | FFh |
| 0Fh | Output Port 7 | FFh |
| 10h | Interrupt Status Port 0 | 00h |
| 11h | Interrupt Status Port 1 | 00h |
| 12h | Interrupt Status Port 2 | 00h |
| 13h | Interrupt Status Port 3 | 00h |
| 14h | Interrupt Status Port 4 | 00h |
| 15h | Interrupt Status Port 5 | 00h |
| 16h | Interrupt Status Port 6 | 00h |
| 17h | Interrupt Status Port 7 | 00h |
| 18h | Port Select | 00h |
| 19h | Interrupt Mask | FFh |

Table 6. The Device Register Address Map (continued)

| Address | Register | Default Register Value |
|---------|------------------------------|------------------------|
| 1Ah | Select PWM for Port Output | 00h |
| 1Bh | Inversion | 00h |
| 1Ch | Pin Direction - Input/Output | 00h |
| 1Dh | Drive Mode - Pull Up | FFh |
| 1Eh | Drive Mode - Pull Down | 00h |
| 1Fh | Drive Mode - Open Drain High | 00h |
| 20h | Drive Mode - Open Drain Low | 00h |
| 21h | Drive Mode - Strong | 00h |
| 22h | Drive Mode - Slow Strong | 00h |
| 23h | Drive Mode - High-Z | 00h |
| 24h | Reserved | None |
| 25h | Reserved | None |
| 26h | Reserved | None |
| 27h | Reserved | None |
| 28h | PWM Select | 00h |
| 29h | Config PWM | 00h |
| 2Ah | Period PWM | FFh |
| 2Bh | Pulse Width PWM | 80h |
| 2Ch | Programmable Divider | FFh |
| 2Dh | Enable WDE, EEE, EERO | 00h |
| 2Eh | Device ID/Status | 20h/40h/60h |
| 2Fh | Watchdog | 00h |
| 30h | Command | 00h |

Register Descriptions

The registers for the CY8C95xx are described in the sections that follow. Note that the PWM registers are located at addresses 28h to 2Bh.

Input Port Registers (00h–07h)

These registers represent actual logical levels on the pins and are used for I/O port reading operations. They are read only. The Inversion registers changes the state of reads to these ports.

Output Port Registers (08h–0Fh)

These registers are used for writing data to GPIO ports. By default, all ports are in the pull up mode allowing quasi-bidirectional I/O. To allow input operations without reconfiguration, these registers have to store '1's.

Output register data also affects pin states when PWMs are enabled. See [Table 7 on page 12](#) for details.

See [Figure 7 on page 10](#) illustrates port read/write procedures.

The Inversion registers have no effect on these ports.

Int. Status Port Registers (10h–17h)

Each '1' bit in these registers signals that there was a change in the corresponding input line since the last read of that Interrupt Status register. Each Interrupt (Int.) Status register is cleared only after a read of that register.

If a PWM is assigned to a pin, then all state changes of the PWM sets the corresponding bit in the Interrupt Status register. If the pin's interrupt mask is cleared and the PWM is set to the slowest possible rate allowed (driven by the programmable clock source with divide register 2Dh set to FFh), then the INT line also drives on the PWM state change.

Port Select Register (18h)

This register configures the GPort. Write a value of 0–7 to this register to select the port to program with registers 19h–23h.

Interrupt Mask Port Register (19h)

The Interrupt Mask register enables or disables activation of the INT line when GPIO input levels are changed. Each '1' in the Interrupt Mask register masks (disables) interrupts generated from the corresponding input line of the GPort selected by the Port Select register (18h).

Select PWM Register (1Ah)

This register allows each port to act as a PWM output. By default, all ports are configured as GPIO lines. Each '1' in this register connects the corresponding pin of the GPort selected by the Port Select register (18h) to the PWM output. Output register data also affects the pin state when a PWM is enabled. See [Table 7](#).

Note that a pin used as PWM output must be configured to the appropriate drive mode. See [Table 9](#) for more information.

[Table 7](#) describes the logic of the Output and Select PWM registers.

Table 7. Output and Select PWM Registers Logic

| Output | Select PWM | Pin State |
|--------|------------|-------------|
| 0 | 0 | 0 |
| 1 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 1 | Current PWM |

Inversion Register (1Bh)

This register can invert the logic of the input ports. Each '1' written to this register inverts the logic of the corresponding bit in the Input register of the GPort selected by the Port Select register (18h).

The Input registers' logic is presented in [Table 8](#). These registers have no effect on outputs or PWMs.

Table 8. Inversion Register Logic

| Pin State | Invert | Input |
|-----------|--------|-------|
| 0 | 0 | 0 |
| 1 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 1 | 0 |

Port Direction Register (1Ch)

Each bit in a port is configurable as either an input or an output. To perform this configuration, the Port Direction register (1Ch) is used for the GPort selected by the Port Select register (18h). If a bit in this register is set (written with '1'), the corresponding port pin is enabled as an input. If a bit in this register is cleared (written with '0'), the corresponding port pin is enabled as an output.

Drive Mode Registers (1Dh–23h)

Each port's data pins can be set separately to one of seven available modes: pull up or down, open drain high/low, strong drive fast/slow, or high-impedance input. To perform this configuration, the seven drive mode registers are used for the GPort selected by the Port Select register (18h). Each '1' written to this register changes the corresponding line drive mode. Registers 1Dh through 23h have last register priority meaning that the bit set to high in which the last register was written overrides those that came before. Reading these registers reflects the actual setting, not what was originally written.

Table 9. Drive Mode Register Settings

| Reg. | Pin State | Description |
|------|---------------------|---|
| 1Dh | Resistive Pull Up | Resistive High, Strong Low (default) |
| 1Eh | Resistive Pull Down | Strong High, Resistive Low |
| 1Fh | Open Drain High | Slow Strong High, High Z Low |
| 20h | Open Drain Low | Slow Strong Low, High Z High |
| 21h | Strong Drive | Strong High, Strong Low, Fast Output Mode |
| 22h | Slow Strong Drive | Strong High, Strong Low, Slow Output Mode |
| 23h | High Impedance | High Z |

PWM Select Register (28h)

This register is configured the PWM. Write a value of 00h–0Fh to this register to select the PWM to program with registers 29h–2Bh.

Config (29h)

This register selects the clock source for the PWM selected by the PWM Select register (28h) and interrupt logic.

There are six available clock sources: 32 kHz (default), 24 MHz, 1.5 MHz, 93.75 kHz, 367.6 Hz, or previous PWM output. The 367.6 Hz clock is user programmable. It divides the 93.75 kHz clock source by the divisor stored in the Divider register (2Ch). The default divide ratio is 255. (see Table 10 for details). By default, all PWMs are clocked from 32 kHz.

Table 10. PWM Clock Sources

| Config PWM | PWM Clock Source |
|------------|-------------------------|
| xxxx000b | 32 kHz (default) |
| xxxx001b | 24 MHz |
| xxxx010b | 1.5 MHz |
| xxxx011b | 93.75 kHz |
| xxxx100b | 367.6 Hz (programmable) |
| xxxx101b | Previous PWM |

Each PWM can generate an interrupt at the rising or falling edge of the output pulse. There is a limitation on the clock source for a PWM to generate an interrupt. Only the slowest speed source (programmed to 367.6 Hz) with the divider equal to 255 allows interrupt generation. Consequently, to create a PWM interrupt, it is necessary to choose the programmable divider output as the clock source (write xxxx100b to Config register (29h)), write 255 to the Divide register (2Ch), and select PWM for pin output (1Ah).

Interrupt status is reflected in the Interrupt Status registers (10h-17h) and can cause INT line activation if enabled by the corresponding mask bit in the Interrupt Mask register.

Period Register (2Ah)

Table 11. Period Register

| Config PWM | PWM Interrupt on |
|------------|------------------------------|
| xxx0xxx | Falling pulse edge (default) |
| xxx1xxx | Rising pulse edge |

This register sets the period of the PWM counter. Allowed values are between 1 and FFh. The effective output waveform period of the PWM is:

$$t_{OUT} = Period \cdot t_{CLK}$$

Pulse Width Register (2Bh)

This register sets the pulse width of the PWM output. Allowed values are between zero and the (Period - 1) value. The duty cycle ratio can be computed using the following equation:

$$DutyCycle = \frac{PulseWidth}{Period}$$

Divider Register (2Ch)

This register sets the frequency on the output of the programmable divider:

$$Frequency = \frac{93.75 \text{ kHz}}{Divider}$$

Allowed values are between 1 and 255.

Enable Register (2Dh)

The WDE bit configures the write disable pin to operate either as a GPIO or as WD. It also enables/disables EEPROM operations (EEE bit) or makes the EEPROM read-only (EERO bit). Bit assignments are shown in Table 12 on page 13.

Table 12. Enable Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|----------|---|---|---|---|------|-----|-----|
| Function | Reserved | | | | | EERO | EEE | WDE |
| Default | Reserved | | | | | 0 | 0 | 0 |

Each '1' enables the corresponding feature, '0' disables.

Writes to this register differ from other registers. The write sequence to modify the Enable register is as follows:

1. Send device I²C address with bit 0.
2. Send register address 2Dh.
3. Send unlock key - the sequence of three bytes: 43h, 4Dh, 53h; ('C', 'M', 'S' in ASCII bytes).
4. Send new Enable register value.

This write sequence secures the register from accidental changes. The register can be read without the use of the unlock key.

By default, EERO and EEPROM (EEE bit) are disabled and WD line (WDE bit) is set to GPIO (WD disabled).

When performing a burst write operation that crosses this register, the data written to this register is ignored and the address increments to 2Eh.

Device ID/Status Register (2Eh)

This register stores device identifiers (2xh/4xh/6xh) and reflects which settings were loaded during startup, either factory defaults (FD) or user defaults (UD). By default during startup, the device attempts to load the user default block. If it is corrupted then factory defaults are loaded and the low nibble of this register is set high to inform which set is active. The high nibble is always equal to 2 for CY8C9520A, 4 for CY8C9540A, and 6 for CY8C9560A.

This register is read-only.

Table 13. Device ID Status Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|----------------------------|---|---|---|----------|---|---|-------|
| Function | Device Family (2, 4, or 6) | | | | Reserved | | | FD/UD |

Watchdog Register (2Fh)

This register controls the internal Watchdog timer. This timer can trigger a device reset if the device is not responding to I²C requests due to misconfiguration. Device operation is not affected when the Watchdog register = 0. If the I²C master writes any non zero value to the Watchdog register, the countdown mechanism is activated and each second the register is decremented. Upon transition from 1 to 0, the device is rebooted, which restores user defaults. After reboot, the Watchdog register value is reset to zero. Any I²C transaction (addressing the Expander) resets the Watchdog register to the previously stored value. Any device reboot (caused by a POR or Watchdog) sets the Watchdog register to zero (turns off the Watchdog feature). The Watchdog timer can be disabled by writing zero to the Watchdog register (2Fh) or by using the Reconfigure Device Cmd (07h).

Note The Watchdog timer is not intended to track precise time intervals. The timer's frequency can vary in range between -50% on up to +100%. This variation must be taken into account when selecting the appropriate value for the Watchdog register.

Command Register (30h)

This register sends commands to the device, including current configuration as new POR defaults, restore factory defaults, define POR defaults, read POR defaults, write device configuration, read device configuration, and reconfigure device with stored POR defaults. The command set is presented in Table 14.

Note Registers are not restored in parallel. Do not assume any particular order to the restoration process.

Table 14. Available Commands

| Command | Description |
|---------|---|
| 01h | Store device configuration to EEPROM POR defaults |
| 02h | Restore Factory Defaults |
| 03h | Write EEPROM POR defaults |
| 04h | Read EEPROM POR defaults |
| 05h | Write device configuration |
| 06h | Read device configuration |
| 07h | Reconfigure device with stored POR defaults |

Commands Description

Store Config to E² POR Defaults Cmd (01h)

The current ports settings (drive modes and output data) and other configuration registers are saved in the EEPROM by using the store configuration command (Cmd). These settings are automatically loaded after the next device power up or if the 07h command is issued.

Restore Factory Defaults Cmd (02h)

This command replaces the saved user configuration with the factory default configuration. Current settings are unaffected by this command. New settings are loaded after the next device power up or if the 07h command is issued.

Write E² POR Defaults Cmd (03h)

This command sends new power up defaults to the CY8C95xx without changing current settings unless the 07h command is issued afterwards. This command is followed by 147 data bytes according to Table 15. The CRC is calculated as the XOR of the 146 data bytes (00h-91h). If the CRC check fails or an incomplete block is sent, then the slave responds with a NAK and the data does not get saved to EEPROM.

To define new POR defaults the user must:

- Write command 03h
- Write 146 data bytes with new values of registers
- Write 1 CRC byte calculated as XOR of previous 146 data bytes.

Content of the data block is described in Table 15.

Table 15. POR Defaults Data Structure

| Offset | Value |
|---------|---------------------------------------|
| 00h–07h | Output Port 0–7 |
| 08h–0Fh | Interrupt mask Port 0–7 |
| 10h–17h | Select PWM Port 0–7 |
| 18h–1Fh | Inversion Port 0–7 |
| 20h–27h | Pin Direction Port 0–7 |
| 28h | Resistive pull up Drive Mode Port 0 |
| 29h | Resistive pull down Drive Mode Port 0 |
| 2Ah | Open drain high Drive Mode Port 0 |
| 2Bh | Open drain low Drive Mode Port 0 |
| 2Ch | Strong drive Drive Mode Port 0 |
| 2Dh | Slow strong drive Drive Mode Port 0 |
| 2Eh | High impedance Drive Mode Port 0 |
| 2Fh–35h | Drive Modes Port 1 |
| 36h–3Ch | Drive Modes Port 2 |
| 3Dh–43h | Drive Modes Port 3 |
| 44h–4Ah | Drive Modes Port 4 |
| 4Bh–51h | Drive Modes Port 5 |
| 52h–58h | Drive Modes Port 6 |
| 59h–5Fh | Drive Modes Port 7 |
| 60h | Config setting PWM0 |
| 61h | Period setting PWM0 |
| 62h | Pulse Width setting PWM0 |
| 63h–65h | PWM1 settings |
| ... | ... |
| 8Dh–8Fh | PWM15 settings |
| 90h | Divider |
| 91h | Enable |
| 92h | CRC |

Read E2 POR Defaults Cmd (04h)

This command reads the POR settings stored in the EEPROM.

To read POR defaults the user must:

- Write command 04h
- Read 146 data bytes (see [Table 15 on page 14](#))
- Read 1 CRC byte.

Write Device Config Cmd (05h)

This command sends a new device configuration to the CY8C95xx. It is followed by 146 data bytes according to [Table 15](#). The CRC is calculated as the XOR of the 146 data bytes (00h-91h). If the CRC check fails or an incomplete block is sent, then the slave responds with a NAK and the device does not use the data. This gives the user 'flat-address-space' access to all device settings.

To set the current device configuration the user must:

- Write command 05h
- Write 146 data bytes with new values of registers
- Write 1 CRC byte calculated as XOR of previous 146 data bytes.

If the CRC check passes, then the device uses the new settings immediately.

Content of the data block is described in [Table 15 on page 14](#).

Read Device Config Cmd (06h)

This command reads the current device configuration. It gives the user 'flat-address-space' access to all device settings.

To read device configuration the user must:

- Write command 06h
- Read 146 data bytes (see [Table 15 on page 14](#)).
- Read 1 CRC byte.

Reconfigure Device Cmd (07h)

This command immediately reconfigures the device with actual POR defaults from EEPROM. It has the same effect on the registers as a POR.

Electrical Specifications

This section lists the DC and AC electrical specifications of the CY8C95xxA device. For the most up to date electrical specifications, confirm that you have the most recent data sheet by going to the web at <http://www.cypress.com>.

Specifications are valid for $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ and $T_J \leq 100\text{ }^{\circ}\text{C}$, except where noted.

Absolute Maximum Ratings

Table 16. Absolute Maximum Ratings

| Symbol | Description | Min | Typ | Max | Units | Notes |
|-----------------------|--|-------------------|-----|-------------------|-------|---|
| T _{STG} | Storage temperature | -55 | 25 | +100 | °C | Higher storage temperatures reduces data retention time. Recommended storage temperature is +25 °C ± 25 °C. Extended duration storage temperatures above 65°C degrades reliability. |
| T _{BAKETEMP} | Bake Temperature | - | 125 | See package label | °C | |
| T _{BAKETIME} | Bake Time | See package label | - | 72 | Hours | |
| T _A | Ambient temperature with power applied | -40 | - | +85 | °C | |
| V _{dd} | Supply voltage on Vdd relative to Vss | -0.5 | - | +6.0 | V | |
| V _{IO} | DC input voltage | Vss - 0.5 | - | Vdd + 0.5 | V | |
| V _{IOZ} | DC voltage applied to tri-state | Vss - 0.5 | - | Vdd + 0.5 | V | |
| I _{MIO} | Maximum current into any port pin | -25 | - | +50 | mA | |
| ESD | Electro Static Discharge Voltage | 2000 | - | - | V | Human Body Model ESD. |
| LU | Latch up current | - | - | 200 | mA | |

Operating Temperature

Table 17. Operating Temperature

| Symbol | Description | Min | Typ | Max | Units | Notes |
|----------------|----------------------|-----|-----|------|-------|--|
| T _A | Ambient temperature | -40 | - | +85 | °C | |
| T _J | Junction temperature | -40 | - | +100 | °C | The temperature rise from ambient to junction is package specific. See “ Thermal Impedances per Package ” on page 23. The user must limit the power consumption to comply with this requirement. |

DC Electrical Characteristics

DC Chip-Level Specifications

Table 18 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, or 3.0 V to 3.6 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 18. CY8C9520A DC Chip-Level Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|------------------|--------------------------------------|------|-----|------|-------|--|
| V _{DD} | Supply voltage | 3.00 | – | 5.25 | V | |
| I _{DD} | Supply current V _{DD} 5 V | – | 3.8 | 5 | mA | Conditions are 5.0 V, T _A = 25 °C, I _{OH} = 0. |
| I _{DD3} | Supply current V _{DD} 3.3 V | – | 2.3 | 3 | mA | Conditions are 3.3 V, T _A = 25 °C, I _{OH} = 0. |

Table 19. CY8C9540A DC Chip-Level Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|------------------|--------------------------------------|------|-----|------|-------|--|
| V _{DD} | Supply voltage | 3.00 | – | 5.25 | V | |
| I _{DD} | Supply current V _{DD} 5 V | – | 6 | 9 | mA | Conditions are 5.0 V, T _A = 25 °C, I _{OH} = 0. |
| I _{DD3} | Supply current V _{DD} 3.3 V | – | 3.3 | 6 | mA | Conditions are 3.3 V, T _A = 25 °C, I _{OH} = 0. |

Table 20. CY8C9560A DC Chip-Level Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|------------------|--------------------------------------|------|-----|------|-------|--|
| V _{DD} | Supply voltage | 3.00 | – | 5.25 | V | |
| I _{DD} | Supply current V _{DD} 5 V | – | 15 | 25 | mA | Conditions are 5.0 V, T _A = 25 °C, I _{OH} = 0. |
| I _{DD3} | Supply current V _{DD} 3.3 V | – | 5 | 9 | mA | Conditions are 3.3 V, T _A = 25 °C, I _{OH} = 0. |

DC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, or 3.0 V to 3.6 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 21. DC Programming Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|-----------------------|--|-----------|-----|-----|-------|------------------------------|
| Flash _{ENPB} | Flash (EEPROM) endurance (by block) | 10,000 | – | – | – | Erase/write cycles by block. |
| Flash _{ENT} | Flash endurance (total) ^[3] | 1,800,000 | – | – | – | Erase/write cycles. |
| Flash _{DR} | Flash data retention | 10 | – | – | Years | |

DC I²C Specifications

Table 22 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, or 3.0 V to 3.6 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 22. DC I²C Specifications^[4]

| Symbol | Description | Min | Typ | Max | Units | Notes |
|-------------------|------------------|-----------------------|-----|------------------------|-------|-----------------------------------|
| V _{IL2C} | Input low level | – | – | 0.3 × V _{DD} | V | 3.0 V ≤ V _{DD} ≤ 3.6 V |
| | | – | – | 0.25 × V _{DD} | V | 4.75 V ≤ V _{DD} ≤ 5.25 V |
| V _{IH2C} | Input high level | 0.7 × V _{DD} | – | – | V | 3.0 V ≤ V _{DD} ≤ 5.25 V |

Note

- A maximum of 180 x 10,000 block endurance cycles is allowed. This may be balanced between operations on 180x1 blocks of 10,000 maximum cycles each, 180x2 blocks of 5,000 maximum cycles each, or 180x4 blocks of 2,500 maximum cycles each (to limit the total number of cycles to 180x10,000 and that no single block ever sees more than 10,000 cycles).
- All GPIO meet the DC GPIO VIL and VIH specifications found in the DC GPIO Specifications sections. The I²C GPIO pins also meet the above specs.

DC GPIO Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, or 3.0 V to 3.6 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 23. DC GPIO Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|------------------|-----------------------------------|-----------------------|-----|------|-------|---|
| V _{OH} | High output level | V _{dd} - 1.0 | – | – | V | I _{OH} = 10 mA for any one pin, V _{dd} = 4.75 to 5.25 V. 40 mA maximum combined I _{OH} for GPort0; GPort2_Bit3; GPort3; GPort5_Bit2, 3, 6, 7; GPort6. 40 mA maximum combined I _{OH} for GPort1; GPort2_Bit0, 1, 2; GPort4; GPort5_Bit0, 1, 4, 5; GPort7. 80 mA maximum combined I _{OH} . |
| V _{OL} | Low output level | – | – | 0.75 | V | I _{OL} = 25 mA for any one pin, V _{dd} = 4.75 to 5.25 V. 100 mA maximum combined I _{OL} for GPort0; GPort2_Bit3; GPort3; GPort5_Bit2, 3, 6, 7; GPort6. 100 mA maximum combined I _{OL} for GPort1; GPort2_Bit0, 1, 2; GPort4; GPort5_Bit0, 1, 4, 5; GPort7. 200 mA maximum combined I _{OL} . |
| I _{OH} | High Level Source Current | 10 | – | – | mA | V _{OH} = V _{dd} - 1.0 V, see the limitations of the total current in the note for V _{OH} |
| I _{OL} | Low Level Sink Current | 25 | – | – | mA | V _{OL} = 0.75 V, see the limitations of the total current in the note for V _{OL} |
| V _{IL} | Input low level | – | – | 0.8 | V | V _{dd} = 3.0 to 5.5. |
| V _{IH} | Input high level | 2.1 | – | – | V | V _{dd} = 3.0 to 5.5. |
| I _{IL} | Input leakage (absolute value) | – | 1 | – | nA | Gross tested to 1 μA. |
| C _{IN} | Capacitive load on pins as input | – | 3.5 | 10 | pF | Package and pin dependent. Temp = 25 °C. |
| C _{OUT} | Capacitive load on pins as output | – | 3.5 | 10 | pF | Package and pin dependent. Temp = 25 °C. |
| R _{PU} | Pull-up resistor | 4 | 5.6 | 8 | kΩ | None |
| R _{PD} | Pull-down resistor | 4 | 5.6 | 8 | kΩ | None |

AC Electrical Characteristics

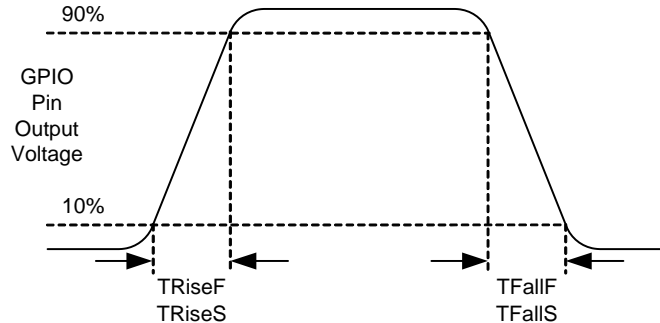
AC GPIO Specifications

Table 24 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, or 3.0 V to 3.6 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only or unless otherwise specified.

Table 24. AC GPIO Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|-------------------------|---|------|-----|-------|-------|---|
| F_{GPIO} | GPIO Operating Frequency | 0 | – | 12 | MHz | Normal Strong Mode |
| T_{RiseF} | Rise time, normal strong mode, Load = 50 pF | 3 | – | 18 | ns | $V_{\text{dd}} = 4.75$ to 5.25 V, 10%–90% |
| T_{FallF} | Fall time, normal strong mode, Load = 50 pF | 2 | – | 18 | ns | $V_{\text{dd}} = 4.75$ to 5.25 V, 10%–90% |
| T_{RiseS} | Rise time, slow strong mode, Load = 50 pF | 10 | 27 | – | ns | $V_{\text{dd}} = 3$ to 5.25 V, 10%–90% |
| T_{FallS} | Fall time, slow strong mode, Load = 50 pF | 10 | 22 | – | ns | $V_{\text{dd}} = 3$ to 5.25 V, 10%–90% |
| T_{IOAccess} | IO access time | – | – | 2.485 | ms | None |
| $T_{\text{Pulsewidth}}$ | Minimum pulse width on I/Os to assert INT line. | 5.03 | – | – | ms | No I ² C activity or EEPROM operation happens during input pulse duration. |

Figure 8. GPIO Timing Diagram



AC PWM Specifications

Table 25 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, or 3.0 V to 3.6 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only or unless otherwise specified.

Table 25. AC PWM Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|----------------|---|------|-----|------|-------|---|
| Jitter24MHzPWM | 24 MHz based PWM peak-to-peak period jitter | – | 0.1 | 1.5 | % | 24 MHz, 1.5 MHz, 93.75 kHz and 367.6 Hz (programmable) sources. |
| Jitter32kHzPWM | 32 kHz-based PWM peak-to-peak period jitter | – | 2.5 | 5.0 | % | 32 kHz clock source. |
| F24MHzPWM | Input Frequency of 24 MHz based PWM | 23.4 | 24 | 24.6 | MHz | |
| F32kHzPWM | Input Frequency of 32 kHz based PWM | 15 | 32 | 64 | kHz | |
| F1.5MHzPWM | Input frequency of 1.5 MHz based PWM | 1.46 | 1.5 | 1.53 | MHz | |

Table 25. AC PWM Specifications

| | | | | | | |
|--------------|--|-------|-------|-------|-----|--|
| F93.75kHzPWM | Input Frequency of 93.75 kHz based PWM | 91.40 | 93.75 | 96.09 | kHz | |
|--------------|--|-------|-------|-------|-----|--|

AC I²C Specifications

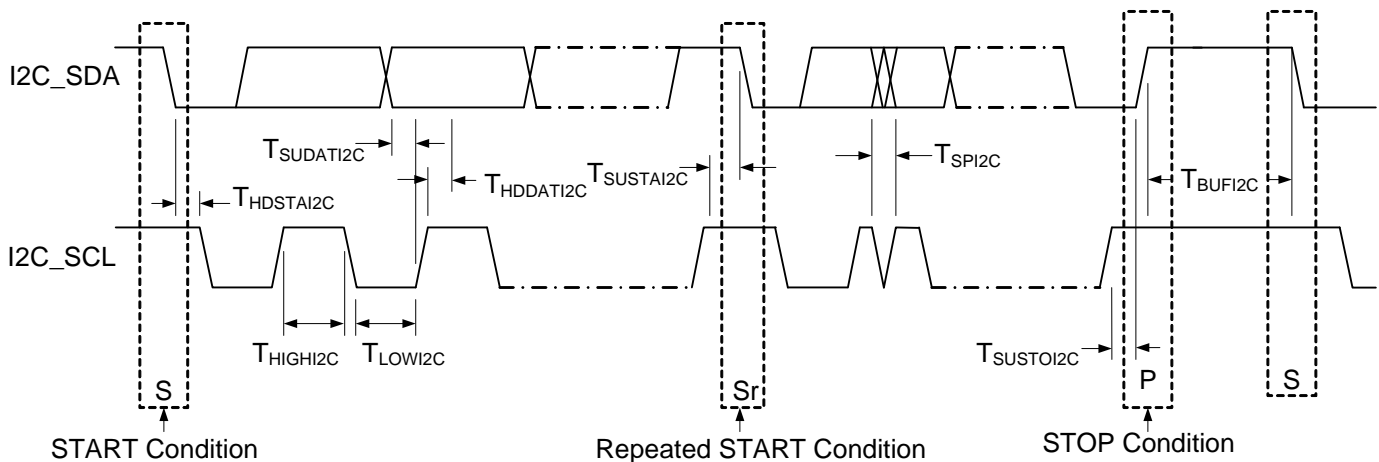
Table 26 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, or 3.0 V to 3.6 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only or unless otherwise specified.

Table 26. AC Characteristics of the I²C SDA and SCL Pins

| Symbol | Description | Standard Mode | | Units | Notes |
|-----------------------|--|---------------|-----|-------|-------|
| | | Min | Max | | |
| F _{SCL I2C} | SCL clock frequency | 0 | 100 | kHz | |
| T _{HDSTAI2C} | Hold time (repeated) START condition. After this period, the first clock pulse is generated. | 4.0 | – | μs | |
| T _{LOWI2C} | LOW period of the SCL clock | 4.7 | – | μs | |
| T _{HIGHI2C} | HIGH period of the SCL clock | 4.0 | – | μs | |
| T _{SUSTAI2C} | Setup time for a repeated START condition | 4.7 | – | μs | |
| T _{HDDATI2C} | Data hold time | 0 | – | μs | |
| T _{SUDATI2C} | Data setup time | 250 | – | ns | |
| T _{SUSTOI2C} | Setup time for STOP condition | 4.0 | – | μs | |
| T _{BUFI2C} | Bus free time between a STOP and START Condition | 4.7 | – | μs | |
| T _{SPI2C} | Pulse width of spikes are suppressed by the input filter. | – | – | ns | |

Note: Fast mode I²C is not supported.

Figure 9. Definition for Timing for Standard Mode on the I²C Bus



AC EEPROM Write Specifications

Table 27 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, or 3.0 V to 3.6 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only or unless otherwise specified.

Table 27. AC EEPROM Write Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|-------------------------------|---------------------------|-----|-----|-----|-------|--------------------------------|
| T _{EEPROMWrite_Hot} | EEPROM Erase + Write time | – | – | 100 | ms | 0 °C ≤ T _j ≤ 100 °C |
| T _{EEPROMWrite_Cold} | EEPROM Erase + Write time | – | – | 200 | ms | –40 °C ≤ T _j ≤ 0 °C |

Packaging Dimensions

This section illustrates the packaging specifications for the CY8C95xxA device, along with the thermal impedances for each package and the solder reflow peak temperature.

Important Note Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the emulator pod drawings at <http://www.cypress.com>.

Figure 10. 28-pin SSOP (210 Mils) Package Outline

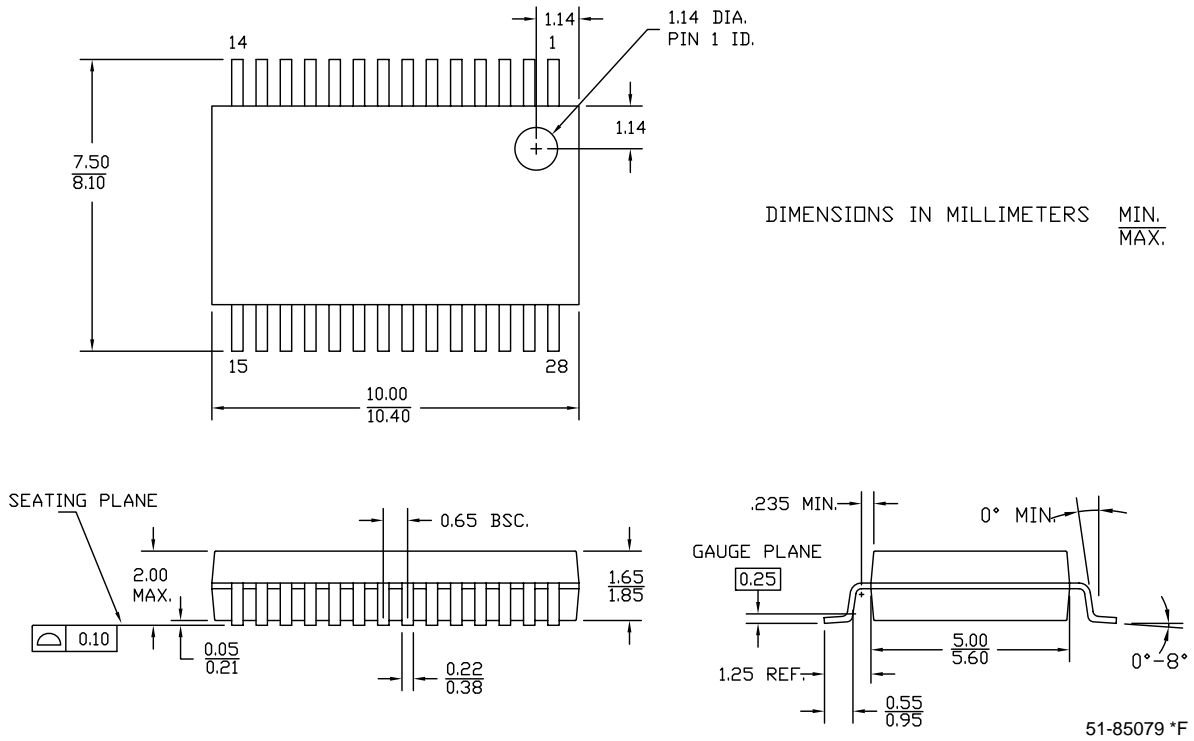


Figure 11. 48-pin SSOP (300 Mils) Package Outline

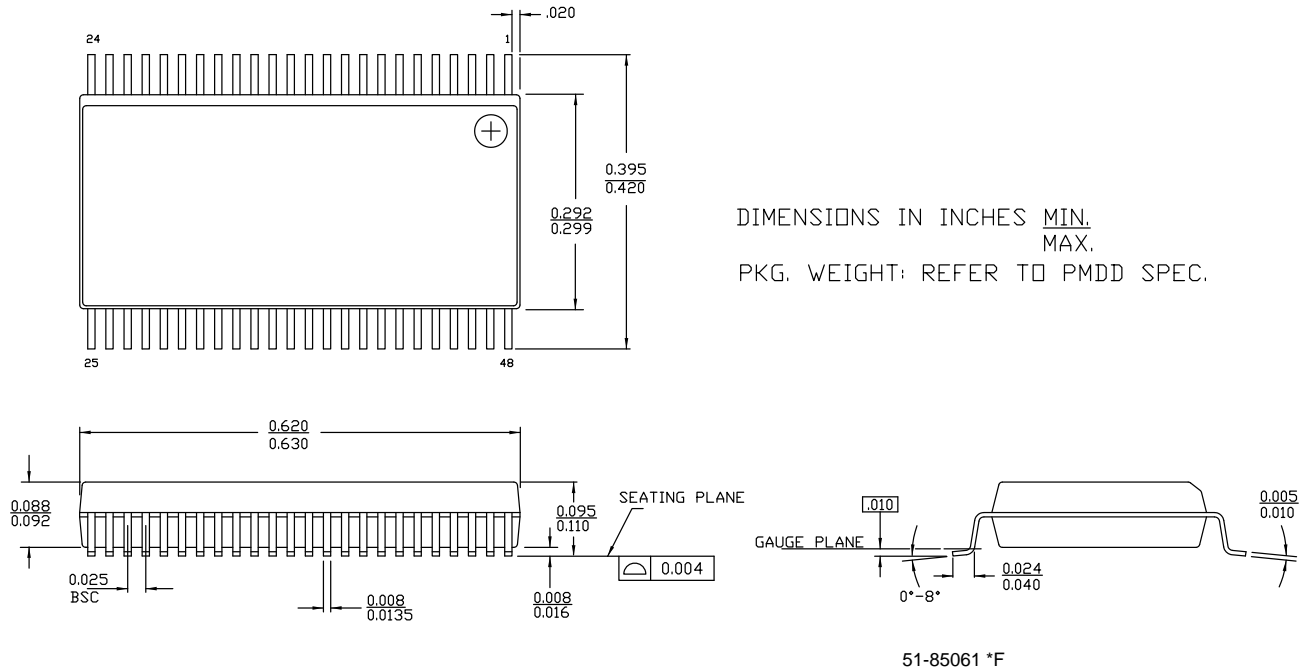
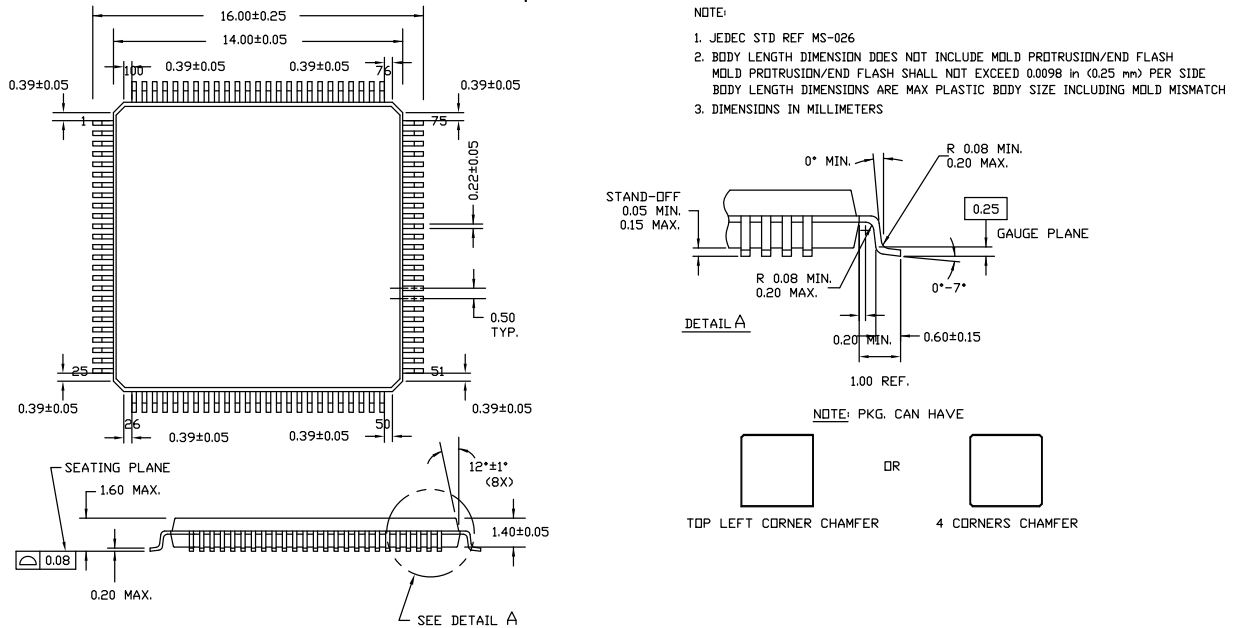


Figure 12. 100-pin TQFP (14 x 14 x 1.0 mm) Package Outline



Thermal Impedances

Table 28. Thermal Impedances per Package

| Package | Typical θ_{JA} [5] |
|--------------|---------------------------|
| 28-pin SSOP | 101 °C/W |
| 48-pin SSOP | 69 °C/W |
| 100-pin TQFP | 48 °C/W |

Solder Reflow Specifications

Table 29 shows the solder reflow temperature limits that must not be exceeded.

Table 29. Solder Reflow Specifications

| Package | Maximum Peak Temperature (T_C) | Maximum Time above $T_C - 5$ °C |
|--------------|------------------------------------|---------------------------------|
| 28-pin SSOP | 260 °C | 30 seconds |
| 48-pin SSOP | 260 °C | 30 seconds |
| 100-pin TQFP | 260 °C | 30 seconds |

Notes

5. $T_J = T_A + \text{POWER} \times \theta_{JA}$.

Features and Ordering Information

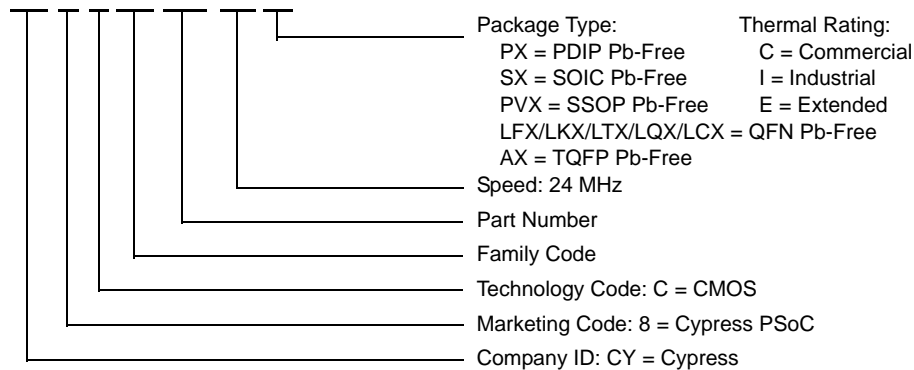
Table 30 lists the CY8C95xxA device's key package features and ordering codes. A definition of the ordering number code follows.

Table 30. CY8C95xxA Device Key Features and Ordering Information

| Package | Ordering Code ^[6] | EEPROM (Bytes) | Temperature Range | PWM Sources | Configurable I/O Pins |
|---------------------------------------|------------------------------|----------------|-------------------|-------------|-----------------------|
| 28 Pin (210 Mil) SSOP | CY8C9520A-24PVXI | 3K | -40 °C to +85°C | 4 | 20 |
| 28 Pin (210 Mil) SSOP (Tape and Reel) | CY8C9520A-24PVXIT | 3K | -40 °C to +85°C | 4 | 20 |
| 48 Pin (300 Mil) SSOP | CY8C9540A-24PVXI | 11K | -40 °C to +85°C | 8 | 40 |
| 48 Pin (300 Mil) SSOP (Tape and Reel) | CY8C9540A-24PVXIT | 11K | -40 °C to +85°C | 8 | 40 |
| 100 Pin TQFP | CY8C9560A-24AXI | 27K | -40 °C to +85°C | 16 | 60 |
| 100 Pin TQFP (Tape and Reel) | CY8C9560A-24AXIT | 27K | -40 °C to +85°C | 16 | 60 |

Ordering Code Definitions

CY 8 C 9 xxx-SPxx



Note

6. The A after the existing port expander part number indicates new device firmware.

Acronyms

Table 31 lists the acronyms that are used in this document.

Table 31. Acronyms Used in this Datasheet

| Acronym | Description | Acronym | Description |
|---------|---|-------------------|---|
| AC | alternating current | POR | power on reset |
| API | application programming interface | PSoC [®] | Programmable System-on-Chip |
| CMOS | complementary metal oxide semiconductor | PWM | pulse width modulator |
| CRC | cyclic redundancy check | SSOP | shrink small-outline package |
| DC | direct current | TQFP | thin quad flat pack |
| EEPROM | electrically erasable programmable read-only memory | UART | universal asynchronous receiver / transmitter |
| GPIO | general purpose I/O | USB | universal serial bus |
| I/O | input/output | WDT | watchdog timer |
| MSB | most-significant bit | XRES | external reset |
| PCB | printed circuit board | | |

Document Conventions

Units of Measure

Table 32 lists the units of measures.

Table 32. Units of Measure

| Symbol | Unit of Measure | Symbol | Unit of Measure |
|--------|-----------------------------|--------|-----------------|
| °C | degree Celsius | mm | millimeter |
| Hz | hertz | ms | millisecond |
| kHz | kilohertz | nA | nanoampere |
| kΩ | kilohm | ns | nanosecond |
| MHz | megahertz | Ω | ohm |
| μA | microampere | % | percent |
| μs | microsecond | pF | picofarad |
| μV | microvolt | V | volt |
| μVrms | microvolts root-mean-square | W | watt |
| mA | milliampere | | |

Numeric Conventions

Numeric Naming

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase 'h' (for example, '14h' or '3Ah'). Hexadecimal numbers may also be represented by a '0x' prefix, the C coding convention. Binary numbers have an appended lowercase 'b' (for example, '01010100b' or '01000011b'). Numbers not indicated by an 'h' or 'b' are decimals.

Glossary

| | |
|---|--|
| active high | <ol style="list-style-type: none"> 1. A logic signal having its asserted state as the logic 1 state. 2. A logic signal having the logic 1 state as the higher voltage of the two states. |
| analog blocks | The basic programmable opamp circuits. These are SC (switched capacitor) and CT (continuous time) blocks. These blocks can be interconnected to provide ADCs, DACs, multi-pole filters, gain stages, and much more. |
| analog-to-digital (ADC) | A device that changes an analog signal to a digital signal of corresponding magnitude. Typically, an ADC converts a voltage to a digital number. The digital-to-analog (DAC) converter performs the reverse operation. |
| Application programming interface (API) | A series of software routines that comprise an interface between a computer application and lower level services and functions (for example, user modules and libraries). APIs serve as building blocks for programmers that create software applications. |
| asynchronous | A signal whose data is acknowledged or acted upon immediately, irrespective of any clock signal. |
| bandgap reference | A stable voltage reference design that matches the positive temperature coefficient of V_T with the negative temperature coefficient of V_{BE} , to produce a zero temperature coefficient (ideally) reference. |
| bandwidth | <ol style="list-style-type: none"> 1. The frequency range of a message or information processing system measured in hertz. 2. The width of the spectral region over which an amplifier (or absorber) has substantial gain (or loss); it is sometimes represented more specifically as, for example, full width at half maximum. |
| bias | <ol style="list-style-type: none"> 1. A systematic deviation of a value from a reference value. 2. The amount by which the average of a set of values departs from a reference value. 3. The electrical, mechanical, magnetic, or other force (field) applied to a device to establish a reference level to operate the device. |
| block | <ol style="list-style-type: none"> 1. A functional unit that performs a single function, such as an oscillator. 2. A functional unit that may be configured to perform one of several functions, such as a digital PSoC block or an analog PSoC block. |
| buffer | <ol style="list-style-type: none"> 1. A storage area for data that is used to compensate for a speed difference, when transferring data from one device to another. Usually refers to an area reserved for IO operations, into which data is read, or from which data is written. 2. A portion of memory set aside to store data, often before it is sent to an external device or as it is received from an external device. 3. An amplifier used to lower the output impedance of a system. |
| bus | <ol style="list-style-type: none"> 1. A named connection of nets. Bundling nets together in a bus makes it easier to route nets with similar routing patterns. 2. A set of signals performing a common function and carrying similar data. Typically represented using vector notation; for example, address[7:0]. 3. One or more conductors that serve as a common connection for a group of related devices. |
| clock | The device that generates a periodic signal with a fixed frequency and duty cycle. A clock is sometimes used to synchronize different logic blocks. |
| comparator | An electronic circuit that produces an output voltage or current whenever two input levels simultaneously satisfy predetermined amplitude requirements. |
| compiler | A program that translates a high level language, such as C, into machine language. |
| configuration space | In PSoC devices, the register space accessed when the XIO bit, in the CPU_F register, is set to '1'. |
| crystal oscillator | An oscillator in which the frequency is controlled by a piezoelectric crystal. Typically a piezoelectric crystal is less sensitive to ambient temperature than other circuit components. |
| cyclic redundancy check (CRC) | A calculation used to detect errors in data communications, typically performed using a linear feedback shift register. Similar calculations may be used for a variety of other purposes such as data compression. |
| data bus | A bi-directional set of signals used by a computer to convey information from a memory location to the central processing unit and vice versa. More generally, a set of signals used to convey data between digital functions. |

Glossary (continued)

| | |
|---------------------------------|---|
| debugger | A hardware and software system that allows you to analyze the operation of the system under development. A debugger usually allows the developer to step through the firmware one step at a time, set break points, and analyze memory. |
| dead band | A period of time when neither of two or more signals are in their active state or in transition. |
| digital blocks | The 8-bit logic blocks that can act as a counter, timer, serial receiver, serial transmitter, CRC generator, pseudo-random number generator, or SPI. |
| digital-to-analog (DAC) | A device that changes a digital signal to an analog signal of corresponding magnitude. The analog-to-digital (ADC) converter performs the reverse operation. |
| duty cycle | The relationship of a clock period high time to its low time, expressed as a percent. |
| emulator | Duplicates (provides an emulation of) the functions of one system with a different system, so that the second system appears to behave like the first system. |
| External Reset (XRES) | An active high signal that is driven into the PSoC device. It causes all operation of the CPU and blocks to stop and return to a pre-defined state. |
| Flash | An electrically programmable and erasable, non-volatile technology that provides you the programmability and data storage of EPROMs, plus in-system erasability. Non-volatile means that the data is retained when power is OFF. |
| Flash block | The smallest amount of Flash ROM space that may be programmed at one time and the smallest amount of Flash space that may be protected. A Flash block holds 64 bytes. |
| frequency | The number of cycles or events per unit of time, for a periodic function. |
| gain | The ratio of output current, voltage, or power to input current, voltage, or power, respectively. Gain is usually expressed in dB. |
| I ² C | A two-wire serial computer bus by Philips Semiconductors (now NXP Semiconductors). I ² C is an Inter-Integrated Circuit. It is used to connect low-speed peripherals in an embedded system. The original system was created in the early 1980s as a battery control interface, but it was later used as a simple internal bus system for building control electronics. I ² C uses only two bi-directional pins, clock and data, both running at +5 V and pulled high with resistors. The bus operates at 100 kbits/second in standard mode and 400 kbits/second in fast mode. |
| ICE | The in-circuit emulator that allows you to test the project in a hardware environment, while viewing the debugging device activity in a software environment (PSoC Designer). |
| input/output (I/O) | A device that introduces data into or extracts data from a system. |
| interrupt | A suspension of a process, such as the execution of a computer program, caused by an event external to that process, and performed in such a way that the process can be resumed. |
| interrupt service routine (ISR) | A block of code that normal code execution is diverted to when the M8C receives a hardware interrupt. Many interrupt sources may each exist with its own priority and individual ISR code block. Each ISR code block ends with the RETI instruction, returning the device to the point in the program where it left normal program execution. |
| jitter | <ol style="list-style-type: none"> 1. A misplacement of the timing of a transition from its ideal position. A typical form of corruption that occurs on serial data streams. 2. The abrupt and unwanted variations of one or more signal characteristics, such as the interval between successive pulses, the amplitude of successive cycles, or the frequency or phase of successive cycles. |
| low-voltage detect (LVD) | A circuit that senses V _{dd} and provides an interrupt to the system when V _{dd} falls below a selected threshold. |
| M8C | An 8-bit Harvard-architecture microprocessor. The microprocessor coordinates all activity inside a PSoC by interfacing to the Flash, SRAM, and register space. |
| master device | A device that controls the timing for data exchanges between two devices. Or when devices are cascaded in width, the master device is the one that controls the timing for data exchanges between the cascaded devices and an external interface. The controlled device is called the slave device . |

Glossary (continued)

| | |
|-----------------------------|---|
| microcontroller | An integrated circuit chip that is designed primarily for control systems and products. In addition to a CPU, a microcontroller typically includes memory, timing circuits, and IO circuitry. The reason for this is to permit the realization of a controller with a minimal quantity of chips, thus achieving maximal possible miniaturization. This in turn, reduces the volume and the cost of the controller. The microcontroller is normally not used for general-purpose computation as is a microprocessor. |
| mixed-signal | The reference to a circuit containing both analog and digital techniques and components. |
| modulator | A device that imposes a signal on a carrier. |
| noise | <ol style="list-style-type: none"> 1. A disturbance that affects a signal and that may distort the information carried by the signal. 2. The random variations of one or more characteristics of any entity such as voltage, current, or data. |
| oscillator | A circuit that may be crystal controlled and is used to generate a clock frequency. |
| parity | A technique for testing transmitting data. Typically, a binary digit is added to the data to make the sum of all the digits of the binary data either always even (even parity) or always odd (odd parity). |
| Phase-locked loop (PLL) | An electronic circuit that controls an oscillator so that it maintains a constant phase angle relative to a reference signal. |
| pinouts | The pin number assignment: the relation between the logical inputs and outputs of the PSoC device and their physical counterparts in the printed circuit board (PCB) package. Pinouts involve pin numbers as a link between schematic and PCB design (both being computer generated files) and may also involve pin names. |
| port | A group of pins, usually eight. |
| Power on reset (POR) | A circuit that forces the PSoC device to reset when the voltage is below a pre-set level. This is one type of hardware reset. |
| PSoC® | Cypress Semiconductor's PSoC® is a registered trademark and Programmable System-on-Chip™ is a trademark of Cypress. |
| PSoC Designer™ | The software for Cypress' Programmable System-on-Chip technology. |
| pulse width modulator (PWM) | An output in the form of duty cycle which varies as a function of the applied measurand |
| RAM | An acronym for random access memory. A data-storage device from which data can be read out and new data can be written in. |
| register | A storage device with a specific capacity, such as a bit or byte. |
| reset | A means of bringing a system back to a know state. See hardware reset and software reset. |
| ROM | An acronym for read only memory. A data-storage device from which data can be read out, but new data cannot be written in. |
| serial | <ol style="list-style-type: none"> 1. Pertaining to a process in which all events occur one after the other. 2. Pertaining to the sequential or consecutive occurrence of two or more related activities in a single device or channel. |
| settling time | The time it takes for an output signal or value to stabilize after the input has changed from one value to another. |
| shift register | A memory storage device that sequentially shifts a word either left or right to output a stream of serial data. |
| slave device | A device that allows another device to control the timing for data exchanges between two devices. Or when devices are cascaded in width, the slave device is the one that allows another device to control the timing of data exchanges between the cascaded devices and an external interface. The controlling device is called the master device. |
| SRAM | An acronym for static random access memory. A memory device where you can store and retrieve data at a high rate of speed. The term static is used because, after a value is loaded into an SRAM cell, it remains unchanged until it is explicitly altered or until power is removed from the device. |
| SROM | An acronym for supervisory read only memory. The SROM holds code that is used to boot the device, calibrate circuitry, and perform Flash operations. The functions of the SROM may be accessed in normal user code, operating from Flash. |

Glossary (continued)

| | |
|----------------|---|
| stop bit | A signal following a character or block that prepares the receiving device to receive the next character or block. |
| synchronous | 1. A signal whose data is not acknowledged or acted upon until the next active edge of a clock signal. 2. A system whose operation is synchronized by a clock signal. |
| tri-state | A function whose output can adopt three states: 0, 1, and Z (high-impedance). The function does not drive any value in the Z state and, in many respects, may be considered to be disconnected from the rest of the circuit, allowing another output to drive the same net. |
| UART | A UART or universal asynchronous receiver-transmitter translates between parallel bits of data and serial bits. |
| user modules | Pre-build, pre-tested hardware/firmware peripheral functions that take care of managing and configuring the lower level Analog and Digital PSoC Blocks. User Modules also provide high level API (Application Programming Interface) for the peripheral function. |
| user space | The bank 0 space of the register map. The registers in this bank are more likely to be modified during normal program execution and not just during initialization. Registers in bank 1 are most likely to be modified only during the initialization phase of the program. |
| V_{DD} | A name for a power net meaning “voltage drain.” The most positive power supply signal. Usually 5 V or 3.3 V. |
| V_{SS} | A name for a power net meaning “voltage source.” The most negative power supply signal. |
| watchdog timer | A timer that must be serviced periodically. If it is not serviced, the CPU resets after a specified period of time. |

Errata

This section describes the errata for CY8C9560A device. Details include the trigger condition, scope of impact, available workaround, and silicon revision applicability. Contact your local Cypress Sales Representative if you have questions.

Part Numbers Affected

| Part Number |
|-------------|
| CY8C9560A |

Qualification Status

CY8C9560A Rev. A – In Production

Errata Summary

The following table defines the errata applicability to available devices.

| Items | Part Number | Silicon Revision | Fix Status |
|--|-------------|------------------|---|
| 1. The command 01h cannot store more than 128 bytes of configuration data from SRAM to EEPROM. | CY8C9560A | A | No silicon fix planned. Workaround is required. |

1. The command 01h cannot store more than 128 bytes of configuration data from SRAM to EEPROM.

□ Problem Definition

The Store Config to E² POR Defaults Cmd (01h) can write only up to 128 bytes of configuration data from SRAM to the EEPROM. Configuration data exceeding 128 bytes are ignored.

□ Parameters Affected

NA

□ Trigger Condition

NA

□ Scope of Impact

Configuration data from SRAM to EEPROM exceeding 128 bytes are ignored.

□ Workaround

As a workaround, use the Write E² POR Defaults Cmd (03h) command to explicitly write all configuration data to EEPROM using I²C.

□ Fix Status

No fixes are planned. You must use the recommended workaround.

Document History Page

| Document Title: CY8C9520A/CY8C9540A/CY8C9560A, 20-, 40-, and 60-Bit I/O Expander with EEPROM | | | | |
|--|---------|-----------------|-----------------|--|
| Document Number: 38-12036 | | | | |
| Revision | ECN | Orig. of Change | Submission Date | Description of Change |
| ** | 346754 | HMT | See ECN | New silicon, document. |
| *A | 392484 | HMT | See ECN | Correct pin 79 on the TQFP. Add AC PWM Output Jitter spec. table. Upgrade to CY Perform logo and update zip code and trademarks. |
| *B | 1336984 | HMT / AESA | See ECN | Update typical and recommended Storage Temperature per industrial specs. Update copyright and trademarks. Add Watchdog timer details. Add "A" to existing part numbers to indicate new firmware. Fix errors. Implement CY template. |
| *C | 2843174 | YARA | 01/08/2010 | Added Contents . Updated Overview . Updated Pin 11 description in Figure 2 on page 5 . Modified Note 3. Added I _{OH} and I _{OL} specifications in DC GPIO Specifications . Removed "Output Jitter" from AC PWM Specifications section on page 18. Added F24MHzPWM, F32kHzPWM, and F93.5kHzPWM specifications in Table 25 . Added Table 27 . |
| *D | 2903402 | NJF | 04/01/2010 | Updated Cypress website links Added T _{BAKETEMP} and T _{BAKETIME} parameters Updated package diagrams |
| *E | 3110285 | NJF | 12/14/10 | Added text "When the part is held in reset all In and Out pins are held at their default High-Z State" to section "External Reset Pin (XRES)" on page 9. Added DC I ² C Specifications table. Updated Units of Measure, Acronyms, Glossary, and References sections. Updated solder reflow specifications. No specific changes made to I ² C Timing Diagram. It has been updated for clearer understanding. |
| *F | 3381717 | NPD | 09/23/11 | Updated solder reflow specifications to improve clarity. Updated package diagrams. |
| *G | 4512488 | DIMA | 09/24/2014 | Updated Pin Descriptions : Updated Extendable Soft Addressing : Updated description. Updated Interrupt Pin (INT) : Updated description. Updated Electrical Specifications : Updated DC Electrical Characteristics : Updated DC GPIO Specifications : Updated Table 23 : Added R _{PU} , R _{PD} parameters and their details. Updated AC Electrical Characteristics : Updated AC GPIO Specifications : Updated Table 24 : Added TIOAccess parameter and its details. Updated AC I2C Specifications : Updated Table 26 (Removed the column "Fast Mode"). Updated Figure 9 (No change in figure, removed "Fast" in caption only). Updated Packaging Dimensions : spec 51-85061 – Changed revision from *E to *F. spec 51-85048 – Changed revision from *E to *I. Updated to new template. Completing Sunset Review. |
| *H | 4569861 | ASRI | 11/22/2014 | Added Errata . |
| *I | 4708108 | DIMA | 04/01/2015 | Added minimum input pulse width in Table 24 . Removed reference to obsolete application note, AN2304. |

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