270mW Stereo Cap-Free Headphone Driver

Features

- **No Output Capacitor Required**
- **Dual Supply Voltage (PV_{DD}>V_{DD})**
  - **– V_{DD}=1.8 ~5.5V**
  - **– PV_{DD}=2.2 ~ 5.5V**
- **Meeting VISTA Requirements**
- **Output Power**
  at 1% THD+N
  -200mW, at V_{DD}=3.3V, PV_{DD}=5.0V, R_L=16Ω
  -55mW, at V_{DD}=1.8V, PV_{DD}=3.0V, R_L=16Ω
  at 10% THD+N
  -270mW, at V_{DD}=3.3V, PV_{DD}=5.0V, R_L=16Ω
  -70mW, at V_{DD}=1.8V, PV_{DD}=3.0V, R_L=16Ω
- **Less External Components Required**
- **High PSRR: 80dB at 217Hz**
- **Fast Start-Up Time : 120ms**
- **Short-Circuit and Thermal Protection**
- **Surface-Mount Package**
  - **– TQFN4x4-20B (with Enhanced Thermal Pad)**
  - **– TSSOP-16**
  - **– TQFN3x3-16 (with Enhanced Thermal Pad)**
  (for APA2176A)
- **Lead Free and Green Devices Available**
  (RoHS Compliant)

Applications

- **Headsets**
- **PDAs**
- **Portable Multimedia Devices**
- **Notebooks**

General Description

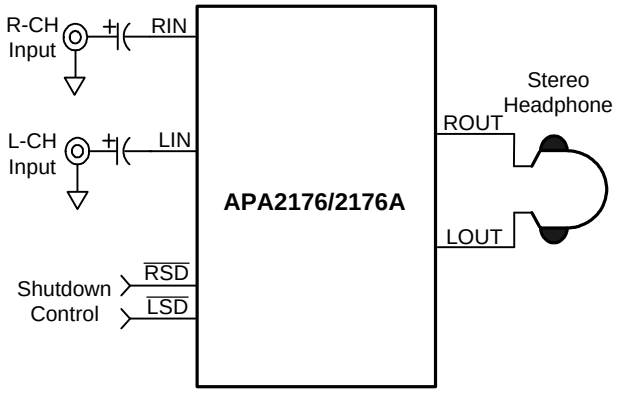
The APA2176/2176A is a stereo, fixed gain, and cap-free headphone driver which is available in TQFN4x4 20-pin, TQFN3x3 16-pin (APA2176A) or TSSOP-16 package. Dual supply voltage provides higher efficiency and better power ripple rejection.

The APA2176/2176A is designed with ground-reference output and no need the output capacitors for DC blocking. The advantages of eliminating the output capacitor are saving the cost, PCB's space, and component height.

The built-in gain setting can minimize the external component counts and save the PCB space. High PSRR provides increased immunity to noise and RF rectification. In addition to these features, a fast start-up time and small package size make the APA2176/2176A an ideal choice for portable multimedia devices.

Moreover, the APA2176/2176A is also equipped other features. For example, at THD+N=1%, it is capable of driving 200mW at V_{DD}=3.3V, PV_{DD}=5.0V into 16Ω. In addition, it provides thermal and short circuit protections.

Simplified Application Circuit



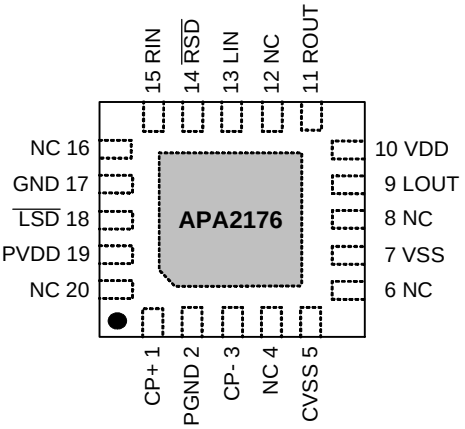
ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

Ordering and Marking Information

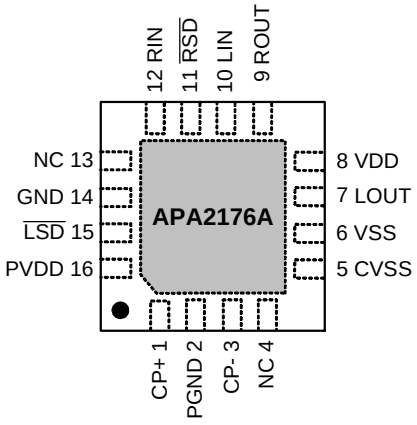
APA2176 APA2176A □□□-□□□ Assembly Material Handling Code Temperature Range Package Code	Package Code QB : TQFN4x4-20B O : TSSOP-16 QB : TQFN3x3-16 (APA2176A) Operating Ambient Temperature Range I : -40 to 85 °C Handling Code TR : Tape & Reel Assembly Material G : Halogen and Lead Free Device
APA2176 QB : 	XXXXX - Date Code
APA2176 O : 	XXXXX - Date Code
APA2176A QB : 	XXXXX - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines “Green” to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Pin Configuration

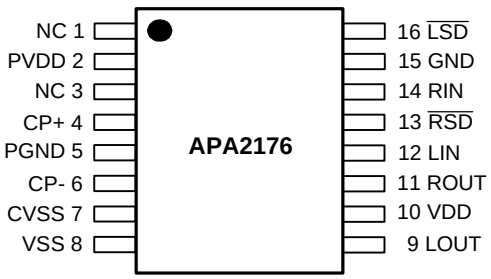


TQFN4x4-20B (Top View)



TQFN3x3-16 (Top View)

=Thermal Pad (connected the Thermal Pad to ground plane for better heat dissipation)



TSSOP-16 (Top View)

Absolute Maximum Ratings (Note 1)

(Over operating free-air temperature range unless otherwise noted.)

Symbol	Parameter	Rating	Unit
V_{DD}	Supply Voltage (VDD to GND)	-0.3 to 6	V
PV_{DD}	Charge Pump Supply Voltage (PVDD to PGND)	-0.3 to 6	V
V_{PGND_GND}	PGND to GND Voltage	-0.3 to 0.3	V
$V_{\overline{RSD}}$, $V_{\overline{LSD}}$	Input Voltage ($\overline{RSD}$ and $\overline{LSD}$ to GND)	-0.3 to V_{DD}+0.3	V
V_{SS}, CV_{SS}	VSS and CVSS to GND and PGND Voltage	-6 to 0.3	V
V_{ROUT}, V_{LOUT}	ROUT and LOUT to GND Voltage	V_{SS}-0.3 to V_{DD}+0.3	V
V_{CP+}	CP+ to PGND Voltage	-0.3 to PV_{DD}+0.3	V
V_{CP-}	CP- to PGND Voltage	CV_{SS}-0.3 to 0.3	V
T_J	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature Range	-65 to +150	°C
T_{SDR}	Maximum Lead Soldering Temperature, 10 Seconds	260	°C
P_D	Power Dissipation	Internally Limited	W

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics (Note 2,3)

Symbol	Parameter		Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in Free Air	TQFN3x3-16 TQFN4x4-20B TSSOP16	55 43 100	°C/W
θ_{JC}	Junction-to-Case Resistance in Free Air	TQFN3x3-16 TQFN4x4-20B	10 8	°C/W

Note 2: Please refer to “Thermal Pad Consideration”. 2 layered 5 in2 printed circuit boards with 2oz trace and copper through several thermal vias. The thermal pad is soldered on the PCB.

Note 3: The case temperature is measured at the center of the exposed pad on the underside of the TQFN3x3-16 and TQFN4x4-20B packages.

Recommended Operating Conditions (Note 4)

Symbol	Parameter		Range	Unit
V_{DD}	Supply Voltage		1.8 ~ 5.5	V
PV_{DD}	Charge Pump Power Supply Voltage		2.2 ~ 5.5	V
V_{IH}	High Level Threshold Voltage	$\overline{RSD}$, $\overline{LSD}$	0.6PV_{DD} ~ PV_{DD}	V
V_{IL}	Low Level Threshold Voltage	$\overline{RSD}$, $\overline{LSD}$	0 ~ 0.3PV_{DD}	V
V_{ICM}	Common Mode Input Voltage		~ V_{DD}-1	V
T_A	Ambient Temperature		-40 ~ 85	°C
T_J	Junction Temperature		-40 ~ 125	°C
R_L	Headphone Resistance		14 ~	Ω

Note 4: Refer to the typical application circuit.

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Electrical Characteristics

Unless otherwise specified, these specifications apply over V_{DD}=3.3V, PV_{DD}=5V, V_{PGND}=V_{GND}=0V, and C_{CPO}=C_{CPF}=2.2µF. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions	APA2176/2176A			Unit
			Min.	Typ.	Max.	
SUPPLY CURRENT						
I_{DD}	V_{DD} Supply Current		-	2.0	4.0	mA
I_{PVDD}	PV_{DD} Supply Current		-	3.2	6.5	mA
$I_{SD(VDD)}$	V_{DD} Shutdown Current	$V_{\overline{RSD}}$ = $V_{\overline{LSD}}$ = 0	-	1.0	5.0	µA
$I_{SD(PVDD)}$	PV_{DD} Shutdown Current	$V_{\overline{RSD}}$ = $V_{\overline{LSD}}$ = 0	-	1.0	5.0	µA
CHARGE PUMP						
f_{OSC}	Switching Frequency		450	510	570	kHz
Req	Charge Pump Equivalent Resistance	C_{CPO}=C_{CPF}=2.2µF	6	7	9	Ω
POWER-ON-RESET						
	Rising VDD Threshold	PV_{DD}=5V	1.67	1.7	1.73	V
	Falling VDD Threshold	PV_{DD}=5V	1.57	1.6	1.63	V
AMPLIFIERS						
Av	Internal Voltage Gain	No Load	-1.55	-1.5	-1.45	V/V
ΔA_V	Gain Match		-	1.0	-	%
R_i	Input Resistance		12	14	16	kΩ
SR	Slew Rate		-	2.5	-	V/µs
C_L	Maximum Capacitive Load		-	400	-	pF
$T_{start-up}$	Start-Up Time from Shutdown		-	120	-	µs
V_{DD}=3.3V, PV_{DD}=5.0V, T_A=25°C						
P_O	Output Power	THD+N = 1%, f_{in}=1kHz, in Phase R_L = 16Ω R_L = 32Ω	125	200 150	-	mW
		THD+N = 10%, f_{in}=1kHz, in Phase R_L = 16Ω R_L = 32Ω	170	270 200	-	
THD+N	Total Harmonic Distortion Plus Noise	f_{in} = 1kHz P_O = 140mW, R_L = 16Ω P_O = 105mW, R_L = 32Ω V_O = 1.7Vrms, R_L = 10kΩ	-	0.04 0.03 0.002	-	%
Crosstalk	Channel Separation	f_{in} = 1kHz P_O = 140mW, R_L = 16Ω V_O = 1.7Vrms, R_L = 10kΩ	-	78 90	-	dB
PSRR	Power Supply Rejection Ratio	R_L = 16Ω, f_{in}=217Hz	-	90	-	dB
V_{OS}	Output Offset Voltage	R_L = 32Ω	-5	-	5	mV
S/N	Signal to Noise Ratio	With A-weighting Filter P_O = 105mW, R_L = 32Ω	-	95	-	dB
Vn	Noise Output Voltage	R_L = 32Ω	-	15	-	µV (rms)

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Electrical Characteristics (Cont.)

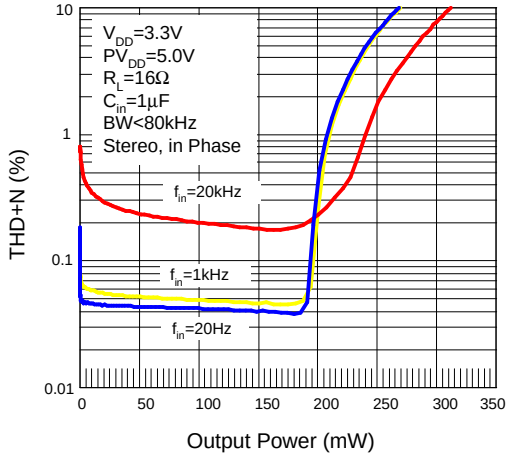
Unless otherwise specified, these specifications apply over V_{DD}=3.3V, PV_{DD}=5V, V_{PGND}=V_{GND}=0V, and C_{CPO}=C_{CPF}=2.2µF. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions	APA2176/2176A			Unit
			Min.	Typ.	Max.	
V_{DD}=1.8V, PV_{DD}=3.0V, T_A=25°C						
P_O	Output Power	THD+N = 1%, f_{in}=1kHz, in Phase R_L = 16Ω R_L = 32Ω	 35	 55 40	 - 	mW
		THD+N = 10%, f_{in}=1kHz, in Phase R_L = 16Ω R_L = 32Ω	 45	 70 55	 - 	
THD+N	Total Harmonic Distortion Plus Noise	f_{in} = 1kHz P_O = 40mW, R_L = 16Ω P_O = 30mW, R_L = 32Ω V_O = 0.9Vrms, R_L = 10kΩ	-	 0.04 0.03 0.002	-	%
Crosstalk	Channel Separation	f_{in} = 1kHz P_O = 40mW, R_L = 16Ω V_O = 0.9Vrms, R_L = 10kΩ	-	 78 90	-	dB
PSRR	Power Supply Rejection Ratio	R_L = 16Ω, f_{in}=217Hz	-	82	-	dB
V_{OS}	Output Offset Voltage	R_L = 32Ω	-5	-	5	mV
S/N	Signal to Noise Ratio	With A-weighting Filter P_O = 30mW, R_L = 32Ω	-	95	-	dB
Vn	Noise Output Voltage	R_L = 32Ω	-	15	-	µV (rms)

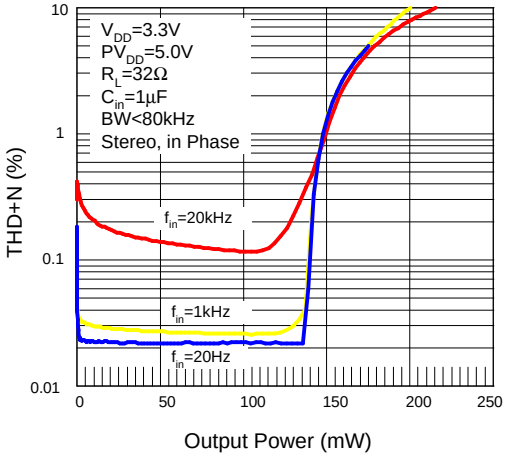
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Typical Operating Characteristics

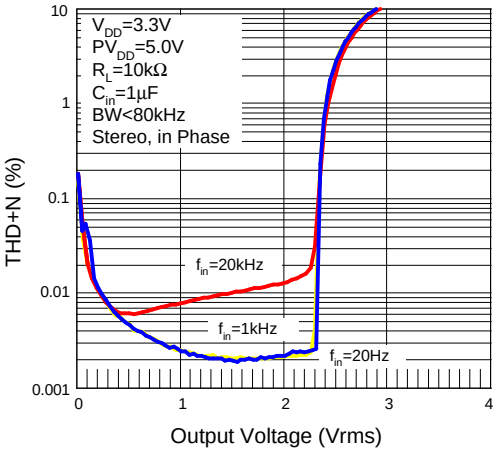
THD+N vs. Output Power



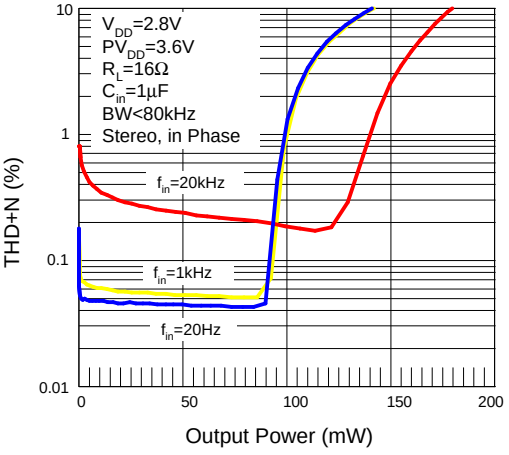
THD+N vs. Output Power



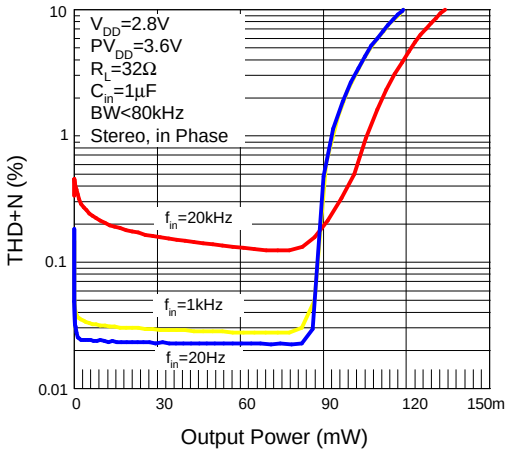
THD+N vs. Output Voltage



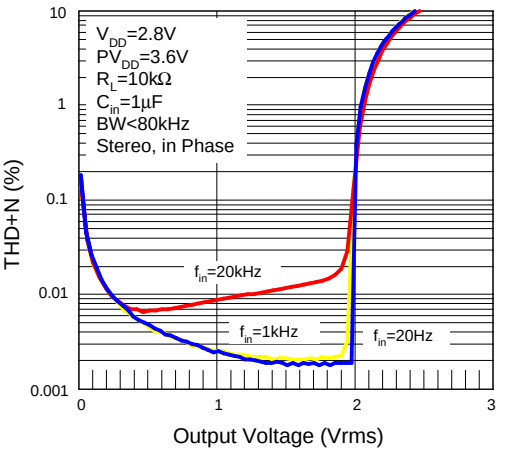
THD+N vs. Output Power



THD+N vs. Output Power



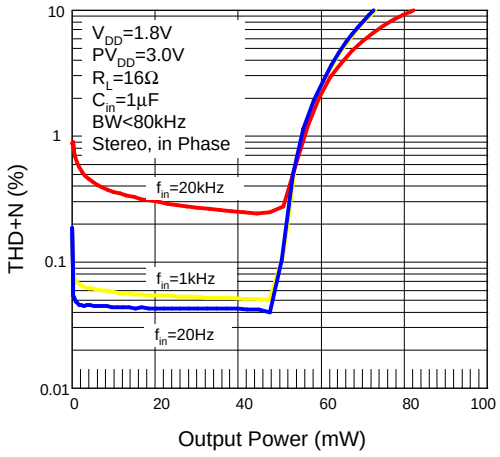
THD+N vs. Voltage



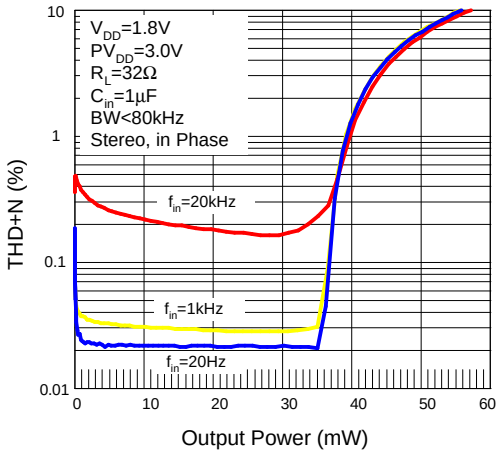
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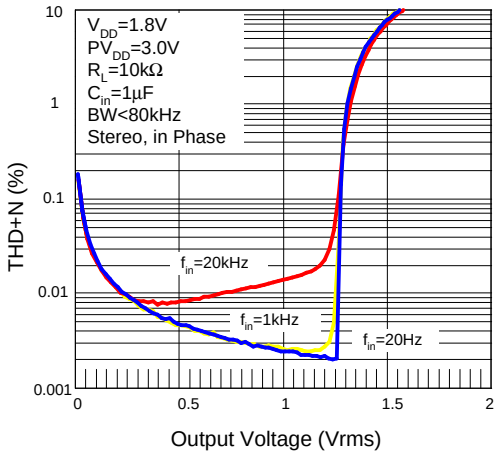
THD+N vs. Output Power



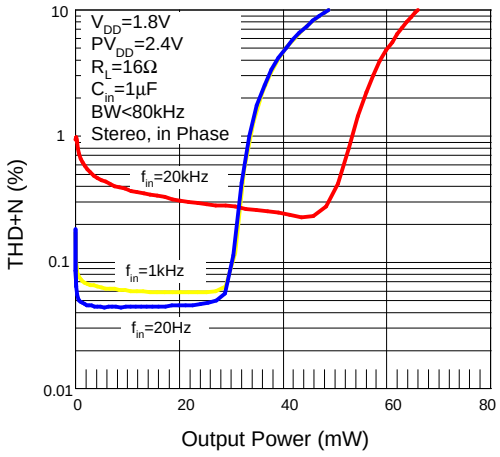
THD+N vs. Output Power



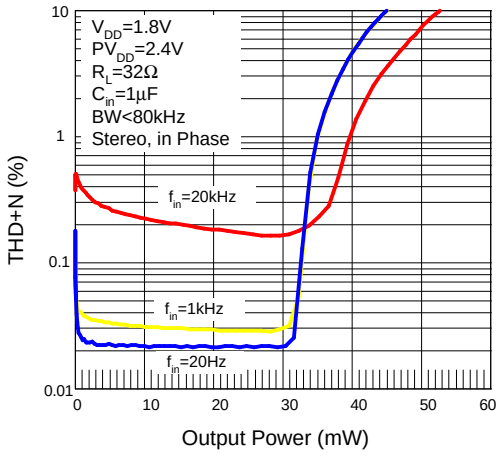
THD+N vs. Voltage



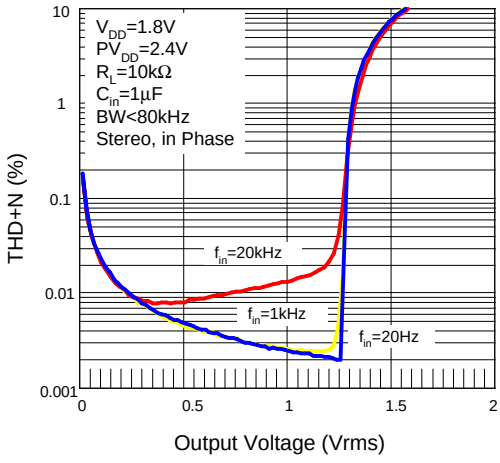
THD+N vs. Output Power



THD+N vs. Output Power

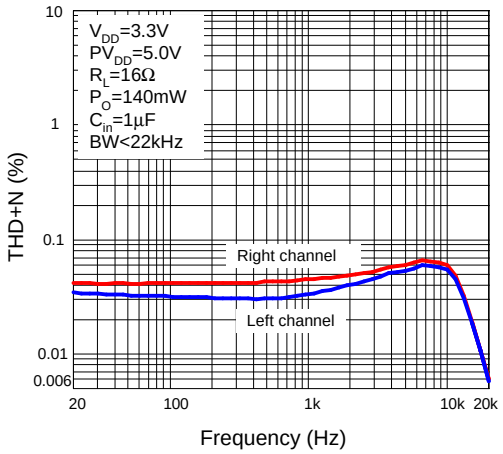


THD+N vs. Voltage

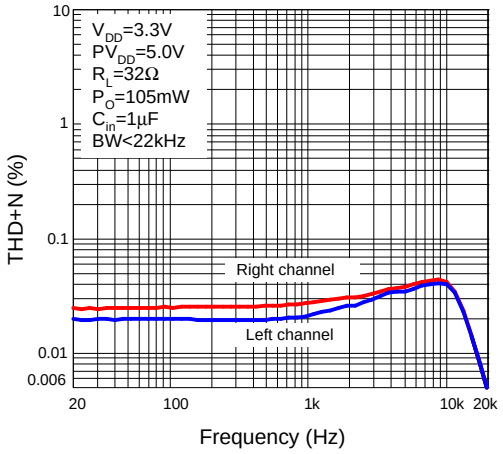


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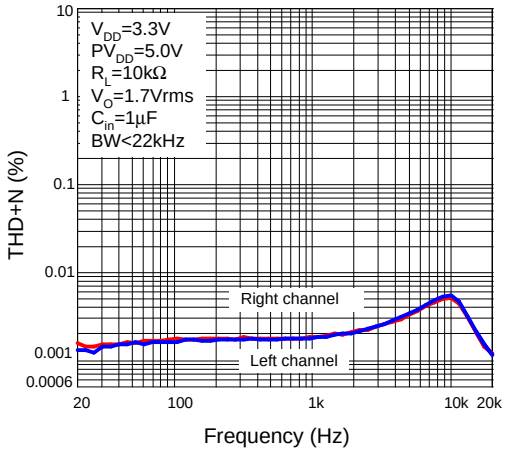
THD+N vs. Frequency



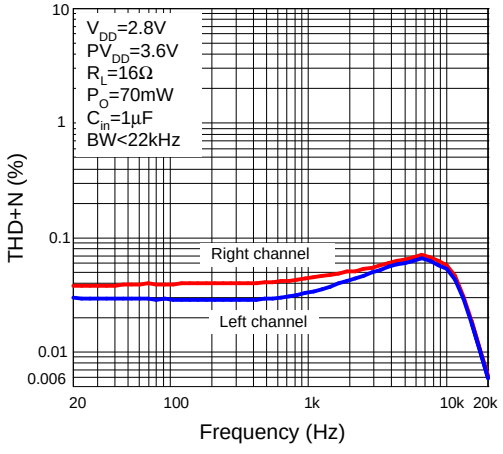
THD+N vs. Frequency



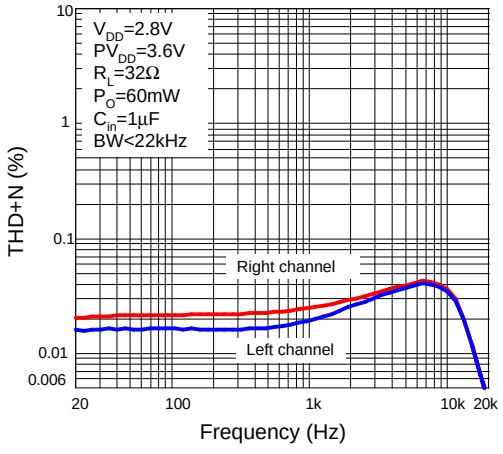
THD+N vs. Frequency



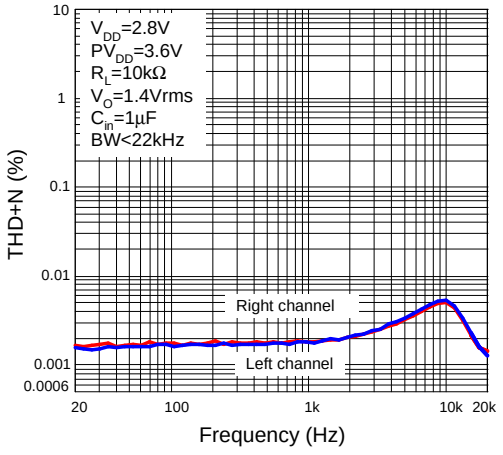
THD+N vs. Frequency



THD+N vs. Frequency



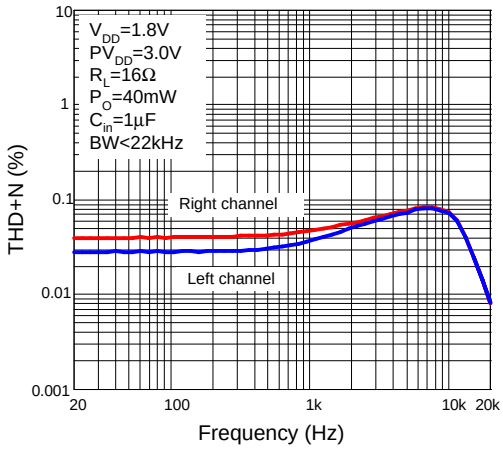
THD+N vs. Frequency



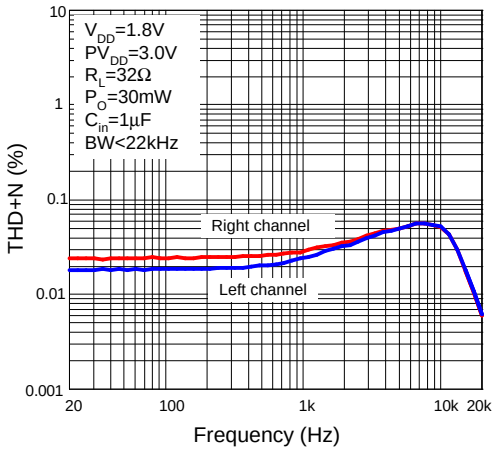
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Typical Operating Characteristics (Cont.)

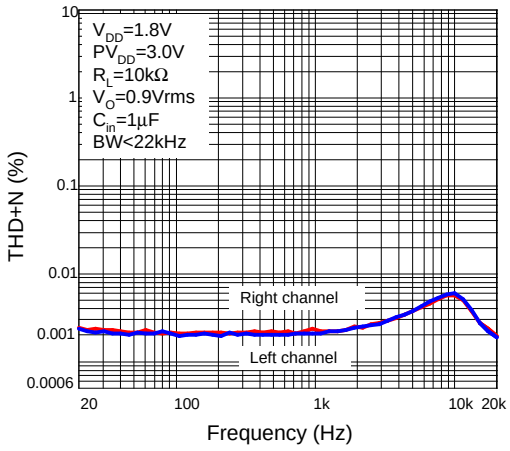
THD+N vs. Frequency



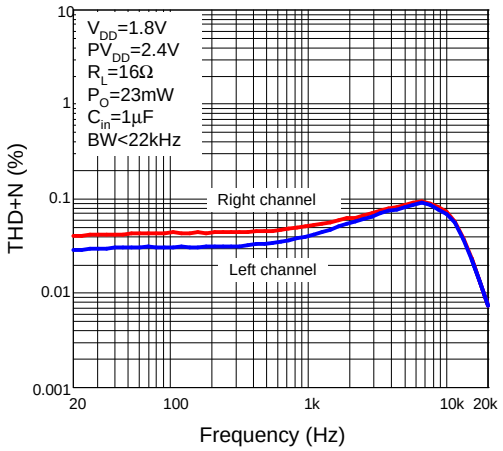
THD+N vs. Frequency



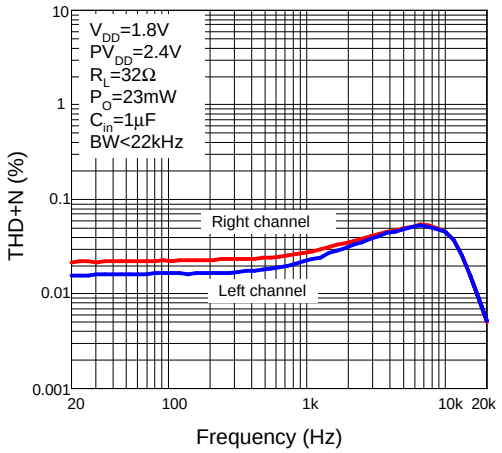
THD+N vs. Frequency



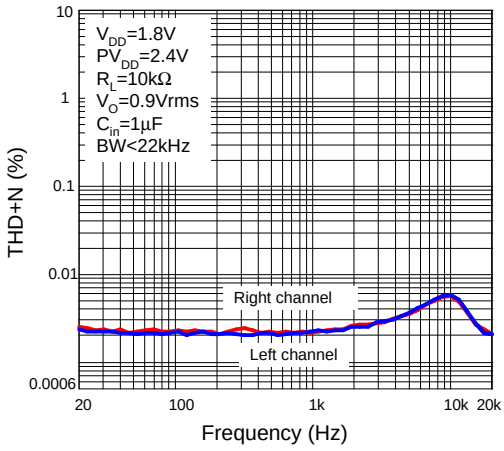
THD+N vs. Frequency



THD+N vs. Frequency



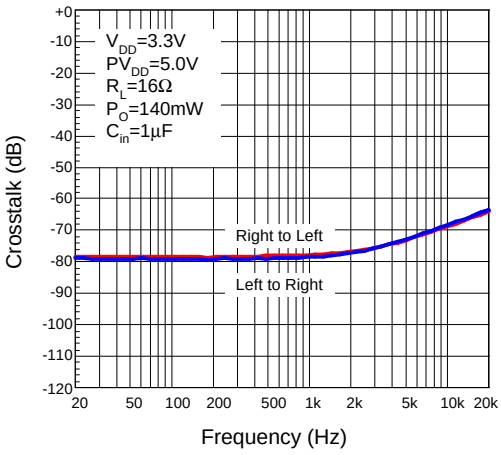
THD+N vs. Frequency



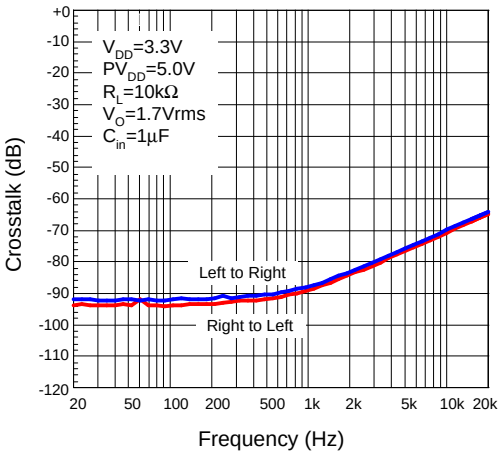
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Typical Operating Characteristics (Cont.)

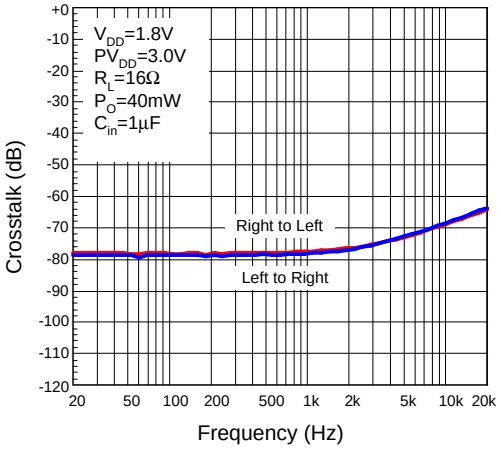
Crosstalk vs. Frequency



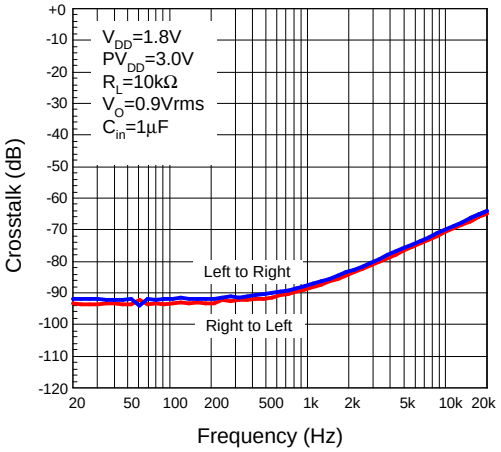
Crosstalk vs. Frequency



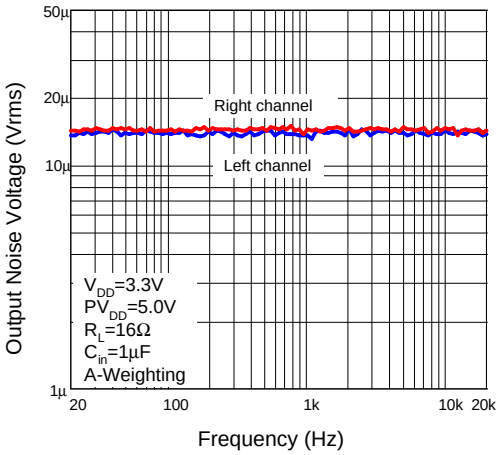
Crosstalk vs. Frequency



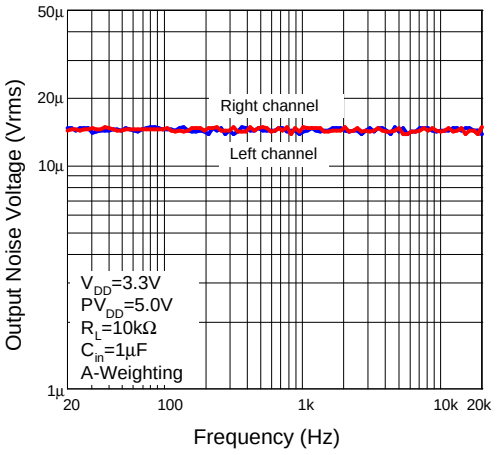
Crosstalk vs. Frequency



Output Noise Voltage vs. Frequency

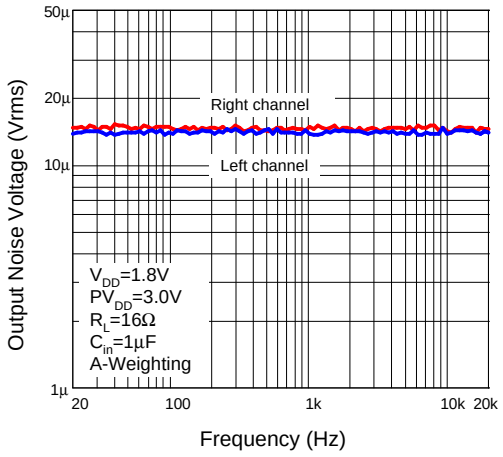


Output Noise Voltage vs. Frequency

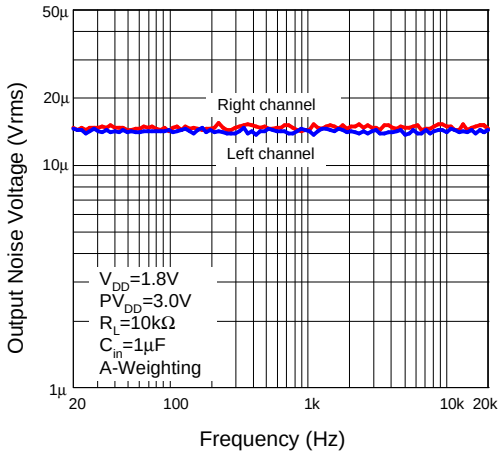


Typical Operating Characteristics (Cont.)

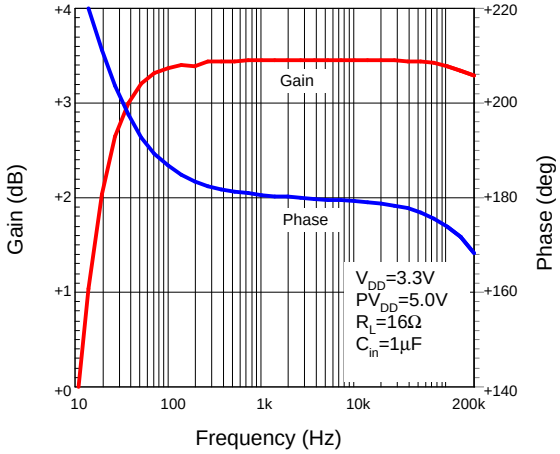
Output Noise Voltage vs. Frequency



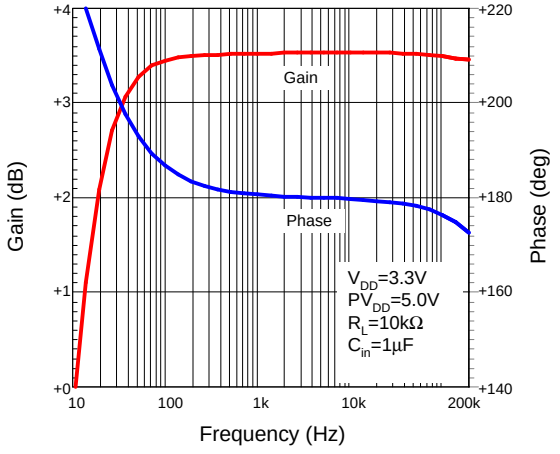
Output Noise Voltage vs. Frequency



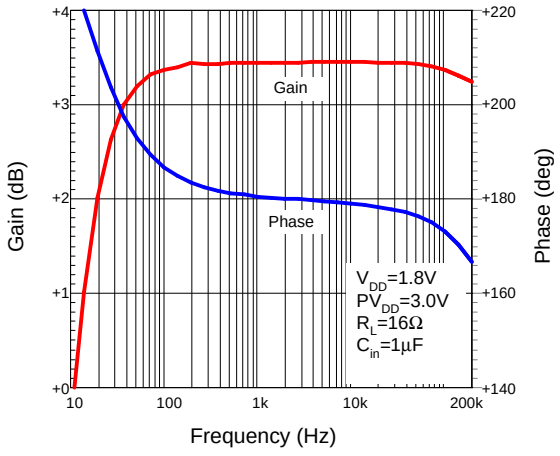
Frequency Response



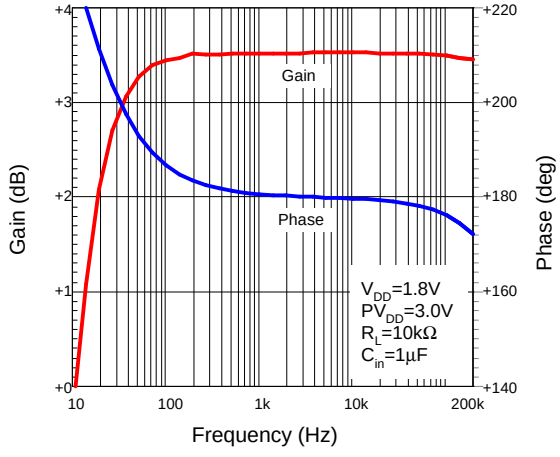
Frequency Response



Frequency Response

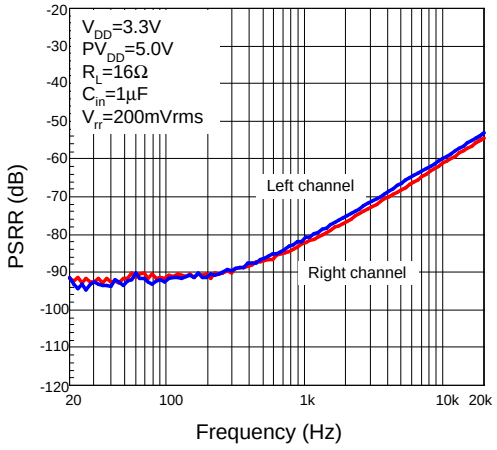


Frequency Response

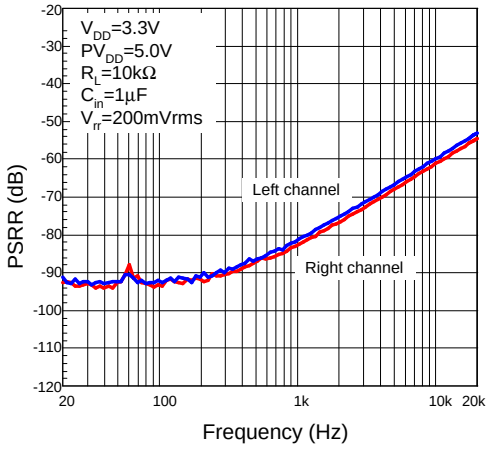


Typical Operating Characteristics (Cont.)

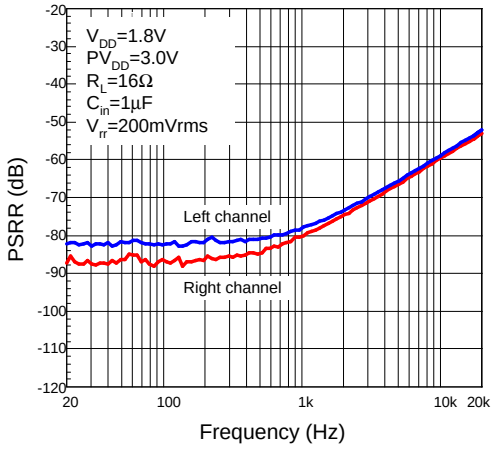
PSRR vs. Frequency



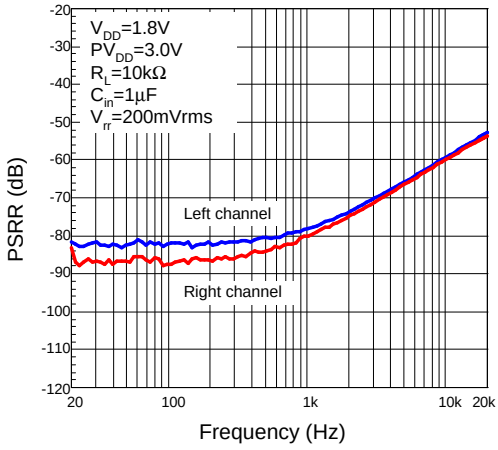
PSRR vs. Frequency



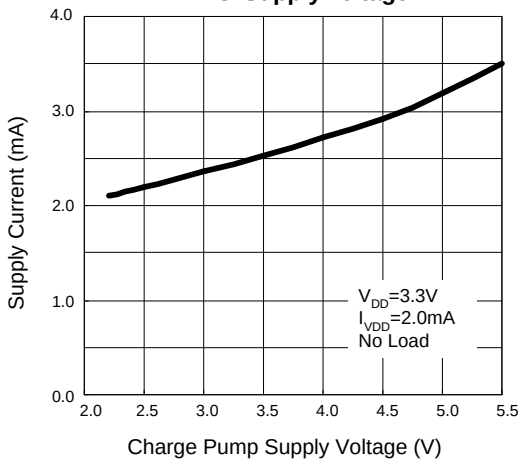
PSRR vs. Frequency



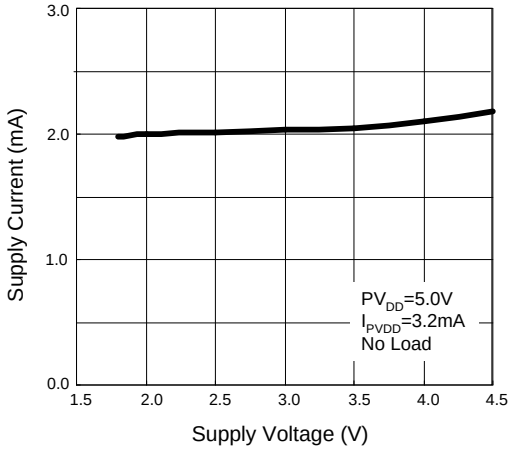
PSRR vs. Frequency



Charge Pump Supply Current vs. Supply Voltage



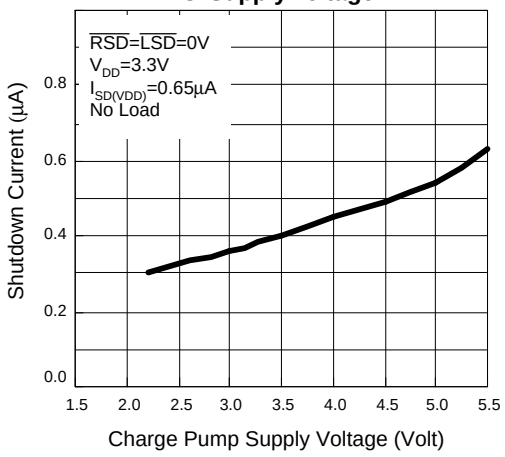
Supply Current vs. Supply Voltage



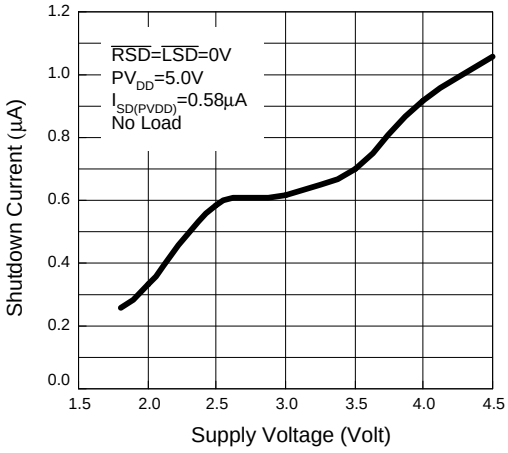
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Typical Operating Characteristics (Cont.)

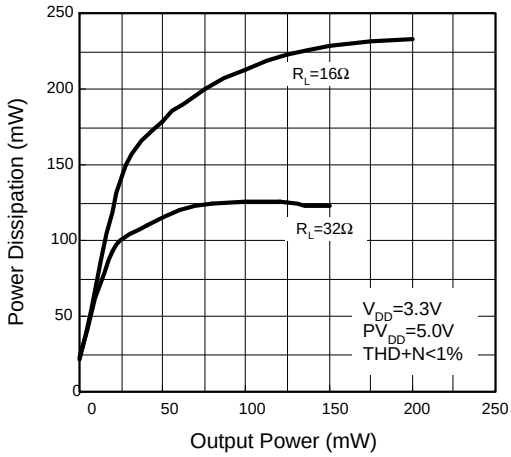
Charge Pump Shutdown Current vs. Supply Voltage



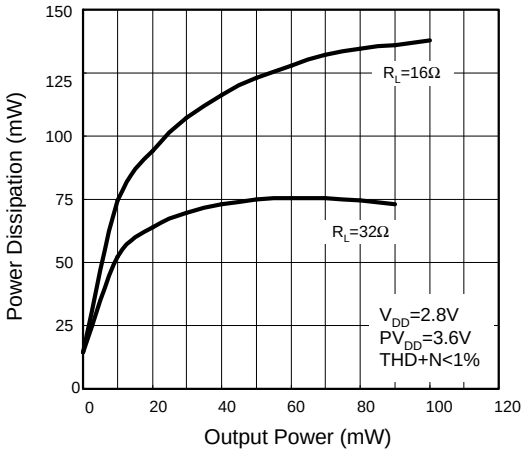
Shutdown Current vs. Supply Voltage



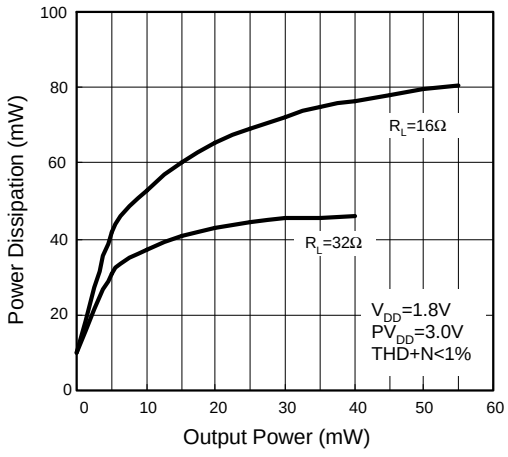
Power Dissipation vs. Output Power



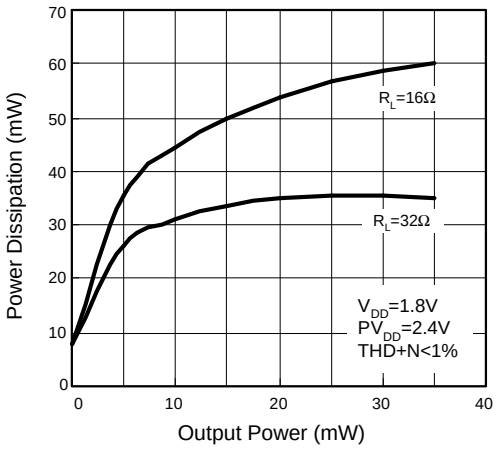
Power Dissipation vs. Output Power



Power Dissipation vs. Output Power

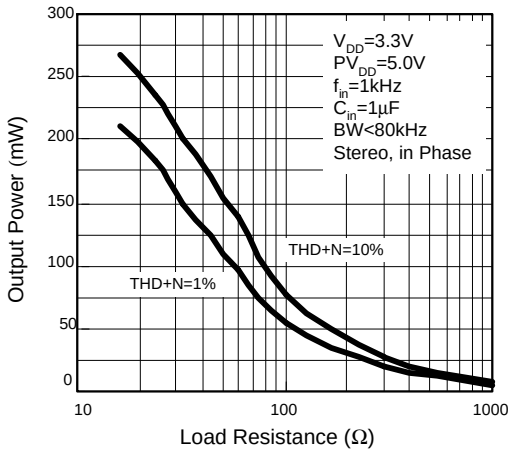


Power Dissipation vs. Output Power

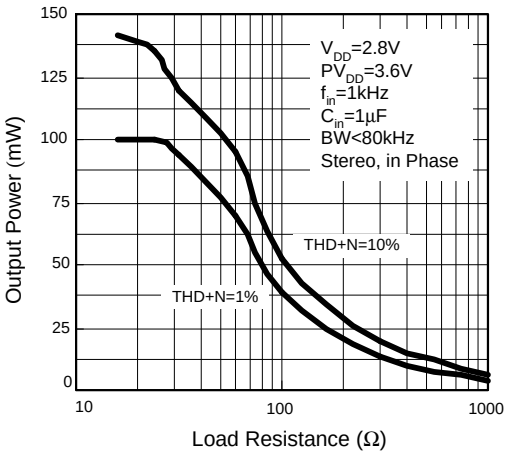


Typical Operating Characteristics (Cont.)

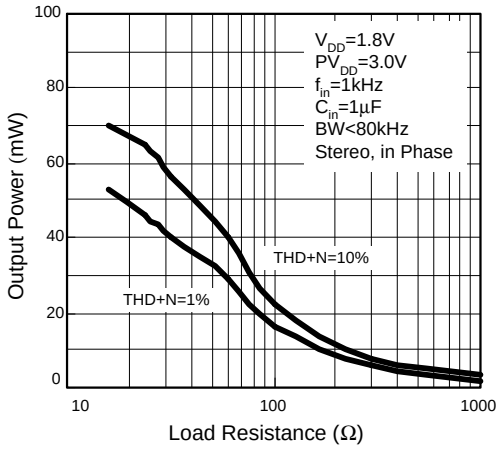
Output Power vs. Load Resistance



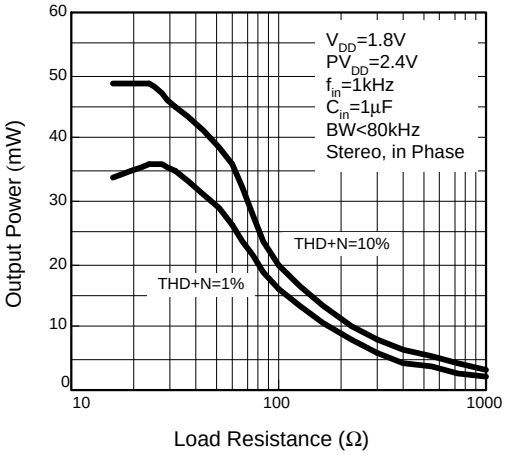
Output Power vs. Load Resistance



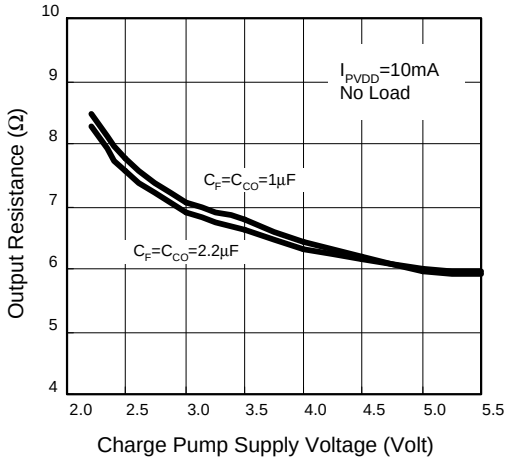
Output Power vs. Load Resistance



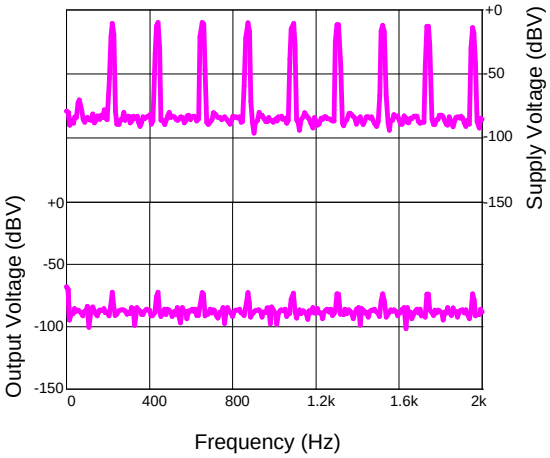
Output Power vs. Load Resistance



Charge Pump Output Resistance vs. Supply Voltage

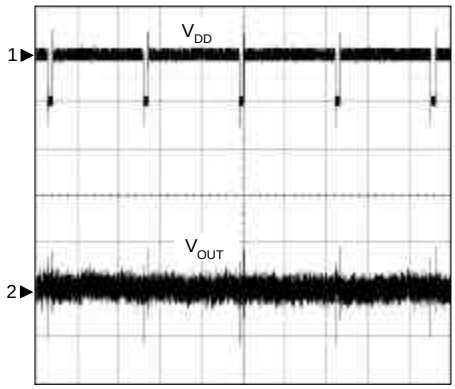


GSM Power Supply Rejection vs.Frequency



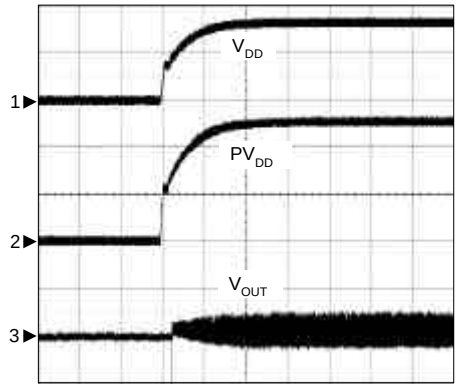
Operating Waveforms

GSM Power Supply Rejection vs. Time



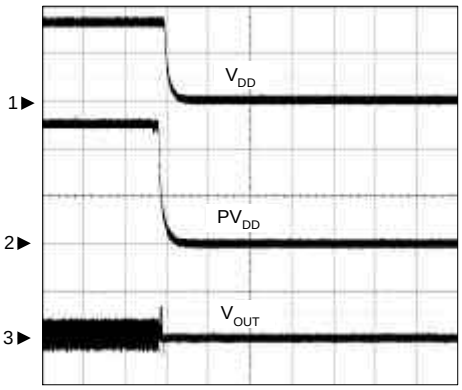
CH1: V_{DD}, 500mV/Div, DC
V_{DD} Offset = 3.3V
CH2: V_{OUT} , 20mV/Div, DC
TIME: 20ms/Div

Output Transient at Turn on



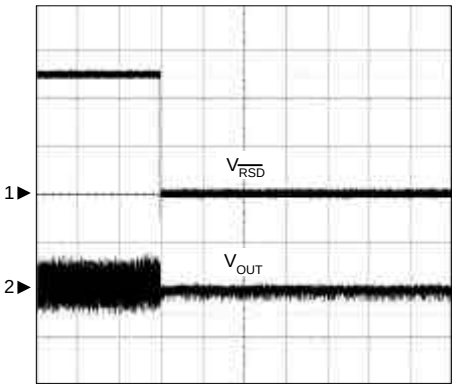
CH1: V_{DD}, 2V/Div, DC
CH2: PV_{DD}, 2V/Div, DC
CH3: V_{OUT}, 20mV/Div, DC
TIME: 5ms/Div

Output Transient at Power off



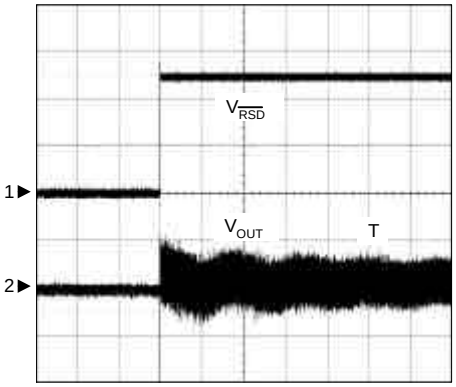
CH1: V_{DD}, 2V/Div, DC
CH2: PV_{DD}, 2V/Div, DC
CH3: V_{OUT}, 20mV/Div, DC
TIME: 100ms/Div

Output Transient at Shutdown Active



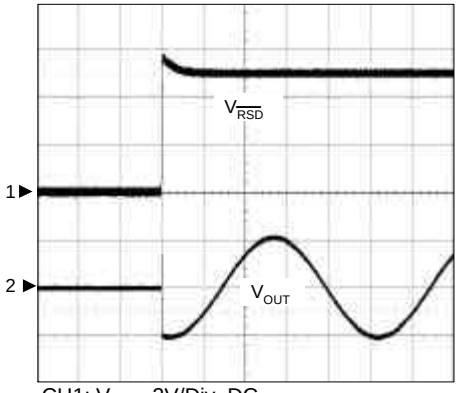
CH1: $V_{\overline{RSD}}$, 2V/Div, DC
CH2: V_{OUT}, 20mV/Div, DC
TIME: 20ms/Div

Output Transient at Shutdown Release



CH1: $V_{\overline{RSD}}$, 2V/Div, DC
CH2: V_{OUT}, 20mV/Div, DC
TIME: 20ms/Div

Shutdown Release

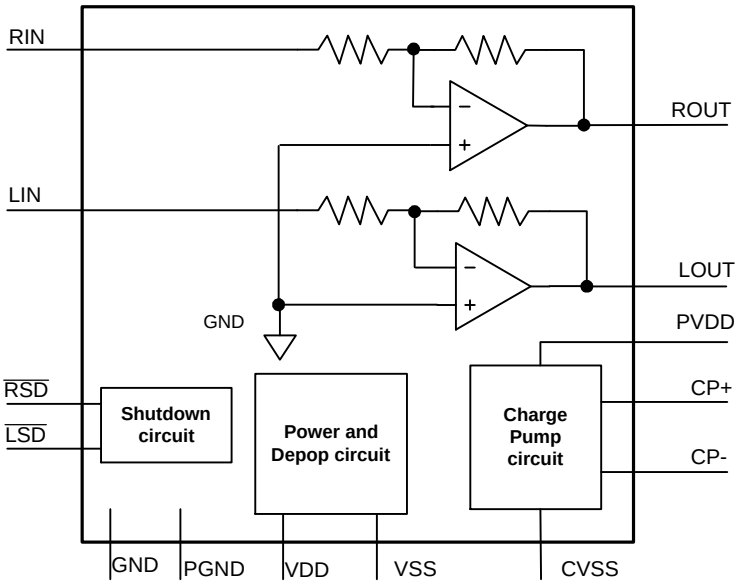


CH1: $V_{\overline{RSD}}$, 2V/Div, DC
CH2: V_{OUT}, 1V/Div, DC
TIME: 200µs/Div

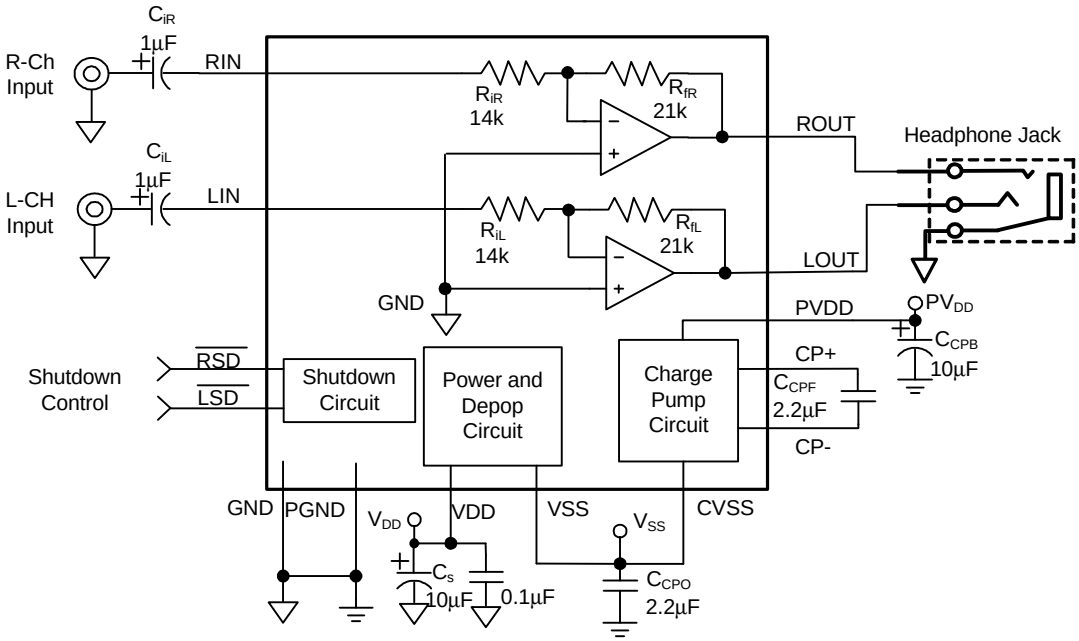
Pin Description

PIN				FUNCTION
NO.			NAME	
TQFN4x4-20B	TSSOP-16	TQFN3x3-16 (FOR APA2176A)		
1	4	1	CP+	Charge pump flying capacitor positive connection.
2	5	2	PGND	Charge pump ground.
3	6	3	CP-	Charge pump flying capacitor negative connection.
4, 6, 8, 12, 16, 20	1, 3	4, 13	NC	No Connection.
5	7	5	CVSS	Charge pump output.
7	8	6	VSS	Connect this pin to CVSS.
9	9	7	LOUT	Left channel output for headphone.
10	10	8	VDD	Supply voltage input pin.
11	11	9	ROUT	Right channel output for headphone.
13	12	10	LIN	Left channel audio signal input pin.
14	13	11	$\overline{RSD}$	Right channel shutdown mode control pin. A low-level voltage applied on this pin shuts off the right channel headphone driver.
15	14	12	RIN	Right channel audio signal input pin.
17	15	14	GND	Ground connection for circuitry.
18	16	15	$\overline{LSD}$	Left channel shutdown mode control pin. A low-level voltage applied on this pin shuts off the left channel headphone driver.
19	2	16	PVDD	Charge pump power supply voltage input pin.

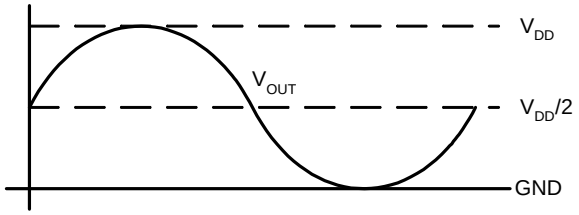
Block Diagram



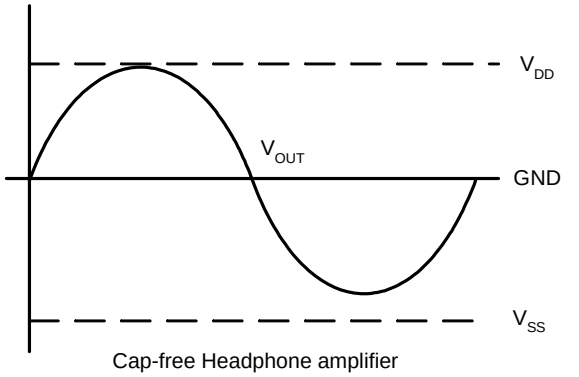
Typical Application Circuit



Function Description



Conventional Headphone amplifier



Cap-free Headphone amplifier

Figure 1. Cap-Free Operation

The APA2176/2176A is a stereo, fixed gain, cap-free headphone driver. The gain is set by internal resistors, input resistors (R_i), and feedback resistors (R_f) with -1.5V/V (See Typical Application Circuit).

The APA2176/2176A's headphone drivers use a charge pump to invert the positive power supply (PV_{DD}) to negative power supply (CV_{SS}), see figure1. The headphone drivers operate at this bipolar power supply (V_{DD} and V_{SS}) and the outputs reference refers to the ground. This feature eliminates the output capacitors which are used in conventional single-ended headphone amplifiers. Compared with the single power supply amplifiers, the power supply voltage is almost double.

Shutdown Function

In order to reduce power consumption, the APA2176/2176A contain two shutdown signal input pins ($\overline{LSD}$ for left channel and $\overline{RSD}$ for right channel) to allow respective shutdown which turns off the bias current of the amplifier. This shutdown feature turns the amplifier off when logic low is placed on the $\overline{RSD}$ or $\overline{LSD}$ pin for the APA2176/2176A. The trigger point between a logic high and logic low level is typically $0.6PV_{DD}$ and $0.3PV_{DD}$. It is highly recommended to switch between ground and the supply voltage PVDD to provide maximum device performance. By switching the both $\overline{RSD}$ and $\overline{LSD}$ pins to low level, the amplifier enters a low-consumption current circumstance, with charge pump disabled, and very small I_{DD} for the APA2176/2176A. The charge pump is enabled once either $\overline{RSD}$ or $\overline{LSD}$ pin is pulled to high. In normal operating, the APA2176/2176A's $\overline{RSD}$ and $\overline{LSD}$ pins should be pulled to high level to keep the IC out of the shutdown mode. The $\overline{RSD}$ and $\overline{LSD}$ pins should be tied to a definite voltage to avoid unwanted mode changing.

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Application Information

Charge Pump Flying Capacitor (C_{CPF})

The flying capacitor (C_{CPF}) affects the load transient of the charge pump. If the capacitor's value is too small, and then this increases charge pump's output resistance and degrades the performance of headphone amplifier.
Increasing the flying capacitor's value improves the load transient of charge pump. It is recommended to use the low ESR ceramic capacitors (X7R type is recommended) above 2.2µF.

Charge Pump Output Capacitor (C_{CPO})

The charge pump needs an output capacitor(C_{CPO}) to filter the negative output current pulse flowing into CVSS pin as well as reduces the output voltage ripple (CVSS). The capacitor also sucks in surge current flowing from the V_{SS} pin, the negative power input pin for the amplifiers. The output ripple is determined by the capacitance, ESR, and current ripple of the output capacitor. Increasing the value of output capacitor and decreasing the ESR can reduce the voltage ripple. Using a low-ESR ceramic capacitor greater than 2.2µF is recommended. For reducing the parasitic inductance and improving the noise decoupling, place the capacitor near the CVSS and the PGND pins as close as possible.

Charge Pump Bypass Capacitor (C_{CPB})

The bypass capacitor(C_{CPB}) connected with PV_{DD} pin supplies the charge pump with surge current as well as reduces the voltage ripple on PV_{DD} pin. Using a low-ESR ceramic capacitor 10µF(typical) is recommended. For reducing the parasitic inductance and improving the noise decoupling, place the capacitor near the PV_{DD} and the PGND pins as close as possible.

Input Capacitor (C_i)

In the typical application, an input capacitor (C_i) is required to allow the amplifier to bias the input signal to the proper DC level for optimum operation. In this case, C_i and the input impedance R_i from a high-pass filter with the cutoff frequency are determined in the following equation:

$$f_{C(highpass)} = \frac{1}{2\pi R_i C_i} \quad (1)$$

The value of C_i is important to consider carefully because it directly affects the low frequency performance of the circuit. Consider the example where R_i is 14kΩ and the specification that calls for a flat bass response down to 10Hz. The equation is reconfigured as below:

$$C_i = \frac{1}{2\pi R_i f_C} \quad (2)$$

When the input resistance variation is considered, the C_i is 1µF. Therefore, a value in the range of 1µF to 2.2µF would be chosen. A further consideration for this capacitor is the leakage path from the input source through the input network (R_i + R_f, C_i) to the load.
This leakage current creates a DC offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason, a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the negative side of the capacitor should face the amplifiers' inputs in most applications because the DC level of the amplifiers' inputs are held at 0V. Please note that it is important to confirm the capacitor polarity in the application.

Power Supply Decoupling (C_s)

The APA2176/2176A is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD+N) as low as possible. Power supply decoupling also prevents the oscillations caused by long lead length between the amplifier and the speaker.
The optimum decoupling is achieved by using two different types of capacitor that targets on different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series- resistance (ESR) ceramic capacitor, typically 0.1µF, is placed as close as possible to the device VDD lead for the best performance. For filtering lower frequency noise signals, a large aluminum electrolytic capacitor of 10µF or greater placed near the audio power amplifier is recommended.

Thermal Consideration

Linear power amplifiers dissipate a significant amount of heat in the package in normal operating condition. The

Application Information (Cont.)

Thermal Consideration (Cont.)

first consideration to calculate maximum ambient temperatures is the numbers from the Power Dissipation vs. Output Power graphs are per channel values, therefore, the dissipation of the IC heat needs to be doubled for two-channel operation. Given θ_{JA}, the maximum allowable junction temperature (T_{JMax}), the total internal dissipation (P_D), and the maximum ambient temperature can be calculated with the following equation. The maximum recommended junction temperature for the APA2176/2176A is 150°C. The internal dissipation figures are taken from the Power Dissipation vs. Output Power graphs. The APA2176/2176A is designed with a thermal shutdown protection that turns the device off when the junction temperature surpasses 150°C to prevent damaging the IC.

Layout Consideration

1. All components should be placed close to the APA2176/2176A. For example, the input capacitor (C_i) should be close to APA2176/2176A's input pins to avoid causing noise coupling to APA2176/2176A's high impedance inputs; the decoupling capacitor (C_S) should be placed by the APA2176/2176A's power pin to decouple the power rail noise.
2. The output traces should be short, wide (>50mil), and symmetric.
3. The input trace should be short and symmetric.
4. The power trace width should be greater than 50mil.
5. The TQFN Thermal PAD should be soldered on PCB, and the ground plane needs soldered mask (to avoid short circuit) except the Thermal PAD area.

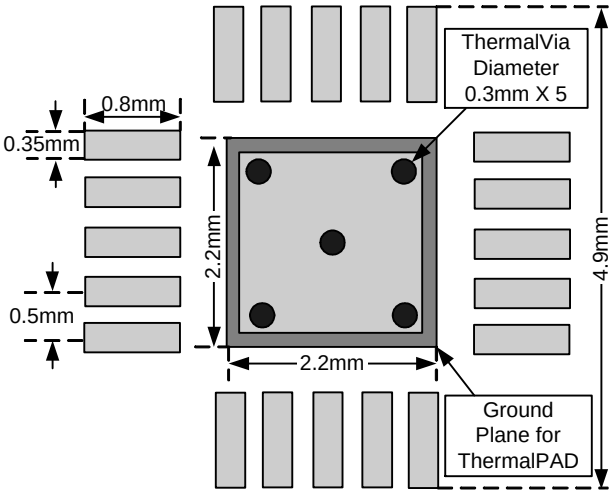


Figure 2. TQFN4x4-20B Layout Recommendation

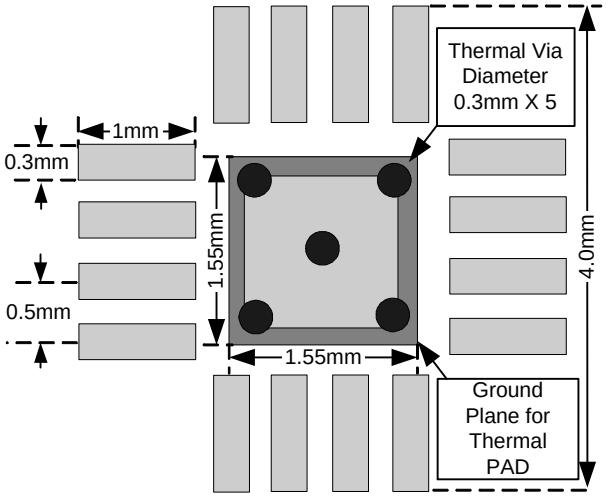
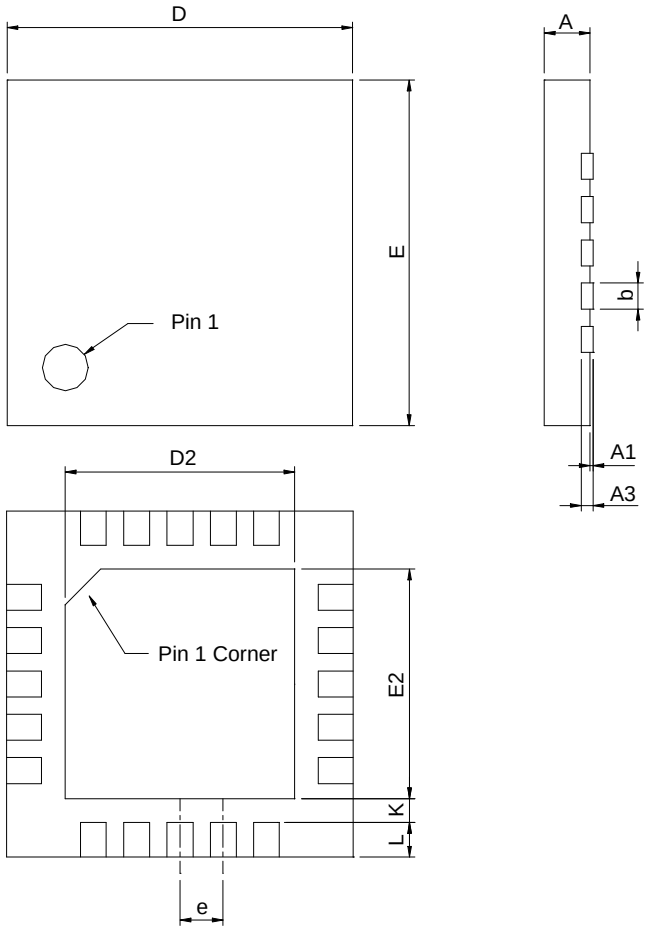


Figure 3. TQFN3x3-16 Layout Recommendation

Package Information

TQFN4x4-20B



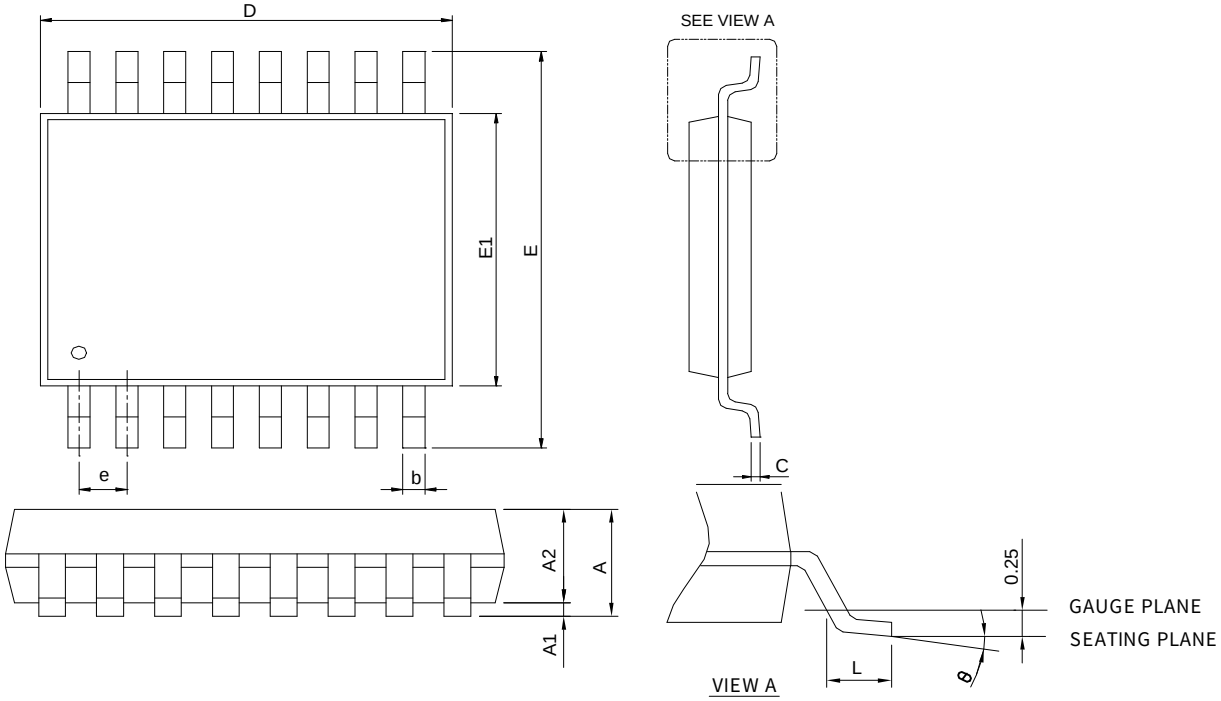
SYMBOL	TQFN4x4-20B			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.008	0.012
D	3.90	4.10	0.154	0.161
D2	2.00	2.70	0.079	0.106
E	3.90	4.10	0.154	0.161
E2	2.00	2.70	0.079	0.106
e	0.50 BSC		0.020 BSC	
L	0.35	0.45	0.014	0.018
K	0.20		0.008	

Note : 1. Followed from JEDEC MO-220 VGGD-5.

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Package Information

TSSOP-16

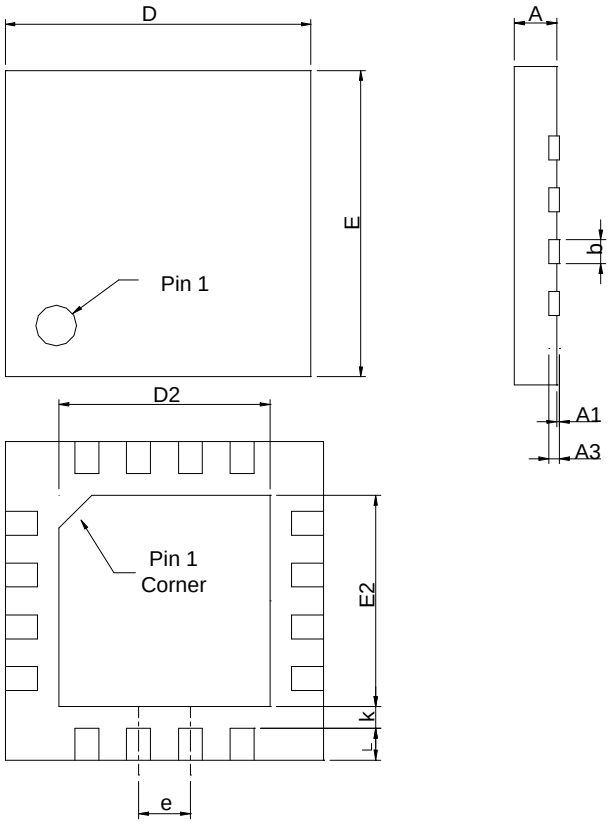


SYMBOL	TSSOP-16			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.20		0.047
A1	0.05	0.15	0.002	0.006
A2	0.80	1.05	0.031	0.041
b	0.19	0.30	0.007	0.012
c	0.09	0.20	0.004	0.008
D	4.90	5.10	0.193	0.201
E	6.20	6.60	0.244	0.260
E1	4.30	4.50	0.169	0.177
e	0.65 BSC		0.026 BSC	
L	0.45	0.75	0.018	0.030
θ	0°	8°	0°	8°

Note : 1. Follow from JEDEC MO-153 AB.
2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.
3. Dimension "E1" does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 10 mil per side.

Package Information

TQFN3x3-16

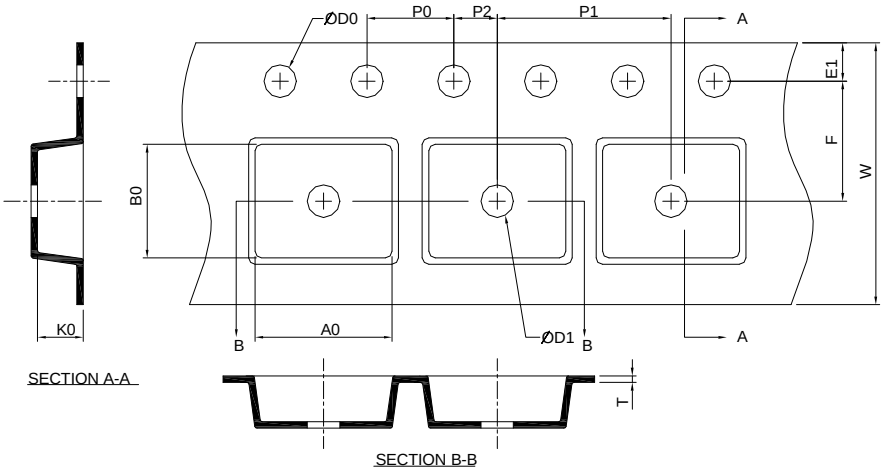


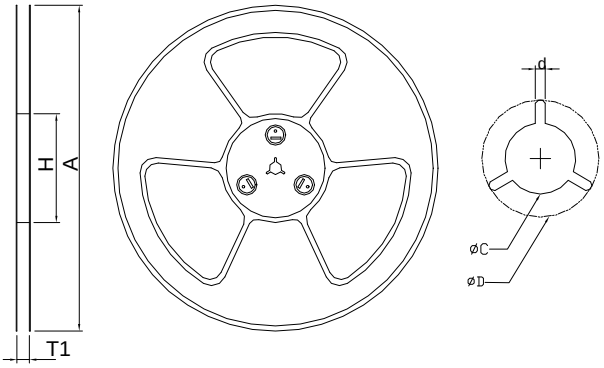
SYMBOL	TQFN3x3-16			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.007	0.012
D	2.90	3.10	0.114	0.122
D2	1.50	1.80	0.059	0.071
E	2.90	3.10	0.114	0.122
E2	1.50	1.80	0.059	0.071
e	0.50 BSC		0.020 BSC	
L	0.30	0.50	0.012	0.020
K	0.20		0.008	

Note : Follow JEDEC MO-220 WEED-4.

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Carrier Tape & Reel Dimensions





Application	A	H	T1	C	d	D	W	E1	F
TQFN4x4-20B	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	4.30±0.20	4.30±0.20	1.30±0.20
Application	**A**	**H**	**T1**	**C**	**d**	**D**	**W**	**E1**	**F**
TSSOP-16	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.50±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.00±0.10	8.00±0.10	2.00±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	6.90±0.20	5.40±0.20	1.60±0.20
Application	**A**	**H**	**T1**	**C**	**d**	**D**	**W**	**E1**	**F**
TQFN3x3-16	330±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	3.30±0.20	3.30±0.20	1.30±0.20

(mm)

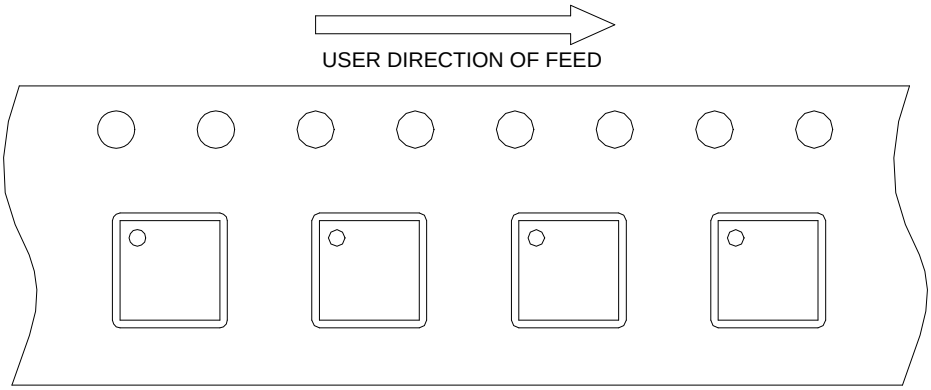
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Devices Per Unit

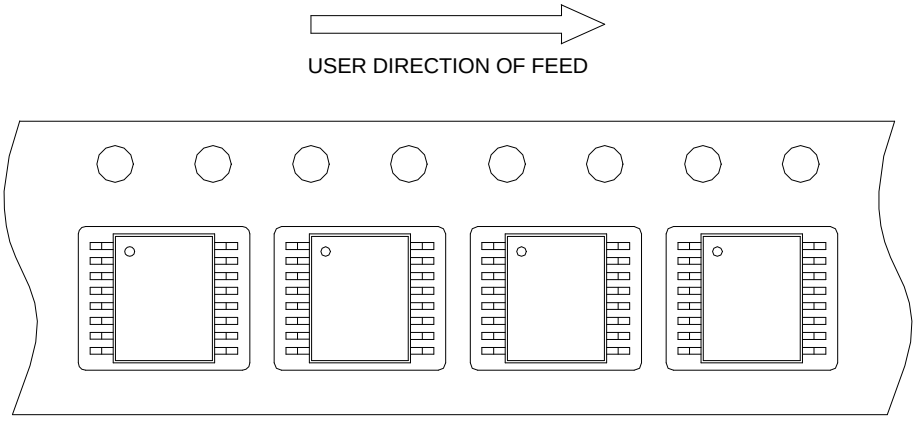
Package Type	Unit	Quantity
TQFN4x4-20B	Tape & Reel	3000
TSSOP-16	Tape & Reel	2500
TQFN3x3-16	Tape & Reel	3000

Taping Direction Information

TQFN4x4-20B

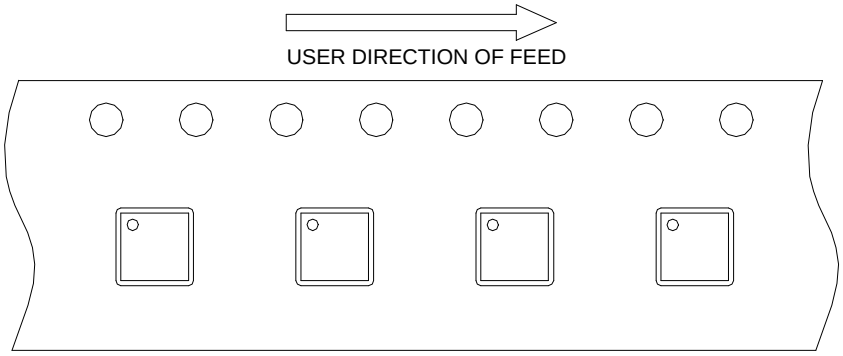


TSSOP-16

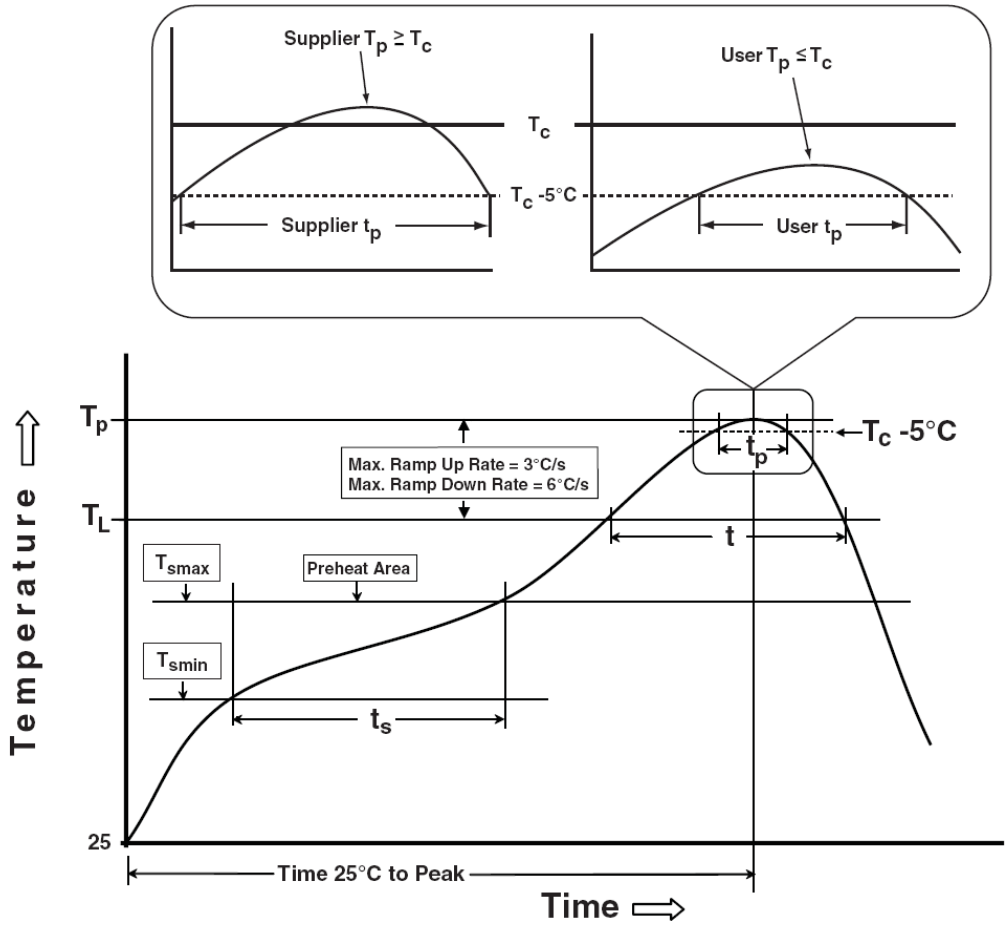


Taping Direction Information (Cont.)

TQFN3x3-16



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ³350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_j=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

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