

## Two Channel, Five Level, High Speed Ultrasound Driver IC

### Features

- ▶ Advanced CMOS technology
- ▶  $\pm 4.75$  to 12.9V gate drive voltage
- ▶ 2A output source and sink current
- ▶ 6.5ns rise and fall time with 1nF load
- ▶ 10ns propagation delay
- ▶  $\pm 2$ ns matched delay times
- ▶ 12 matched channels
- ▶ 1.8V to 3.3V CMOS logic interface
- ▶ Smart logic threshold
- ▶ Low inductance package

### Applications

- ▶ Medical ultrasound imaging
- ▶ Piezoelectric transducer drivers
- ▶ Metal flaw detection
- ▶ Non-Destructive Testing (NDT)

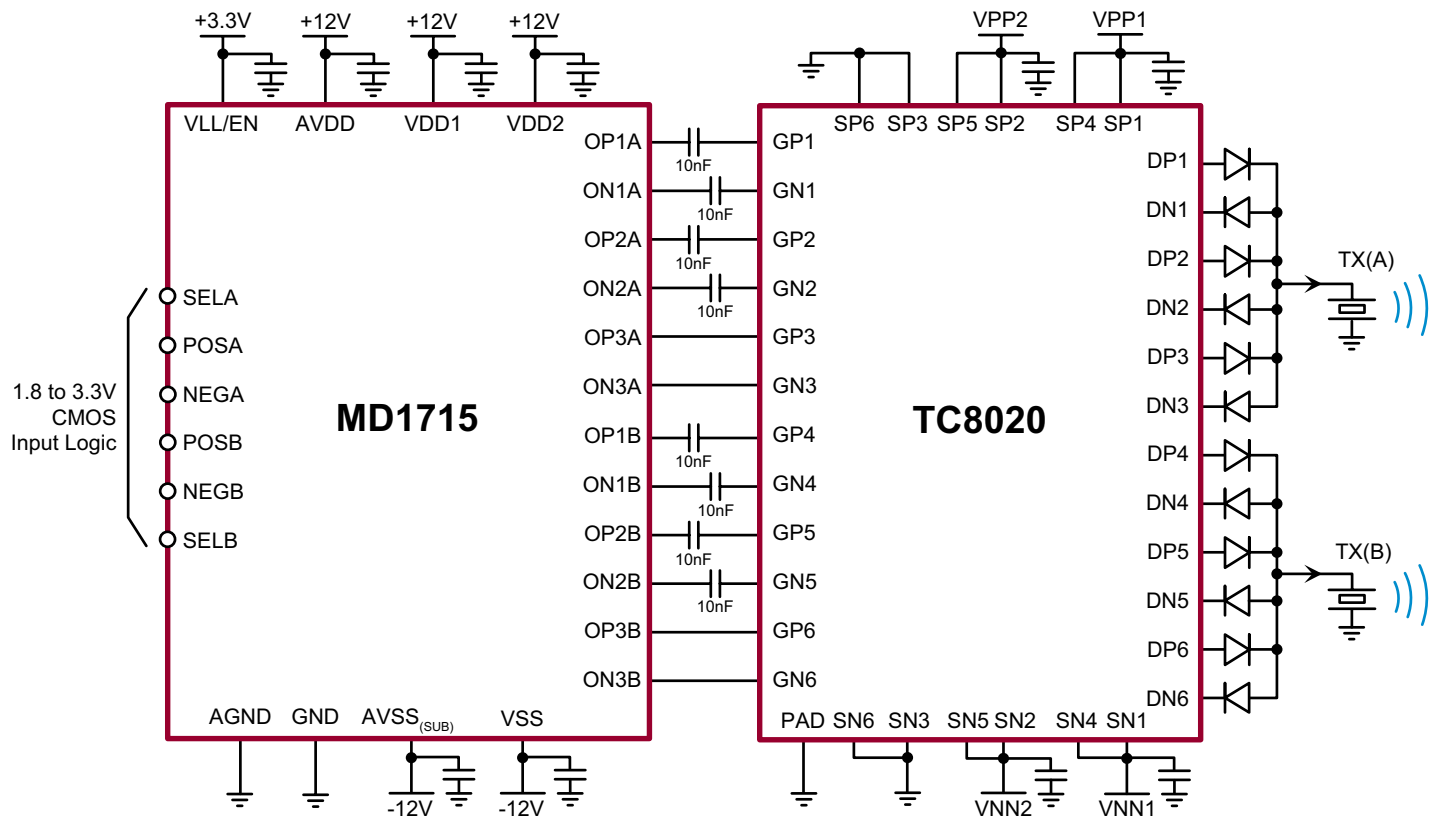
### General Description

The Supertex MD1715, paired with the Supertex TC8020, forms a two channel, five level, high voltage, high speed transmit pulser chip set. The chip set is designed for medical ultrasound imaging applications, but can also be used for metal flaw detection, Non-Destructive Testing (NDT), and piezoelectric transducer drivers.

The MD1715 is a two channel logic controller circuit with 12 low impedance MOSFET gate drivers. There are two sets of control logic inputs, one each for channels A and B. Each channel consists of three pairs of MOSFET gate drivers. These drivers are designed to match the drive requirements of the Supertex TC8020.

The TC8020 is the output stage of the pulser, with six pairs of MOSFETs. Each pair consists of a P-channel and an N-channel MOSFET. They are designed to have the same impedance and can provide typical peak currents of  $\pm 3.5$  amps at 200V.

### Typical Application Circuit



## Ordering Information

| Device | Package Option                                                        |
|--------|-----------------------------------------------------------------------|
|        | 40-Lead QFN<br>6.00x6.00mm body<br>1.0mm height (max)<br>0.50mm pitch |
| MD1715 | MD1715K6-G                                                            |

-G indicates package is RoHS compliant ("Green")



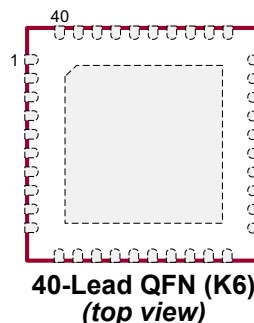
## Absolute Maximum Ratings

| Parameter                                          | Value           |
|----------------------------------------------------|-----------------|
| GND and AGND, Ground                               | 0V              |
| $V_{LL}$ logic input pin                           | -0.5V to +5.5V  |
| $AV_{DD}$ , $V_{DD1}$ , positive gate drive supply | -0.5V to +14.5V |
| $V_{DD2}$ , positive gate drive supply             | -0.5V to +14.5V |
| $AV_{SS}$ , $V_{SS}$ , negative gate drive supply  | -14.5V to +0.5V |
| Storage temperature                                | -65°C to 150°C  |
| Power dissipation*                                 | 1.3W            |

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

\* 1.0oz 4-layer 3x4" PCB

## Pin Configuration



## Package Marking

MD1715  
LLLLLL  
YYWW  
AAA CCC

L = Lot Number  
YY = Year Sealed  
WW = Week Sealed  
A = Assembler ID  
C = Country of Origin  
— = "Green" Packaging

Package may or may not include the following marks: Si or

40-Lead QFN (K6)

## Operating Supply Voltages

| Sym                   | Parameter                  | Min   | Typ | Max   | Units | Conditions                                   |
|-----------------------|----------------------------|-------|-----|-------|-------|----------------------------------------------|
| $V_{LL}$              | Logic supply               | 1.8   | 3.3 | 3.6   | V     | ---                                          |
| $AV_{DD}$             | Positive analog supply     | 8.0   | -   | 12.9  | V     | $AV_{DD} \geq (V_{DD1} \text{ or } V_{DD2})$ |
| $V_{DD2}$ , $V_{DD1}$ | Positive gate drive supply | 4.75  | -   | 12.9  | V     | ---                                          |
| $AV_{SS}$ , $V_{SS}$  | Negative gate drive supply | -12.9 | -   | -4.75 | V     | ---                                          |

## Operating Supply Current

(Over operating conditions unless otherwise specified,  $V_{LL} = 3.3V$ ,  $AV_{DD} = V_{DD1} = V_{DD2} = +12V$ ,  $AV_{SS} = V_{SS} = -12V$ ,  $T_A = 25^\circ C$ )

| Sym                | Parameter                           | Min | Typ | Max | Units | Conditions              |
|--------------------|-------------------------------------|-----|-----|-----|-------|-------------------------|
| I <sub>VLL</sub>   | Logic reference current             |     | 10  |     | μA    | V <sub>LL</sub> = 3.3V  |
| I <sub>AVDDQ</sub> | AV <sub>DD</sub> power down current | -   | 0.4 | -   | mA    | EN = 0, all inputs Low. |
| I <sub>VSSQ</sub>  | V <sub>VSS</sub> power down current | -   | 0.1 | -   |       |                         |
| I <sub>VDD1Q</sub> | V <sub>DD1</sub> power down current | -   | 10  | 25  | μA    |                         |
| I <sub>VDD2Q</sub> | V <sub>DD2</sub> power down current | -   | 10  | 25  |       |                         |

## Operating Supply Current

(Over operating conditions unless otherwise specified,  $V_{LL} = 3.3V$ ,  $AV_{DD} = V_{DD1} = V_{DD2} = +12V$ ,  $AV_{SS} = V_{SS} = -12V$ ,  $T_A = 25^\circ C$ )

| Sym          | Parameter                  | Min | Typ | Max | Units   | Conditions                                                              |
|--------------|----------------------------|-----|-----|-----|---------|-------------------------------------------------------------------------|
| $I_{AVDDEN}$ | $AV_{DD}$ power up current | -   | 2.0 | 3.0 | mA      | EN = 1, all inputs low.                                                 |
| $I_{VSSSEN}$ | $V_{SS}$ power up current  | -   | 0.7 | 1.0 | mA      |                                                                         |
| $I_{VDD1EN}$ | $V_{DD1}$ power up current | -   | 10  | -   | $\mu A$ |                                                                         |
| $I_{VDD2EN}$ | $V_{DD2}$ power up current | -   | 10  | -   | $\mu A$ |                                                                         |
| $I_{AVDDCW}$ | $AV_{DD}$ CW 5MHz current  | -   | 10  | -   | mA      | A&B channel on at 5.0MHz no load,<br>$V_{DD1} = 12V$ , $V_{DD2} = 5.0V$ |
| $I_{VSSCW}$  | $V_{SS}$ CW 5MHz current   | -   | 5.0 | -   |         |                                                                         |
| $I_{VDD1CW}$ | $V_{DD1}$ CW 5MHz current  | -   | 25  | -   | mA      | A&B channel on at 5.0MHz no load,<br>$V_{DD1} = 5.0V$ , $V_{DD2} = 12V$ |
| $I_{VDD2CW}$ | $V_{DD2}$ CW 5MHz current  | -   | 25  | -   | mA      | A&B channel on at 5.0MHz no load,<br>$V_{DD1} = 12V$ , $V_{DD2} = 5.0V$ |

## AC Electrical Characteristics

(Over operating conditions unless otherwise specified,  $V_{LL} = 3.3V$ ,  $AV_{DD} = V_{DD1} = V_{DD2} = +12V$ ,  $AV_{SS} = V_{SS} = -12V$ ,  $T_A = 25^\circ C$ )

| Sym                 | Parameter                           | Min | Typ       | Max | Units   | Conditions                                                      |
|---------------------|-------------------------------------|-----|-----------|-----|---------|-----------------------------------------------------------------|
| $t_{irf}$           | Input rise & fall time              | -   | -         | 10  | ns      | Logic input edge speed requirement                              |
| $t_r$               | Output rise time                    | -   | 6.5       | -   | ns      | 1nF load, see timing diagram, input signal rise/fall time 2.0ns |
| $t_f$               | Output fall time                    | -   | 6.5       | -   | ns      | ---                                                             |
| $t_{dr}$            | Output rise delay                   | -   | 10        | -   | ns      | ---                                                             |
| $t_{df}$            | Output fall delay                   | -   | 10        | -   | ns      | ---                                                             |
| $ t_r - t_f $       | Rise and fall time matching         | -   | 1.0       | -   | -       | For each channel                                                |
| $ t_{dr} - t_{df} $ | Propagation delay matching          | -   | 1.0       | -   | -       | ---                                                             |
| $t_{dm}$            | Delay time matching                 | -   | $\pm 2.0$ | -   | ns      | Ch to Ch and Device to Device                                   |
| $\Delta t_j$        | Output jitter                       | -   | 20        | -   | ps      | $V_{DD} = 10V$                                                  |
| $t_{EN\_ON}$        | IC enable time                      | -   | 25        | 50  | $\mu s$ | ---                                                             |
| $t_{EN\_OFF}$       | IC disable time                     | -   | 0.5       | 2.0 | $\mu s$ | ---                                                             |
| HD2                 | 2 <sup>nd</sup> harmonic distortion | -40 | -         | -   | dB      | ---                                                             |

## P-Channel Gate Driver Outputs

| Sym          | Parameter                  | Min | Typ | Max | Units    | Conditions           |
|--------------|----------------------------|-----|-----|-----|----------|----------------------|
| $R_{SINK}$   | Output sink resistance     | -   | 5.0 | 6.0 | $\Omega$ | $I_{SINK} = 100mA$   |
| $R_{SOURCE}$ | Output source resistance   | -   | 5.0 | 6.0 | $\Omega$ | $I_{SOURCE} = 100mA$ |
| $I_{SINK}$   | Peak output sink current   | 1.7 | 2.0 | -   | A        | ---                  |
| $I_{SOURCE}$ | Peak output source current | 1.7 | 2.0 | -   | A        | ---                  |

## N-Channel Gate Driver Outputs

| Sym          | Parameter                  | Min | Typ | Max | Units    | Conditions           |
|--------------|----------------------------|-----|-----|-----|----------|----------------------|
| $R_{SINK}$   | Output sink resistance     | -   | 5.0 | 6.0 | $\Omega$ | $I_{SINK} = 100mA$   |
| $R_{SOURCE}$ | Output source resistance   | -   | 5.0 | 6.0 | $\Omega$ | $I_{SOURCE} = 100mA$ |
| $I_{SINK}$   | Peak output sink current   | 1.7 | 2.0 | -   | A        | ---                  |
| $I_{SOURCE}$ | Peak output source current | 1.7 | 2.0 | -   | A        | ---                  |

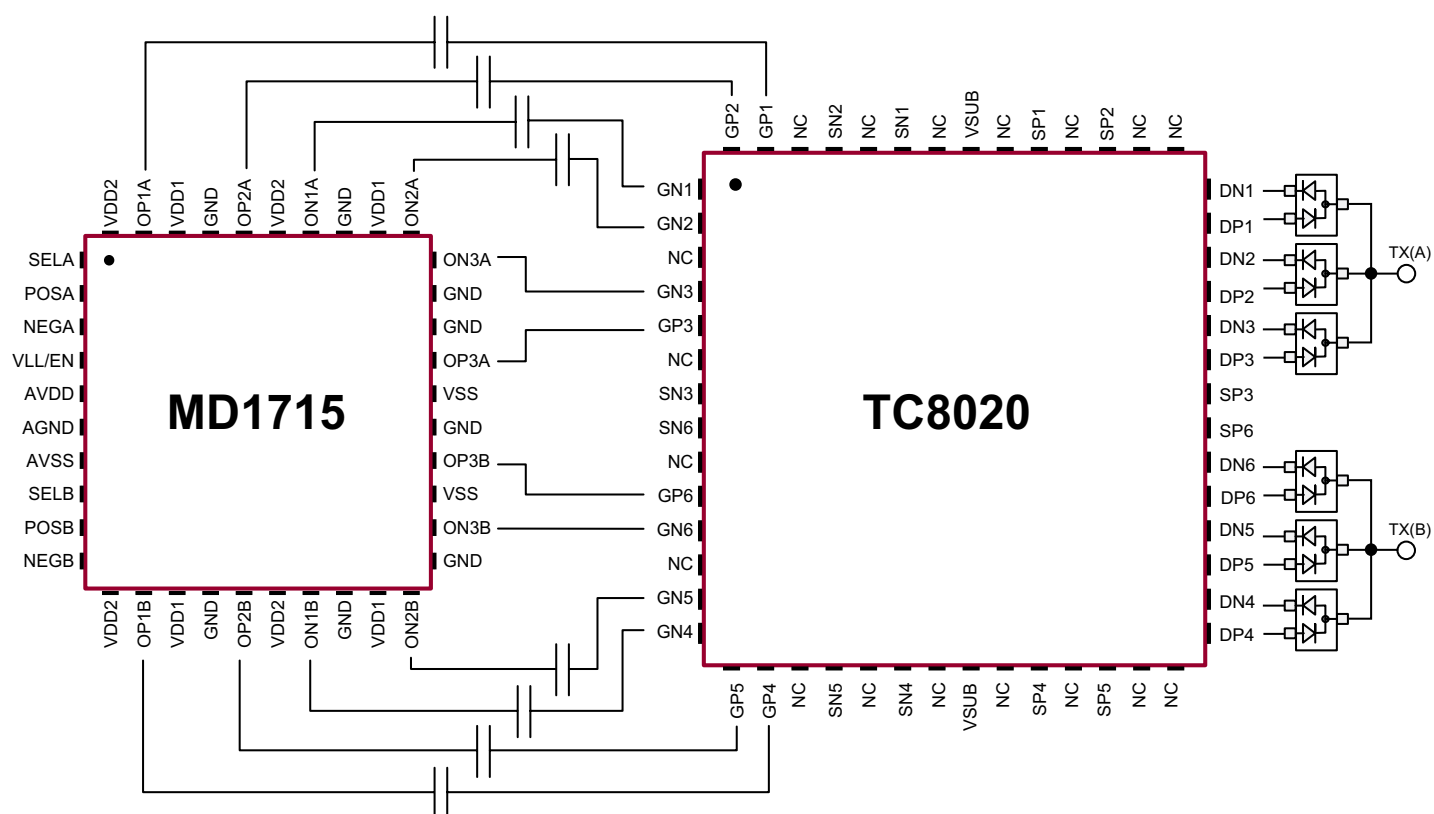
## Logic Inputs

| Sym       | Parameter                | Min         | Typ | Max         | Units   | Conditions                    |
|-----------|--------------------------|-------------|-----|-------------|---------|-------------------------------|
| $V_{ENL}$ | Chip disable low voltage | 0           | -   | 0.3         | V       | VLL/EN is a dual function pin |
| $V_{IH}$  | Input logic high voltage | $0.8V_{LL}$ | -   | $V_{LL}$    | V       | ---                           |
| $V_{IL}$  | Input logic low voltage  | 0           | -   | $0.2V_{LL}$ | V       | ---                           |
| $I_{IH}$  | Input logic high current | -           | -   | 1.0         | $\mu A$ | ---                           |
| $I_{IL}$  | Input logic low current  | -1.0        | -   | -           | $\mu A$ | ---                           |

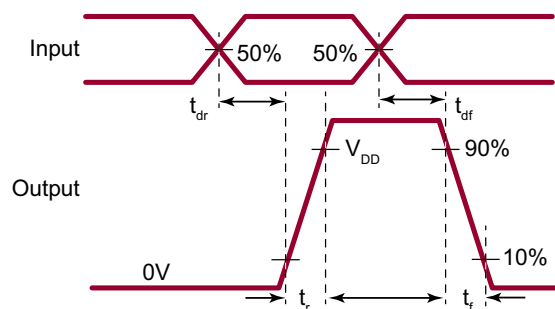
## Truth Table for Channels A and B

| EN  | Logic Inputs A |      |      | SP1<br>to<br>DP1                                                                     | SN1<br>to<br>DN1 | SP2<br>to<br>DP2 | SN2<br>to<br>DN2 | SP3<br>to<br>DP3 | SN3<br>to<br>DN3 |
|-----|----------------|------|------|--------------------------------------------------------------------------------------|------------------|------------------|------------------|------------------|------------------|
|     | SELA           | POSA | NEGA |                                                                                      |                  |                  |                  |                  |                  |
| 1   | 0              | 0    | 0    | OFF                                                                                  | OFF              | OFF              | OFF              | ON               | ON               |
| 1   | 0              | 0    | 1    | OFF                                                                                  | OFF              | OFF              | ON               | OFF              | OFF              |
| 1   | 0              | 1    | 0    | OFF                                                                                  | OFF              | ON               | OFF              | OFF              | OFF              |
| 1   | 0              | 1    | 1    | OFF                                                                                  | OFF              | OFF              | OFF              | OFF              | OFF              |
| 1   | 1              | 0    | 0    | OFF                                                                                  | OFF              | OFF              | OFF              | ON               | ON               |
| 1   | 1              | 0    | 1    | OFF                                                                                  | ON               | OFF              | OFF              | OFF              | OFF              |
| 1   | 1              | 1    | 0    | ON                                                                                   | OFF              | OFF              | OFF              | OFF              | OFF              |
| 1   | 1              | 1    | 1    | OFF                                                                                  | OFF              | OFF              | OFF              | OFF              | OFF              |
| EN  | Logic Inputs B |      |      | SP4<br>to<br>DP4                                                                     | SN4<br>to<br>DN4 | SP5<br>to<br>DP5 | SN5<br>to<br>DN5 | SP6<br>to<br>DP6 | SN6<br>to<br>DN6 |
|     | SELB           | POSB | NEGB |                                                                                      |                  |                  |                  |                  |                  |
| 1   | 0              | 0    | 0    | OFF                                                                                  | OFF              | OFF              | OFF              | ON               | ON               |
| 1   | 0              | 0    | 1    | OFF                                                                                  | OFF              | OFF              | ON               | OFF              | OFF              |
| 1   | 0              | 1    | 0    | OFF                                                                                  | OFF              | ON               | OFF              | OFF              | OFF              |
| 1   | 0              | 1    | 1    | OFF                                                                                  | OFF              | OFF              | OFF              | OFF              | OFF              |
| 1   | 1              | 0    | 0    | OFF                                                                                  | OFF              | OFF              | OFF              | ON               | ON               |
| 1   | 1              | 0    | 1    | OFF                                                                                  | ON               | OFF              | OFF              | OFF              | OFF              |
| 1   | 1              | 1    | 0    | ON                                                                                   | OFF              | OFF              | OFF              | OFF              | OFF              |
| 1   | 1              | 1    | 1    | OFF                                                                                  | OFF              | OFF              | OFF              | OFF              | OFF              |
| 0   | X              | X    | X    | OFF                                                                                  | OFF              | OFF              | OFF              | ON               | ON               |
| 0→1 | 0              | 0    | 0    | EN transitions from low to high or high to low should occur at all logic inputs low. |                  |                  |                  |                  |                  |
| 1→0 | 0              | 0    | 0    |                                                                                      |                  |                  |                  |                  |                  |

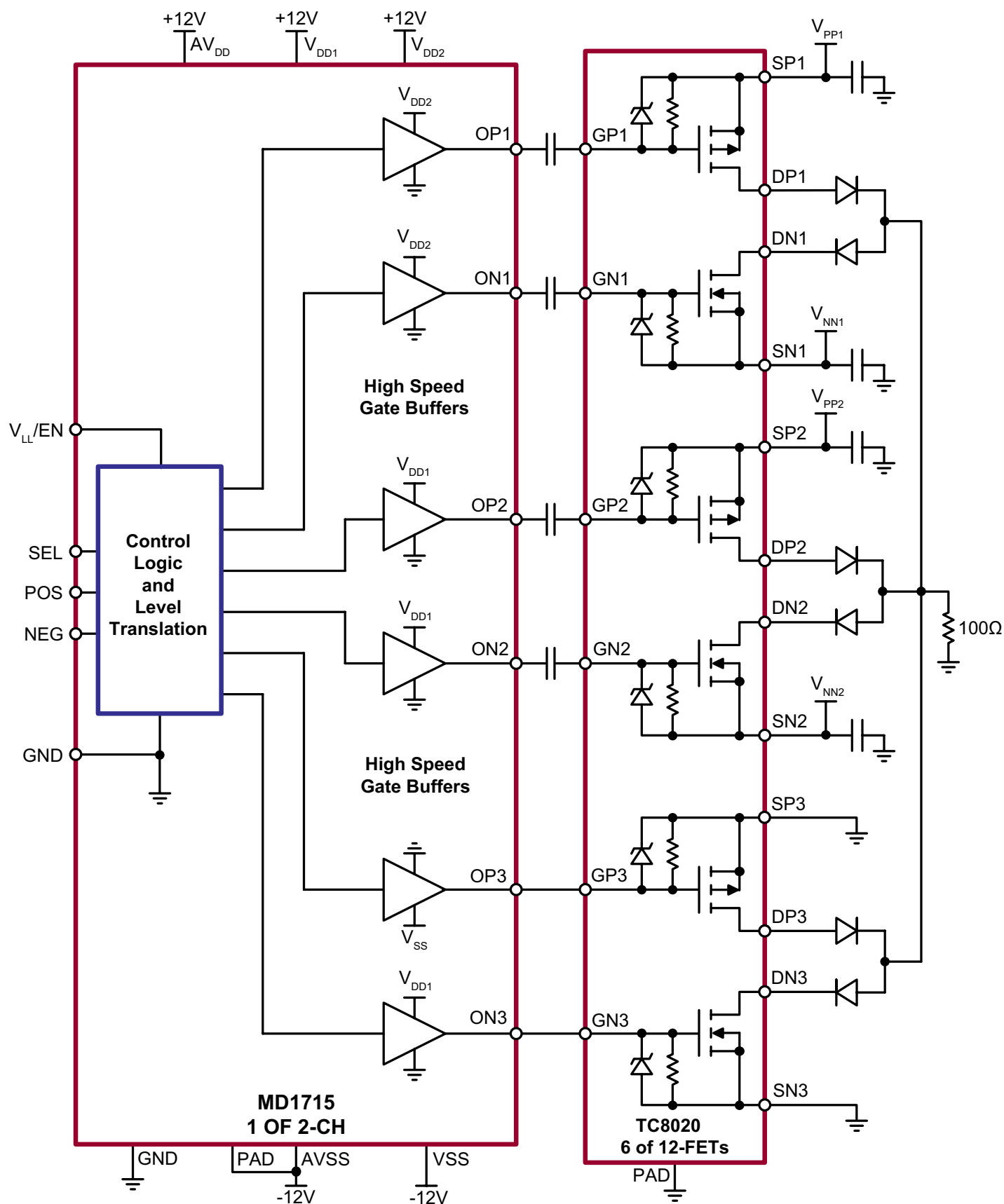
## Circuit Pin Layout



## Timing Diagram



## Detail Circuit



## Pin Descriptions

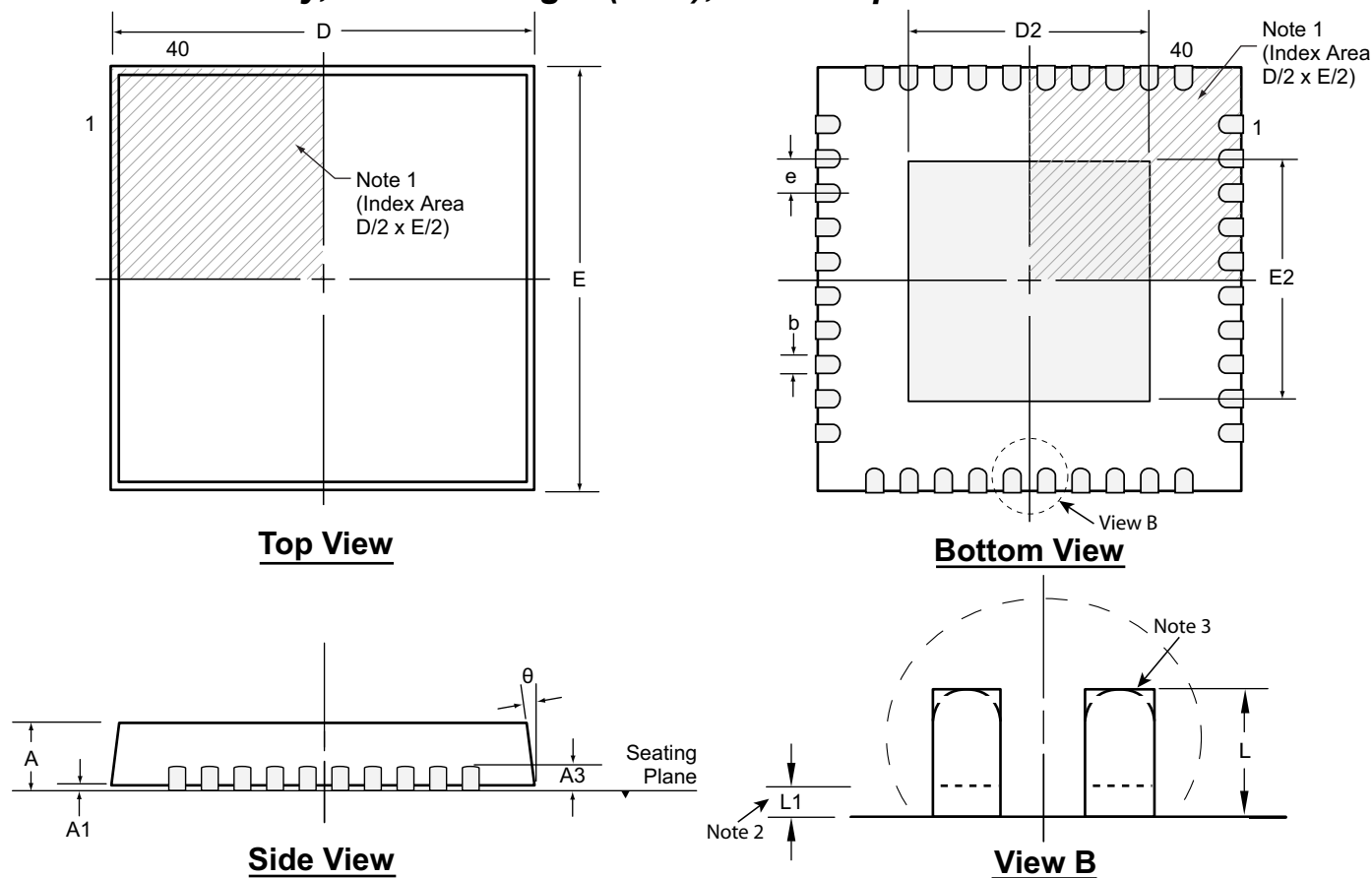
| Pin # | Name   | Description                                                                                                                                      |
|-------|--------|--------------------------------------------------------------------------------------------------------------------------------------------------|
| 1     | SELA   | SEL input logic control for channel A. See logic truth table for details.                                                                        |
| 2     | POSA   | POS input logic control for channel A. See logic truth table for details.                                                                        |
| 3     | NEGA   | NEG input logic control for channel A. See logic truth table for details.                                                                        |
| 4     | VLL/EN | Logic Hi reference voltage and chip enable input.                                                                                                |
| 5     | AVDD   | Positive supply voltage of analog circuitry. AVDD should be same or higher potential than the highest voltages of VDD1 or VDD2.                  |
| 6     | AGND   | Digital Ground.                                                                                                                                  |
| 7     | AVSS   | Negative supply voltage of analog circuitry and connection of IC substrate. Should be at the same potential as VSS.                              |
| 8     | SELB   | SEL input logic control for channel B. See logic truth table for details.                                                                        |
| 9     | POSB   | POS input logic control for channel B. See logic truth table for details.                                                                        |
| 10    | NEGB   | NEG input logic control for channel B. See logic truth table for details.                                                                        |
| 11    | VDD2   | Positive supply voltage of the gate drivers for the output stage OP1, ON1 in A and B channels. VDD2 can be at a different voltage than VDD1.     |
| 12    | OP1B   | First output P-Channel gate drivers for channel B.                                                                                               |
| 13    | VDD1   | Positive supply voltage of the gate drivers for the output stage for OP2, ON2, ON3 in A and B channels. VDD1 can be different voltage than VDD2. |
| 14    | GND    | Power Ground.                                                                                                                                    |
| 15    | OP2B   | Second output P-Channel gate drivers for channel B.                                                                                              |
| 16    | VDD2   | Positive supply voltage of the gate drivers for the output stage OP1, ON1 in A and B channels. VDD2 can be at a different voltage than VDD1.     |
| 17    | ON1B   | First output N-Channel gate drivers for channel B.                                                                                               |
| 18    | GND    | Power Ground.                                                                                                                                    |
| 19    | VDD1   | Positive supply voltage of the gate drivers for the output stage for OP2, ON2, ON3 in A and B channels. VDD1 can be different voltage than VDD2. |
| 20    | ON2B   | Second output N-Channel gate drivers for channel B.                                                                                              |
| 21    | GND    | Power Ground.                                                                                                                                    |
| 22    | ON3B   | Damping output N-Channel gate drivers for channel B.                                                                                             |
| 23    | VSS    | Negative supply voltage for gate drive of OP3. Should be the same voltage as AVSS.                                                               |
| 24    | OP3B   | Damping output P-Channel gate drivers for channel B.                                                                                             |
| 25    | GND    | Power Ground.                                                                                                                                    |
| 26    | VSS    | Negative supply voltage for gate drive of OP3. Should be the same voltage as AVSS.                                                               |
| 27    | OP3A   | Damping output P-Channel gate drivers for channel A.                                                                                             |
| 28    | GND    | Power Ground.                                                                                                                                    |
| 29    | GND    | Power Ground.                                                                                                                                    |
| 30    | ON3A   | Damping output N-Channel gate drivers for channel A.                                                                                             |
| 31    | ON2A   | Second output N-Channel gate drivers for channel A.                                                                                              |

**Pin Descriptions** (cont.)

| Pin #      | Name        | Description                                                                                                                                      |
|------------|-------------|--------------------------------------------------------------------------------------------------------------------------------------------------|
| 32         | VDD1        | Positive supply voltage of the gate drivers for the output stage for OP2, ON2, ON3 in A and B channels. VDD1 can be different voltage than VDD2. |
| 33         | GND         | Power Ground.                                                                                                                                    |
| 34         | ON1A        | First output N-Channel gate drivers for channel A.                                                                                               |
| 35         | VDD2        | Positive supply voltage of the gate drivers for the output stage OP1, ON1 in A and B channels. VDD2 can be at a different voltage than VDD1.     |
| 36         | OP2A        | Second output P-Channel gate drivers for channel A.                                                                                              |
| 37         | GND         | Power Ground.                                                                                                                                    |
| 38         | VDD1        | Positive supply voltage of the gate drivers for the output stage for OP2, ON2, ON3 in A and B channels. VDD1 can be different voltage than VDD2. |
| 39         | OP1A        | First output P-Channel gate drivers for channel A.                                                                                               |
| 40         | VDD2        | Positive supply voltage of the gate drivers for the output stage OP1, ON1 in A and B channels. VDD2 can be at a different voltage than VDD1.     |
| Center Pad | Thermal pad | IC substrate, must connect to $AV_{SS}$ externally                                                                                               |

## 40-Lead QFN Package Outline (K6)

6.00x6.00mm body, 1.00mm height (max), 0.50mm pitch



### Notes:

1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.
2. Depending on the method of manufacturing, a maximum of 0.15mm pullback (L1) may be present.
3. The inner tip of the lead may be either rounded or square.

| Symbol         |     | A    | A1   | A3       | b    | D     | D2   | E     | E2   | e        | L     | L1   | $\theta^\circ$ |
|----------------|-----|------|------|----------|------|-------|------|-------|------|----------|-------|------|----------------|
| Dimension (mm) | MIN | 0.80 | 0.00 | 0.20 REF | 0.18 | 5.85* | 1.05 | 5.85* | 1.05 | 0.50 BSC | 0.30† | 0.00 | 0              |
|                | NOM | 0.90 | 0.02 |          | 0.25 | 6.00  | -    | 6.00  | -    |          | 0.40† | -    | -              |
|                | MAX | 1.00 | 0.05 |          | 0.30 | 6.15* | 4.45 | 6.15* | 4.45 |          | 0.50† | 0.15 | 14             |

JEDEC Registration MO-220, Variation VJJD-6, Issue K, June 2006.

\* This dimension is not specified in the JEDEC drawing.

† This dimension differs from the JEDEC drawing.

**Drawings not to scale.**

**Supertex Doc. #:** DSPD-40QFNK66X6P050, Version C041009.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

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