



# P-Channel 20 V (D-S) MOSFET

PRODUCT SUMMARY						
V <sub>DS</sub> (V)	$R_{DS(on)}(\Omega)$	I <sub>D</sub> (A) <sup>a</sup>	Q <sub>g</sub> (Typ.)			
	0.041 at V <sub>GS</sub> = - 4.5 V	- 4				
- 20	0.054 at V <sub>GS</sub> = - 2.5 V	- 4	12.5 nC			
	0.100 at V <sub>GS</sub> = - 1.8 V	- 4				

D

SOT-363

SC-70 (6-LEADS)

### **FEATURES**

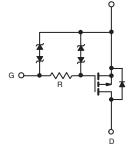
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFET
- Typical ESD Performance 1500 V
- 100 % R<sub>q</sub> Tested
- Compliant to RoHS Directive 2002/95/EC



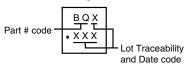
ROHS COMPLIANT HALOGEN FREE

### **APPLICATIONS**

- Load Switch for Portable Devices
  - Cellular Phone
  - DSC
  - Portable Game Console
  - MP3
  - GPS



Marking Code



Ordering Information: Si1441EDH-T1-GE3 (Lead (Pb)-free and Halogen-free)

P-Channel MOSFET

<b>ABSOLUTE MAXIMUM RATINGS</b>	<b>S</b> (T <sub>A</sub> = 25 °C, unle	ss otherwise not	ed)		
Parameter		Symbol	Limit	Unit	
Drain-Source Voltage	V <sub>DS</sub>	- 20	V		
Gate-Source Voltage		V <sub>GS</sub>	± 10	V	
	T <sub>C</sub> = 25 °C		- 4 <sup>a</sup>		
Continuous Drain Current (T = 150 °C)	T <sub>C</sub> = 70 °C		- 4	A	
Continuous Drain Current (T <sub>J</sub> = 150 °C)	T <sub>A</sub> = 25 °C	I <sub>D</sub>	- 4 <sup>a, b, c</sup>		
	T <sub>A</sub> = 70 °C		- 4 <sup>a, b, c</sup>		
Pulsed Drain Current (t = 300 μs)	1	I <sub>DM</sub>	- 25		
Outliness Outline Date Divide Outline	T <sub>C</sub> = 25 °C		- 2.3		
Continuous Source-Drain Diode Current	T <sub>A</sub> = 25 °C	I <sub>S</sub>	- 1.3 <sup>b, c</sup>		
	T <sub>C</sub> = 25 °C		2.8		
Maximum Power Dissipation	T <sub>C</sub> = 70 °C	В	1.8	w	
	T <sub>A</sub> = 25 °C	P <sub>D</sub>	1.6 <sup>b, c</sup>	vv	
	T <sub>A</sub> = 70 °C		1.0 <sup>b, c</sup>		
Operating Junction and Storage Temperature Ra	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150	- °C		
Soldering Recommendations (Peak Temperature		260			

THERMAL RESISTANCE RATINGS							
Parameter		Symbol	Typical	Maximum	Unit		
Maximum Junction-to-Ambient <sup>b, d</sup>	t ≤ 5 s	R <sub>thJA</sub>	60	80	°C/W		
Maximum Junction-to-Foot (Drain)	Steady State	$R_{thJF}$	34	45	C/VV		

### Notes:

- a. Package limited.
- b. Surface mounted on 1" x 1" FR4 board.
- c. t = 5 s.
- d. Maximum under steady state conditions is 125 °C/W.

# Si1441EDH

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Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	V <sub>DS</sub>	$V_{GS} = 0 \text{ V}, I_D = -250 \mu\text{A}$	- 20			V	
V <sub>DS</sub> Temperature Coefficient	$\Delta V_{DS}/T_{J}$	J 050 v A		- 11			
V <sub>GS(th)</sub> Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I <sub>D</sub> = - 250 μA		2.6		mV/°C	
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$	- 0.4		- 1	V	
Cata Causaa Laaliana		$V_{DS} = 0 \text{ V}, V_{GS} = \pm 10 \text{ V}$			± 8		
Gate-Source Leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 4.5 \text{ V}$			± 1	٠	
Zara Cata Valtaga Drain Current	_	V <sub>DS</sub> = - 20 V, V <sub>GS</sub> = 0 V			- 1	μΑ	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	$V_{DS} = -20 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55 \text{ °C}$			- 10		
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \le -5 \text{ V}, V_{GS} = -10 \text{ V}$	- 15			Α	
		V <sub>GS</sub> = - 4.5 V, I <sub>D</sub> = - 5 A		0.034	0.041		
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	$V_{GS} = -2.5 \text{ V}, I_D = -4.4 \text{ A}$		0.045	0.054	Ω	
		V <sub>GS</sub> = - 1.8 V, I <sub>D</sub> = - 1 A		0.067	0.100	1	
Forward Transconductance <sup>a</sup>	9 <sub>fs</sub>	V <sub>DS</sub> = - 10 V, I <sub>D</sub> = - 5 A		16		S	
Dynamic <sup>b</sup>							
Total Gate Charge		$V_{DS} = -10 \text{ V}, V_{GS} = -8 \text{ V}, I_D = -5 \text{ A}$		22	33	nC	
Gate-Source Charge	Q <sub>g</sub>			12.5	19		
	Q <sub>gs</sub>	$V_{DS} = -10 \text{ V}, V_{GS} = -4.5 \text{ V}, I_{D} = -5 \text{ A}$		1.8			
Gate-Drain Charge	$Q_{gd}$			3.3			
Gate Resistance	$R_{g}$	f = 1 MHz	0.08	0.43	0.86	kΩ	
Turn-On Delay Time	t <sub>d(on)</sub>			150	225		
Rise Time	t <sub>r</sub>	$V_{DD}$ = - 10 V, $R_L$ = 1.4 $\Omega$		300	450		
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D \cong -4 \text{ A}, V_{GEN} = -4.5 \text{ V}, R_g = 1 \Omega$		1620	2430		
Fall Time	t <sub>f</sub>			560	840		
Turn-On Delay Time	t <sub>d(on)</sub>			50	100	ns	
Rise Time	t <sub>r</sub>	$V_{DD}$ = - 10 V, $R_L$ = 1.4 $\Omega$		90	180		
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D \cong -4 \text{ A}, V_{GEN} = -10 \text{ V}, R_g = 1 \Omega$		2500	3750	1	
Fall Time	t <sub>f</sub>			600	900		
<b>Drain-Source Body Diode Characterist</b>	ics						
Continuous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C			- 2.3	Α.	
Pulse Diode Forward Current	I <sub>SM</sub>				- 25	A	
Body Diode Voltage	$V_{SD}$	I <sub>S</sub> = - 4 A, V <sub>GS</sub> = 0 V		- 0.85	- 1.2	V	
Body Diode Reverse Recovery Time	t <sub>rr</sub>			18	36	ns	
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>	1 4 A 41/44 400 A/ T 05 00		8	16	nC	
Reverse Recovery Fall Time	ta	$I_F = -4 \text{ A}, \text{ dI/dt} = 100 \text{ A/}\mu\text{s}, T_J = 25 ^{\circ}\text{C}$		18		ns	
Reverse Recovery Rise Time	t <sub>b</sub>			10			

### Notes:

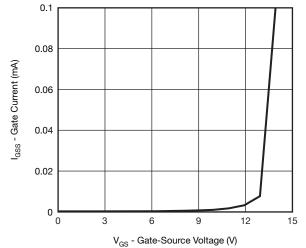
- a. Pulse test; pulse width  $\leq 300~\mu s,$  duty cycle  $\leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

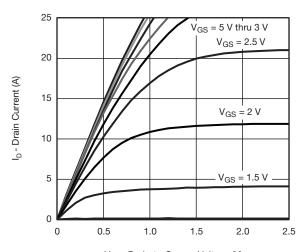




### TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

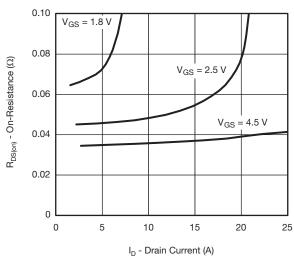


Gate Current vs. Gate-Source Voltage

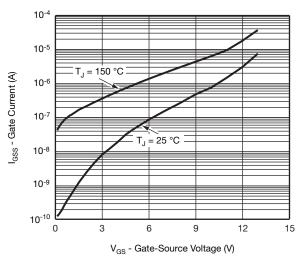


V<sub>DS</sub> - Drain-to-Source Voltage (V)

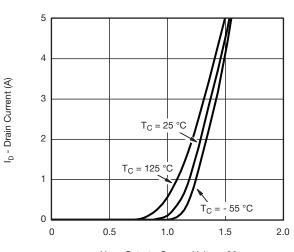
Output Characteristics



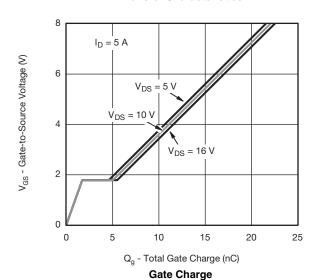
On-Resistance vs. Drain Current



Gate Current vs. Gate-Source Voltage



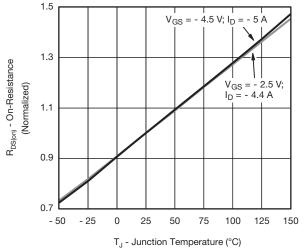
V<sub>GS</sub> - Gate-to-Source Voltage (V) **Transfer Characteristics** 



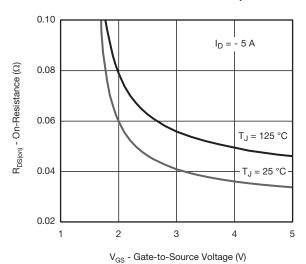
# Si1441EDH

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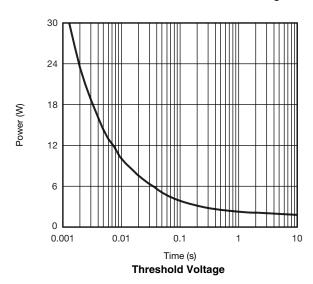
### TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

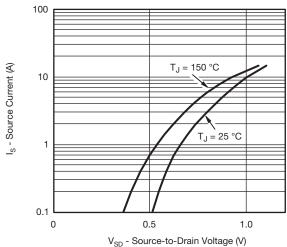


### On-Resistance vs. Junction Temperature

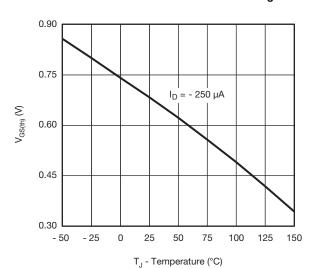


On-Resistance vs. Gate-to-Source Voltage

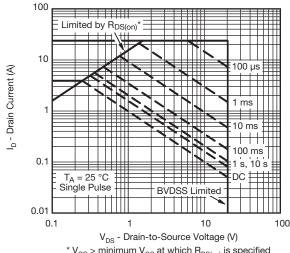




Source-Drain Diode Forward Voltage



Single Pulse Power, Junction-to-Ambient

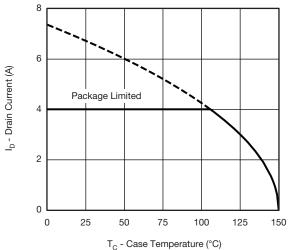


\*  $V_{GS}$  > minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

Safe Operating Area, Junction-to-Ambient

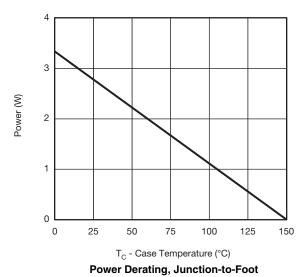


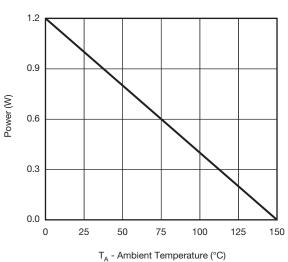
### TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



### Ourset Desettest

### **Current Derating\***





Power Derating, Junction-to-Ambient

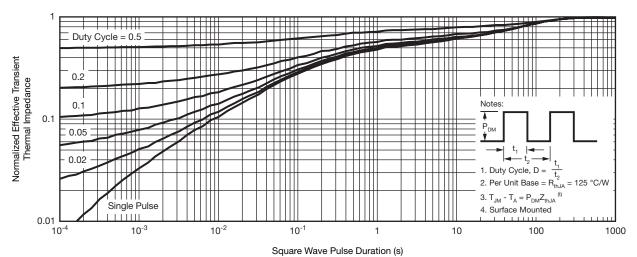
<sup>\*</sup> The power dissipation  $P_D$  is based on  $T_{J(max)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

### Si1441EDH

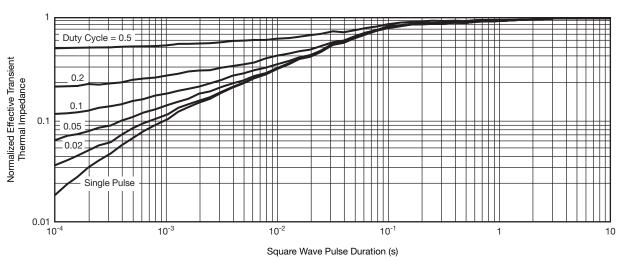
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### TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



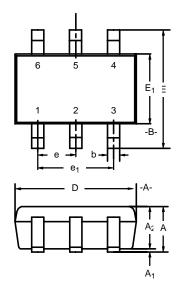
Normalized Thermal Transient Impedance, Junction-to-Foot

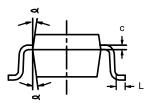
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### SC-70: 6-LEADS





	MILLIMETERS			INCHES		S
Dim	Min	Nom	Max	Min	Nom	Max
Α	0.90	_	1.10	0.035	_	0.043
A <sub>1</sub>	-	_	0.10	-	_	0.004
A <sub>2</sub>	0.80	_	1.00	0.031	_	0.039
b	0.15	_	0.30	0.006	_	0.012
С	0.10	-	0.25	0.004	-	0.010
D	1.80	2.00	2.20	0.071	0.079	0.087
Ε	1.80	2.10	2.40	0.071	0.083	0.094
E <sub>1</sub>	1.15	1.25	1.35	0.045	0.049	0.053
е	0.65BSC				0.026BSC	;
e <sub>1</sub>	1.20	1.30	1.40	0.047	0.051	0.055
L	0.10	0.20	0.30	0.004	0.008	0.012
کے	7°Nom				7°Nom	

DWG: 5550





# Single-Channel LITTLE FOOT® SC-70 6-Pin MOSFET Copper Leadframe Version Recommended Pad Pattern and Thermal Performance

### INTRODUCTION

The new single 6-pin SC-70 package with a copper leadframe enables improved on-resistance values and enhanced thermal performance as compared to the existing 3-pin and 6-pin packages with Alloy 42 leadframes. These devices are intended for small to medium load applications where a miniaturized package is required. Devices in this package come in a range of on-resistance values, in n-channel and p-channel versions. This technical note discusses pin-outs, package outlines, pad patterns, evaluation board layout, and thermal performance for the single-channel version.

### **BASIC PAD PATTERNS**

See Application Note 826, Recommended Minimum Pad Patterns With Outline Drawing Access for Vishay Siliconix MOSFETs, (http://www.vishay.com/doc?72286) for the basic pad layout and dimensions. These pad patterns are sufficient for the low to medium power applications for which this package is intended. Increasing the drain pad pattern yields a reduction in thermal resistance and is a preferred footprint. The availability of four drain leads rather than the traditional single drain lead allows a better thermal path from the package to the PCB and external environment.

### **PIN-OUT**

Figure 1 shows the pin-out description and Pin 1 identification. The pin-out of this device allows the use of four pins as drain leads, which helps to reduce on-resistance and junction-to-ambient thermal resistance.

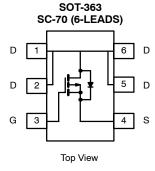


FIGURE 1.

For package dimensions see outline drawing SC-70 (6-Leads) (http://www.vishay.com/doc?71154)

### **EVALUATION BOARDS — SINGLE SC70-6**

The evaluation board (EVB) measures 0.6 inches by 0.5 inches. The copper pad traces are the same as in Figure 2. The board allows examination from the outer pins to 6-pin DIP connections, permitting test sockets to be used in evaluation testing. See Figure 3.

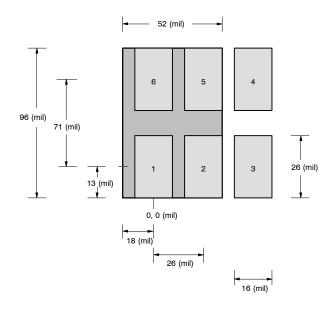
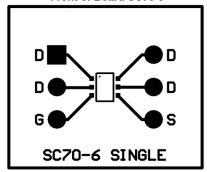


FIGURE 2. SC-70 (6 leads) Single

The thermal performance of the single 6-pin SC-70 has been measured on the EVB, comparing both the copper and Alloy 42 leadframes. This test was first conducted on the traditional Alloy 42 leadframe and was then repeated using the 1-inch<sup>2</sup> PCB with dual-side copper coating.



Front of Board SC70-6



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Back of Board SC70-6

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FIGURE 3.

### THERMAL PERFORMANCE

### **Junction-to-Foot Thermal Resistance** (Package Performance)

The junction to foot thermal resistance is a useful method of comparing different packages thermal performance.

A helpful way of presenting the thermal performance of the 6-Pin SC-70 copper leadframe device is to compare it to the traditional Alloy 42 version.

Thermal performance for the 6-pin SC-70 measured as junction-to-foot thermal resistance, where the "foot" is the drain lead of the device at the bottom where it meets the PCB. The junction-to-foot thermal resistance is typically 40°C/W in the copper leadframe and 163°C/W in the Alloy 42 leadframe - a four-fold improvement. This improved performance is obtained by the enhanced thermal conductivity of copper over Alloy 42.

### **Power Dissipation**

The typical  $R\theta_{JA}$  for the single 6-pin SC-70 with copper leadframe is 103°C/W steady-state, compared with 212°C/W for the Alloy 42 version. The figures are based on the 1-inch<sup>2</sup> FR4 test board. The following example shows how the thermal resistance impacts power dissipation for the two different leadframes at varying ambient temperatures.

ALLOY 42 LEADFRAME				
Room Ambient 25 °C Elevated Ambient 60 °C				
$P_D = \frac{T_{J(max)} - T_A}{R\theta_{JA}}$	$P_D = \frac{T_{J(max)} - T_A}{R\theta_{JA}}$			
$P_{D} = \frac{150^{\circ}C - 25^{\circ}C}{212^{\circ}C/W}$	$P_{D} = \frac{150^{\circ}C - 25^{\circ}C}{212^{\circ}C/W}$			
$P_D = 590 \text{ mW}$	$P_D = 425 \text{ mW}$			

COOPER LEADFRAME				
Room Ambient 25 °C	Elevated Ambient 60 °C			
$P_{D} = \frac{T_{J(max)} - T_{A}}{R\theta_{JA}}$ $P_{D} = \frac{150^{\circ}C - 25^{\circ}C}{124^{\circ}C/W}$	$P_{D} = \frac{T_{J(max)} - T_{A}}{R\theta_{JA}}$ $P_{D} = \frac{150^{\circ}C - 60^{\circ}C}{124^{\circ}C/W}$			
$P_{D} = 1.01 \text{ W}$	P <sub>D</sub> = 726 mW			

As can be seen from the calculations above, the compact 6-pin SC-70 copper leadframe LITTLE FOOT power MOSFET can handle up to 1 W under the stated conditions.

### **Testing**

To further aid comparison of copper and Alloy 42 leadframes, Figure 5 illustrates single-channel 6-pin SC-70 thermal performance on two different board sizes and two different pad patterns. The measured steady-state values of  $R\theta_{JA}$  for the two leadframes are as follows:

LITTLE FOOT 6-PIN SC-70					
	Alloy 42	Copper			
1) Minimum recommended pad pattern on the EVB board V (see Figure 3.	329.7°C/W	208.5°C/W			
<ol> <li>Industry standard 1-inch<sup>2</sup> PCB with maximum copper both sides.</li> </ol>	211.8°C/W	103.5°C/W			

The results indicate that designers can reduce thermal resistance ( $R\theta_{1\Delta}$ ) by 36% simply by using the copper leadframe device rather than the Alloy 42 version. In this example, a 121°C/W reduction was achieved without an increase in board area. If increasing in board size is feasible, a further 105°C/W reduction could be obtained by utilizing a 1-inch<sup>2</sup> square PCB area.

The copper leadframe versions have the following suffix:

Single: Si14xxEDH Dual: Si19xxEDH Complementary: Si15xxEDH

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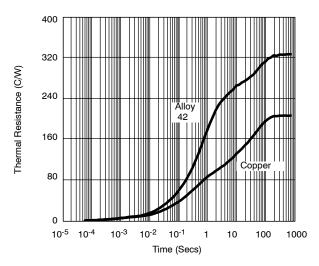


FIGURE 4. Leadframe Comparison on EVB

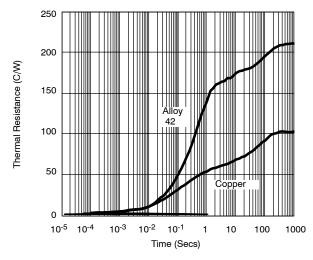
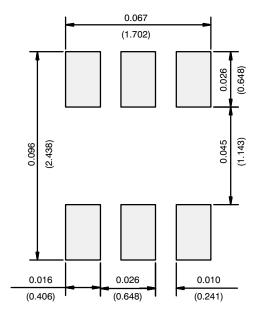


FIGURE 5. Leadframe Comparison on Alloy 42 1-inch<sup>2</sup> PCB



### **RECOMMENDED MINIMUM PADS FOR SC-70: 6-Lead**



Recommended Minimum Pads Dimensions in Inches/(mm)

Return to Index



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Vishay Intertechnology, Inc. hereby certifies that all its products that are identified as Halogen-Free follow Halogen-Free requirements as per JEDEC JS709A standards. Please note that some Vishay documentation may still make reference to the IEC 61249-2-21 definition. We confirm that all the products identified as being compliant to IEC 61249-2-21 conform to JEDEC JS709A standards.

Revision: 02-Oct-12 Document Number: 91000

### **ПОСТАВКА** ЭЛЕКТРОННЫХ КОМПОНЕНТОВ

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Для оперативного оформления запроса Вам необходимо перейти по данной ссылке:

### http://moschip.ru/get-element

Вы можете разместить у нас заказ для любого Вашего проекта, будь то серийное производство или разработка единичного прибора.

В нашем ассортименте представлены ведущие мировые производители активных и пассивных электронных компонентов.

Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

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