

2.1GHz Band LNA GaAs MMIC

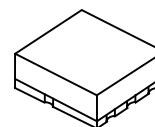
■GENERAL DESCRIPTION

NJG1126HB6 is a LNA IC designed for 2.1GHz band W-CDMA cellular phone. This IC has the function which bypasses LNA, and high gain mode or low gain mode can be chosen.

High IIP3 and a low noise are achieved at the High gain mode. And low current consumption can be achieved at the low gain mode because LNA enters the state of the standby.

A small and thin package of USB8 is adopted.

■PACKAGE OUTLINE

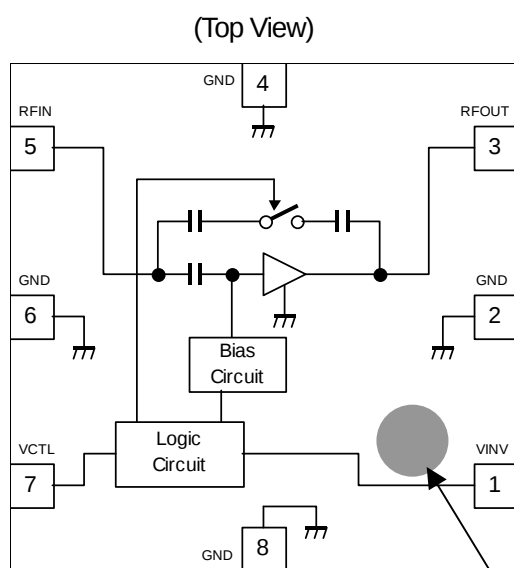


NJG1126HB6

■FEATURES

- | | | |
|------------------------------------|---|--|
| ●Low voltage operation | +2.7V typ. | |
| ●Low CTL voltage operation | +1.85V typ. | |
| ●Low current consumption | 2.2mA typ. | @V _{CTL} =1.85V |
| | 1uA typ. | @V _{CTL} =0V |
| ●High gain | 16.5dB typ. | @V _{CTL} =1.85V, f _{RF} =2140MHz |
| ●Low noise figure | 1.4dB typ. | @V _{CTL} =1.85V, f _{RF} =2140MHz |
| ●Pin at 1dB Gain Compression point | -12.0dBm typ. | @V _{CTL} =1.85V, f _{RF} =2140MHz |
| | +11.0dBm typ. | @V _{CTL} =0V, f _{RF} =2140MHz |
| ●High input IP3 | 0dBm typ. | @V _{CTL} =1.85V, f _{RF} =2140MHz |
| | +16.0dBm typ. | @V _{CTL} =0V, f _{RF} =2140MHz |
| ●Small package | USB8-B6 (Package size: 1.5mmx1.5mmx0.55mm typ.) | |

■PIN CONFIGURATION



1 Pin INDEX

Pin Connection

1. V_{INV}
2. GND
3. RF OUT
4. GND
5. RF IN
6. GND
7. V_{CTL}
8. GND

Note: Specifications and description listed in this catalog are subject to change without prior notice.

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■ABSOLUTE MAXIMUM RATINGS

$T_a=+25^{\circ}\text{C}$, $Z_s=Z_f=50\Omega$

PARAMETERS	SYMBOL	CONDITIONS	RATINGS	UNITS
Supply voltage	V_{DD}		5.0	V
Inverter supply voltage	V_{INV}		5.0	V
Control voltage	V_{CTL}		5.0	V
Input power	P_{in}	$V_{DD}=2.85\text{V}$	+15	dBm
Power dissipation	P_D	on PCB board, $T_{jmax}=150^{\circ}\text{C}$	135	mW
Operating temperature	T_{opr}		-40~+85	$^{\circ}\text{C}$
Storage temperature	T_{stg}		-55~+150	$^{\circ}\text{C}$

■ELECTRICAL CHARACTERISTICS 1 (DC)

(General Conditions: $V_{DD}=V_{INV}=2.85\text{V}$, $T_a=+25^{\circ}\text{C}$, $Z_s=Z_f=50\Omega$)

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating voltage	V_{DD}		2.5	2.85	3.2	V
Inverter supply voltage	V_{INV}		2.5	2.85	3.2	V
Control voltage (High)	$V_{CTL(H)}$		1.5	1.85	$V_{INV}+0.3$	V
Control voltage (Low)	$V_{CTL(L)}$		0	0	0.3	V
Operating current1 (LNA High Gain Mode)	I_{DD1}	RF OFF, $V_{CTL}=1.85\text{V}$	-	2.2	3.2	mA
Operating current2 (LNA High Gain Mode)	I_{DD2}	RFOFF, $V_{CTL}=0\text{V}$	-	1	5	μA
Inverter current1 (LNA High Gain Mode)	I_{INV1}	RF OFF, $V_{CTL}=1.85\text{V}$	-	90	150	μA
Inverter current2 (LNA High Gain Mode)	I_{INV2}	RF OFF, $V_{CTL}=0\text{V}$	-	16	50	μA
Control current	I_{CTL}	RF OFF, $V_{CTL}=1.85\text{V}$	-	5	20	μA

■ELECTRICAL CHARACTERISTICS 2 (LNA High Gain Mode)

(General Conditions: $V_{DD}=V_{INV}=2.7V$, $V_{CTL}=1.85V$, $freq=2140MHz$, $T_a=+25^{\circ}C$, $Z_s=Z_L=50\Omega$)

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Small signal gain1	Gain1		15.0	16.5	19.0	dB
Noise figure1	NF1	Exclude PCB & connector losses (IN: 0.09dB)	-	1.4	1.7	dB
1dB gain compression output power1	$P_{-1dB(IN)}1$		-15.5	-12.0	-	dBm
3rd order Input Intercept Point1	IIP3_1	$f1=f_{RF}$, $f2=f_{RF}+100kHz$, $P_{in}=-32dBm$	-5.0	0	-	dBm
RF IN VSWR1	$VSWR_i1$		-	1.6	2.2	-
RF OUT VSWR1	$VSWR_o1$		-	1.5	2.2	-

■ELECTRICAL CHARACTERISTICS 2 (LNA Low Gain Mode)

(General Conditions: $V_{DD}=V_{INV}=2.7V$, $V_{CTL}=0V$, $freq=2140MHz$, $T_a=+25^{\circ}C$, $Z_s=Z_L=50\Omega$)

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Small signal gain2	Gain2		-10.0	-7.0	-5.5	dB
Noise figure2	NF2	Exclude PCB & connector losses (IN: 0.09dB)	-	7.0	10.0	dB
1dB gain compression output power2	$P_{-1dB(IN)}2$		+4.5	+11.0	-	dBm
3rd order Input Intercept Point2	IIP3_2	$F1=f_{RF}$, $f2=f_{RF}+100kHz$, $P_{in}=-16dBm$	0	+16.0	-	dBm
RF IN VSWR2	$VSWR_i2$		-	1.5	2.0	-
RF OUT VSWR2	$VSWR_o2$		-	1.5	2.0	-

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■ TERMINAL INFORMATION

No.	SYMBOL	DESCRIPTION
1	VINV	Supply voltage terminal for internal logic circuit (inverter). Please place a bypass capacitor between this and GND for avoiding RF noise from outside.
2	GND	Ground terminal.
3	RFOUT	RF signal comes out from this terminal, and goes through an external matching circuit connected to this. Inductor L3 as shown in the application circuit is a part of an external matching circuit, and also provide DC power to LNA. Capacitor C2 as shown in the application circuit is a bypass capacitor.
4	GND	Ground terminal.
5	RFIN	RF input signal is input to this terminal through an external matching circuit connected to this terminal. A DC blocking capacitor is not required.
6	GND	Ground terminal.
7	VCTL	Control port. A logic control signal is required to select High or Low gain mode of LNA. This terminal is set to more than +1.5V of logical high level for High gain mode of LNA, and set to 0~+0.3V of logical low level for Low gain mode.
8	GND	Ground terminal.

CAUTION

- 1) Ground terminal (No.2, 4, 6, 8) should be connected to the ground plane as close as possible for excellent RF performance, because distance to GND makes parasitic inductance.

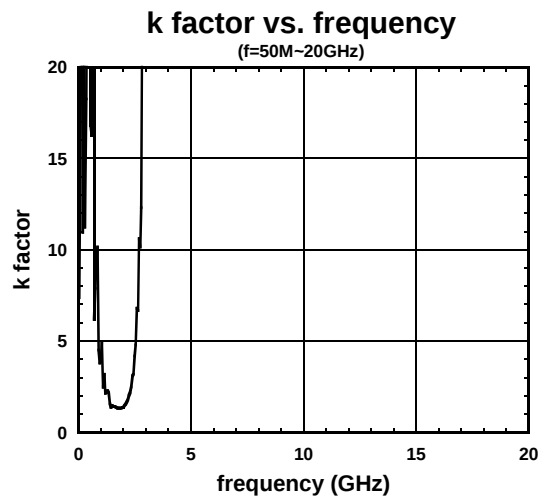
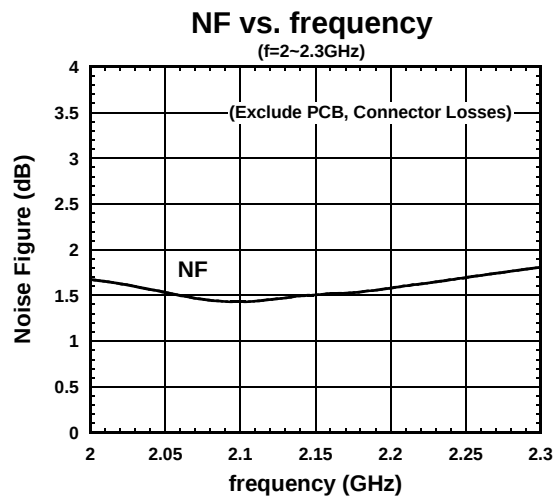
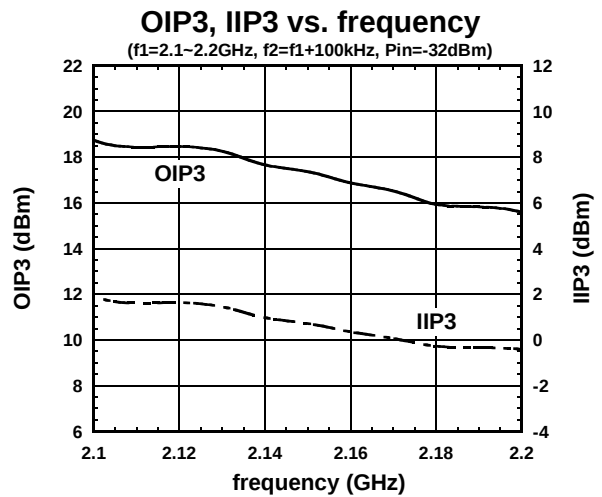
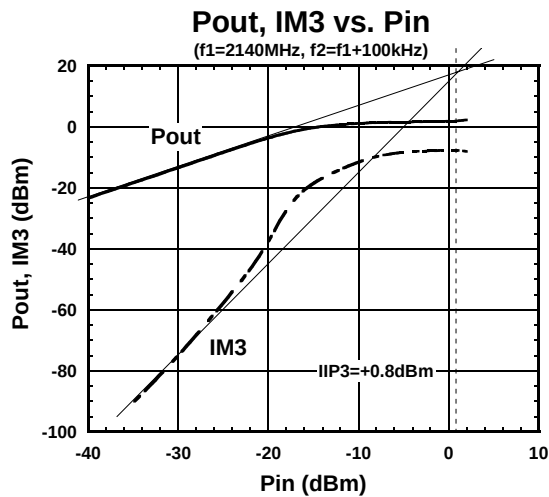
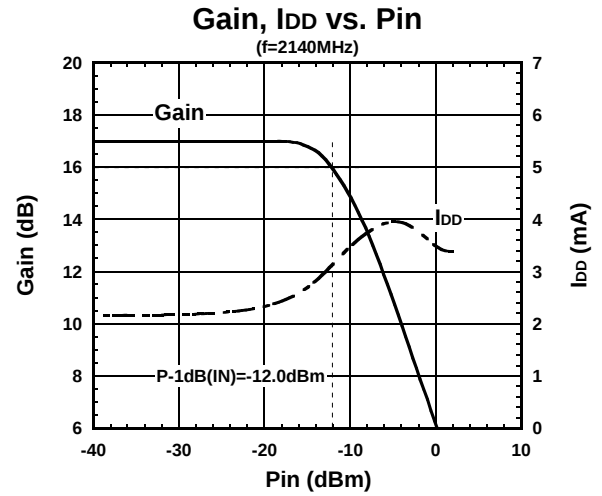
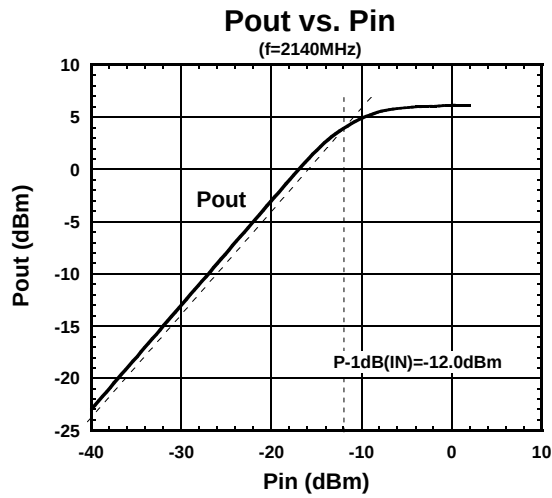
■ TRUTH TABLE

"H"= $V_{CTL}(H)$, "L"= $V_{CTL}(L)$

V_{CTL}	Gain Mode	LNA
L	Low	bypass
H	High	pass

ELECTRICAL CHARACTERISTICS (LNA High Gain Mode)

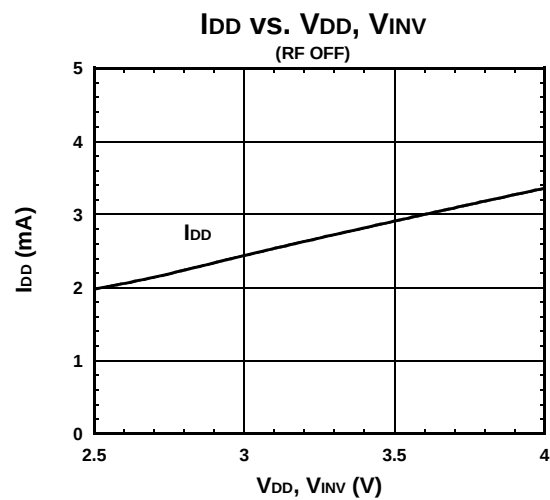
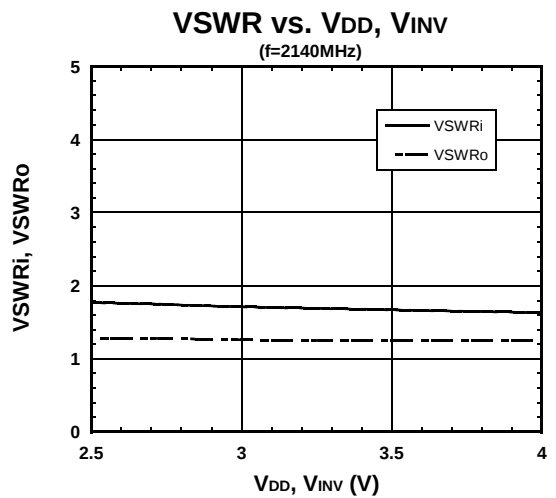
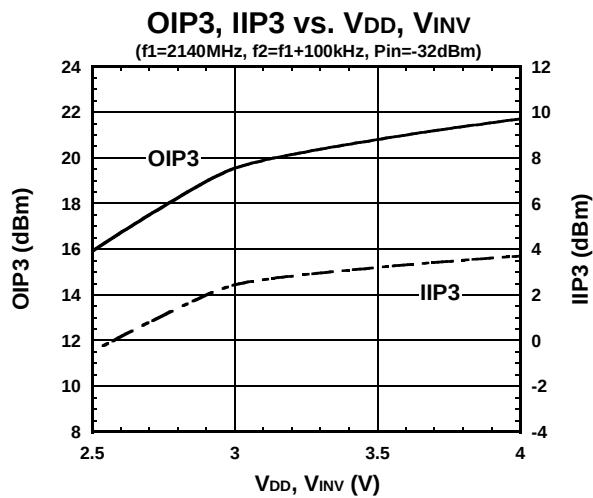
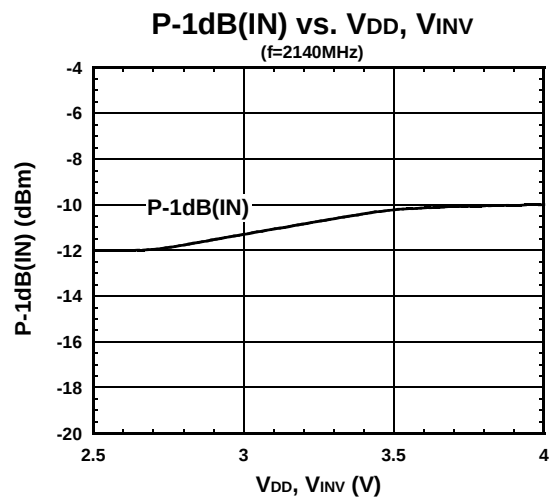
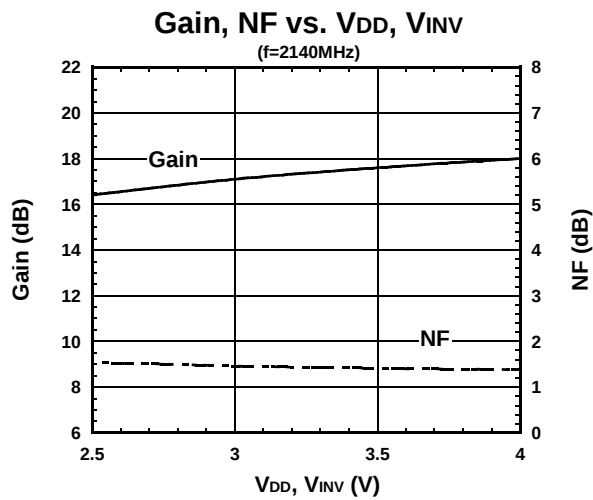
General Conditions: $T_a=+25^{\circ}\text{C}$, $V_{DD}=V_{INV}=2.7\text{V}$, $V_{CTL}=1.85\text{V}$, $Z_S=Z_I=50\Omega$



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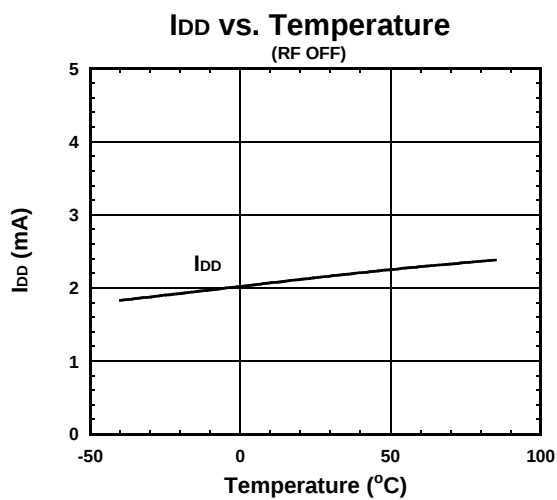
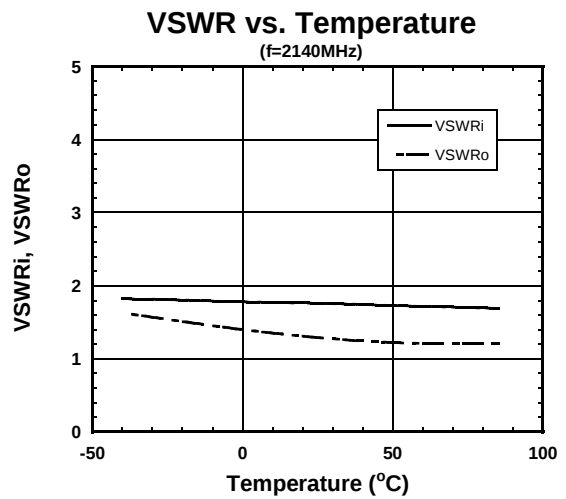
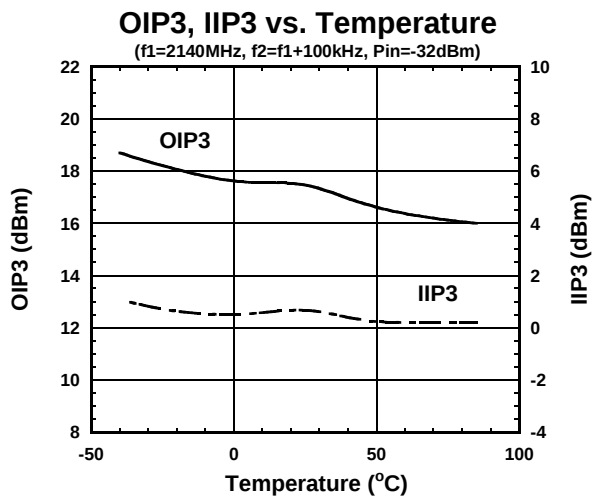
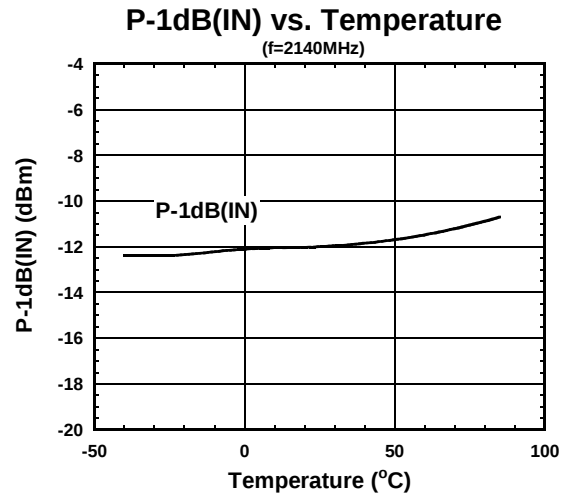
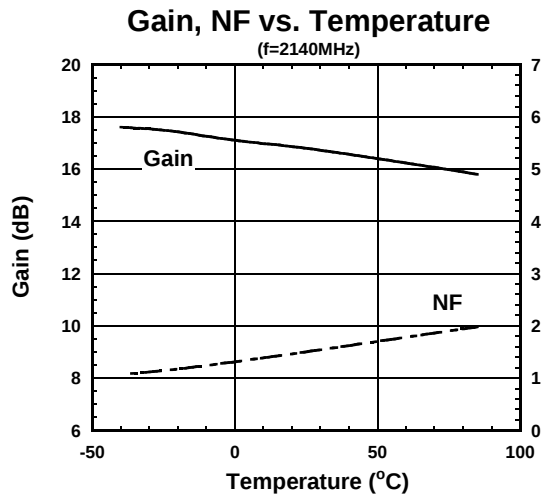
ELECTRICAL CHARACTERISTICS (LNA High Gain Mode)

General Conditions: $T_a=+25^{\circ}\text{C}$, $V_{DD}=V_{INV}=2.7\text{V}$, $V_{CTL}=1.85\text{V}$, $Z_S=Z_L=50\Omega$



ELECTRICAL CHARACTERISTICS (LNA High Gain Mode)

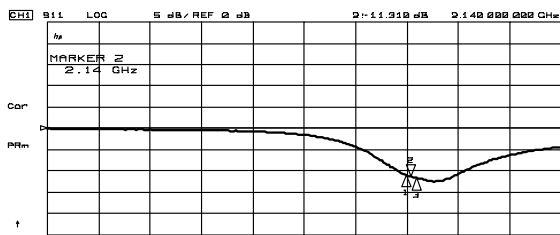
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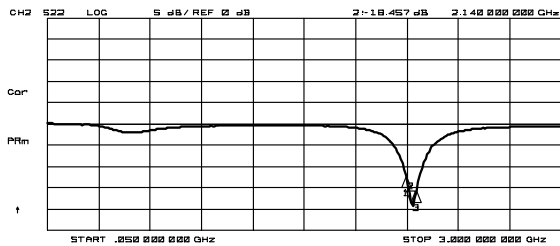
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ELECTRICAL CHARACTERISTICS (LNA High Gain Mode)

General Conditions: $T_a = +25^\circ\text{C}$, $V_{DD} = V_{INV} = 2.7\text{V}$, $V_{CTL} = 1.85\text{V}$, $Z_S = Z_I = 50\Omega$



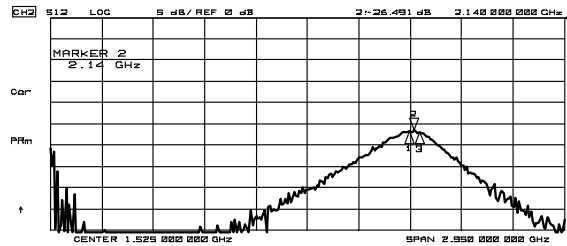
CH1 Markers
1: -10.998 dB
2: 11.000 GHz
3: -11.918 dB
2.17000 GHz



CH2 Markers
1: -12.134 dB
2: 11.000 GHz
3: -15.655 dB
2.17000 GHz



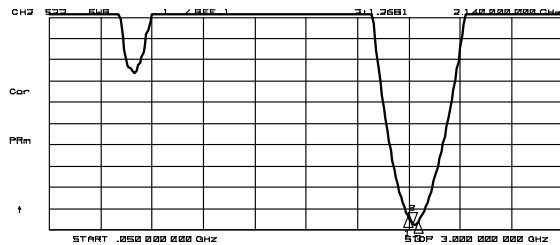
CH1 Markers
1: 16.778 dB
2: 11.000 GHz
3: 16.363 dB
2.17000 GHz



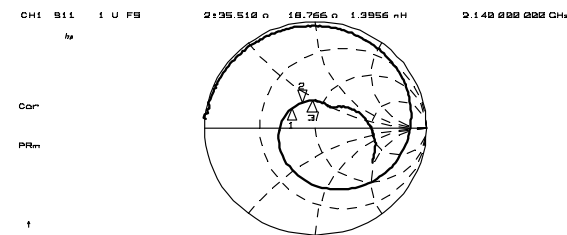
CH2 Markers
1: 26.792 dB
2: 11.000 GHz
3: 26.928 dB
2.17000 GHz



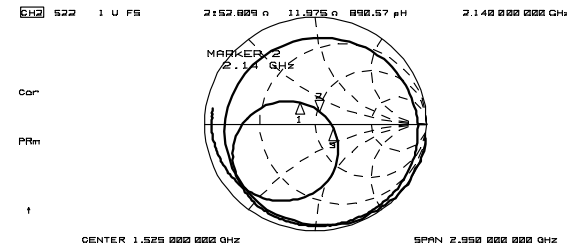
CH1 Markers
1: 1.7893
2: 11.000 GHz
3: 1.7121
2.17000 GHz



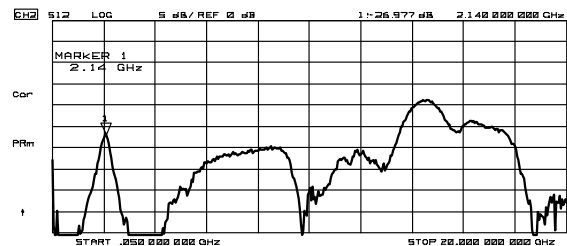
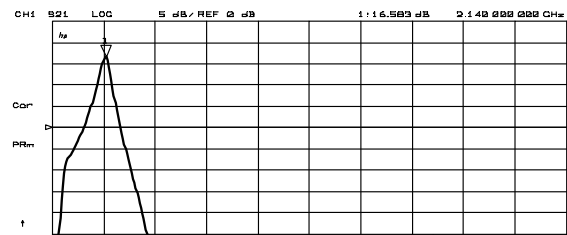
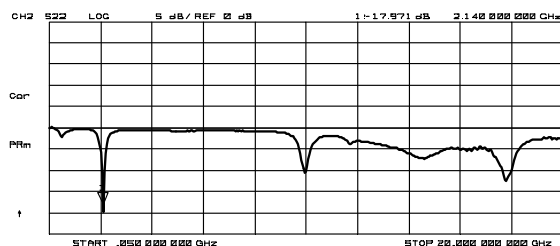
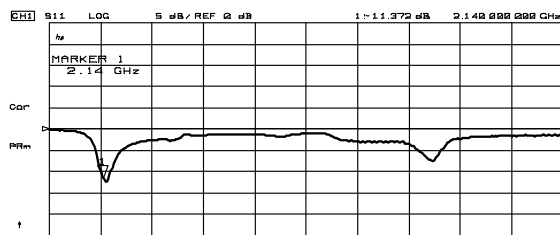
CH2 Markers
1: 1.6469
2: 11.000 GHz
3: 1.3998
2.17000 GHz



CH1 Markers
1: 38.883 n
2: 12.695 n
3: 41.324 n
2.17000 GHz

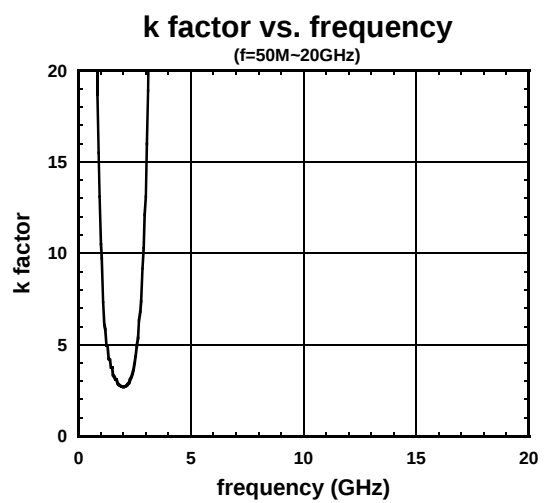
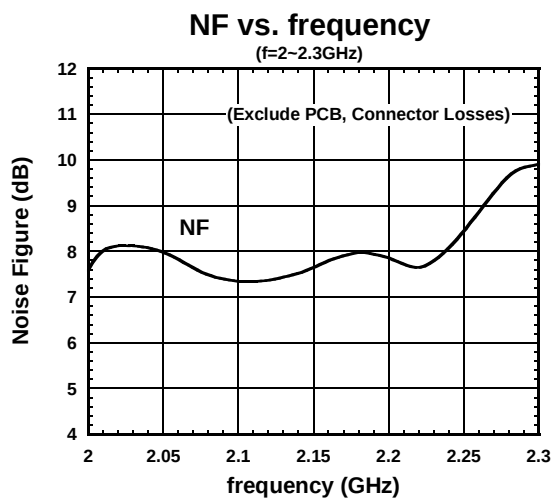
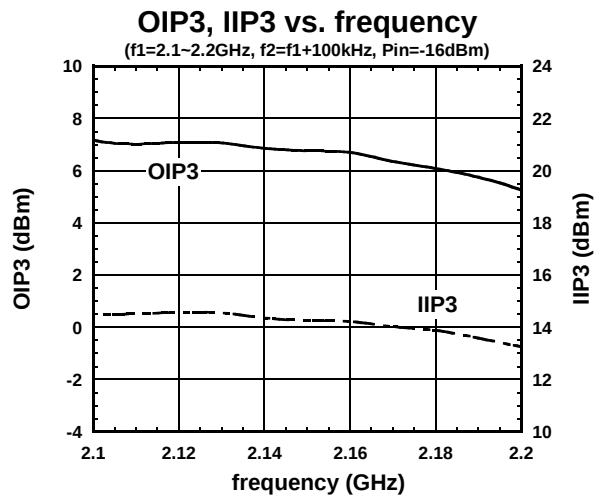
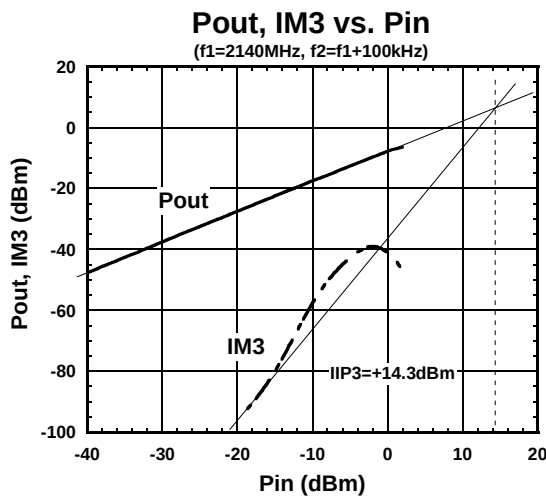
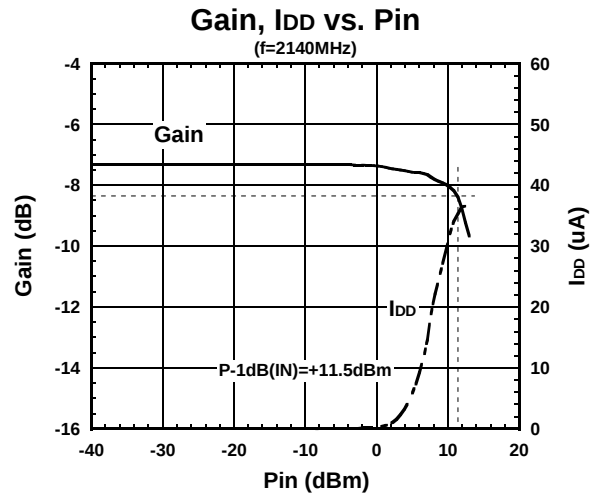
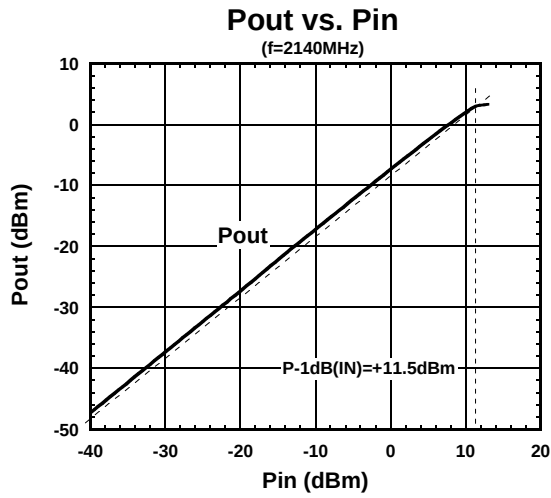


CH2 Markers
1: 35.129 n
2: 15.152 n
3: 59.582 n
2.17000 GHz



ELECTRICAL CHARACTERISTICS (LNA Low Gain Mode)

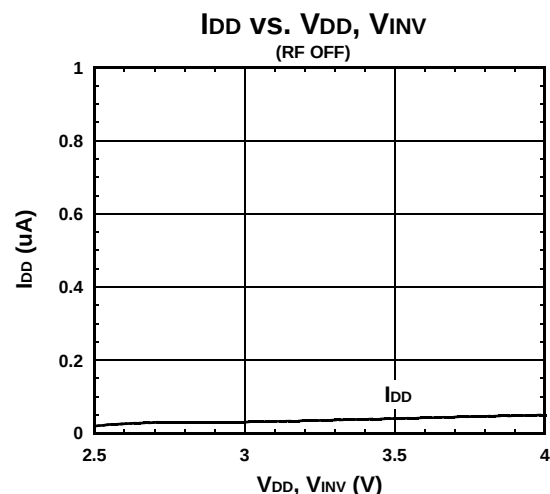
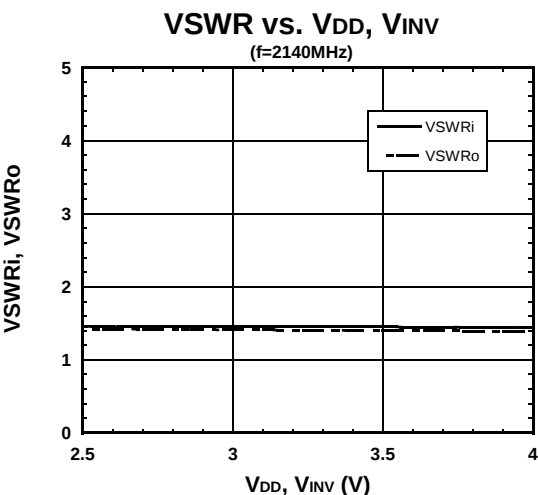
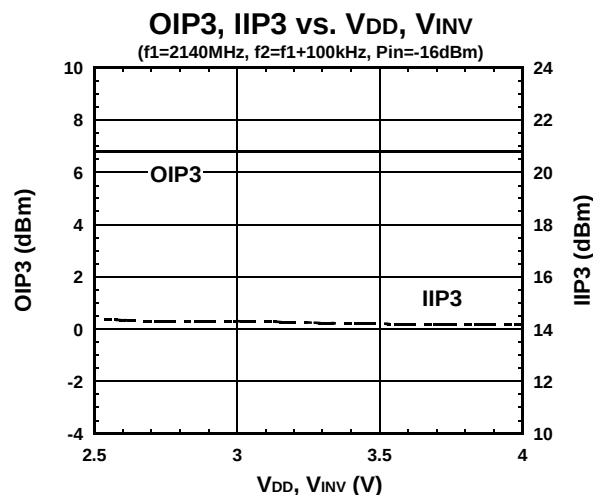
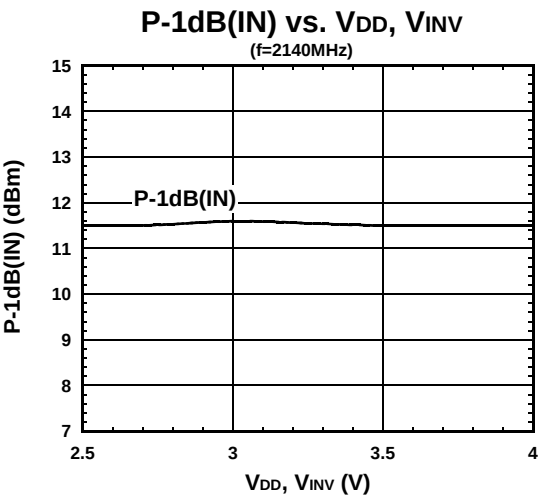
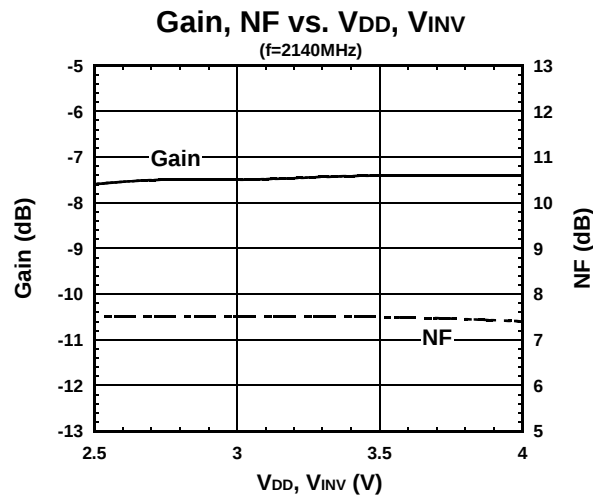
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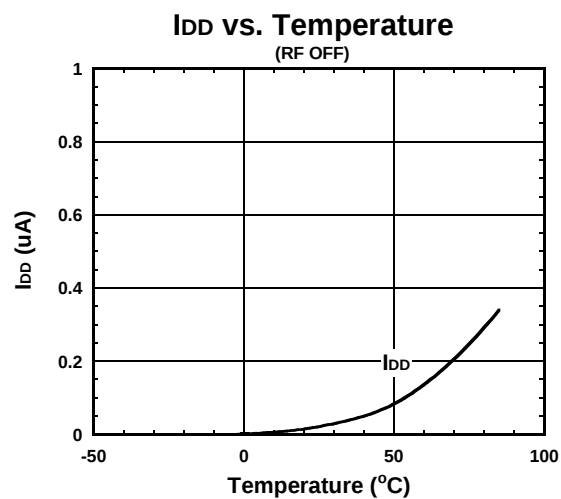
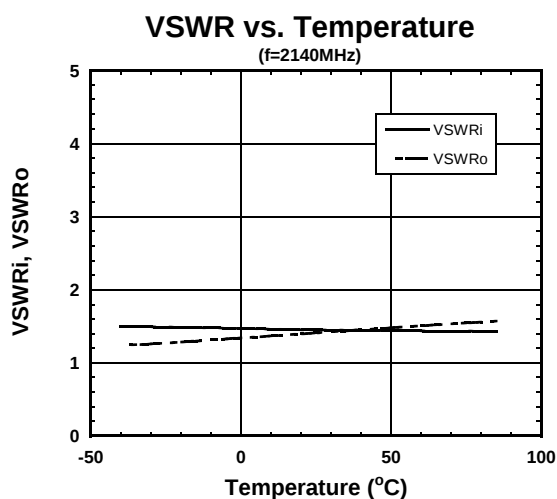
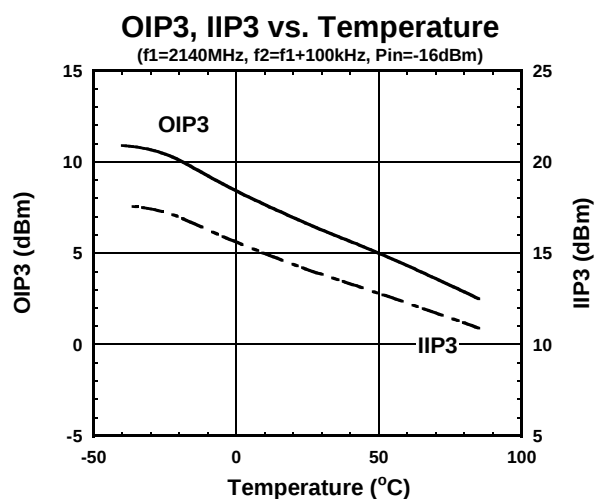
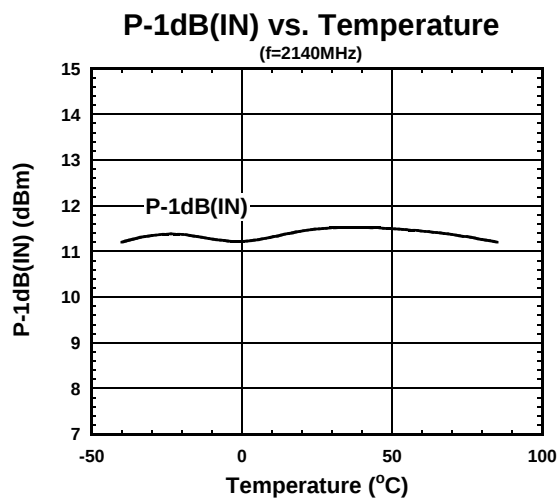
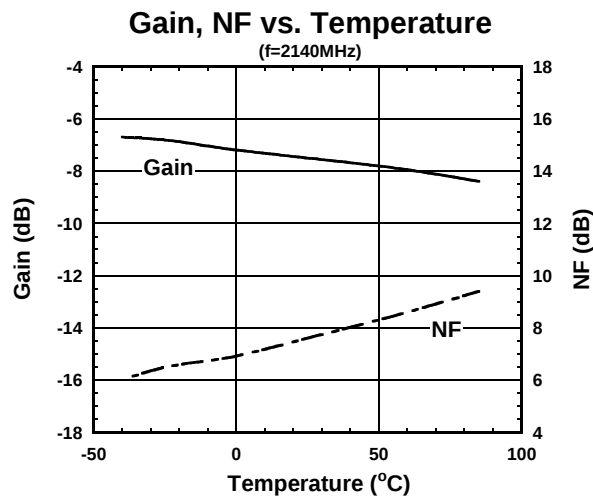
ELECTRICAL CHARACTERISTICS (LNA Low Gain Mode)

General Conditions: Ta=+25°C, V_{DD}=V_{INV}=2.7V, V_{CTL}=0V, Z_S=Z_L=50Ω



ELECTRICAL CHARACTERISTICS (LNA Low Gain Mode)

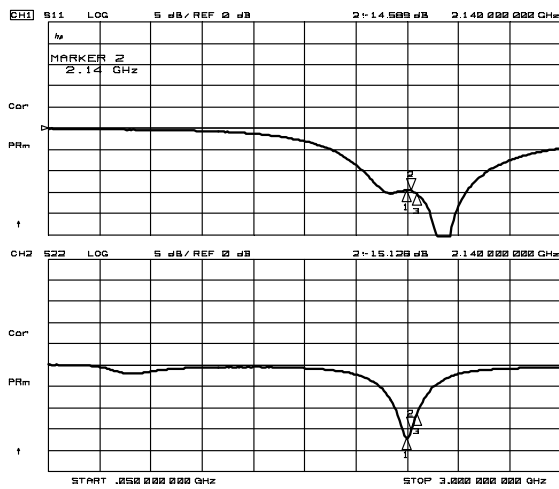
General Conditions: $T_a = +25^\circ\text{C}$, $V_{DD} = V_{INV} = 2.7\text{V}$, $V_{CTL} = 0\text{V}$, $Z_S = Z_L = 50\Omega$



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ELECTRICAL CHARACTERISTICS (LNA Low Gain Mode)

General Conditions: $T_a = +25^\circ\text{C}$, $V_{DD} = V_{INV} = 2.7\text{V}$, $V_{CTL} = 0\text{V}$, $Z_S = Z_L = 50\Omega$

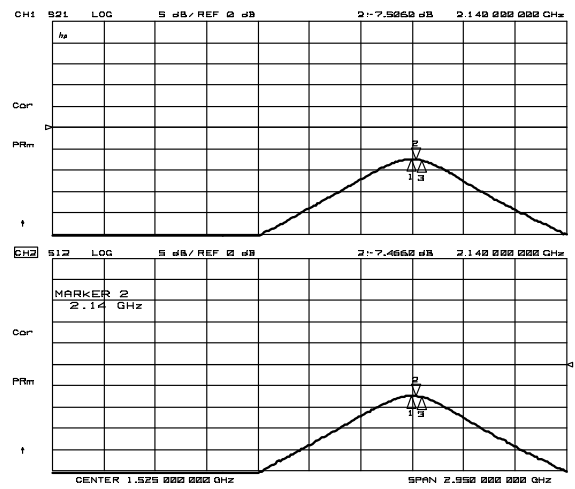


CH1 Markers

1:-14.447 dB
2:11000 GHz
3:-15.361 dB
2:17000 GHz

CH2 Markers

1:-17.023 dB
2:11000 GHz
3:-11.481 dB
2:17000 GHz

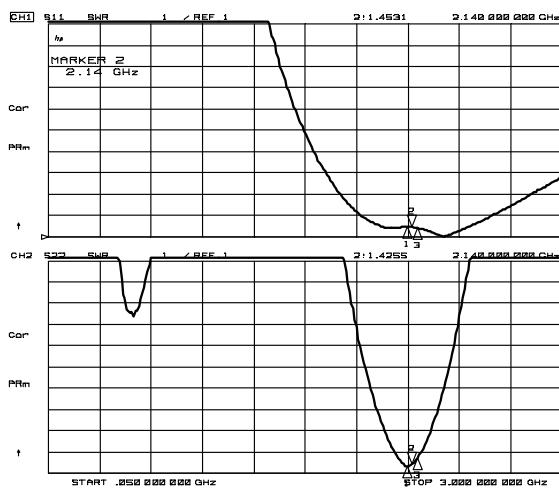


CH1 Markers

1:-7.440 dB
2:11000 GHz
3:-7.714 dB
2:17000 GHz

CH2 Markers

1:-7.440 dB
2:11000 GHz
3:-7.713 dB
2:17000 GHz

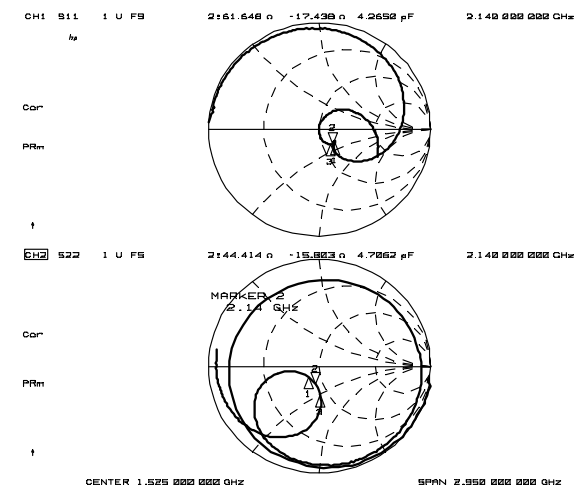


CH1 Markers

1:-1.4668
2:11000 GHz
3:-1.4105
2:17000 GHz

CH2 Markers

1:-1.3256
2:11000 GHz
3:-1.7556
2:17000 GHz

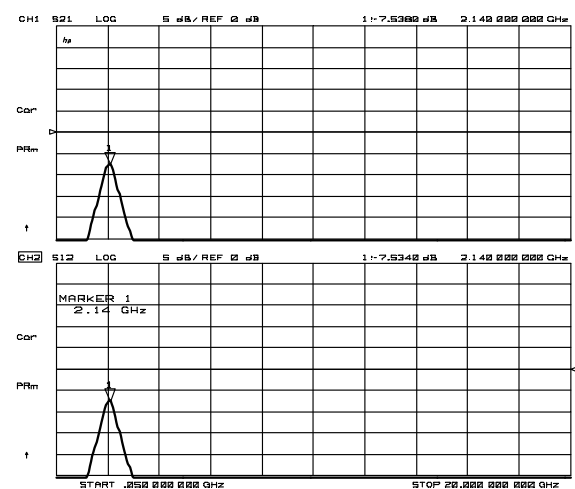
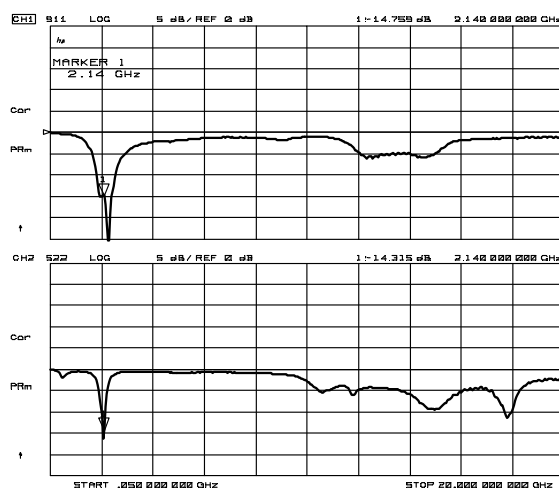


CH1 Markers

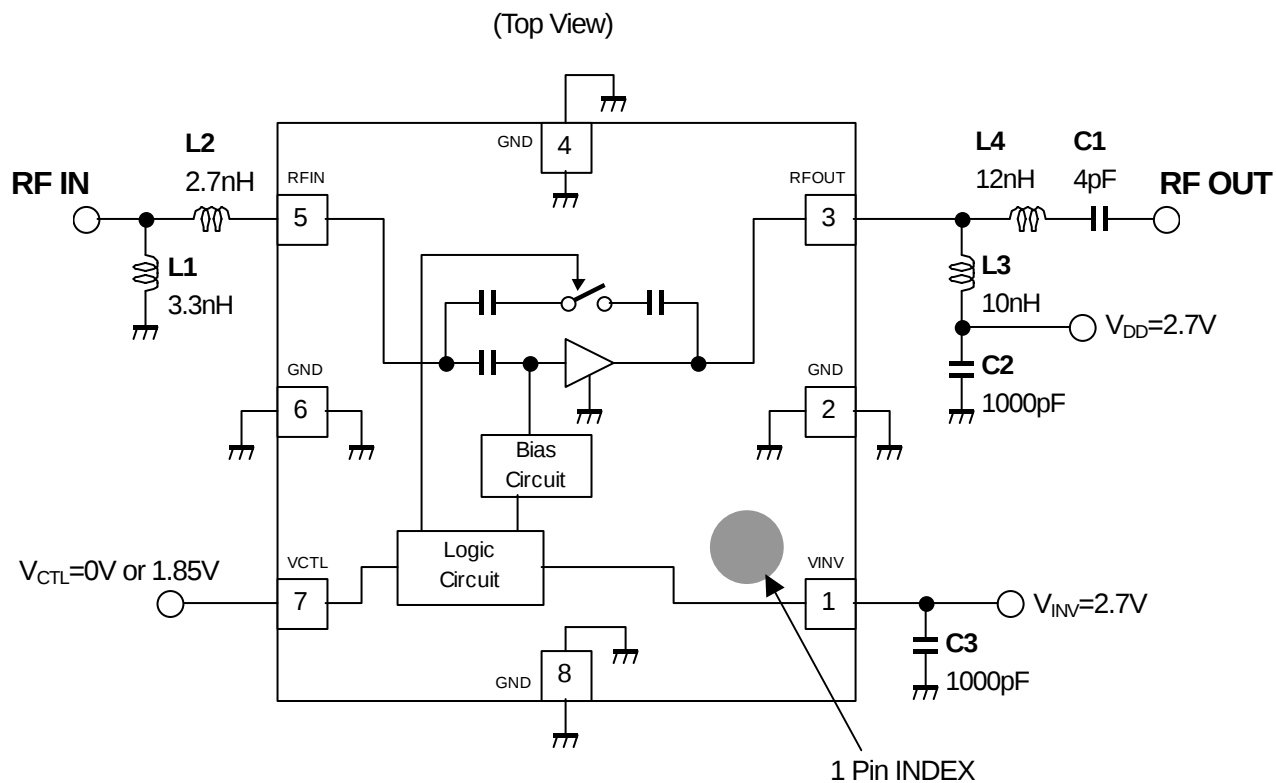
1:64.916 n
-16.932 Q
2:11000 GHz
3:58.572 n
-15.568 Q
2:17000 GHz

CH2 Markers

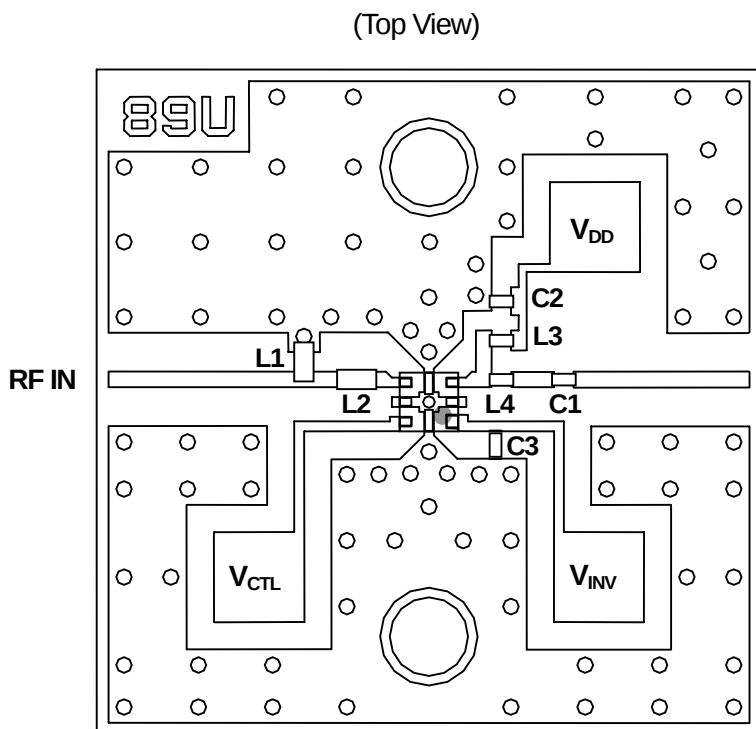
1:48.482 n
-9.8028 Q
2:11000 GHz
3:44.195 n
-25.348 Q
2:17000 GHz



APPLICATION CIRCUIT



TEST PCB LAYOUT



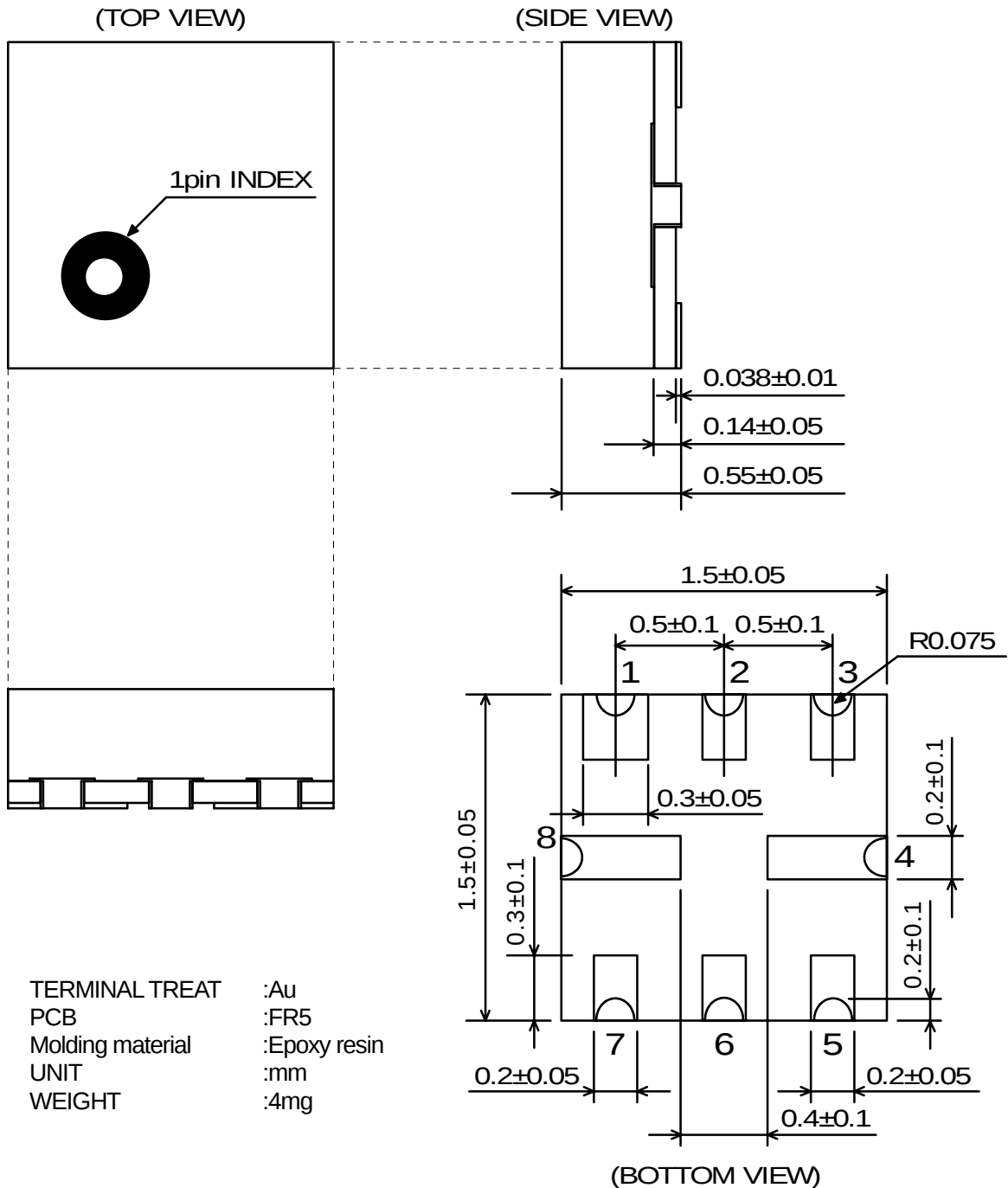
PARTS LIST

Parts ID	Comment
L1, L2	TAIYO-YUDEN (HK1005)
L3, L4	TDK (MLG0603Q)
C1~C3	MURATA (GRM03)

PCB (FR-4)
 $t=0.2\text{mm}$
 MICROSTRIP LINE WIDTH
 $=0.4\text{mm}$ ($Z_0=50\Omega$)
 PCB SIZE=17.0mmx17.0mm

NJG1126HB6

■PACKAGE OUTLINE (USB8-B6)



Cautions on using this product

This product contains Gallium-Arsenide (GaAs) which is a harmful material.

- Do NOT eat or put into mouth.
- Do NOT dispose in fire or break up this product.
- Do NOT chemically make gas or powder with this product.
- To waste this product, please obey the relating law of your country.

[CAUTION]

The specifications on this databook are only given for information, without any guarantee as regards either mistakes or omissions. The application circuits in this databook are described only to show representative usages of the product and not intended for the guarantee or permission of any right including the industrial rights.

This product may be damaged with electric static discharge (ESD) or spike voltage. Please handle with care to avoid these damages.

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Данный компонент на территории Российской Федерации

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