

Inverter Grade Thyristors (Stud Version), 195 A



TO-209AB (TO-93)

FEATURES

- Center amplifying gate
- High surge current capability
- Low thermal impedance
- High speed performance
- Compression bonding
- Designed and qualified for industrial level
- Material categorization: For definitions of compliance please see www.vishay.com/doc299912


RoHS
COMPLIANT

TYPICAL APPLICATIONS

- Inverters
- Choppers
- Induction heating
- All types of force-commutated converters

PRODUCT SUMMARY

$I_{T(AV)}$	195 A
V_{DRM}/V_{RRM}	400 V, 800 V
V_{TM}	1.80 V
I_{TSM} at 50 Hz	4900 A
I_{TSM} at 60 Hz	5130 A
I_{GT}	200 mA
T_J	-40 °C to 125 °C
Package	TO-209AB (TO-93)
Diode variation	Single SCR

MAJOR RATINGS AND CHARACTERISTICS

PARAMETER	TEST CONDITIONS	VALUES	UNITS
$I_{T(AV)}$		195	A
	T_C	85	°C
$I_{T(RMS)}$		306	A
I_{TSM}	50 Hz	4900	
	60 Hz	5130	
I^2t	50 Hz	120	kA ² s
	60 Hz	110	
V_{DRM}/V_{RRM}		400 to 800	V
t_q		15 to 20	μs
T_J		-40 to 125	°C

ELECTRICAL SPECIFICATIONS

VOLTAGE RATINGS

TYPE NUMBER	VOLTAGE CODE	V_{DRM}/V_{RRM} , MAXIMUM REPETITIVE PEAK VOLTAGE V	V_{RSM} , MAXIMUM NON-REPETITIVE PEAK VOLTAGE V	I_{DRM}/I_{RRM} MAXIMUM AT $T_J = T_J$ MAXIMUM mA
VS-ST183S	04	400	500	40
	08	800	900	

**CURRENT CARRYING CAPABILITY**

FREQUENCY							UNITS
50 Hz	570	370	900	610	7040	5220	A
400 Hz	560	360	940	630	3200	2280	
1000 Hz	500	300	925	610	1780	1200	
2500 Hz	340	190	760	490	880	560	
Recovery voltage V_r	50		50		50		V
Voltage before turn-on V_d	V_{DRM}		V_{DRM}		V_{DRM}		
Rise of on-state current di/dt	50		-		-		A/μs
Case temperature	60	85	60	85	60	85	°C
Equivalent values for RC circuit	47/0.22		47/0.22		47/0.22		Ω/μF

ON-STATE CONDUCTION

PARAMETER	SYMBOL	TEST CONDITIONS			VALUES	UNITS	
Maximum average on-state current at case temperature	I _{T(AV)}	180° conduction, half sine wave			195	A	
					85	°C	
Maximum RMS on-state current	I _{T(RMS)}	DC at 74 °C case temperature			306	A	
Maximum peak, one half cycle, non-repetitive surge current	I _{TSM}	t = 10 ms	No voltage reapplied	Sinusoidal half wave, initial T _J = T _J maximum	4900		
		t = 8.3 ms			5130		
		t = 10 ms	100 % V _{RRM} reapplied		4120		
		t = 8.3 ms			4310		
Maximum I ² t for fusing	I ² t	t = 10 ms	No voltage reapplied		120	kA ² s	
		t = 8.3 ms			110		
		t = 10 ms	100 % V _{RRM} reapplied		85		
		t = 8.3 ms			78		
Maximum I ² √t for fusing	I ² √t	t = 0.1 to 10 ms, no voltage reapplied			1200	kA ² √s	
Maximum peak on-state voltage	V _{TM}	I _{TM} = 600 A, T _J = T _J maximum, t _p = 10 ms sine wave pulse			1.80	V	
Low level value of threshold voltage	V _{T(TO)1}	(16.7 % × π × I _{T(AV)}) < I < π × I _{T(AV)} , T _J = T _J maximum			1.40		
High level value of threshold voltage	V _{T(TO)2}	(I > π × I _{T(AV)}), T _J = T _J maximum			1.45		
Low level value of forward slope resistance	r _{t1}	(16.7 % × π × I _{T(AV)}) < I < π × I _{T(AV)} , T _J = T _J maximum			0.67	mΩ	
High level value of forward slope resistance	r _{t2}	(I > π × I _{T(AV)}), T _J = T _J maximum			0.58		
Maximum holding current	I _H	T _J = 25 °C, I _T > 30 A			600	mA	
Typical latching current	I _L	T _J = 25 °C, V _A = 12 V, R _a = 6 Ω, I _G = 1 A			1000		

**SWITCHING**

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum non-repetitive rate of rise of turned-on current	di/dt	$T_J = T_J$ maximum, $V_{DRM} = \text{Rated } V_{DRM}$ $I_{TM} = 2 \times di/dt$	1000	A/ μ s
Typical delay time	t_d	$T_J = 25^\circ\text{C}$, $V_{DM} = \text{Rated } V_{DRM}$, $I_{TM} = 50$ A DC, $t_p = 1$ μ s Resistive load, gate pulse: 10 V, 5 Ω source	1.1	μ s
Maximum turn-off time	minimum t_q maximum	$T_J = T_J$ maximum, $I_{TM} = 300$ A, commutating $di/dt = 20$ A/ μ s $V_R = 50$ V, $t_p = 500$ μ s, $dV/dt: 200$ V/ μ s	15	
			20	

BLOCKING

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum critical rate of rise of off-state voltage	dV/dt	$T_J = T_J$ maximum, linear to 80 % V_{DRM} , higher value available on request	500	V/ μ s
Maximum peak reverse and off-state leakage current	I_{RRM} , I_{DRM}	$T_J = T_J$ maximum, rated V_{DRM}/V_{RRM} applied	40	mA

TRIGGERING

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum peak gate power	P_{GM}	$T_J = T_J$ maximum, $f = 50$ Hz, $d\% = 50$	60	W
Maximum average gate power	$P_{G(AV)}$		10	
Maximum peak positive gate current	I_{GM}	$T_J = T_J$ maximum, $t_p \leq 5$ ms	10	A
Maximum peak positive gate voltage	$+V_{GM}$		20	V
Maximum peak negative gate voltage	$-V_{GM}$		5	
Maximum DC gate current required to trigger	I_{GT}	$T_J = T_J$ maximum $V_A = 12$ V, $R_a = 6$ Ω	200	mA
Maximum DC gate voltage required to trigger	V_{GT}		3	V
Maximum DC gate current not to trigger	I_{GD}	$T_J = T_J$ maximum, rated V_{DRM} applied	20	mA
Maximum DC gate voltage not to trigger	V_{GD}		0.25	V

THERMAL AND MECHANICAL SPECIFICATIONS

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum junction operating temperature range	T_J		-40 to 125	$^\circ\text{C}$
Maximum storage temperature range	T_{Stg}		-40 to 150	
Maximum thermal resistance, junction to case	R_{thJC}	DC operation	0.105	K/W
Maximum thermal resistance, case to heatsink	R_{thCS}	Mounting surface, smooth, flat and greased	0.04	
Mounting torque, ± 10 %		Non-lubricated threads	31 (275)	N $\cdot$ m (lbf $\cdot$ in)
		Lubricated threads	24.5 (210)	
Approximate weight			280	g
Case style		See dimensions - link at the end of datasheet	TO-209AB (TO-93)	

 ΔR_{thJC} CONDUCTION

CONDUCTION ANGLE	SINUSOIDAL CONDUCTION	RECTANGULAR CONDUCTION	TEST CONDITIONS	UNITS
180 $^\circ$	0.016	0.012	$T_J = T_J$ maximum	K/W
120 $^\circ$	0.019	0.020		
90 $^\circ$	0.025	0.027		
60 $^\circ$	0.036	0.037		
30 $^\circ$	0.060	0.060		

Note

- The table above shows the increment of thermal resistance R_{thJC} when devices operate at different conduction angles than DC

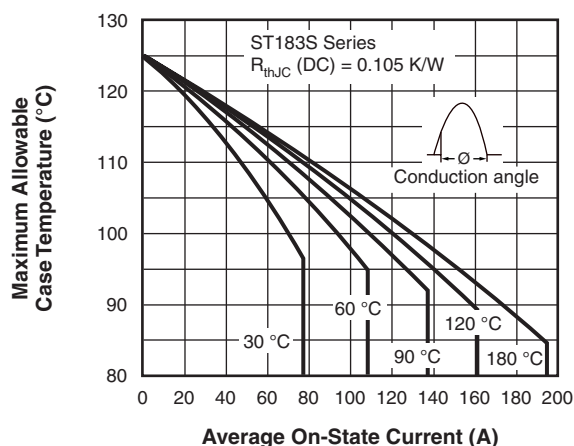


Fig. 1 - Current Ratings Characteristics

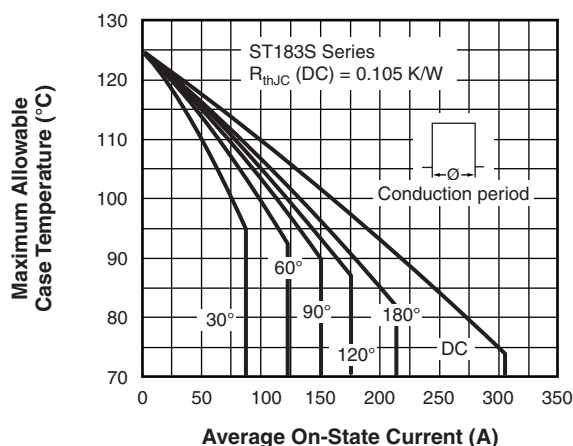


Fig. 2 - Current Ratings Characteristics

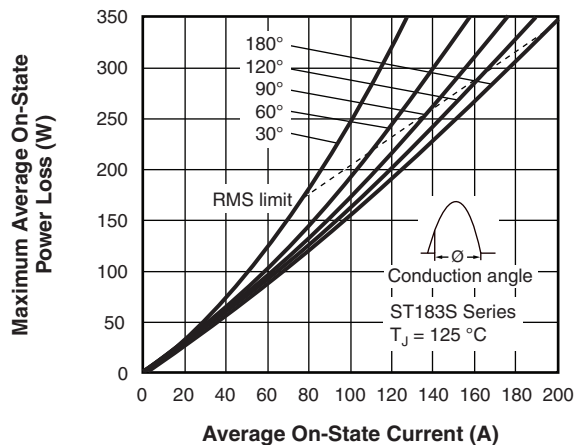


Fig. 3 - On-State Power Loss Characteristics

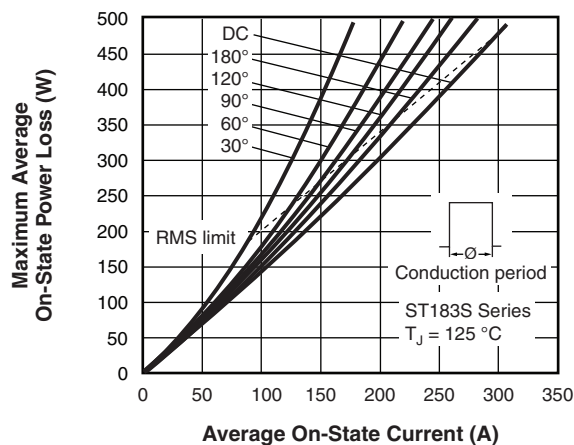
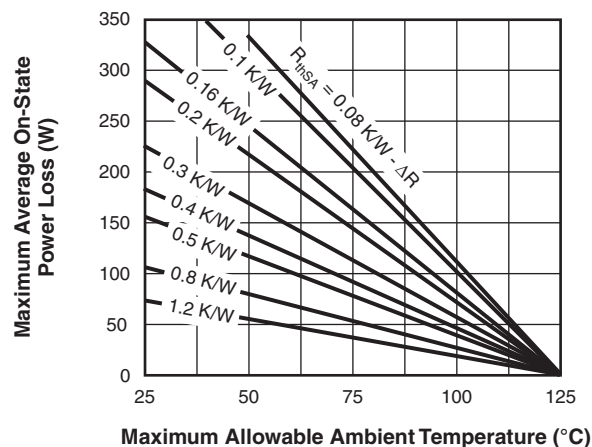
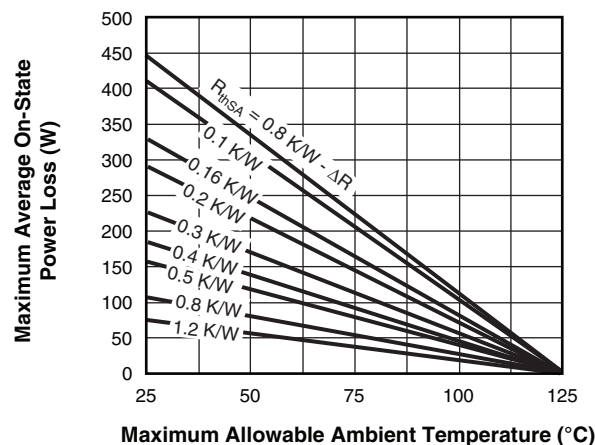


Fig. 4 - On-State Power Loss Characteristics



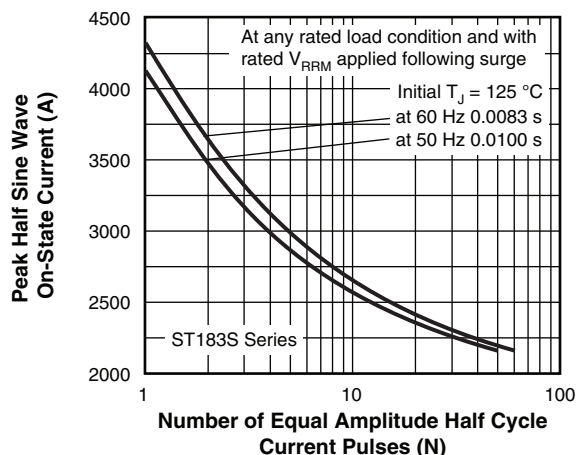


Fig. 5 - Maximum Non-Repetitive Surge Current

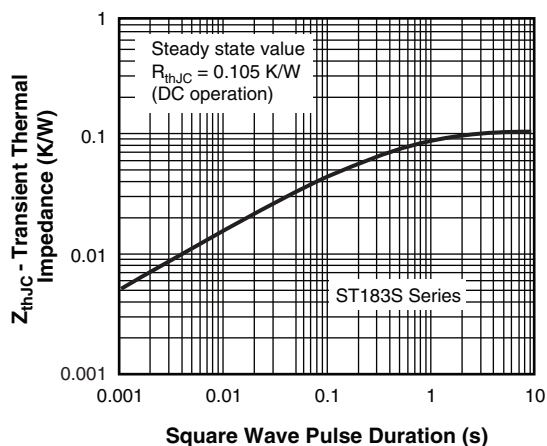
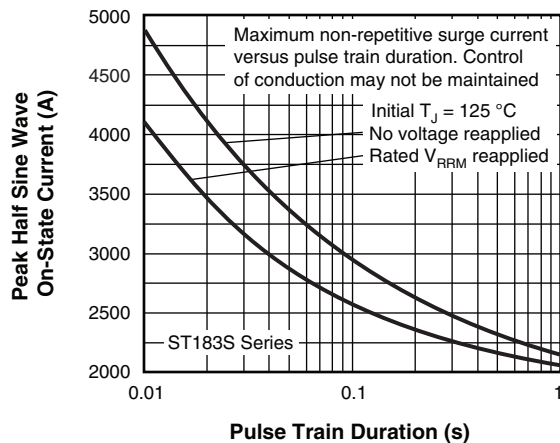

Fig. 8 - Thermal Impedance Z_{thJC} Characteristics


Fig. 6 - Maximum Non-Repetitive Surge Current

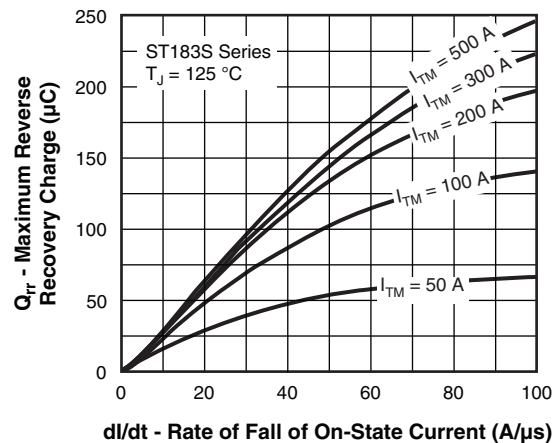


Fig. 9 - Reverse Recovered Charge Characteristics

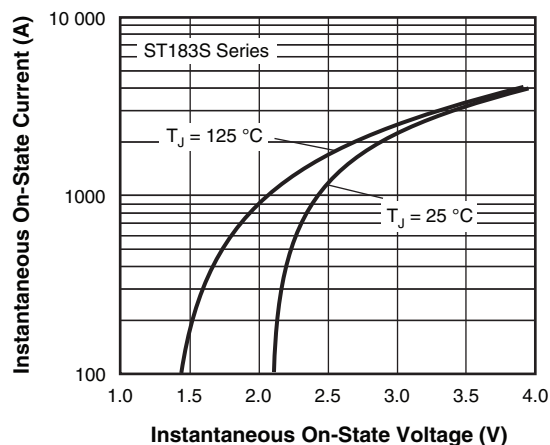


Fig. 7 - On-State Voltage Drop Characteristics

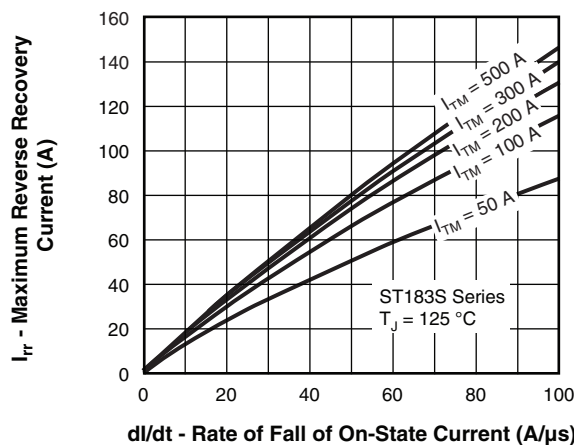


Fig. 10 - Reverse Recovery Current Characteristics

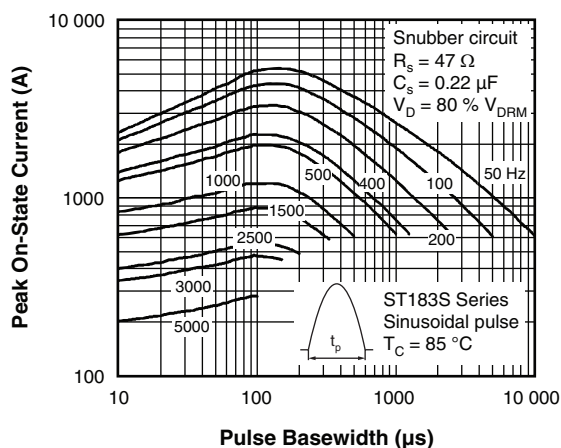
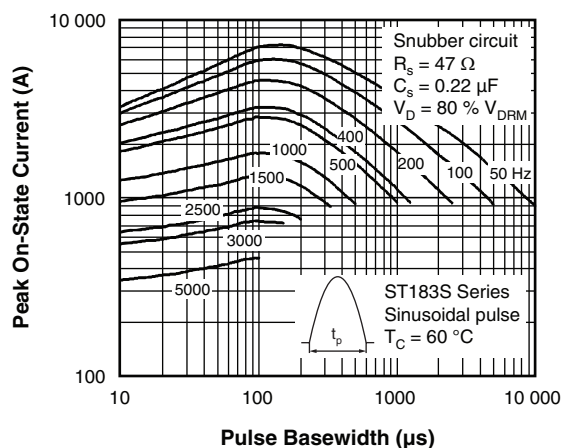


Fig. 11 - Frequency Characteristics

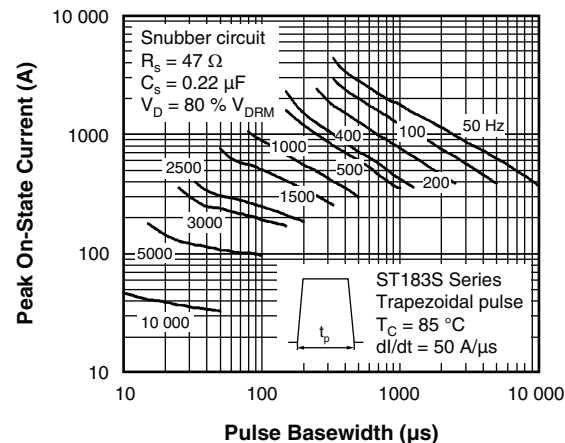
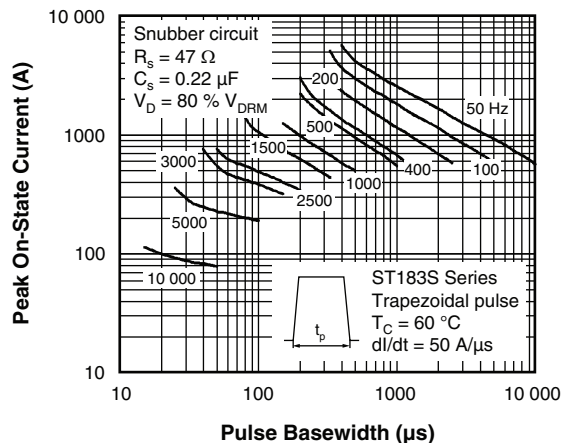


Fig. 12 - Frequency Characteristics

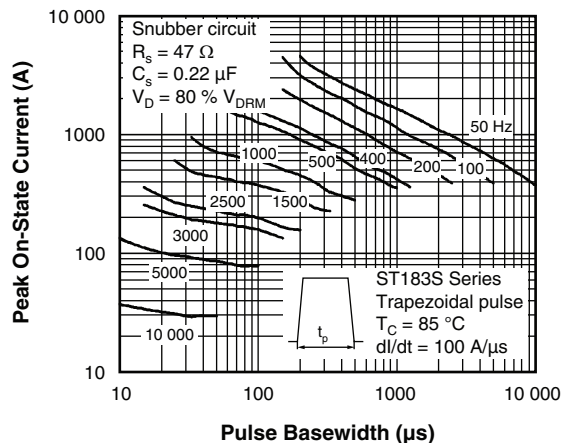
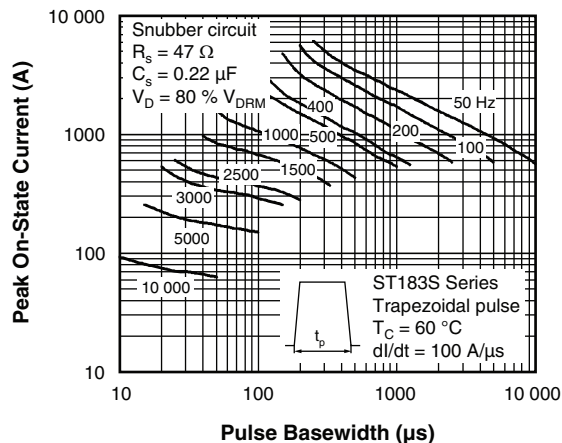


Fig. 13 - Frequency Characteristics

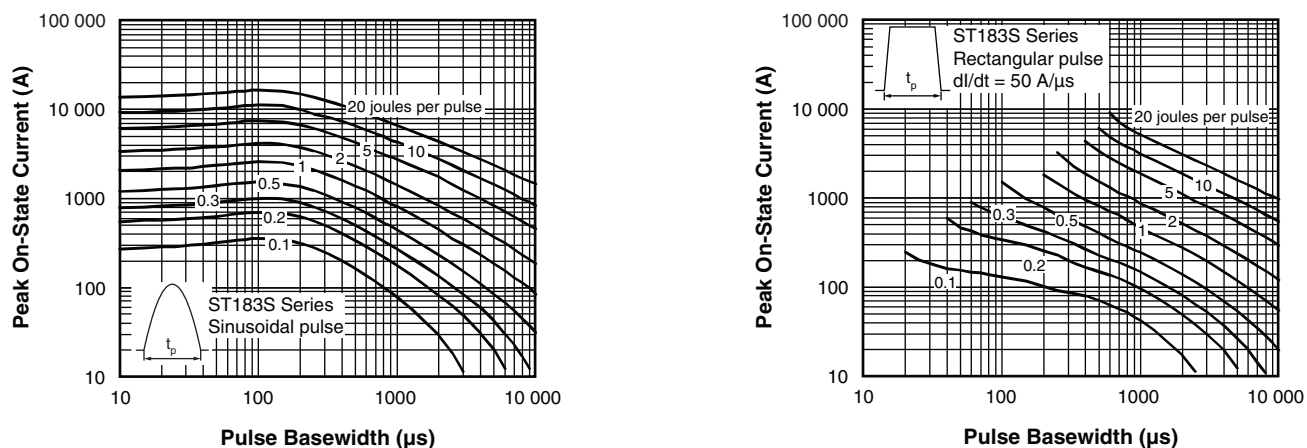


Fig. 14 - Maximum On-State Energy Power Loss Characteristics

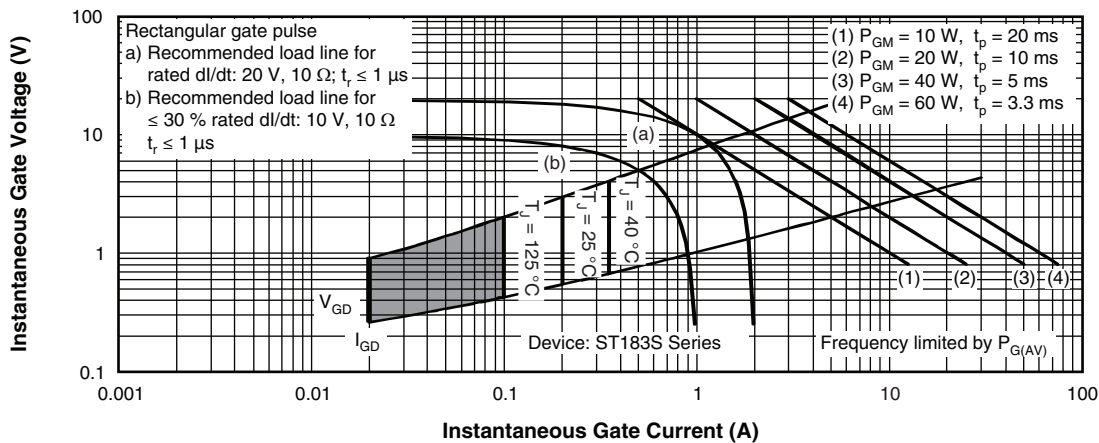


Fig. 15 - Gate Characteristics


ORDERING INFORMATION TABLE

Device code	VS-	ST	18	3	S	08	P	F	K	0	P
	1	2	3	4	5	6	7	8	9	10	11
1	- Vishay Semiconductors product										
2	- Thyristor										
3	- Essential part number										
4	- 3 = Fast turn-off										
5	- S = Compression bonding stud										
6	- Voltage code x 100 = V_{RRM} (see Voltage Ratings table)										
7	- P = Stud base 3/4" 16UNF-2A										
8	- Reapplied dV/dt code (for t_q test condition)										
9	- t_q code										
10	- 0 = Eyelet terminals (gate and auxiliary cathode leads) 1 = Fast-on terminals (gate and auxiliary cathode leads)										
11	- None = standard production - P = Lead (Pb)-free										

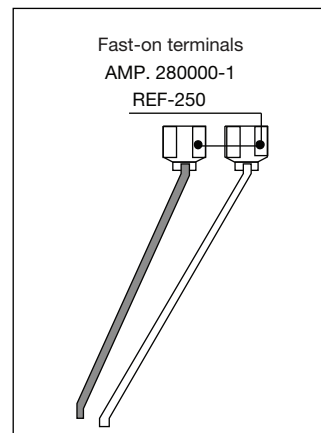
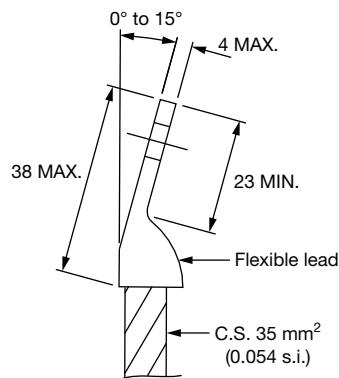
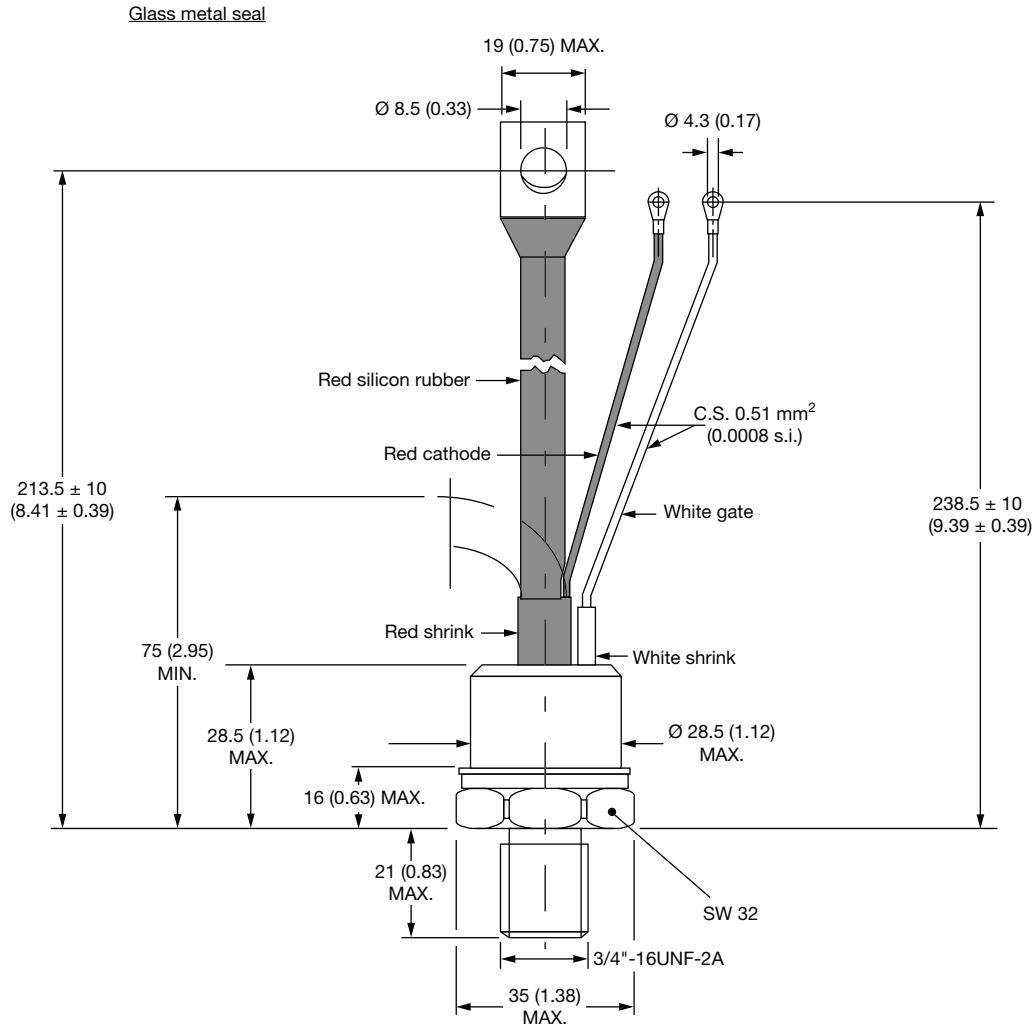
dV/dt - t_q combinations available		
dV/dt (V/ μ s)		200
t_q (μ s)	15	FL
	20	FK

Note: For metric device M16 x 1.5 contact factory

LINKS TO RELATED DOCUMENTS	
Dimensions	www.vishay.com/doc?95077

TO-209AB (TO-93)

DIMENSIONS in millimeters (inches)





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