TVS Diodes

Transient Voltage Suppressor Diodes

ESD102-U1-02ELS

Uni-directional Ultra-low Capacitance ESD / Transient Protection Diode

ESD102-U1-02ELS

Data Sheet

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1 Uni-directional Ultra-low Capacitance ESD / Transient Protection Diode

1.1 Features

- ESD / Transient protection of high speed data lines exceeding
  - **IEC61000-4-2 (ESD): ±20 kV (air / contact)**
  - **IEC61000-4-4 (EFT): ±2.5 kV / 50 A (5/50 ns)**
  - **IEC61000-4-5 (surge): ±3 A (8/20 µs)**
- Maximum working voltage: V_{RWM} **= 3.3 V**
- Ultra low capacitance C_L **= 0.4 pF (typical)**
- Very low clamping voltage: V_{CL} **= 8 V** (typical)at I_{PP} = 16 A **[2]**
- Very low dynamic resistance: R_{DYN} **= 0.19 Ω (typical)** **[2]**
- Pb-free (RoHS compliant) and halogen free package, very small form factor 0.62 x 0.32 x 0.31 mm^3

1.2 Application Examples

- USB 3.0, 10/100/1000 Ethernet, Firewire, DVI, HDMI, S-ATA, DisplayPort
- Mobile HDMI Link, MDDI, MIPI, SWP / NFC

1.3 Product Description

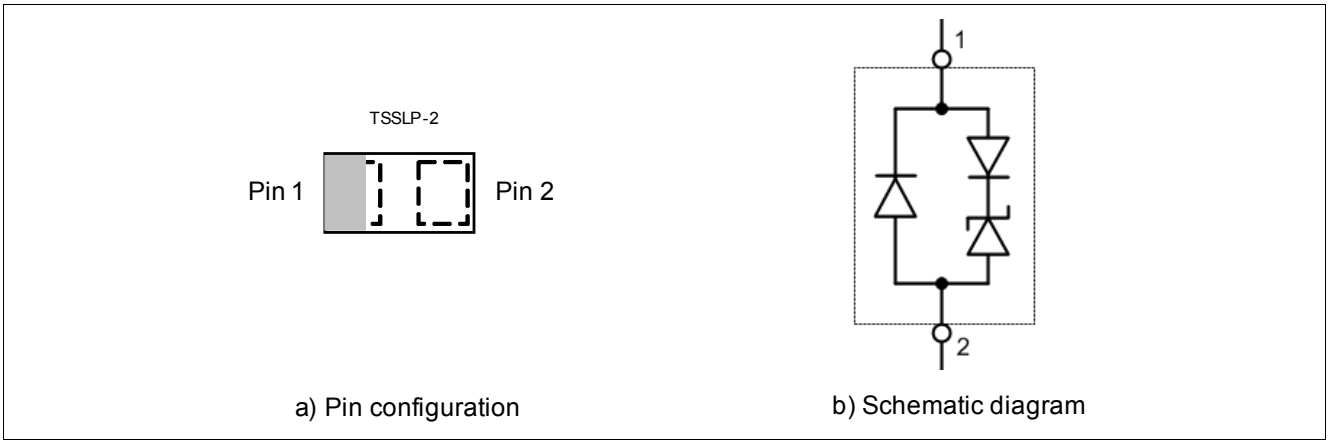

Figure 1 Pin Configuration and Schematic Diagram

Table 1 Ordering Information

Type	Package	Configuration	Marking code
ESD102-U1-02ELS	TSSLP-2-3	1 line, uni-directional	F

2 Characteristics

Table 2 Maximum Rating at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit
		Min.	Typ.	Max.	
ESD (air / contact) discharge[1)]	V_{ESD}	-20	–	20	kV
Peak pulse current (t_p = 8/20 µs)[2)]	I_{PP}	-3	–	3	A
Operating temperature range	T_{OP}	-40	–	125	°C
Storage temperature	T_{stg}	-65	–	150	°C

1) V_{ESD} according to IEC61000-4-2 (R = 330 Ω, C = 150 pF)

2) I_{PP} according to IEC61000-4-5

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

2.1 Electrical Characteristics at T_A = 25 °C, unless otherwise specified

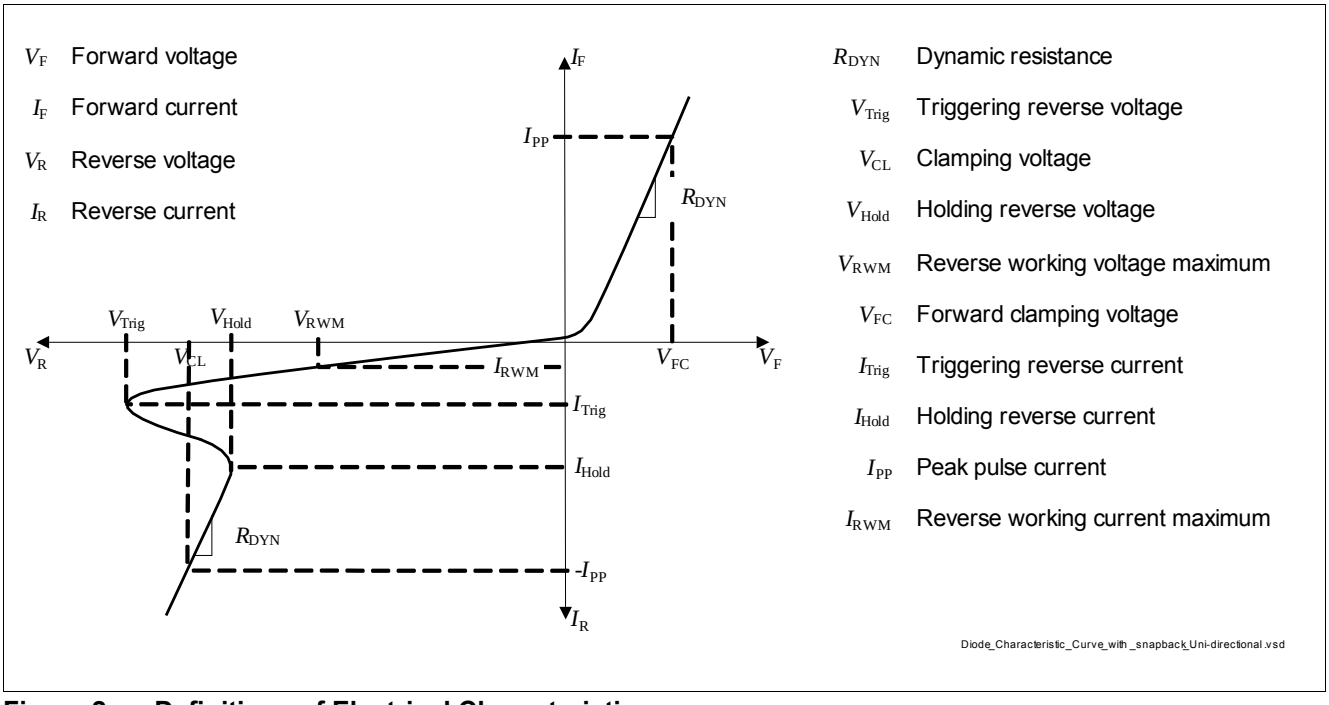

Figure 2 Definitions of Electrical Characteristics

Table 3 DC Characteristics at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Reverse working voltage	V_{RWM}	–	–	3.3	V	Pin 1 to Pin 2
Breakdown voltage	V_{BR}	–	6.5	–	V	from Pin 1 to Pin 2 voltage forced
Reverse current	I_R	–	1	50	nA	V_R = 3.3 V, from Pin 1 to Pin 2

Table 4 RF Characteristics at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Line capacitance[1]	C_L	–	0.4	0.65	pF	V_R = 0 V, f = 1 MHz
		–	0.4	0.65	pF	V_R = 0 V, f = 1 GHz
Series inductance	L_S	–	0.2	–	nH	

1) Total capacitance line to ground

Table 5 ESD Characteristics at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Trigger voltage[1] **[2]**	V_{TRIG}	–	7.2	–	V	TLP, from Pin 1 to Pin 2
Reverse clamping voltage[1] **[2]**	V_{CL}	–	8	–	V	TLP, I_{PP} = 16 A, from Pin 1 to Pin 2
		–	11	–	V	TLP, I_{PP} = 30 A, from Pin 1 to Pin 2
Forward clamping voltage[1] **[2]**	V_{FC}	–	6	–	V	TLP, I_{PP} = 16 A, from Pin 2 to Pin 1
		–	9	–	V	TLP, I_{PP} = 30 A, from Pin 2 to Pin 1
Dynamic resistance[1] **[2]**	R_{DYN}	–	0.19	–	Ω	TLP, Pin 1 to Pin 2
		–	0.23	–	Ω	TLP, Pin 2 to Pin 1

1) Please refer to Application Note AN210. ANSI/ESD STM5.5.1 - Electrostatic Discharge Sensitivity Testing using Transmission Line Pulse (TLP), t_p = 100ns, t_r = 0.6 ns, I_{TLP} and V_{TLP} averaging window: t_1 = 30 ns to t_2 = 60 ns, extraction of dynamic TLP characteristic between I_{PP1} = 10 A and I_{PP2} = 40 A.

2.2 Typical Characteristics at T_A=25°C, unless otherwise specified

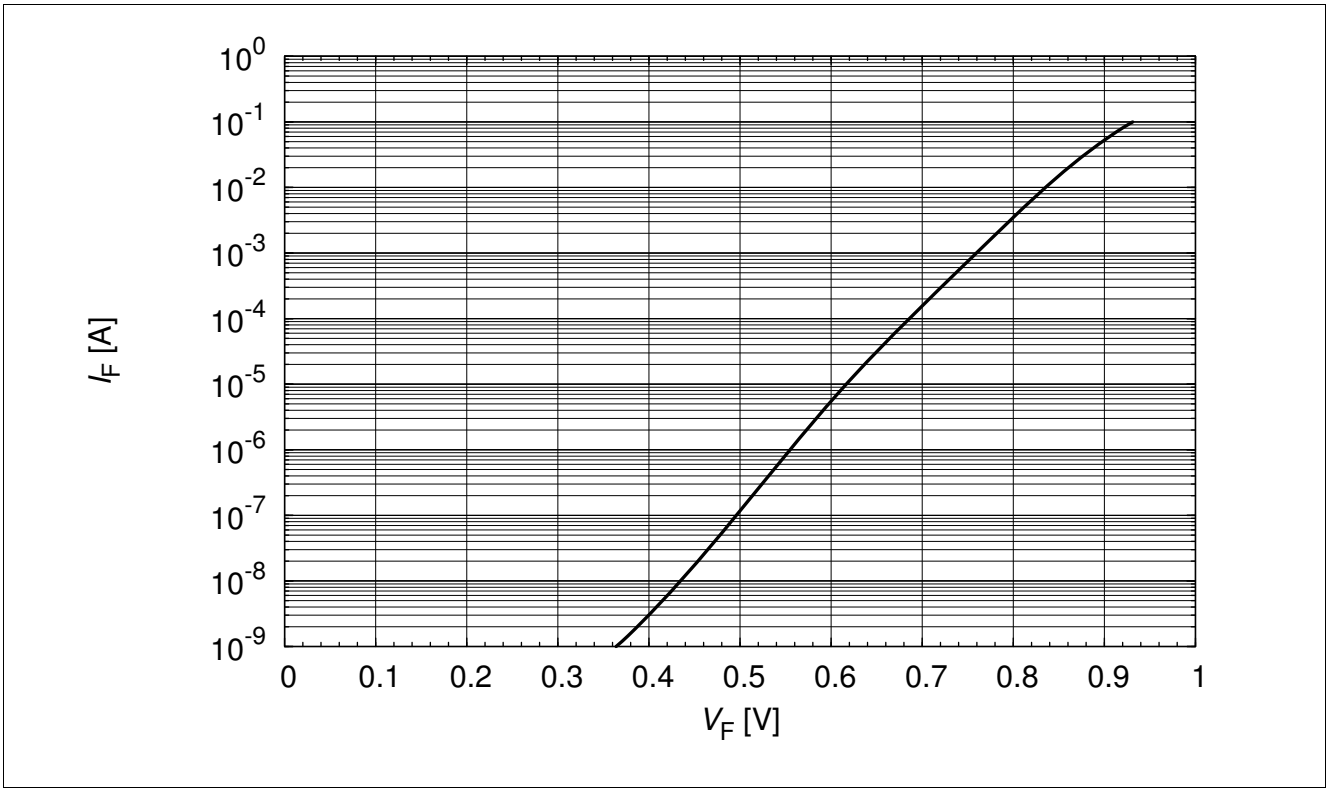

Figure 3 Forward current, $I_F = (V_F)$

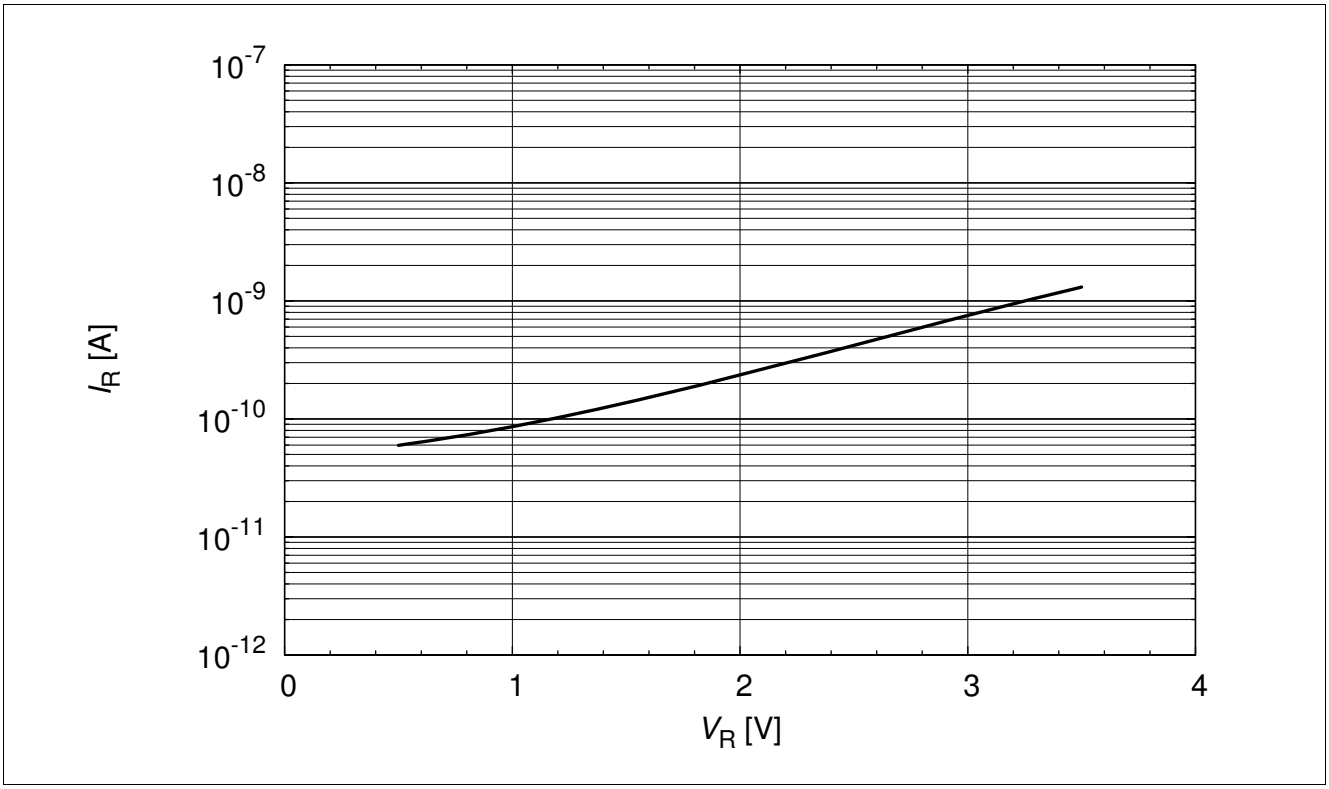

Figure 4 Reverse current, $I_R = (V_R)$

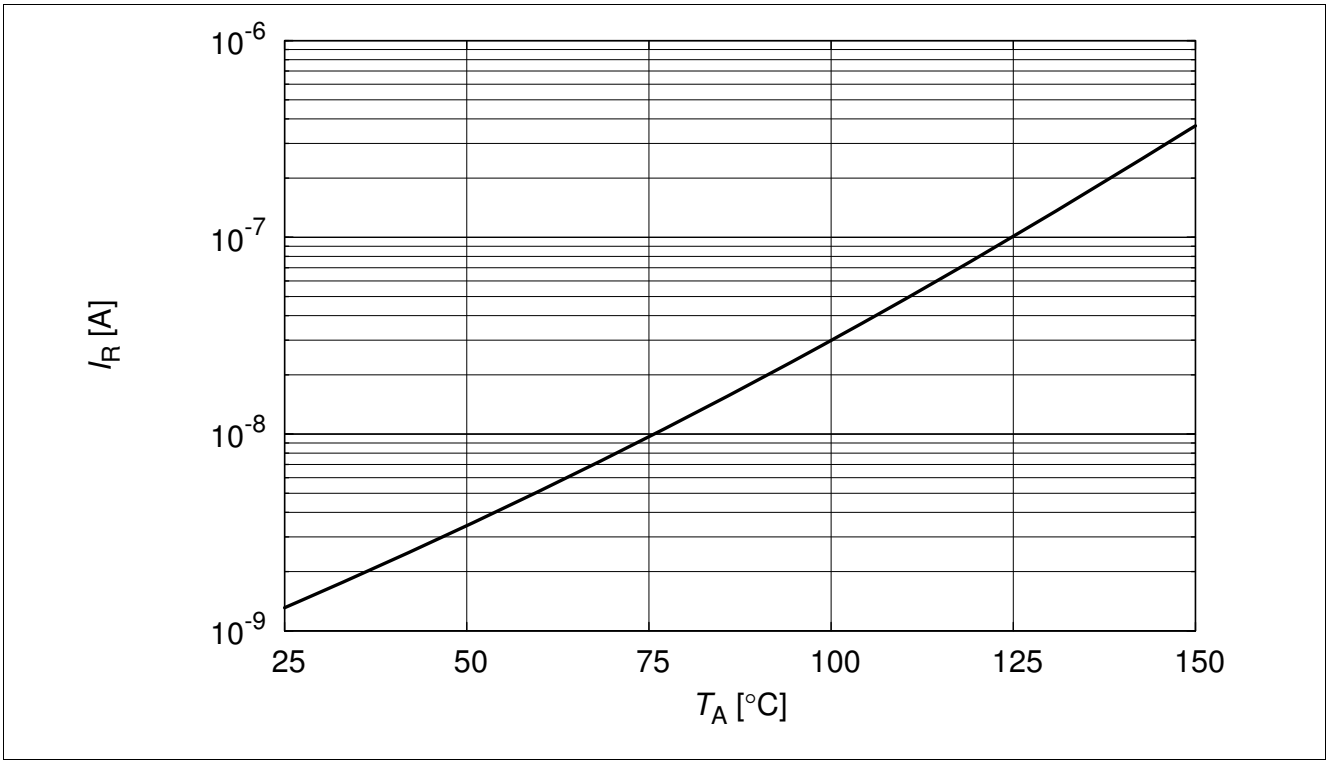

Figure 5 **Reverse current $I_R = f(T_A)$, V_R = 3.3 V**

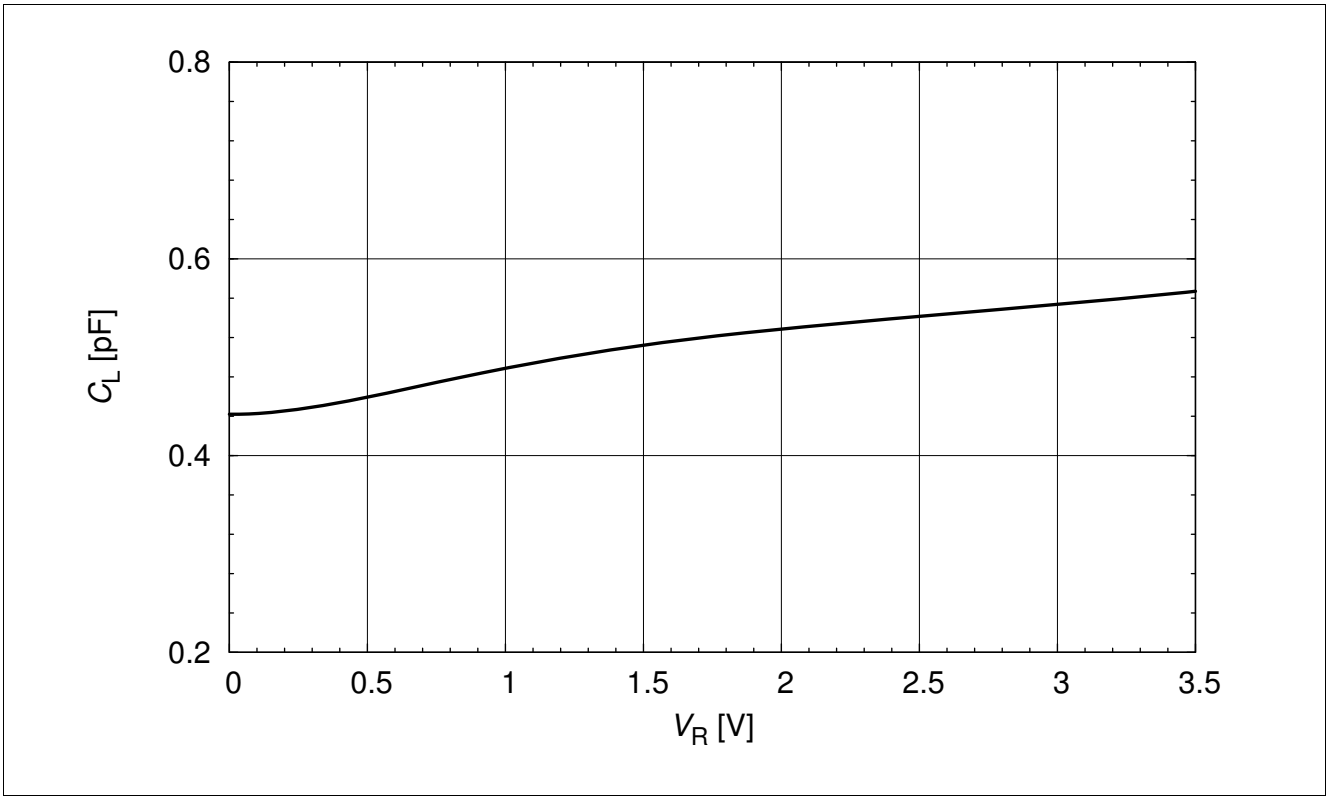

Figure 6 **Line capacitance $C_L = f(V_R)$, f = 1MHz, from pin 1 to pin 2**

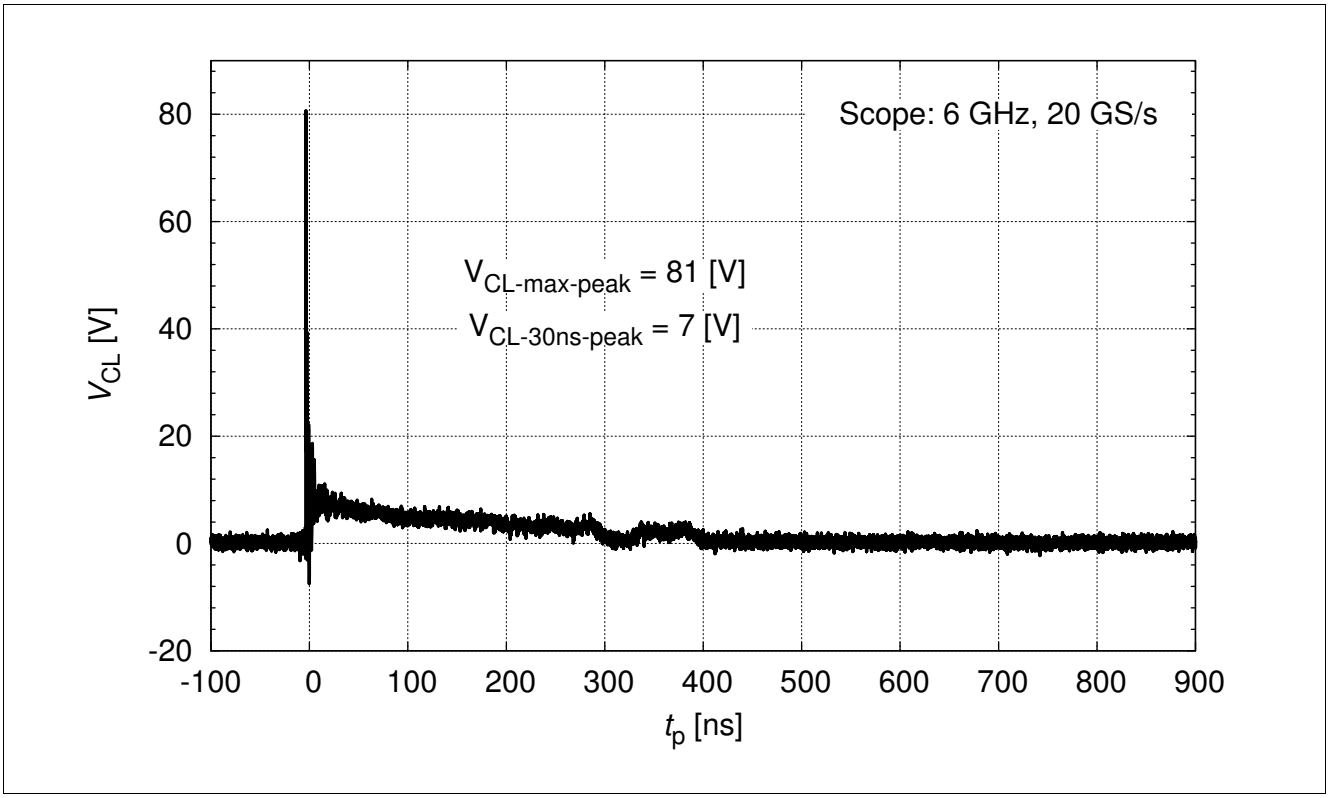

Figure 7 IEC61000-4-2 V_{CL} = *f*(*t*), 8 kV positive pulse from pin 1 to pin 2

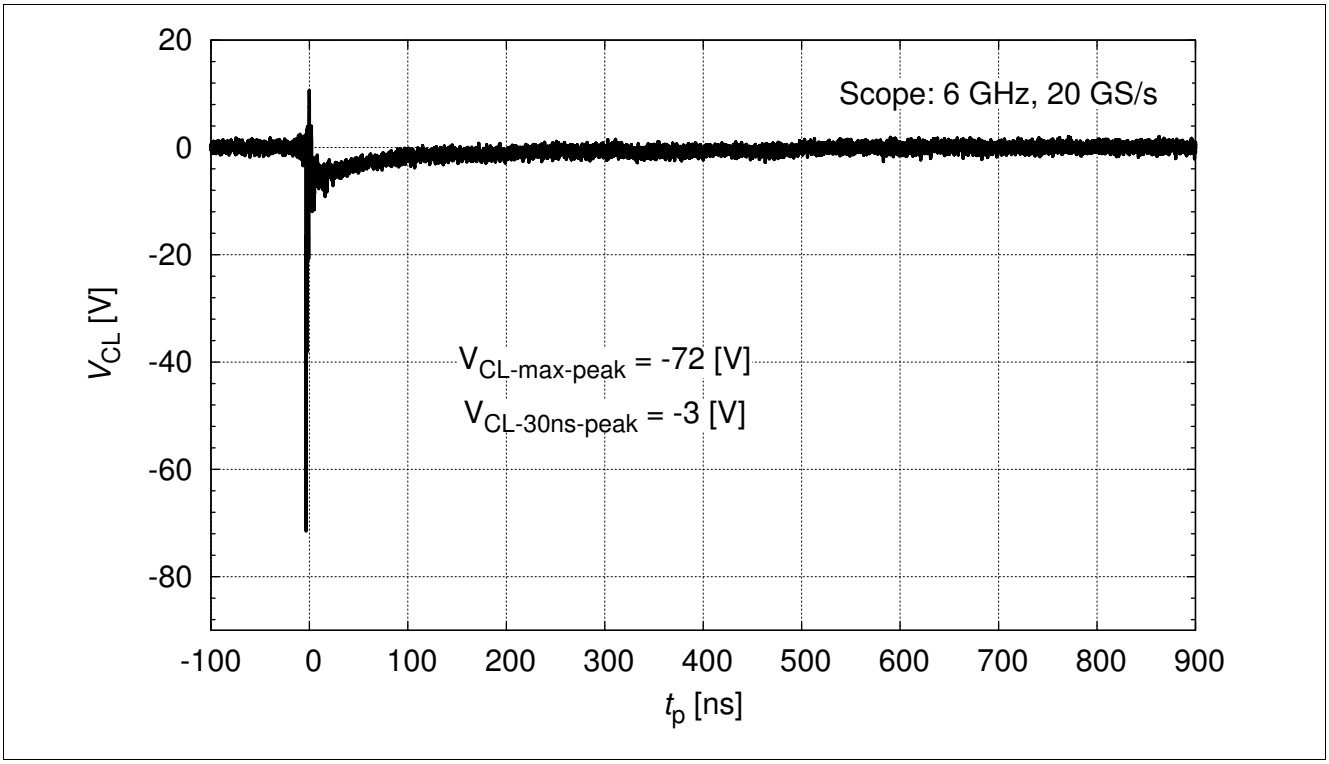

Figure 8 IEC61000-4-2 V_{CL} = *f*(*t*), 8 kV negative pulse from pin 1 to pin 2

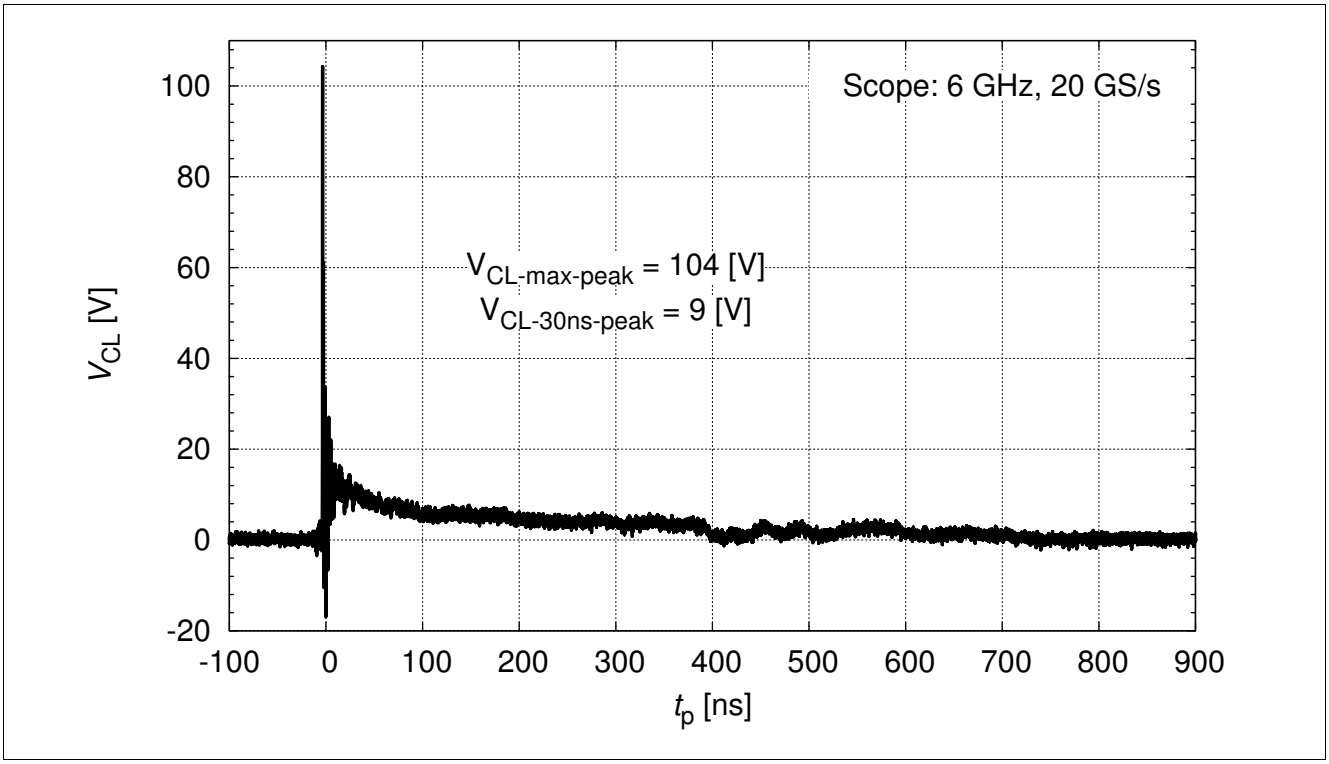

Figure 9 IEC61000-4-2 $V_{CL} = f(t)$, 15 kV positive pulse from pin 1 to pin 2

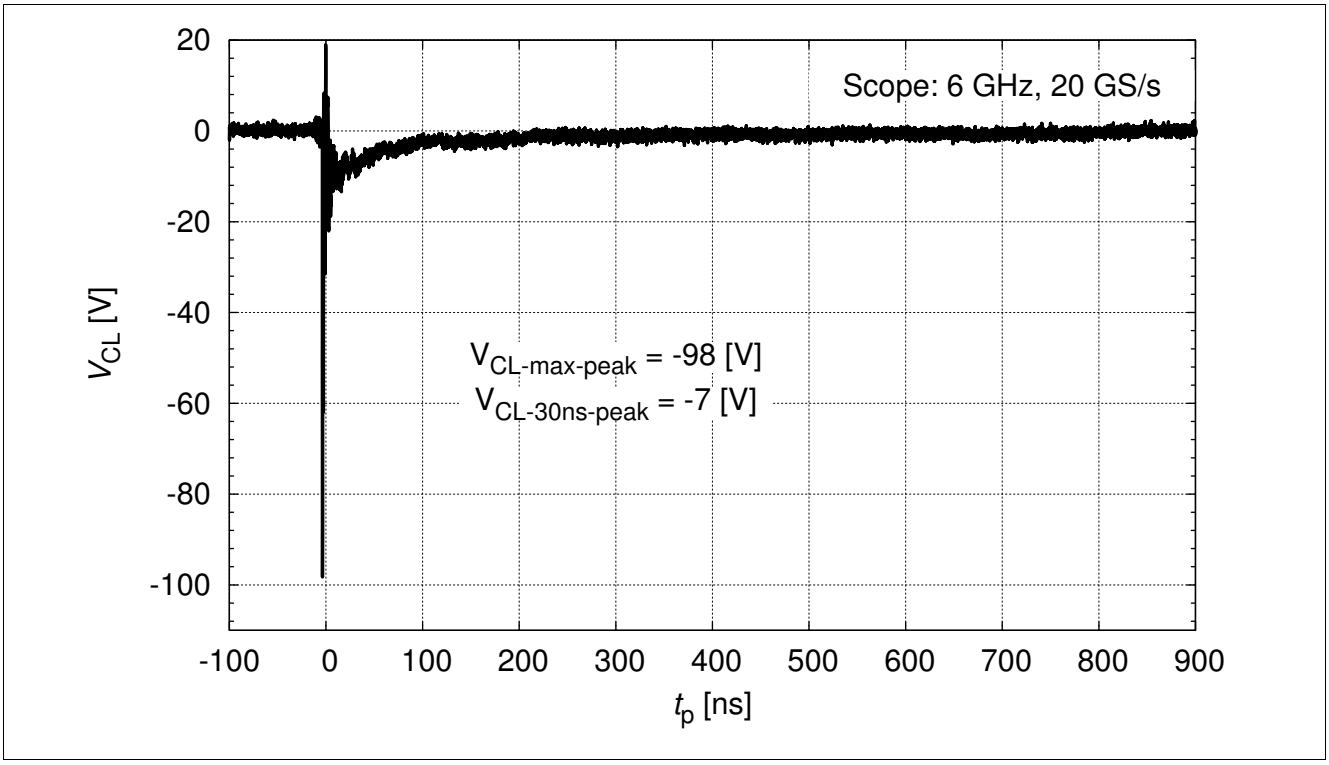

Figure 10 IEC61000-4-2 $V_{CL} = f(t)$, 15 kV negative pulse from pin 1 to pin 2

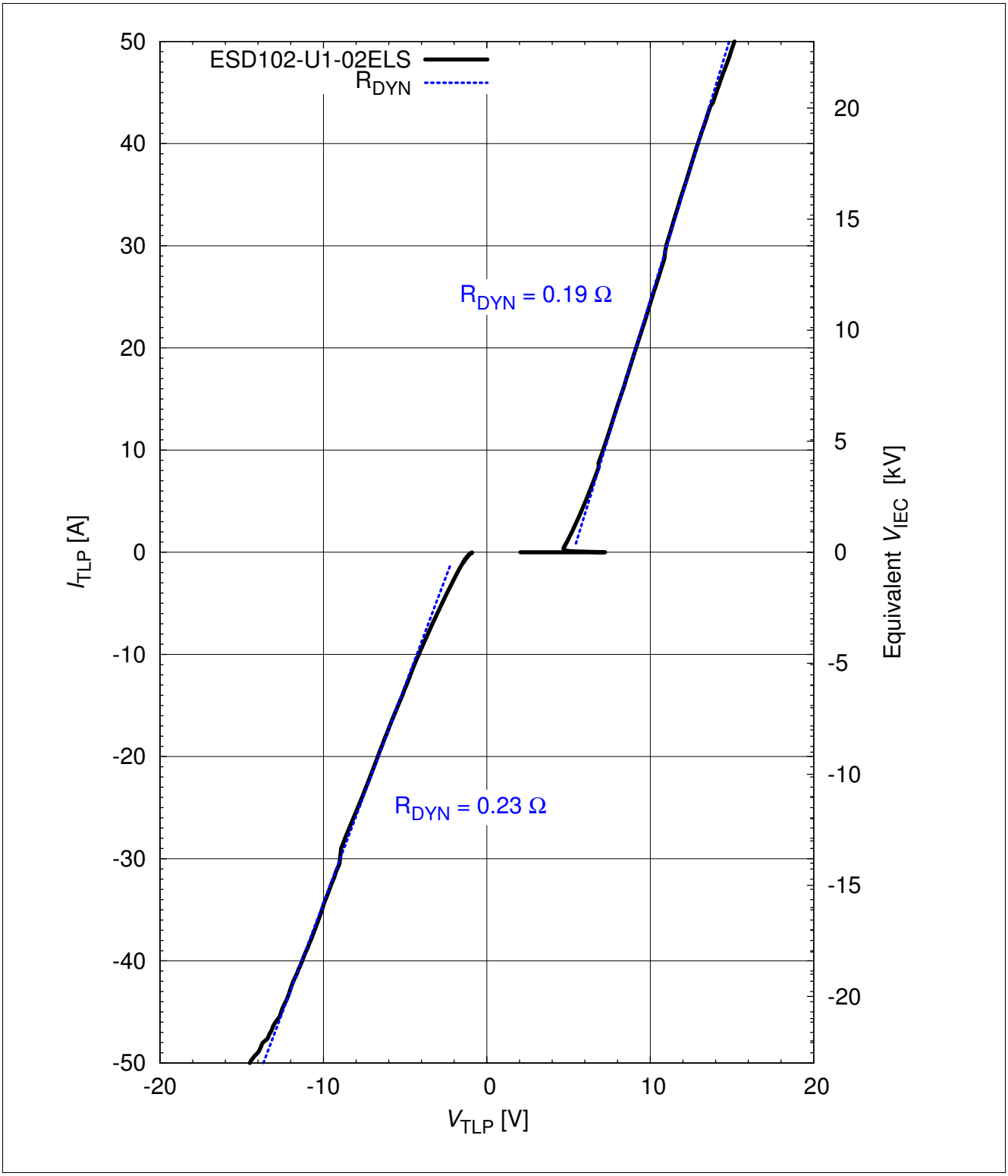

Figure 11 Clamping voltage $V_{TLP} = f(I_{TLP})$, [2]

Note: TLP parameter: Z_0 = 50 Ω, t_p = 100 ns, t_r = 600 ps, averaging window: t_1 = 30 ns to t_2 = 60 ns, extraction of dynamic resistance using least squares fit of TLP charactertistic between I_{PP1} = 10 A and I_{PP2} = 40 A. The equivalent stress level V_{IEC} according IEC 61000-4-2 (R = 330 Ω, C = 150 pF) is calculated at the broad peak of the IEC waveform at t = 30 ns with 2 A / kV

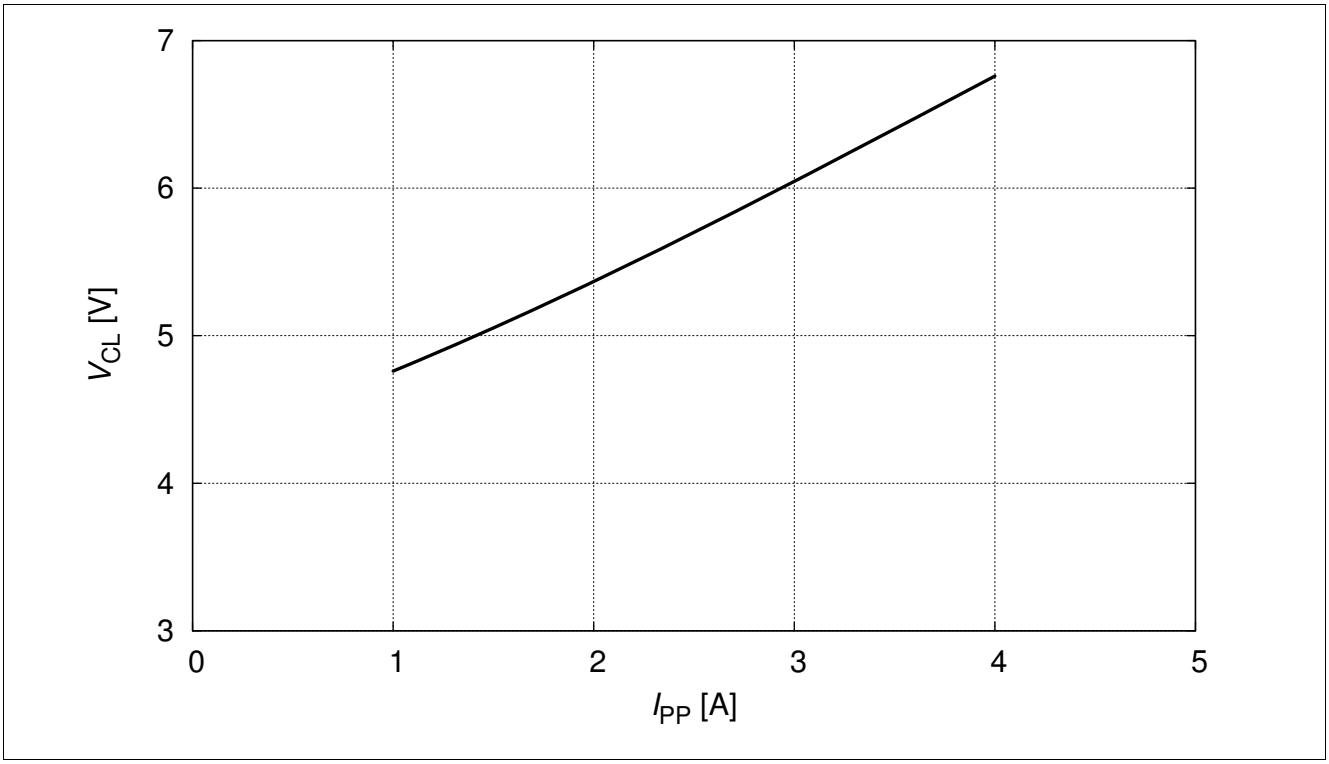

Figure 12 Reverse clamping voltage $I_{PP} = f(V_{CL})$, from pin 1 to pin 2 according to IEC61000-4-5 (8/20 µs)

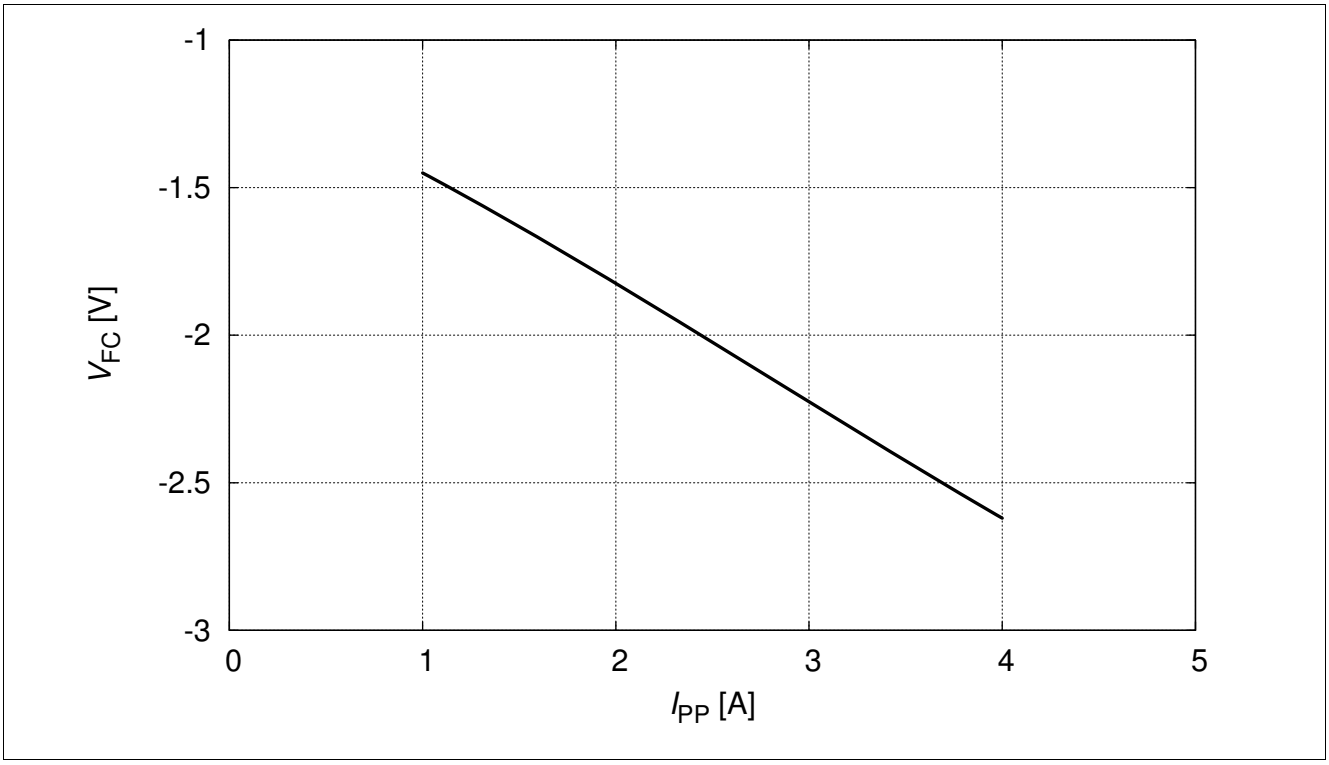

Figure 13 Forward clamping voltage $I_{PP} = f(V_{FC})$, from pin 1 to pin 2 according to IEC61000-4-5 (8/20 µs)

3 Application Information

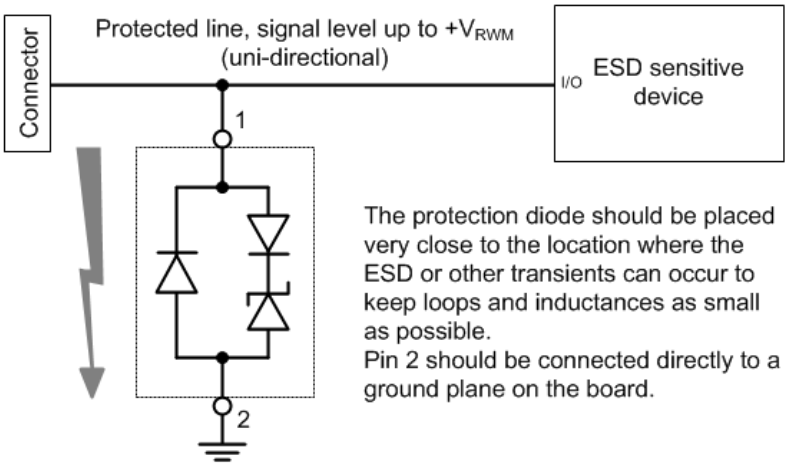

Figure 14 Single line, uni-directional ESD / Transient protection[2]

4 Package Information

4.1 TSSLP-2-3 (mm) [3]

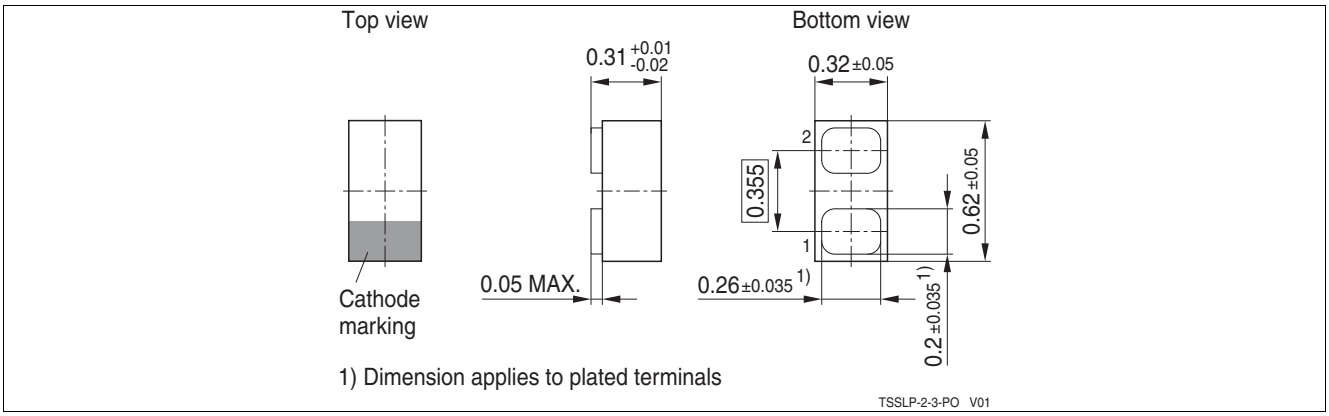

Figure 15 Package outline for TSSLP-2-3 (dimension in mm)

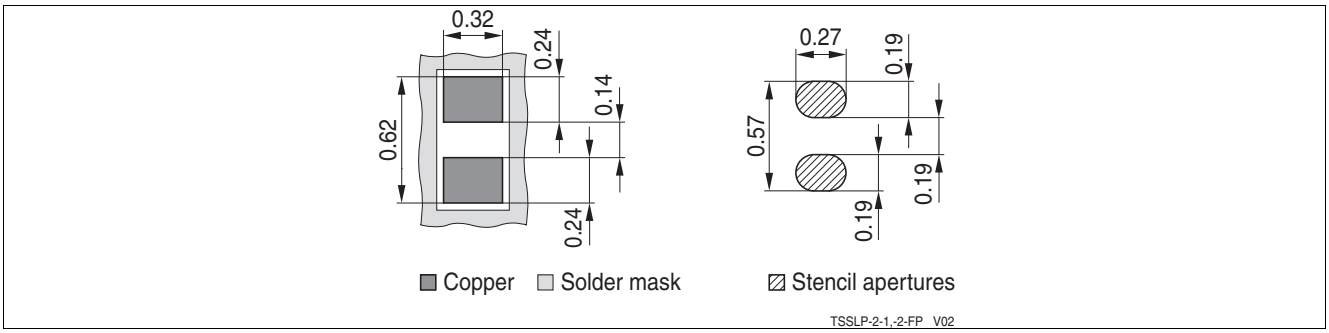

Figure 16 Package footprint for TSSLP-2-3 (dimension in mm)

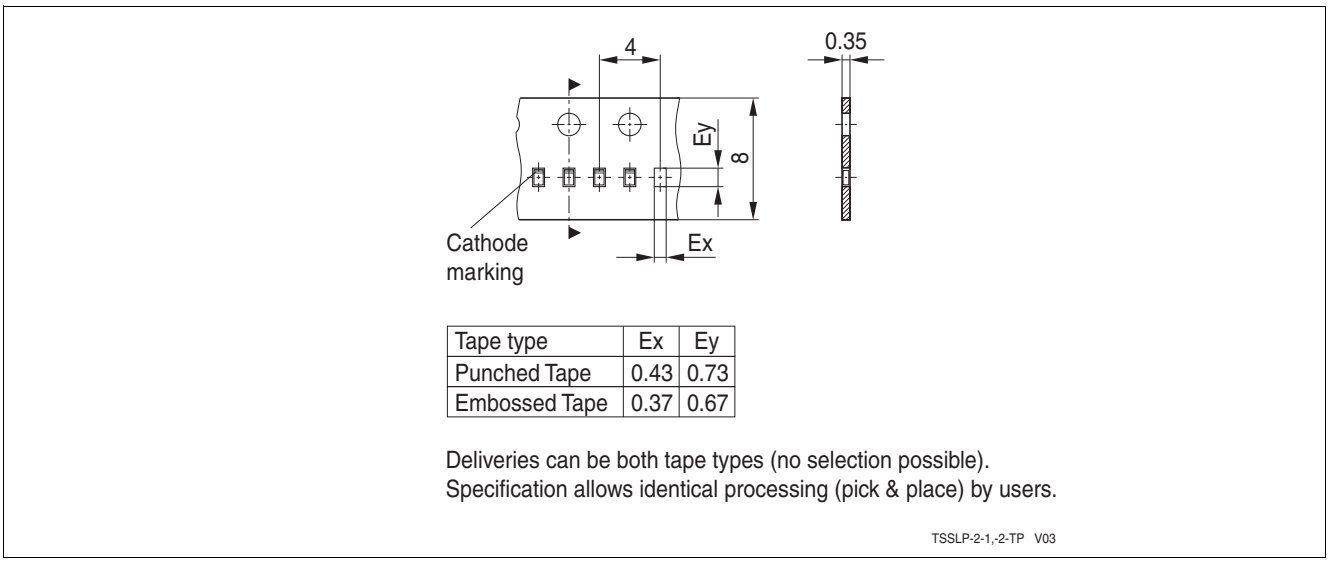

Figure 17 Tape and Reel Information for TSSLP-2-3 (dimension in mm)

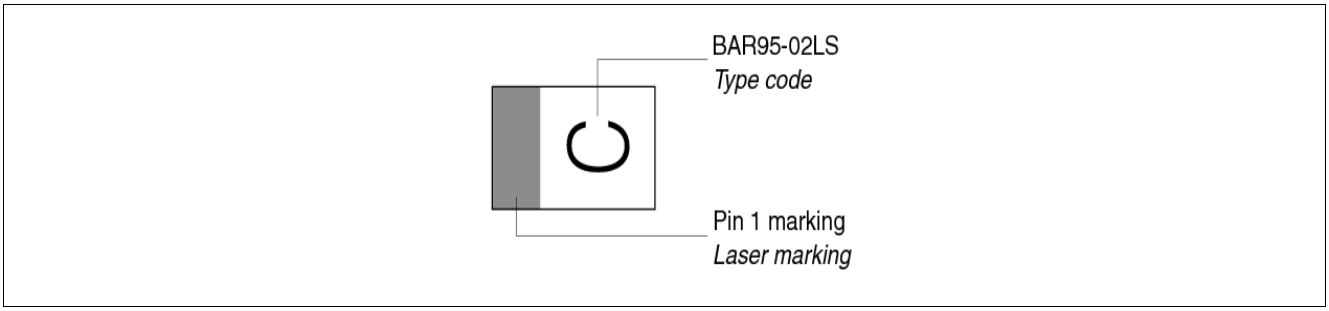

Figure 18 Marking for TSSLP-2-3 (example)

References

[1] On-chip ESD protection for integrated circuits, Albert Z. H. Wang, ISBN:0-7923-7647-1

[2] Infineon AG - **Application Note AN210:** Effective ESD Protection Design at System Level Using VF-TLP Characterization Methodology

[3] Infineon AG - Recommendations for PCB Assembly of Infineon TSLP and TSSLP Package

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Офис по работе с юридическими лицами:

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:
moschip.ru
moschip.ru_4
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moschip.ru_9