D2-4P Family Audio SOC

Intelligent Digital Amplifier PWM Controller and Audio Processor

FN8766
Rev 2.00
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The D2-4P (ISL59372 and ISL59373) devices are complete System-on-Chip (SoC) Class-D digital audio amplifiers. These devices combine high-performance integrated Power Stages, digital audio processing, and amplifier control in a single controller to offer a complete, powerful, and very cost-effective audio solution for high volume and cost-critical products.

This 4th generation digital audio Processor (D2-4P) device combines extensive integrated Digital Signal Processor (DSP) audio processing with amplifier control for a complete audio solution. Its ease of integration into the existing system architecture provides complete audio support for all system product and amplifier functions.

The four configurable Power Stages operate as four separate Half-Bridge outputs, as two Full-Bridge outputs, or in combinations of Half-Bridge plus Full-Bridge, which provides the ideal loudspeaker driver solutions. Separate PWM outputs provide additional combinations to drive headphone outputs or line-level stereo and subwoofer outputs.

Related Literature

For a full list of related documents, visit our website:

- ISL59372 and ISL59373 device pages

Features

- All digital Class-D amplifier and controller with integrated Digital Signal Processing (DSP)
- Four integrated Power Stages supporting:
  - 2 Channels, Bridged
  - 4 Channels, Half-Bridge
  - 2 Channels, Half-Bridge, plus 1 Channel, Bridged
- Output power (bridged):
  - 20W (8Ω, ≤1% THD); 30W (8Ω, ≤10% THD)
- Fully programmable Digital Signal Processing (DSP)
  - Up to 4 programmable 32-bit digital audio processing engines with coefficient RAM, filters, and mixers/routers
- Flexible 32-bit/8-DSP-based Enhancement Algorithm and STMicroelectronics STA381BW Audio Enhancement Algorithms
- I²S-based to PDM™ digital audio inputs
- Asynchronous sample rate converters; sample rates from 8kHz to 192kHz
- Wide 10V to 26V Power Stage HV supply range, plus internally-generated gate drive supply
- Temperature and undervoltage lockout monitoring and individual channel protection

Applications

- PC/ multimedia speakers
- Digital TV audio systems
- Portable device docking stations
- Powered speaker systems

Typical System Implementation

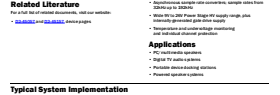

FIGURE 1. SYSTEM APPLICATION IMPLEMENTING 2.1 STEREO BRIDGE-LOADED PLUS HEADPHONE OUTPUTS

Ordering information

PART NUMBER (Notes 1, 2)	PART MARKING	AUDIO PROCESSING PERFORMANCE SUPPORT (Note 3)	TEMP. RANGE (°C)	TAPE AND REEL (QUANTITY) (Note 4)	PACKAGE (RoHS-Compliant)	PKG. DWG. #
ISL 80387-2P	ISL80387-2P	D2 Audio DSP Sound Enhancement Algorithm	-20 to +85		68 Ld QFN	L68.10x10C
ISL 80387-2P-T	ISL80387-2P	D2 Audio DSP Sound Enhancement Algorithm	-20 to +85	3k	68 Ld QFN	L68.10x10C
ISL 80387-2P-T	ISL80387-2P-T	D2 Audio DSP Sound Enhancement Algorithm: DTS® HD Master Audio™	-20 to +85	-	68 Ld QFN	L68.10x10C
ISL 80387-2P-T	ISL80387-2P-T	D2 Audio DSP Sound Enhancement Algorithm: DTS® HD Master Audio™	-20 to +85	3k	68 Ld QFN	L68.10x10C

NOTES:

1. The D2-4P chooses support and is processing algorithms for the D2 Audio DSP Sound Enhancement Algorithm set. DTS® HD | MONO HD™ audio enhancement features. Algorithm support for future enhancements is device dependent. See the device part number for feature support.
2. See TB347 for details about reel specifications.
3. These Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. The Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
4. For Moisture Sensitivity Level (MSL), see the ISL80387-2P data sheet and the TB363 tech brief. For more information about MSL, see TB363.

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Absolute Maximum Ratings (Note 1)

Supply Voltage	
AVDD, PVDD, DVDD	-0.3V to +28.0V
PVDD_PWRGD	-0.3V to 6.0V
PLLVDD, DVDD	-0.3V to 2.4V
Input Voltage	
Logic Input (SCL)	-0.3V to PVDD +0.3V
XTALI	-0.3V to PLLVDD +0.3V
Input Current, Any Pin but Supplies	±20mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W) θ_{JC} (°C/W)
56 Ld QFN Package (Note 2, 3)	29 1.5
Maximum Junction Temperature	-40°C to +150°C
Pb-Free Reflow Profile	see TB493

Recommended Operating Conditions

Temperature Range	-20°C to +85°C
High Voltage Supply Voltage, PVDD	
Class D Mode	8.2V to 24.0V
Digital LDO Supply Voltage, PVDD_DVDD	2.3V
Core Supply Voltage, DVDD	1.8V
PLL Supply Voltage, PLLVDD	1.8V
Minimum Load Impedance (AVDD,SAD,CAD,DAD, R_L)	4Ω

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

NOTES:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See TB379.
2. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.
3. Absolute Maximum parameters are not tested in production.

Electrical Specifications V_{DD} = +24°C, AVDD=PVDD=+24V, DVDD=PLLVDD= 1.8V ±5%, RVDD=PWRGD= 3.3V ±5%. All grounds at 0.0V, All voltages referenced to ground, PLL at 22.5792MHz, VBIT at 2.5792MHz, over recommended operating conditions unless otherwise noted.

PARAMETER	DESCRIPTION	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Digital Input High Logic Level (Except XTALI Pin)			V_{IH}	2	-	-	V
Digital Input Low Logic Level (Except XTALI Pin)			V_{IL}	-	-	0.8	V
High Level Output Drive Voltage (Except I²C Bus Open Drain Outputs)			V_{OH}	RVDD - 0.4	-	-	V
Low Level Output Drive Voltage (Except I²C Bus or Write-Once Strength Control)			V_{OL}	-	-	0.4	V
High Level Input Drive Voltage (XTALI Pin)			V_{XIH}	0.7	-	PLLVDD	V
Low Level Input Drive Voltage (XTALI Pin)			V_{XIL}	-	-	0.3	V
Input Leakage Current (Note 4)			I_{IL}	-	-	±10	µA
Input Capacitance			C_{IN}	-	-	8	pF
Output Capacitance	All Outputs Except XTALO Pin		C_{OUT}	-	-	8	pF
	XTALO			-	20	-	pF
µP/SPI Power Mode			Mode	-	200	-	mA
Internal Pull-Up Resistance on PWRD/SDO (for µP/SPI/I²C/3-WIRE, ADPS, µP/SPI)				-	300	-	kΩ
Digital I/O Supply Pin Voltage, Current			RVDD	3	3.3	3.6	V
		Active Current	RVDD mA	-	1	-	mA
		Power-Down Current		-	0.01	-	mA
Core Supply Pins			DVDD	1.7	1.8	1.9	V
		Active Current		-	100	-	mA
		Power-Down Current (Note 4)		-	4	-	mA

Electrical Specifications T_A = -20°C to +70°C for 0°C ≤ VVDD3.3 ≤ 3.6V, 2.4V ≤ VVDD2.5 ≤ 2.6V, 1.4V ≤ VVDD1.5 ≤ 1.6V, 1.0V ≤ VVDD0.9 ≤ 1.2V, 2.0V ≤ VVDD1.8 ≤ 2.0V, all voltages with respect to ground, PLL at 24.576 MHz, DAC at 256fS/48kHz, over recommended operating conditions unless otherwise specified.

Features

PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Analog Supply Pins (Vx)		VVDD3.3	3.1	3.3	3.6	V
	Active Current			30		mA
	Power-Down Current (Note 9)			5		µA

CRYSTAL OSCILLATOR

Crystal Frequency (Fundamental Mode Crystal)		fXI	20	24.576	25	MHz
Duty Cycle		DX	40	-	60	%
Start-Up Time (Start-Up Time is Oscillator Enable to Stable Clock Supply to Sender Subsystem)		tXSUP		5	20	ms

PLL

VCO Frequency		fVCO	260	294.912	300	MHz
PLL Lock Time (from power/pad Change)					5	ms

3.3V POWER DOMAIN

Power Down Input Level		VPDL	-0.5	-	0.8	V
PDR Minimum Output Pulse Width		tPDR	5	-	-	µs

1.8V GPIO/SDRAM DOMAIN

Power Down			0.8	0.9	0.7	V
Pulse Width Rejection		tRESET	-	200	-	ns
Minimum Output Pulse Width		tRES	1	2	-	ms

2.5V (Flexible) SDRAM/GPIO DOMAIN

Power Down			2.0	2.1	2.3	V
Pulse Width Rejection		tRESET	-	200	-	ns
Minimum Output Pulse Width		tRES	1	2	-	ms

1.5V CORE DOMAIN - 1.5V TOLERANT GPIO/SDRAM

Core Drive Supply Undervoltage Threshold			-	0.9	-	V
Core Drive Supply Undervoltage Threshold Hysteresis			-	200	-	mV
Core Drive Supply Undervoltage Threshold Glitch Rejection			-	50	-	ns

POWER-ON RESET

High Voltage (+1.8VDC) Undervoltage Protection			-	1	9	V
Overcurrent Trip Threshold			-	8	-	A
Overcurrent De-Glitch			-	4	-	µs
Short-Circuit Current Limit (Peak)			-	8	-	A
Overcurrent Response Time			-	20	-	ns
Thermal Shutdown (Power Staging)			-	160	-	°C
Thermal Shutdown Hysteresis (Power Staging)			-	10	-	°C

NOTES:

8. All input pins are pulled LOW.
9. Input leakage applies to all pins except XTALO.
10. Power-down is with device in reset, and clocks stopped.

Performance Specifications T_A = +25°C, V_{VDD33}=3.300V + 2x1.0VDD = V_{VDD10} = 1.8V ±5%, V_{VDD10} = V_{VDD33} = 3.3V ±5%, All grounds at 0.0V, All voltages referenced to ground, R_L = 2kΩ, R_L(DAC)= 2kΩ, C_L=0.015000µ, over sunning at 22.5792MHz with typical audio data loading.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
T_{VDD33} (Maximum, MOSFETs at +25°C)	T_{VDD33}	-	200	-	mΩ
T_{VDD33} (Maximum)		-	1.0	-	Ω
PWM Switching Rate		-	384	-	kHz
nPOR Input 3V Delay	T_{RAMPP}	-	1.4	-	ms
nPOR Input On-Delay	T_{RAMPR}	-	1.4	-	ms
PERFORMANCE					
4Ω/1.7kΩ, Bridged, Load = 8Ω, 5V/3.6Ω/2.4Ω = 24V	P_{OUT}	-	25	-	W
4Ω/1.7kΩ, Bridged, Load = 8Ω, 5V/3.6Ω/2.4Ω = 24V	P_{OUT}	-	30	-	W
4Ω/1.7kΩ, Half-Bridge, Load = 8Ω, 5V/3.6Ω/2.4Ω = 24V	P_{OUT}	-	7	-	W
4Ω/1.7kΩ, Half-Bridge, Load = 8Ω, 5V/3.6Ω/2.4Ω = 24V	P_{OUT}	-	9	-	W
THD+N					
Load = 8Ω, Power = 25W, Bridged, 2p5m	THD+N	-	0.3	-	%
Load = 8Ω, Power = 25W, Bridged, 2p5m		-	0.05	-	%
SNR	SNR	-	110	-	dB
Efficiency (Power-Stage, Load = 8Ω)		-	93	-	%

Serial Audio Interface Port Timing T_A = -20 ° C+85°C,V_{VDD33} = 3.3V, V_{VDD10} = 1.8V ±5%, V_{VDD10} = V_{VDD33} = 3.3V ±5%, All grounds at 0.0V, All voltages referenced to ground, C_L = 20 pF, RLDAC= 2kΩ, C_L=0.015000µ, over sunning at 22.5792MHz with typical audio data loading.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
f_{MCLK}	MCLK Frequency - (MCLK)	-	-	12.5	MHz
t_{MCLK}	MCLK Pulse Width (high and low) - (MCLK)	40	-	-	ns
t_{LRCLKS}	LRCLK Setup to MCLK Rising - (LRCLK)	20	-	-	ns
t_{LRCLKH}	LRCLK Hold from MCLK Rising - (LRCK)	20	-	-	ns
t_{SDS}	SDIN Setup to MCLK Rising - (SDIN)	20	-	-	ns
t_{SDH}	SDIN Hold from MCLK Rising - (SDIN)	20	-	-	ns

FIGURE 3. SERIAL AUDIO INTERFACE PORT TIMING

Two-Wire I²C Interface Port Timing T_A = -20° C..0/50 ~ PLUS0 ~ 4.8V (4Y5, IN3D = PWRVSS = 3.3V ±10%. All grounds at 0.0V, All voltages referenced to ground.

SYMBOL	DESCRIPTION	MIN	MAX	UNIT
f_{SCL}	SCL Frequency	-	400	kHz
t_{BUF}	Bus Free Time Between Transmissions	4.7	-	µs
$t_{HD;STA}$	SCL Clock Low	4.7	-	µs
$t_{SU;STA}$	SCL Clock High	4.0	-	µs
$t_{HD;STA}$	Setup Time For a (Repeated) Start	4.7	-	µs
$t_{HD;DAT}$	Start Condition Hold Time	5.0	-	µs
$t_{SU;DAT}$	SDA Hold Time SCL Falling (Note 5.1)	-	0.3 (plan)	ns/mV
$t_{SU;STO}$	SDA Set Up Time to SCL Rising	250	-	ns
$t_{HD;STO}$	SDA Output Delay Time From SCL Falling	-	3.6	µs
t_r	Rise Time of Both SDA and SCL (Note 5.2)	-	1	µs
t_f	Fall Time of Both SDA and SCL (Note 5.2)	-	300	ns
t_{LOW}	Setup Time For a Stop Condition	4.7	-	µs

NOTES:

5.1. Data is clocked in as valid on the next SCL(+rising) edge after SCL goes low.

5.2. Limits established by characterization and not production tested.

FIGURE 3. I²C-WIRE INTERFACE TIMING

SPI™ Master Mode Interface Port Timing

T_A = -10 °C, $DVDD$ = $PLLVDD$ = 1.8V ±5%, $RVDD$ = $PVBVDD$ = 3.3V ±10%, All grounds are 0V, All voltages referenced to ground.

SYMBOL	DESCRIPTION	MIN	MAX	UNIT
t_{ch}	MOSI Valid Post Clock Edge		8	ns
t_{cl}	MOSI Setup to Clock Edge	3.0		ns
T_{sck}	MOSI Valid Pre Clock Edge	3 system clock + 2ns		
T_{MIN}	MISO minimum Width	3 system clocks + 2ns		

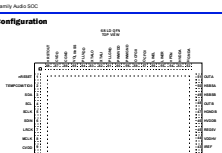
SPI™ Slave Mode Interface Port Timing

T_A = -10 °C, $DVDD$ = $PLLVDD$ = 1.8V ±5%, $RVDD$ = $PVBVDD$ = 3.3V ±10%, All grounds at 0V, All voltages referenced to ground.

SYMBOL	DESCRIPTION	MIN	MAX	UNIT
T_{ch}	MISO Valid Post Clock Edge	3 system clocks + 2ns		
T_{cl}	MOSI Setup to Clock Edge	3.0		ns
T_{sck}	MOSI Valid Pre Clock Edge	3 system clock + 2ns		
T_{MIN}	MISO minimum Width	3 system clocks + 2ns		

FIGURE 6. SPI TIMING

Pin Configuration


R5F523T5
TOP VIEW
nRESET
TEMPSENSTRIG
SDA
SCL
SCL0
SDA0
LRCK
MCLK
CCKO
CDIO
BCKO
RXD0
TEMPSENSOUT
nRESET/EA
VOLUMEO
TEMPVMODE
EXPGPIO0
P30/TXD2/SMOSI2/SSDA2
P31/SSCK2
P32/RXD2/SMISO2/SSCL2
P33/CTS2/RTS2/SS2
P34/SCK2
P35/TXD1/SMOSI1/SSDA1
P36/RXD1/SMISO1/SSCL1
P37/CTS1/RTS1/SS1
P40/SCK1
P41/TXD0/SMOSI0/SSDA0
P42/RXD0/SMISO0/SSCL0
P43/CTS0/RTS0/SS0
P44/SCK0
P45/TXD3/SMOSI3/SSDA3
P46/RXD3/SMISO3/SSCL3
P47/CTS3/RTS3/SS3
P50/SCK3
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PA4/SCK14
PA5/TXD15/SMOSI15/SSDA15
PA6/RXD15/SMISO15/SSCL15
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PK4/SCK32
PK5/TXD33/SMOSI33/SSDA33
PK6/RXD33/SMISO33/SSCL33
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PL3/CTS34/RTS34/SS34
PL4/SCK34
PL5/TXD35/SMOSI35/SSDA35
PL6/RXD35/SMISO35/SSCL35
PL7/CTS35/RTS35/SS35
PM0/SCK35
PM1/TXD36/SMOSI36/SSDA36
PM2/RXD36/SMISO36/SSCL36
PM3/CTS36/RTS36/SS36
PM4/SCK36
PM5/TXD37/SMOSI37/SSDA37
PM6/RXD37/SMISO37/SSCL37
PM7/CTS37/RTS37/SS37
PN0/SCK37
PN1/TXD38/SMOSI38/SSDA38
PN2/RXD38/SMISO38/SSCL38
PN3/CTS38/RTS38/SS38
PN4/SCK38
PN5/TXD39/SMOSI39/SSDA39
PN6/RXD39/SMISO39/SSCL39
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PQ7/CTS43/RTS43/SS43
PR0/SCK43
PR1/TXD44/SMOSI44/SSDA44
PR2/RXD44/SMISO44/SSCL44
PR3/CTS44/RTS44/SS44
PR4/SCK44
PR5/TXD45/SMOSI45/SSDA45
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PS2/RXD46/SMISO46/SSCL46
PS3/CTS46/RTS46/SS46
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PX1/TXD192/SMOSI192/SSDA192
PX2/RXD192/SMISO192/SSCL192
PX3/CTS192/RTS192/SS192
PX4/SCK192
PX5/TXD193/SMOSI193/SSDA193
PX6/RXD193/SMISO193/SSCL193
PX7/CTS193/RTS193/SS193
PY0/SCK193
PY1/TXD194/SMOSI194/SSDA194
PY2/RXD194/SMISO194/SSCL194
PY3/CTS194/RTS194/SS194
PY4/SCK194
PY5/TXD195/SMOSI195/SSDA195
PY6/RXD195/SMISO195/SSCL195
PY7/CTS195/RTS195/SS195
PZ0/SCK195
PZ1/TXD196/SMOSI196/SSDA196
PZ2/RXD196/SMISO196/SSCL196
PZ3/CTS196/RTS196/SS196
PZ4/SCK196
PZ5/TXD197/SMOSI197/SSDA197
PZ6/RXD197/SMISO197/SSCL197
PZ7/CTS197/RTS197/SS197
P00/SCK197
P01/TXD198/SMOSI198/SSDA198
P02/RXD198/SMISO198/SSCL198
P03/CTS198/RTS198/SS198
P04/SCK198
P05/TXD199/SMOSI199/SSDA199
P06/RXD199/SMISO199/SSCL199
P07/CTS199/RTS199/SS199
P10/SCK199
P11/TXD200/SMOSI200/SSDA200
P12/RXD200/SMISO200/SSCL200
P13/CTS200/RTS200/SS200
P14/SCK200
P15/TXD201/SMOSI201/SSDA201
P16/RXD201/SMISO201/SSCL201
P17/CTS201/RTS201/SS201
P20/SCK201
P21/TXD202/SMOSI202/SSDA202
P22/RXD202/SMISO202/SSCL202
P23/CTS202/RTS202/SS202
P24/SCK202
P25/TXD203/SMOSI203/SSDA203
P26/RXD203/SMISO203/SSCL203
P27/CTS203/RTS203/SS203
P30/SCK203
P31/TXD204/SMOSI204/SSDA204
P32/RXD204/SMISO204/SSCL204
P33/CTS204/RTS204/SS204
P34/SCK204
P35/TXD205/SMOSI205/SSDA205
P36/RXD205/SMISO205/SSCL205
P37/CTS205/RTS205/SS205
P40/SCK205
P41/TXD206/SMOSI206/SSDA206
P42/RXD206/SMISO206/SSCL206
P43/CTS206/RTS206/SS206
P44/SCK206
P45/TXD207/SMOSI207/SSDA207
P46/RXD207/SMISO207/SSCL207
P47/CTS207/RTS207/SS207
P50/SCK207
P51/TXD208/SMOSI208/SSDA208
P52/RXD208/SMISO208/SSCL208
P53/CTS208/RTS208/SS208
P54/SCK208
P55/TXD209/SMOSI209/SSDA209
P56/RXD209/SMISO209/SSCL209
P57/CTS209/RTS209/SS209
P60/SCK209
P61/TXD210/SMOSI210/SSDA210
P62/RXD210/SMISO210/SSCL210
P63/CTS210/RTS210/SS210
P64/SCK210
P65/TXD211/SMOSI211/SSDA211
P66/RXD211/SMISO211/SSCL211
P67/CTS211/RTS211/SS211
P70/SCK211
P71/TXD212/SMOSI212/SSDA212
P72/RXD212/SMISO212/SSCL212
P73/CTS212/RTS212/SS212
P74/SCK212
P75/TXD213/SMOSI213/SSDA213
P76/RXD213/SMISO213/SSCL213
P77/CTS213/RTS213/SS213
P80/SCK213
P81/TXD214/SMOSI214/SSDA214
P82/RXD214/SMISO214/SSCL214
P83/CTS214/RTS214/SS214
P84/SCK214
P85/TXD215/SMOSI215/SSDA215
P86/RXD215/SMISO215/SSCL215
P87/CTS215/RTS215/SS215
P90/SCK215
P91/TXD216/SMOSI216/SSDA216
P92/RXD216/SMISO216/SSCL216
P93/CTS216/RTS216/SS216
P94/SCK216
P95/TXD217/SMOSI217/SSDA217
P96/RXD217/SMISO217/SSCL217
P97/CTS217/RTS217/SS217
PA0/SCK217
PA1/TXD218/SMOSI218/SSDA218
PA2/RXD218/SMISO218/SSCL218
PA3/CTS218/RTS218/SS218
PA4/SCK218
PA5/TXD219/SMOSI219/SSDA219
PA6/RXD219/SMISO219/SSCL219
PA7/CTS219/RTS219/SS219
PB0/SCK219
PB1/TXD220/SMOSI220/SSDA220
PB2/RXD220/SMISO220/SSCL220
PB3/CTS220/RTS220/SS220
PB4/SCK220
PB5/TXD221/SMOSI221/SSDA221
PB6/RXD221/SMISO221/SSCL221
PB7/CTS221/RTS221/SS221
PC0/SCK221
PC1/TXD222/SMOSI222/SSDA222
PC2/RXD222/SMISO222/SSCL222
PC3/CTS222/RTS222/SS222
PC4/SCK222
PC5/TXD223/SMOSI223/SSDA223
PC6/RXD223/SMISO223/SSCL223
PC7/CTS223/RTS223/SS223
PD0/SCK223
PD1/TXD224/SMOSI224/SSDA224
PD2/RXD224/SMISO224/SSCL224
PD3/CTS224/RTS224/SS224
PD4/SCK224
PD5/TXD225/SMOSI225/SSDA225
PD6/RXD225/SMISO225/SSCL225
PD7/CTS225/RTS225/SS225
PE0/SCK225
PE1/TXD226/SMOSI226/SSDA226
PE2/RXD226/SMISO226/SSCL226
PE3/CTS226/RTS226/SS226
PE4/SCK226
PE5/TXD227/SMOSI227/SSDA227
PE6/RXD227/SMISO227/SSCL227
PE7/CTS227/RTS227/SS227
PF0/SCK227
PF1/TXD228/SMOSI228/SSDA228
PF2/RXD228/

Pin Descriptions (continued)

Pin #	Pin Name	Type	Voltage Level (V)	Description
63	SCL	I	3.3	Receiver serial clock port, open drain drive with Schmitt-trigger input with fourth-bit input level sampling for both I2C and SPI modes. Requires external pull-up resistor.
64	SDA	I	3.3	I2C serial mode bi-directional SDA(I2C) Input / data bus terminal.
65	SDIN	I	3.3	I2C serial mode data (SDIN) Input / input/out/ports/mode.
66	LRCK	I	3.3	I2C serial audio left / right LRCK Input / input bus/systems.
67	SCLK	O	3.3	I2C serial audio master clock output for external ADC/DAC components, 64 cycles per word. Output is an 8x clock.
68	CVDD	P	3.3	Core power, +1.8VDC is fed to the chip internal DSP, logic, and core blocks.
69	CGND	GND	3.3	Core ground.
70	RXD0	GND	3.3	Digital serial ground. Internally connected to PGND(0).
71	RXD0	I	3.3	Digital serial data input (I2S, Tri-S, 3.3V) input to receiver of the digital I/O and drivers and workers, except for the analog ports. Each of these pins must be connected. Internally connected to PGND(0).
72	TEMPEST_VOL	I/O	3.3	Volume input for the temperature of TEMPEST and VOL inputs. A) Assertion of clock error. B) I2C pin operates as a SPI clock with Bi-directional strength. Upon internal DSP RAM transmission errors, this pin becomes a processor/system clock.
73	+RUN	O	3.3	Status signal output. When active low, a mute switch is in the mute pin low. The output is a 3.3mA, driven signal. Upon internal DSP RAM transmission errors, this pin becomes a processor/system clock.
74	VOL1 / VOL	I/O	3.3	Volume control pulse input and SPI master output, two output data signal. A) detection of clock error. this pin operates as an I2C slave with Bi-directional strength. Upon internal DSP RAM transmission errors, this pin becomes a processor/system clock.
75	TEMPU_VOL	I/O	3.3	Temperature input and SPI master output two output data signal. A) detection of clock error. this pin operates as an I2C slave with Bi-directional strength. Upon internal DSP RAM transmission errors, this pin becomes a processor/system clock.
76	SPIOUT0	O	3.3	SPDIF digital audio data input.
77	SPIOUT1	O	3.3	SPDIF digital output. Requires 1k to PDVP. Audio output and drives as Mark, 3.3V when output up to 0.5MHz. The Mark is on mark.
78	VDD	I	3.3	Hardware boot mode select. For factory use only. Must be set to Mark.
79	VSCL	I	3.3	Interrupt request port 0. One of two IRQ pins, tied to high (3.3V) high or to ground. High/low light status enable/disable for fault and error detection of the user's processor.
80	VSDA	I	3.3	Interrupt request port 0. One of two IRQ pins, tied to high (3.3V) high or to ground. High/low light status enable/disable for fault and error detection of the user's processor.
81	RXD0	GND	3.3	Digital serial ground. Internally connected to PGND(0).
82	VBRDIR / DTXD	I/O	3.3	Output configuration for serial and I2S/MSP output. Bi-directional mode, this pin operates as an input and uses an application installed pull up or pull down connection to the pin to specify one of four amplifier configurations. Bi-directional mode, this pin operates as an output and provides a serial data output. Bi-directional mode, this pin operates as a processor/system clock. When operating as an output, this pin provides 8mA drive strength. This pin may also be called "VBUSDIR" a receiver reference designer, sometimes functional registers or functions.
83	PDVALC / VCLK	I/O	3.3	Output configuration selection input and power supply sync output. Bi-directional mode, this pin operates as an input and uses an application installed pull up or pull down connection to the pin to specify one of four amplifier configurations. Bi-directional mode, this pin operates as an output and provides a serial data output. This pin becomes an output and provides a synchronizing signal to on board power supply circuits. When operating as an output, this pin provides 8mA drive strength. This pin may also be called "VCLK" a receiver reference designer, sometimes functional registers or functions.
84	PRORESET	I/O	3.3	PDVP configuration input, input bus/systems. This pin is pulse-active-monitoring functionality is activated by the internal DSP firmware and is dependent on which of the four amplifier configurations is selected.

Pin Descriptions (continued)

PIN	NAME (Note 1, 2)	I/O	VOLTAGE VDD1_D	DESCRIPTION
28	PROTECT0	I/O	3.3	PWM protection input. Input has hysteresis. This pin is also an error monitoring functionality is activated by internal DSP if timeout event is detected on at least one of the four amplifier configurations.
29	PROTECT1	I/O	3.3	PWM protection input. Input has hysteresis. This pin is also an error monitoring functionality is activated by internal DSP if timeout event is detected on at least one of the four amplifier configurations.
30	nOSC0SD	O	3.3	Overcurrent protection output, channel 0 as open drain. Open drain 30mA driver with internal 200kΩ pull-up (approximate). Pulls low when under- /overcurrent detection of the output stage.
31	nOSC1SD	O	3.3	Overcurrent protection output, channel 0 as open drain. Open drain 30mA driver with internal 200kΩ pull-up (approximate). Pulls low when under- /overcurrent detection of the output stage.
32	nOSC2SD	O	3.3	Overcurrent protection output, channel 0 as open drain. Open drain 30mA driver with internal 200kΩ pull-up (approximate). Pulls low when under- /overcurrent detection of the output stage.
33	nOSC3SD	O	3.3	Overcurrent protection output, channel 0 as open drain. Open drain 30mA driver with internal 200kΩ pull-up (approximate). Pulls low when under- /overcurrent detection of the output stage.
34	VOUT2	P	5V	Output stage 2 high voltage supply power. Separate power pin connected to bootstrap network of the output stage. Connect to VOUT2 pin of the output stage.
35	HIN2G	GND	0V	Output stage 2 high voltage supply ground. Exposed metal ground pin connection. Isolated for each of the output stages. All of the HIN2G/L2 pins connect to system "0V" power ground (see Note 2.0)
36	LIN2G	GND	0V	Output stage 2 high voltage supply ground. Exposed metal ground pin connection. Isolated for each of the output stages. All of the LIN2G/L2 pins connect to system "0V" power ground (see Note 2.0)
37	VDD2	P	5V	PWM power amplifier, channel 2.
38	HGND2	P	0V	High-side boot strap input, channel 2. Capacitor coupled to OUT2 amplifier output.
39	HGND2	I	5V	High-side boot strap input, output channel 2. Capacitor coupled to OUT2 amplifier output.
40	VDD2	P	5V	PWM power amplifier, channel 2.
41	VOUT2	GND	0V	Output stage 2 high voltage supply ground. Exposed metal ground pin connection. Isolated for each of the output stages. All of the VOUT2/L2 pins connect to system "0V" power ground (see Note 2.0)
42	VDD2	P	5V	Output stage 2 high voltage supply power. Separate power pin connected to bootstrap network of the output stages. All of the VDD2/L2 pins connect to system "5V" power (see Note 2.0)
43	VDD3	P	5V	Subwoofer/ channel PWM output with 3.3Vtolerance driving 8 Channels. Tri-Wire network for supporting Subwoofer/ channel PWM output
44	VAA			Do not connect to this pin.
45	VDD1_D	P	3.3V	Digital core voltage supply input. Used for setting the overcurrent error detect internally set threshold. The pin needs to be connected to a 3DVDD resistor to ground to set the overcurrent threshold according to the application.
46	VOUT1	P	5V	Output stage 1 high voltage supply power. Separate power pin connected to bootstrap network of the output stages. All of the VOUT1/L1 pins connect to system "5V" power (see Note 2.0)
47	RESET	P	3.3V	Reset input. Active low. Internal filter. Internal 1.5 MΩ pull-up resistor. Connect from the voltage source provided at the VDD_3V. RESET is used for external connection of de-coupling capacitor.
48	VOUT1	GND	0V	Output stage 1 high voltage supply ground. Exposed metal ground pin connection. Isolated for each of the output stages. All of the VOUT1/L1 pins and the 1DGND pin connect to the system "0V" power source.
49	HGND1	GND	0V	Output stage 1 high voltage supply ground. Exposed metal ground pin connection is provided for each of the output stages. All of the HGND1/L1 pins connect to system "0V" power ground (see Note 2.0)
50	HIN1G	GND	0V	Output stage 1 high voltage supply ground. Exposed metal ground pin connection is provided for each of the output stages. All of the HIN1G/L1 pins connect to system "0V" power ground (see Note 2.0)

Pin Descriptions (continued)

PIN	NAME (Note 13)	VOLTAGE (Note 14)	DESCRIPTION
83	HPOUTL	3.3	Output stage (high voltage supply) power. Connect to power connection to provide for each of the output stages. Connect to the same power source as the HPVDD pin. Decouple to GND.
84	nRDY	3.3	Power down and reset output. Active low. When this signal is low, all the output transistors (active and class-D output stages, but not DAC signal is routed), internal logic and other references remain active during this power down state.
85	LINR	0 - 3.3	"Right" channel PWM output, with 32mA drive strength. Connects to the filter network to supply the line level analog output.
86	LINL	0 - 3.3	"Left" channel PWM output, with 32mA drive strength. Connects to the filter network to supply the line level analog output.
87	HCFG2	1 - 3.3	Control configuration control select. HCFG2 and HCFG1 are high inputs to select the output configuration mode of the output stages. Connects to either the PWRGND ground or PWMGND = 3.3V) through a series 10K resistor to select output configuration mode.
88	HCFG1	1 - 3.3	Control configuration control select. HCFG2 and HCFG1 are high inputs to select the output configuration mode of the output stages. Connects to either the PWRGND ground or PWMGND = 3.3V) through a series 10K resistor to select output configuration mode.
89	PWMGND	P	PWM output pin ground. Internally connected to HGND.
90	PWRGND	P	PWM output pin ground. Internally connected to HGND. Used for PWM gate drivers. Internally connected to HGND.
91	PLLGND	P	PLL analog ground. Tie to a low voltage ground (GND). Should be through a single point connection to isolate this ground from the board, and minimize effects on the PLL.
92	XTALI	P	3.3	Crystal oscillator analog input pin
93	XTALO	P	3.3	Crystal oscillator analog output pin (this output drives the crystal and XTALO does not have a drive strength specification)
94	PLLVDD	P	1.8	PLL analog power. 1.8V.
95	VOLC-nIR	I/S	3.3	Volume control pulse input and IOR slave select. When a device reset is detected, this pin operates as a IOR slave select input. A internal 32 uP interface executes. this pin becomes an input for monitoring up/down pulses from volume control (one of two volume input pins.)
96	CVDD	P	1.8	Core ground
97	CVDD	P	1.8	Core power, +1.8VDC. Used in the chip internal DSP, logic, and interfaces.
98	nRESET	I/S	3.3	Active low system reset signal with 32mA drive strength. This pin drives low when either the RESET_N command detects, PWRDOWN 32V brownout detector, or LED brownout detector goes active (but this output becomes active only when it is set to RESET_N command).

NOTES:

13. All pin names are active high unless otherwise specified. Active low signals have an "n" prefix, such as nRESET.

14. All power and ground pins with the same name must be tied together. In all other pins of their same name (that is, no GOD pins together, GDND pins together, HVDD pins together, and HGND pins together). The GDND and HGND together can be tied and receive the HGND and PWRGND pins are internally connected and tied together on the board.

15. The thermal pad is internally connected to all four HGND ground pins (HGND4, HGND5, HGND6, and HGND7). Any connection to the thermal pad must be made to the common ground for these four ground pins.

Typical Performance Characteristics

Test Considerations

- Typical performance measurements are made using an Audio Precision® 2700 Series audio analyzer.
- Precision power resistors are used for the 8Ω loads/speaker loads.
- Measurements are done using a +5V supply at +25 DVDC.

Full-Bridge Typical Performance Curves

FIGURE 5. THD+N POWER, FULL-BRIDGE

FIGURE 6. THD+N FREQUENCY, FULL-BRIDGE

FIGURE 7. FREQUENCY RESPONSE, FULL-BRIDGE

FIGURE 8. HEADTAKER, FULL-BRIDGE

Half-Bridge Typical Performance Curves

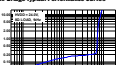

FIGURE 9. THD+N vs POWER, HALF-BRIDGE

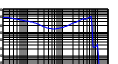

FIGURE 10. THD+N vs FREQUENCY, HALF-BRIDGE

FIGURE 11. FREQUENCY RESPONSE, HALF-BRIDGE

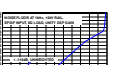

FIGURE 12. S-CODE FLOOR, HALF-BRIDGE

FIGURE 13. D2-4P FUNCTIONAL BLOCK DIAGRAM

Functional Description

Overview

The D2-4P devices, shown in Figure 2.0 on page 2.0, are integrated System-on-Chip (SoC) audio processors and Class D digital audio amplifiers. They offer flexible signal routing selection, signal routing, complete audio processing, PWM amplifiers, and a wide variety of input and output configurations (power bridge, Stereo PBTL and 8 PDM digital input support). All I²C and 2-wire SPI control interfaces, provide integration compatibility with existing system architectures and solutions.

The four configurable power stages can operate as four separate half-bridge outputs, two full-bridge outputs, or in combinations of half-bridge plus full-bridge outputs. Separate power supplies are provided for the power stages, the headphone outputs, or internal circuitry and digital interfaces. These application dependent configurations provide for driving Stereo 2.0 Systems, 2.1 Systems, and Stereo 2.2 (8 Ohm) Speaker solutions, as well as providing Stereo Line outputs, Headphone outputs, or Subwoofer outputs.

Audio output implementations are defined by the configuration of the signal routing matrix, the digital processing blocks, and the four amplifier channels as shown in Figure 2.0. The internal audio processing paths feed a PWM engine, where the five PWM channels are mapped to the configurations mentioned previously and line outputs.

Table 2.0 – Audio Configurations

Configuration	Output Configuration	Description
0	2.0 L/R Speaker	• Powered from and right outputs with 2 equalizers, 2 full bridge drivers • Stereo 2.0 speaker output
1	2.0 L/R + L/R Line	• Powered from and right outputs with 2 equalizers, full bridge drivers • Stereo left + right line level outputs • Subwoofer line level output
2	2.1 L/R + Sub	• Two half bridge drivers for powered left and right outputs • Dependent, full bridge driver for powered subwoofer output • Two stereo left + right line level outputs • Crossover filtering included with audio path signal flow
3	2.2 8Ohm	• Four half bridge drivers for powered left and right outputs • Crossover filtering included with audio path signal flow

The audio path includes a stereo Sample Rate Converter (SRC), two independent audio equalizers, and a variety of high quality audio enhancement algorithms.

Programmable gain parameters for audio processing include volume control, path routing and mixing, high/low pass filtering, equalization, dynamic adjustments, and loudness. These parameters can be adjusted using the D2 Audio Customization GUI, or by using the I²C/SPI serial control interface through the D2-4P's control interface.

Audio Enhancement Features

The D2-4P family devices include the D2 Audio DSP based audio enhancement suite. The D2 Audio DSP includes a set of enhancement algorithms. These device-specific functions are integrated within the firmware as part of the standard audio processing signal flow and are programmable via control registers.

D2 Audio sound enhancement algorithm (included in the D2-4P/D2-4P/D2-4P/D2-4P devices):

- 2-channel stereo spatialization
- Bass enhancement
- Content / user/application EQ presets
- Improved vocal clarity
- Automatic noise and steep equalization/spl optimization
- Automatic loudness/per-setting/equalization/correction

DTS® HD | DTS | WOW HD™

- Included in the D2-4S/D2-4T device

Each of these enhancements uses its own algorithms, where choice of enhancement is specified by device part number. The DTS enhancements (DTS® HD | DTS | WOW HD™) are included in the D2-4S/D2-4T devices. The D2-4S/D2-4T includes only DTS® | DTS | WOW HD™ support. These enhancements also have their own unique set of programmable parameters to control operation.

Serial Audio Digital Input

The D2-4P device includes one Serial Audio Interface (SAI) port for digital audio input and output. The SAI supports I²S, LJ, RJ, TDM, and provides a slave mode only, support for I²S and LJ data input include 1 standard, and an carry up to 24-bit Linear PCM audio words.

The digital audio input from the SAI input port routes directly through the Sample Rate Converter (SRC). Either the I²S digital input or the S/PDIF Digital input can be selected as the audio path source.

S/PDIF Digital Audio I/O

The D2-4P devices include one IEC60958 compliant S/PDIF Digital receiver input and one IEC60958 compatible S/PDIF Digital transmitter.

The S/PDIF Digital receiver input includes an input translator that supports 32 kHz to 192 kHz frequency, and it also has the capability to decode data. The receiver meets the jitter tolerance specified in IEC60958-4.

The 5-POINT Digital Transmitter complies with the consumer applications defined in IEC60958-3. The transmitter supports 24-bit audio data, but does not support user data and channel status.

Compressed digital formats are not decoded within the IEC60937-2/DTS-CD/WAV/DTS-ES formats. Instead, pass-through mode is supported from the SPDIFRX input to the SPDIFTX output. The SPDIFRX block is fully compliant to IEC60937-2 compliant digital compressed audio input information and can be directed to the 5-POINT Digital output.

Sample Rate Converter

The SRC4HP decodes certain 2-channel asynchronous Sample Rate Converter (SRC) blocks in the audio signal processor. The SRC converts audio data input sampled at one input sample rate to a fixed 48kHz output sample rate. The ratio between input and output audio streams is a single rate for system processing.

Audio data processed from the SRC4HP can be directed to the 5-POINT Digital input source with an input sample rate from 32kHz to 96kHz. The SRC4HP can be used for asynchronous rate to fixed output sample rate, and the SRC4HP output data is re-routed by the SRC to further enhance audio quality.

DSP

The 24-bit fixed-point Digital Signal Processor (DSP) controls the majority of audio processing and system control functions on the chip.

Audio path signal routing, programmable parameter processing blocks, and control logic are defined within the device's firmware. Signal flow through the device is also re-defined and processed through hardware-specific function blocks such as the Sample Rate Converter. Hardware-specific functions are provided with the internal DSP firmware, as well as providing for external control of audio processing parameters.

Clock and PLL

Clocks are generated internally using a fundamental-mode crystal connected across the XTALI and XTALO pins. XTALO is an output, and XTALI can be driven by a 3.3V CMOS-level clock source instead of any other circuit. XTALI is an input that connects to the other side of the crystal.

The clock generation section contains a low-jitter PLL to ensure low noise PWM output and a precise master clock source for sample rate conversion and digital audio interfaces. The PLL can be driven by XTALI VCO clock operates at 12x the crystal frequency (12 x 24.576MHz) and provides complete device and system timing functions. It is used throughout the device, including clock generators for timebase detection, system and powerup reset, DAC, 5-POINT Digital transmitter, and PWM engine timing.

Clock and PLL timebase functions are controlled by internal device firmware. They are not programmable and are optimized for device and system operation.

Timers

Two independent timers are used for device and system control. Timer 0 is used for 1ms timebase for system control operations. The other is used for 1ms timebase for software-generated control algorithms. Two 1/0 pins (TM0 and TM1) are associated with the timers. These pin functions are defined by the device firmware. Only TM0 is actually used in relationship to its timer. TM1 is not used. Timer operation is set by the firmware of the comprehensive monitoring algorithm. Timer 1 is used for internal functions of the device. Its pin (TM2) is not used for this timing operation and is defined by device firmware as the nRESTR input pin.

Audio Outputs

Audio outputs are provided through four output power stages, or six power stages for driving loudspeakers. Three additional PWM outputs are also available for driving low-level audio outputs. Combinations of outputs and their audio processing channel assignment are defined by the device's configuration mode settings.

Output Power Stages

The devices include four independent output stages (Figure 24) that are each implemented using a high-side (p-channel MOSFET) and low-side (n-channel MOSFET) switch. Internal overcurrent monitoring is included in each of these four output stages. Depending on the selected configuration mode, three or four stages can be used independently as single half-bridge outputs or as pairs for full-bridge applications.

Audio processed PWM control waveforms are routed to the inputs of the four output stages, labeled on the OUTD1 and OUTD2, and OUTC1 and OUTC2 pins. Each output stage includes internal overcurrent protection, low-to-high and high-to-low current sensing that feeds to internal monitor logic, and provides for nSHDN output shutdown. Temperature and overvoltage monitoring also provide status and input to device protection control.

FIGURE 24. OUTPUT STAGE

Output Options

The D2-4F devices provide four configuration options for the headphone outputs. The HP_SEL pin is used to select the desired option by strapping the GPIO1 pin HIGH or LOW pin. These defined configurations include:

- Two channels of full bridge, Speakout outputs
- Two channels of full bridge, Speakout outputs
- Four channels of half-bridge outputs
- Two channels of half-bridge and one channel of full bridge

Audio processing routing and control supporting the output stage configurations are also provided. Refer to the Application Note AN-HW-0009, *D2-4F/4E/4T/3E/2E/2U Line, Audio path distribution, audio path output routing, and output stage configurations* are automatically set to each of the four available routes based on their configuration settings.

PWM Audio Outputs

Three PWM outputs provide audio for up to three bi-tonal outputs. Audio processing and power management is provided by these PWM outputs based on the device's available configuration settings.

Using only a single passive filter, the PWM outputs drive headphones, speakers, or both. Four PWM output configurations are added. Both PWM outputs can also drive headphone outputs or D_{OUT} at higher line outputs. (alternately, these PWM outputs can be used to drive powered outputs when using additional power stages on the system design).

Control and Operation

Control Register Summary

The control interface provides access to the registers used for audio processing blocks and functions. The primary control interface ("I²C Input or I²S/TDM master input) and all configuration registers are accessible. The control interface port pins can control the configuration register parameters, and each parameter is defined with its specific register address. Programming details, register identification, and parameter simulations are provided in the *D2-4 Family, D2-4F/4E/4T/3E/2E/2U Specification* to this extent.

I²C-2-Wire Control Interface

The D-Wire I²C-compatible interface shares communication with an external controller. This interface is usable through either an external microcontroller host, or for communication to EEPROM, or other compatible memory devices.

The I²C interface supports normal and fast mode operation and is multi-master capable. In I²CD 4F system application, it operates as an I²C slave device where the system controller operates as the I²C master.

Reading and Writing Control Registers

All reads or writes to registers (shown in Tables 3.0 and 3.1) begin with the Device Address byte, followed by the Register Address byte, then Register Address Increment byte, and a Write Condition.

Register writes through the I²C interface are initiated by setting the read/write bit low to write to the device address byte. The Write sequence is shown in Table 3.0 on page 14 as described in Table 3.

Table 3. Pin Assignments

BYTE	BIT(S)	DESCRIPTION
0	Device Address	Device address with Write bit low
1	Register Address [23:16]	Upper-right bits of address
2	Register Address [15:8]	Middle-right bits of address
3	Register Address [7:0]	Lower-right bits of address
4	Data [31:24]	Upper-right bits of host data
5	Data [23:16]	Middle-right bits of host data
6	Data [7:0]	Lower-right bits of write data

All reads to registers, shown in Table 3 on page 14, require two bytes to set the register address, followed by a repeated start condition of sending a Read. Following the device address with the write bit set, and three register address bytes. Next, the master must send a repeated Start, send the device address with the read/write bit set to Read, and read the next three data bytes. The register address increment byte is set to 0x00 when you send a Not Acknowledge (NACK) on the 9th clock pulse and then send a Stop condition to complete the transaction. The device's control interface acknowledges each byte by pulling SDA low on the 9th clock received, following each write byte. The read sequence shown in Table 3.0 is described in Table 4.

Table 4. Pin Assignments

BYTE	BIT(S)	DESCRIPTION
0	Device Address	Device address with Write bit low
1	Register Address [23:16]	Upper-right bits of address
2	Register Address [15:8]	Middle-right bits of address
3	Register Address [7:0]	Lower-right bits of address
4	Device Address	Device address with Read bit high
5	Data [31:24]	Upper-right bits of host data
6	Data [23:16]	Middle-right bits of write data
7	Data [7:0]	Lower-right bits of write data

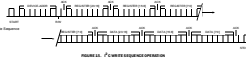

FIGURE 33. I²C WRITE SEQUENCE OPERATION

FIGURE 34. I²C READ SEQUENCE OPERATION

Control Interface Address Spaces

Registers are accessed through the I²C control interface using the I²C channel address of 0x82. This establishes the device as a slave under control through I²C communication as the D2-4P.

Registers and memory spaces are defined within the D2-4P for the I²C control interface using 16-bit addressing. The upper byte of the register address (Bits [23:16]) determines the internal address space used for control read or write access. The remaining 8 bits (Bits [15:0]) determine the actual address within that space.

Programmable settings for the audio processing blocks are internally mapped to the address space defined by the highest order bits (A1 thru. An example, 0x020xxx, where xxx is the address bits to address within this address space.

Storing Parameters to EEPROM

The D2-4P includes parameters data to an EEPROM. If an EEPROM is installed on the application, the programmable parameters can be stored to the EEPROM memory. This stored data can then be recalled on a user reset or power-up.

Serial Peripheral Interface (SPI)

The Serial Peripheral Interface (SPI) is an alternate serial input port that provides an interface for loading parameter data from an optional EEPROM or Flash device during boot-up operation.

The four SPI interface pins are all shared functions:

- Following a reset condition and while the device is initializing the boot-up process, these four SPI pins (TEMPEN*, SDA, SCL/MISO, and VOL1/MISO, VOL2/MISO) function as a SPI input port for external boot loading operations.
- As soon as the boot-up process is completed and the device is ready to begin normal operation, these four pins are set to be used for SPI functions and are available for the firmware for use as dedicated function I/O for another operation.

See the corresponding pin descriptions in Table 2 for more information about these pin functions.

Reset and Device Initialization

The D2-4P must be reset to initialize and begin proper operation. A system reset is initiated by applying a low level to the nRESET input pin. External hardware circuitry or a controller within the amplifier system design provides the reset signal and must connect to the nRESET input to initialize the reset process. Device initialization begins when the nRESET pin is released from its low active state.

The chip contains power-on-reset sensors and brownout detectors on the 3.3V VCC3 and PWRVDD power supplies and the 1.8V CORE power supply. A loss or droop of power from these supplies below the minimum levels for 1.8V and 3.3V will activate the reset output pin, driving it low. The nRESET pin should connect to the nRESET input through hardware on the amplifier design to ensure a proper reset occurs if the power supply voltages drop below their design specifications.

At the deactivation of nRESET, the chip reads the status of the boot mode selection pins (PSDA and PSCK) and begins the boot sequence according to the selected boot mode. The default boot mode is logic-level low. These three pins are equipped either high or low on the system's design (PCB). The state of these pins that is latched into defines the boot mode operation.

Boot Modes

The D2-4P devices contain embedded firmware to operate the device. The boot mode determines how the embedded firmware is to be programmed and logic can be written to the device after it is operational and running. However, parameter data can also be read at boot time, which allows a saved configuration setting to be used, or allows amplifier function to be set through a system microcontroller connected to the SPI or I²C control port. Various boot possible boot modes, allowing control and data to be provided through these boot sources:

- I²C slave (to external microcontroller)
- I²C EEPROM
- Internal device ROM only
- SPI slave

The specific boot mode is selected based on the state of the GPIO[3:0] pins during the boot process. The available boot modes and their functions are shown in Table 4. Note "Boot mode" must be configured before the device is powered up, as the boot process begins immediately after power-up.

TABLE 4. BOOT MODE SETTINGS

BOOT MODE	GPIO3	GPIO2	GPIO1	GPIO0	DESCRIPTION
0	0	0	0	I²C Slave	Operates as an I²C slave based on address GAIN. An external I²C master provides the boot source.
1	0	0	1	I²C Master	Operates as an I²C master and boots from a serial boot ROM with the I²C address 0xA0.
2	0	1	0	SPI Slave	Operates as a SPI slave and boots from a serial boot ROM.
3	0	1	1	ROM Only	SPI Slave. An external MCU provides the boot code.

The device initializes as defined by its boot mode, but gets its configuration and parameter data from the boot device. This boot device is normally a serial EEPROM connected to the SPI port of the amplifier device, with an external controller and an EEPROM, the EEPROM loads first. During this time, the controller must remain off-line.[1] Its boot code offers the reading sequence from the EEPROM to complete.

Power Supply Requirements

The device requires operating power for these voltages.

- PMVDD: 5.0 Volts
  - 3.3V DC supply voltage
  - 5VDD regulated from external and 0 logic
  - PMVDD is the same voltage and is used for the PWM outputs and output stage driver
- CVDD and PLLVDD
  - 1.8V DC supply voltage
  - CVDD operates the internal processor and DSP core
  - PLLVDD also operates at the internal processor voltage levels, but is provided through a separate connection to allow for improved noise filtering for the internal processor requirements
- "High Voltage" (VHDD(AD), and VDDV)
  - VHDD(AD) and VDDV are the "HV" supplies are the "high voltage" supplies used for operating each of the four output power stages.
  - VDDV is used as the source for the on-chip +9V regulator that is used for the output stage drivers.
  - Individual power (VHDD(AD)) and their corresponding ground connections are provided for each channel of the four power stages, providing additional isolation between channel impedance source connections to each of the outputs. All the VHDD(AD) VDDV pins are connected to the same voltage source

Single-Gate Drive Voltage

As one chip-function should prevents the gate drive voltage used for each output stage. A pin is included for each output stage driver (HVBE[4:0]) for connection of a capacitor (nominal, 0.22µF) to form this pin to the device's PWM supply.

Drive is for higher-side FETs on the output stages require a voltage that is higher than the voltage supplied to the VHDD(AD) pins, pumping action of the driving MOSFETs to drive produces the "booststrap" voltage, and uses this capacitor to filter and hold this gate drive voltage. This gate drive voltage is generated without needing a connection to an additional power supply voltage.

Power Supply Synchronization

The the PWSYNC (YES) pin provides a power supply synchronization signal for switching power supplies. If power configures this pin to the frequency and duty cycle needed by the switching power supply. This allows synchronization of switching supplies used with the device to operate without generating in-band audio interference signals. But could occur if the switching power supply is not locked to the amplifier switching.

This PWSYNC (YES) pin is a shared pin (see the multiple-purpose pin descriptions in Table 3 on page 10). During the power-up and initialization, the pin operates as one of its configuration input. Then, after initialization, the pin is used as a clock output signal configuration mode. After completing reset and when the device firmware begins operating, this pin becomes the PWSYNC output.

Power Sequence Requirements

Voltage sensors and brownout detectors monitor supply voltages during all modes of operation. Power-on reset circuitry is also monitoring power-up sequencing of supply voltages to ensure their specified limits. However, during application of power, the CODEC and DSUB LDO regulators' outputs should be brought up together to avoid high current transients that could halt system power supply regulation.

During application of power to the system and while the CODEC and DSUB LDO regulators' outputs are being brought up, both the PSSD and PSRESET signals (if external +3.3V) shall not exceed the voltage that is present at CVDD -0.7

$V_{CVDD} - 0.7$ (minimum) $\leq V_{PSSD}$ (maximum) $\leq V_{CVDD}$

$V_{CVDD} - 0.7$ (minimum) $\leq V_{PSRESET}$ (maximum) $\leq V_{CVDD}$

Failure to meet this requirement may cause the system to momentarily design (3.3V/core) CVDD and DSUB regulator's output(s).

The best practice is for all supplies to feed from regulators using a common power-on control. Supply bus can be achieved by using a single-line voltage supply power source and regulating the 3.3V and 1.8V supplies from that source. See the application note [TechnicalNote1](#) on page 6 all voltages of the same sources must be tied together at a single point.

REGSV

The output stage internal drivers require their own +5VDC supply voltage. An on-chip regulator operates from the VDDHV voltage to provide the +5VDC REGSV voltage. A 1.0µF ceramic or other low capacitor connected to this regulated voltage. A 1.0µF or 0.1µF capacitor should be connected to this pin, and the connection should be as close as practical to the pin. This internal +5V is used only by the output's sige drivers. Do not make other connections to this pin.

Pin and Control Block Functions

I/O Control Pins

Several device pins are used as specific function inputs and outputs to control amplifier and device operation. These pins are described in this section. Pin names are followed by input or output, "out/pu," "out/pd," "in/pu," "in/pd" or "in/out" as appropriate, and their specific function is briefly defined by the D2-4P REGS register. The Pin Assignments and Terminal Functions and Functional Block Diagram sections in this datasheet include illustrations of the functional blocks where these pins are used.

Some pins, such as gain, frequency, and filter functions are set up accordingly by the operational state (for example, resetting, initializing, booting, running) of the D2-4P. Those multiple-purpose pins and their descriptions and uses are described in more detail in Table 8, on page 23.

nPDN Input Pin

The nPDN pin is a control input that is used to power-down the outputs. When this input is pulled low, all audio outputs turn off and the internal oscillator is stopped. The nPDN pin has digital logic to connect to all of the output stages' Hi-Z control logic and other references remain active during this power-down state. Asserting nPDN also causes all I²C registers and memory to be put in default state.

Each of the four output stages incorporates its own latching overcurrent detection circuitry logic. In addition to the separate protection events that occur through firmware control from an overcurrent condition, thermal protection circuitry incorporates other steps to clean the hardware latched shutdown, although issuing nPDN resets the hardware latched shutdown.

The nPDN pin is active low and is inactive when at logic high. In normal operations, it is held high with pull-up to the REGS supply.

nERROR[2-1] Output Pins

Each of the four output stages includes a low-level overload and overcurrent monitor. An overcurrent or overload condition asserts the nERROR output for that channel.

An undervoltage condition for the voltages used by the output stages also asserts nERROR. The nERROR pin is an open-drain output that requires a pull-up resistor to operate.

The nERROR pins are open drain, active-low, and can be wire-or connected together. Depending on the application's wire-or configuration where more than one output stage can be used for a multi-channel, nERROR pin assignments for each audio channel are considered together to provide the monitoring status.

For applications where multiple power supplies are derived from a single source, the nERROR pins for the 4 two-power stages (PWRSEL[2-1]) can be wire-or connected together. See the Application Information section for the nERROR pin connections for the different configuration modes.

IREFPin

The IREF pin sets the overcurrent and overload monitoring threshold. The design requires a 30KΩ resistor to connect from this pin to ground.

Configuration Assignment Pin Differences

The signs of pins are defined in configuration assignment. Multiple pin pairs are used for the designations, and their settings must be considered when requirements for the configuration mode. The pin pairs are:

- GCFG2, GCFG1. Defines the output stage topology and operation of the output configuration
- nERROR[2:0], PWRSEL[2:0]. Defines the audio processing and amplifier control supporting the output configuration

GCFG2, GCFG1 Input Pins

These two pins define the configuration of the four output stages. The GCFG2 pin is used to define the number of channels (2 or 4) and PWRSEL[2:0] signals group if PWRSEL0 is available which of the four output configurations is used in the design. See Pins Descriptions, starting on page 6, for additional information.

nERROR/CFG0 and PSSTNC/CFG1 Pins

These pins define the amplifier configuration mode that the firmware will use during power-up. In addition to the nERROR and CFG1 pins, that act in operation of the output stages, the nERROR/CFG0 and PSSTNC/CFG1 pins also establish audio signal processing path assignments and set up monitoring and protection for the configuration mode. The configuration pin logic states are established by pull-up or pull-down resistors installed on that application.

The configuration defined by these pins is assigned when the CS/WDT/DZ-4000 unit, its reset state. At that time, the high statuses of the PSSTNC/CFG1 and nERROR/ CFG0 pins are latched into internal device registers. These are shared function pins, and after firmware begins executing, their functions are redefined as nERROR and PSSTNC. See Table 6 for more information about these pins and their shared functions.

A Negative Temperature Coefficient (NTC, 330kΩ) resistor connects to the TEMP1/ NTCM pin, and using the resistor's temperature/resistance correlation, the firmware monitors temperature of the NTC resistor. The internal device timing functions associated with the TDD pin provide calibration that is used by the firmware. The TEMP1/ NTCM pin connects to the TEMP2/NTCR pin and is used as a constant room-temperature-dependent reference for this algorithm.

The firmware algorithm is relevant to the DSP. The status from this temperature monitor is used for the temperature protection functions of the device and its application. There are no adjustments or parameters for changing settings.

Temperature Monitoring

The TEMP1/NTCM, TEMP2/ NTCR, and TEMP3/CNS/ TDD pins are used for temperature monitoring of the device and its application. These pins share shared functions (see the package pinout pin descriptions in Table 6 on page 7). During firmware execution, they operate as inputs and outputs for the measurement algorithm. Figure 11 shows the circuit for this temperature measurement implementation.

FIGURE 11: TEMPERATURE MONITOR CIRCUIT

TABLE 5: DSLAM MODE I/O CONTROL PIN ASSIGNMENT AND OPTIONS

PIN NAME	FOR DSLAM MODE CONFIGURATION			FOR DSLAM MODE OPERATION	
	FUNCTION	I/O		FUNCTION	
TSSPIBCT/ SDA	Output	Bit-clock master/slave	Input	Determines master or between master and slave for transferring digital audio	Typical connection is to a 10.0kΩ resistor to select high to enable the SPI master or I2C slave mode. Connection to VSS selects SPI slave mode application.
SCLL/ MISO	Input or Output	SPI master input or slave output. Bidirectional for the I2C bus data.	Input	Selects control Phase B input. Used for encoding	Typical connection is to a 10.0kΩ pull-up resistors and to a 2.2kΩ volume control encoder.
TSSPILI/ MOSI	Input or Output	SPI master output or slave input. Bidirectional for the I2C bus data.	I/O	Determines master or between master and slave for transferring digital audio.	Typical connection is to a 10.0kΩ/VDD pull-up resistor. Connection to VSS selects slave mode for SPI control if SPI is used in application.
nERROR/ CPOL	Output	CPOL0 Configuration Mode Input Select. Clamp all up or pull down to VDD or VSS through a resistor to one of four configuration options.	Output	Active low output amplifier protection and monitoring status indicators.	Connects to +3.3V via a 10 ground with a 10kΩ resistor to select high logic or low for setting the amplifier protection and monitoring status. Use resistor or indicator circuit to provide device (called "FEEDS" on some or between settings.
PWRPLC/ CPO1	Output	CPO1 Configuration Mode Input Select. Clamp all up or pull down to VDD or VSS through a resistor to either high or low to achieve one of 4 amplifier configurations.	Output	Sync Output for Synchronizing On-Board Power Supply regulators	Connects to +3.3V via a 10 ground with a 10kΩ resistor to select high logic or low for setting configurations. Use connection to the clock input logic of the on-board switching regulator (called "PLLCAP" on some between settings.
CS/CO/ nAD	Input	SPI Slave Select.	Input	Volume Control Phase A input. Used for encoding rotary encoder volume control.	Typical connection is to +3.3V with 10kΩ pull-up resistors and to a 2.2kΩ volume control encoder.

Configuration Setting

The configuration mode is assigned through two pairs of pin settings. When the D2-4F exits its reset state, the logic states of the PWRPLC/CPO1 and nERROR/CPO0 pins are latched as the internal device registers. During this initialization time, these pins are configured as inputs. After the initialization sequence, the internal chip hardware begins executing. These pins are reassigned as outputs for their shared functions, and the internal latched logic state for the configuration will remain resistive until the device is powered down or reset again. The DCPO0 and DCPO1 pins are open-drain. Select these pins must remain in their pull-up or pull-down state.

Selection of one of the four configuration modes is defined by engaging the configuration pins high or low:

- DCPO0 and DCPO1define the output power-stage configuration
- nERROR/CPO0 and PWRPLC/CPO1 define the amplifier and channel configuration

These four pins are connected to either a high level (+3.3V) or low level (ground). Pull resistors should be through a 10kΩ resistor and not directly to the supply or ground.

Table 6 on page 28 shows the audio pre-analog channel assignment, audio content, and output assignments for each of the four configuration modes.

Both pairs of configuration setting pins (DCPO0, DCPO1) and (nERROR/CPO0, PWRPLC/CPO1) should be used and both must be set to the same configuration mode.

In modes 2 and 3, the filtering for high and low pass processors is applied to the audio signal flow path, enabling the appropriate high or low pass content to be properly filtered for the PWM output channels.

TABLE 1. CONFIGURATIONS AND CHANNELS ASSIGNMENTS

| Mode | CONFIG0 (Power-on-Reset Latch) | CONFIG1 (Power-on-Reset Latch) | CONFIG2 (Power-on-Reset Latch) | CONFIG3 (Power-on-Reset Latch) | PWM OUTPUT CONFIGURATION | | |

Protection

The D2-4P devices include multiple protection mechanisms. Output overload and overcurrent detect for each output stage provide two levels of monitoring. Temperature monitoring is provided for each output stage. Each of these fault detection functions is latched to the corresponding output.

The D2-4P devices use several strategies to prevent damage from the high voltages, currents, and temperatures present in class-D amplifiers. This protection is also effective against user-induced faults such as shorting, output overload, or output shorts, including both short-to-ground and short-to-ground faults. Protection includes methods such as:

- Output overcurrent
- Output short-circuit
- Over-temperature
- Power-supply brown-out
- Shoot-through overcurrent

Certain levels of protection are managed using on-chip hardware. Other protection is integrated into device firmware, and involves actions to:

- Shut down the outputs for a short-circuit, over-temperature, or undervoltage event.
- Shut down the device if power-supply sensors detect voltages dropping below the valid operating thresholds.
- Provide initialization and device-hardware (if needed) for power-supply sequencing. Power-supply sequencing typically involves controlled shutdown in case of high-current conditions.
- Chip-temperature monitoring provides dual threshold status of high temperature conditions, providing both indication and device shutdown if needed.

Error Reporting

The system and device internal monitoring uses an I²C bus (nERROR/CSEL) as an output to signal a shorted shutdown event or a thermal-overload shutdown event condition. This output can be used to turn on a simple indicator.

The error output is also used to signal an external microcontroller that the I²C bus may be busy. When the error output is low during system initialization, the I²C bus is busy as a master device.

This error output is latched low and only becomes active as an error reporting output after the device firmware initialization and begins running. The error pin is shared as an input (see Table 4.1 in the data sheet) for more information about shared function pins).

The error output is latched low when a fault occurs. Reading the error bit key input goes used to define the configuration mode. A resistor pull-up or pulldown on this pin establishes the mode input configuration at reset. After completing the initialization sequence, these resistors do not affect the error output operation.

Short-Circuit and Overcurrent Sensing

Each PWM output FET includes a dual-threshold overcurrent detection. Overcurrent detection is implemented to protect the system against overcurrent events:

- The lower (threshold) monitors fault conditions such as shorts and overloads at the loudspeaker outputs.
- The higher threshold monitors fault conditions of the PWM output pin
- The nERROR output asserts for the channel detecting the fault.
- For the lower level threshold, nERROR remains asserted as though the duration of the overcurrent event.
- For the higher threshold, the output is latch-low and the nERROR output is asserted. These conditions remain latched until the controller processor clears the fault by writing 1 of the channel's PWM driver the PWM pin fault, when shut down.

The intent is to latch into the shutdown state for the loudspeaker PWM switching transient events.

Protection Timing and Control

The overcurrent detection is governed within a pulse or latched logic level depending on the type of fault and the protection duration of high current. The detector state is presented to the PROTECTED pin.

The PROTECTED1 pins are used as protection inputs to the corresponding PWM output pins. The PROTECTED1 input pins are connected to the corresponding PWM output pins. The PWM output pins and the PROTECTED1 input pins are connected to the lower level on the system and output mode configuration shown in Table 4.1 on page 23.

Thermal Protection and Monitors

Temperature sensing provides two thresholds of temperature monitoring.

If the device reaches the lower threshold, a warning indication is generated and one level of thermal-protection management is triggered.

The lower threshold thermal protection shuts down the device upon a high-threshold temperature condition. If the device reaches the higher temperature threshold, the device shuts down and latches the output stage. It also drives all 3-level outputs to the mid-level (active), providing this shut-down status to the firmware through the connected PROTECTED pin inputs.

Graceful Overcurrent and Short-Circuit

Hard faults from overcurrent or short-circuit conditions shutdown the output stage. Soft faults from overcurrent or short-circuit conditions shutdown. To lower threshold event detections, graceful protection is provided for each output. Specific operation depends on the device and the type of detected event, but action taken is to reduce conditions that contribute to the event, such as reducing gain or incomplete activation of the PWM output drivers.

Overcurrent monitoring status is presented to the PROTECD1 inputs have per-output detector status that drives the

ARMORED Audio power-down/over-detection algorithms in three-ear monitor (three-pair level detection), and dual-detection of an overload condition, automatically reduce PWM gain. This Automatic Gain Control (AGC) action helps prevent audio output clipping and helps avoid related excessive level conditions. **ARMORED** Audio also includes a Dynamic Range Compression (DRC) and PWM gain rollback-recovering thru characteristics and tone-event detection of overloads. At the lower (non-shut-down) high-temperature threshold, the AGC function also acts to attenuate the outputs to attempt to reduce temperature.

Output level gain and level-change effects from the AGC function are similar to operation from a compressor. However, while a compressor is typically used to reduce the dynamic range of audio, the PWM AGC function is controlled through detection of near-overload output levels or from high-temperature detection.

Power Supply Voltage Monitoring

Undervoltage sensors and brownout detectors monitor all supply voltages to the device. The logic and built-in protection of this voltage-monitoring prevents operation until all supply voltages are within their specified limits. If any of these monitored voltages drop below their threshold, the device shuts down its outputs and asserts the nFAULT or nERROR outputs.

Audio Processing

The audio processing, signal flow, and system definition is defined by the D2-4P internal ROM firmware and is executed by the DSP. The firmware defines the audio flow architecture, including the audio processing blocks. Each block is configurable through the I²C/SPI serial communication interfaces. The signal flow and audio processing blocks are shown in Figure 39. This architecture includes audio processing functions for:

- Input selection
- Mixers
- Input compressors and output limiters
- Tone controls
- 5-band and 3-band parametric equalizers
- Router
- High-/low-pass crossover filters
- Volume and output level controls
- Loudness contour

Enhancement Audio Processing

The D2-4XXDT supports the D2-Audio DSP Sound Enhancement Algorithm. The D2-4XXDT supports the DTS®(SRS) WOW HD™ algorithm.

Audio Processing Signal Flow Blocks

INPUT SELECTION

The Input Select register specifies the audio inputs that are assigned to the audio processing input path. Either the I²S or S/PDIF Digital inputs are available.

MIXERS

An input mixer provides a two-input, two-output mixing and routing path. Either input can be mixed at adjustable gain into the left and right channel outputs. The default setting is that through each channel, with full unit-'0' for non-through channels. Attenuation is continuously variable with fine programmable parameters.

Actress mixer provides a path from the two input channels. Stereo mixers are typically used to provide a mix of both stereo input channels for crossover processing and become the source for the crossover channel. Gains for both input channels are adjustable to feed the single stereo mixer output.

TONE CONTROLS

Both input channels contain a tone control block. Each of the tone control blocks is a programmable 5-band equalizer.

Both tonizers can all using programmable coarse frequency and a boost or attenuating gain. The original flow processing automatically provides a smooth transition between tone control changes.

FIGURE 58. 32-BIT AUDIO SIGNAL FLOW

COMPRESSORS AND LIMITERS

Two individual input compressors are included in the input audio path. Each has its own set of parameters. Peak limiters are also included on the input and output channels. The Compressor and Limiter blocks operate identically, and their parameters are adjustable in the same manner as the EQ blocks. Typically, the input EQ blocks are programmed to provide a compression function and the output path blocks are programmed to limit output signal levels. However, each path can be programmed as needed. Each Compressor/Limiter has adjustable Attack and Release Time, Threshold, Attack and Release Time, and Look-Ahead Mode.

MULTI-BAND EQUALIZERS

Three sets of Multi-Band Parametric Equalizers are included in the audio signal processing path. Each band of the equalizer has programmable Gain, Frequency, and Q factor implementation.

A Bi-directional Loss and Speaker Equalizer (BSEQ) are included in both of the two input channels. Four 3-Band Equalizers are also located in the four output channels.

STEREO ROUTER

A 4x4 stereo router assigns any one of the four input channel paths to each of the four output paths. The router performs path assignment only. It does not provide gain or signal level adjustment.

HIGH/ LOW-PASS CROSSOVER FILTERS

High-Pass and Low-Pass filter blocks are provided for each of the four output channels downstream of the Stereo Router and Mixer Mixer. These filter blocks provide a flexible Crossover function for multi-way loudspeaker systems by defining the selected output channel's frequency response.

The High and Low Pass blocks operate together and are implemented as a total of four cascaded biquads. Each of each of the elements are allocated for High Pass functionality and the other two elements are allocated for Low Pass functionality. Complete flexibility allows each element to be optimally defined for the desired filter function. The filter coefficients are those for a type of 6dB, 12dB, 18dB, or 24dB, or can be bypassed. Butterworth, Bessel, or Linkwitz-Riley filter implementations are available.

MASTER VOLUME CONTROL

See the software-controlled Master Volume control to adjust the global volume for all four output channels. Master Volume operates simultaneously adjustable attenuation, from unity gain down to -120dB and cutoff.

Each of the four output channels has its own dedicated output level adjustments that provides individual channel gain or attenuation. Each channel's output level range provide output level adjustment from +12dB to -120dB.

LOUDNESS CONTROL

An individual software-controlled Loudness Control is included in the four output channel's output adjust channels. The Loudness Control curve is customized to allow for dynamically and automatically enhancing the frequency response of the audio signal in accordance with the ISO 226 Equal Loudness Contour. The Loudness Control modifies the audio frequency response as defined by the Robinson/Munson audio response curve. It provides amplitude or volume changes to signals to which the ear does not respond equally at very low listening levels.

SOUND ENHANCEMENT ALGORITHM PROCESSING

The D2-Audio DSP Sound Enhancement Algorithm suite powerfully provides a full set of enhancements to audio that greatly add to the quality and listening experience of sound in automotive applications. The D2-Audio DSP Sound Enhancement Algorithm suite psychoacoustic processing that creates a richly-sounding environment from small speakers and synthesizes the sound and quality equivalent to more complex systems. It is especially suited to consumer products that include televisions, docking stations, and mini-hi-fi stereo products.

Sound enhancement algorithm processing includes:

- 2-channel stereo spatialization
- Bass enhancement
- Content / configuration EQ presets
- Improved vocal clarity
- Automatic room audio setup / equalization / optimization
- Automatic loudspeaker-setup / equalization / correction

The D2-Audio DSP Sound Enhancement Algorithm is completely included within the D2-4P Family devices.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Visit our website to make sure you have the latest datasheet revision.

Date	Revision	Content
Mar.31, 2020	FN6785.2	Changed declaration base part number to "D2-2P" Family Audio SOC. Changed the following terms throughout the datasheet: "DSEadvi" to "3D Audio DSP" "DSE" to "Audio DSP" "SSE-2P" to "D2-2P Family" "Digital Audio Engine" to "Digital Audio Processor" Updated "Dolby Digital Plus Decoder Enhancement Algorithm" Updated Related Literature Updated audio sub-assessment features on page 25. Updated Figure 18 on page 26, Figure 19 on page 28 and Figure 20 on page 31 Removed General overview section. Updated disclaimer.
May.15, 2018	FN6785.1	Updated vector datasheet supporting Internet's new standards. Updated the Ordering Information table on page 2. Updated Figure 1 on page 4 to change to Advanced Internet settings. Added DTS disclaimer.
Jul.29, 2016	FN6785.0	Initial Release

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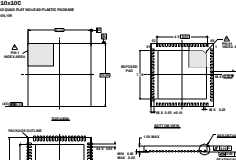
Package Outline Drawing

For the most recent package outline drawing, see L28.10x10C.

L28.10x10C

28 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE

Rev 0, 06/09



NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension is applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin#1 indentifier may be either a mold or mark feature.

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