

3 μ A Comparator with Integrated Reference Voltage

Features:

- Factory Set Reference Voltage
 - Available Voltage: 1.21V and 2.4V
 - Tolerance: $\pm 1\%$ (typical)
- Low Quiescent Current: 2.5 μ A (typical)
- Propagation Delay: 4 μ s with 100 mV Overdrive
- Input Offset Voltage: ± 3 mV (typical)
- Rail-to-Rail Input: $V_{SS} - 0.3$ V to $V_{DD} + 0.3$ V
- Output Options:
 - MCP65R41 $\rightarrow$ Push-Pull
 - MCP65R46 $\rightarrow$ Open-Drain
- Wide Supply Voltage Range: 1.8V to 5.5V
- Packages: SOT23-6

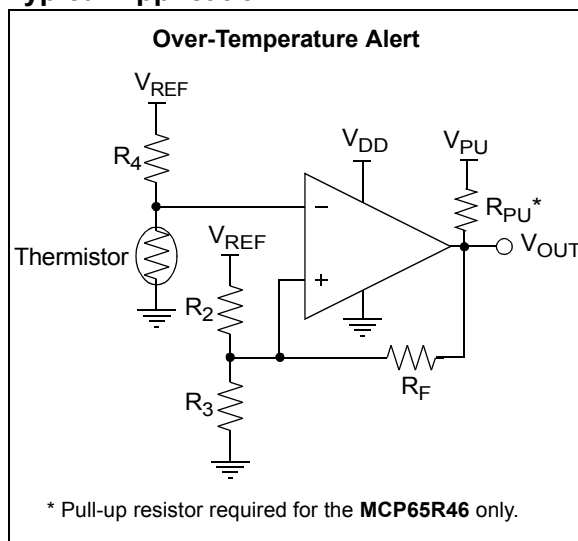
Typical Applications:

- Laptop Computers
- Mobile Phones
- Hand-held Metering Systems
- Hand-held Electronics
- RC Timers
- Alarm and Monitoring Circuits
- Window Comparators

Design Aids:

- Microchip Advanced Part Selector (MAPS)
- Analog Demonstration and Evaluation Boards

Typical Application



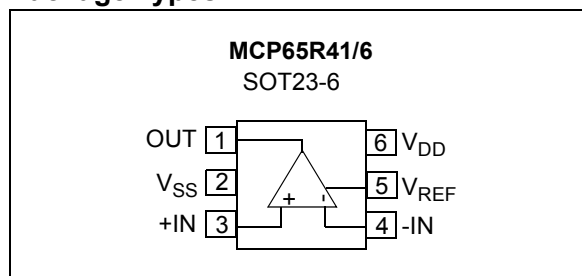
Description:

The Microchip Technology Inc. MCP65R41/6 family of push-pull and open-drain output comparators are offered with integrated reference voltages of 1.21V and 2.4V. This family provides $\pm 1\%$ (typical) tolerance while consuming 2.5 μ A (typical) current. These comparators operate with a single-supply voltage as low as 1.8V to 5.5V, which makes them ideal for low cost and/or battery powered applications.

These comparators are optimized for low-power, single-supply applications with greater than rail-to-rail input operation. The output limits supply current surges and dynamic power consumption while switching. The internal input hysteresis eliminates output switching due to internal noise voltage, reducing current draw. The MCP65R41 output interfaces to CMOS/TTL logic. The open-drain output device MCP65R46 can be used as a level-shifter from 1.6V to 10V using a pull-up resistor. It can also be used as a wired-OR logic.

This family of devices is available in the 6-lead SOT-23 package.

Package Types



MCP65R41/6

NOTES:

1.0 ELECTRICAL CHARACTERISTICS

1.1 Absolute Maximum Ratings†

$V_{DD} - V_{SS}$	7.0V
All other inputs and outputs.....	$V_{SS} - 0.3V$ to $V_{DD} + 0.3V$
Difference Input voltage	$ V_{DD} - V_{SS} $
Output Short Circuit Current	± 25 mA
Current at Input Pins	± 2 mA
Current at Output and Supply Pins	± 50 mA
Storage temperature	-65°C to $+150^{\circ}\text{C}$
Ambient temperature with power applied....	-40°C to $+125^{\circ}\text{C}$
Junction temperature	$+150^{\circ}\text{C}$
ESD protection on all pins (HBM/MM).....	≥ 4 kV/200V
ESD protection on MCP65R46 OUT pin (HBM/MM).....	≥ 4 kV/175V

†**Notice:** Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

Unless otherwise indicated, all limits are specified for: $V_{DD} = +1.8V$ to $+5.5V$, $V_{SS} = \text{GND}$, $T_A = +25^{\circ}\text{C}$, $V_{IN+} = V_{DD}/2$, $V_{IN-} = V_{SS}$, $R_L = 100$ k Ω to $V_{DD}/2$ (**MCP65R41** only), and $R_{\text{Pull-Up}} = 2.74$ k Ω to V_{DD} (**MCP65R46** only).

Parameters	Sym	Min	Typ	Max	Units	Conditions
Power Supply						
Supply Voltage	V_{DD}	1.8	—	5.5	V	
Quiescent Current per Comparator	I_Q	—	2.5	4	μA	$I_{OUT} = 0$
Input						
Input Voltage Range	V_{CMR}	$V_{SS}-0.3$	—	$V_{DD}+0.3$	V	
Common-Mode Rejection Ratio $V_{DD} = 5V$	CMRR	55	70	—	dB	$V_{CM} = -0.3V$ to $5.3V$
		50	65	—	dB	$V_{CM} = 2.5V$ to $5.3V$
		55	70	—	dB	MCP65R41 , $V_{CM} = -0.3V$ to $2.5V$
		50	70	—	dB	MCP65R46 , $V_{CM} = -0.3V$ to $2.5V$
Power Supply Rejection Ratio	PSRR	63	80	—	dB	$V_{CM} = V_{SS}$
Input Offset Voltage	V_{OS}	-10	± 3	+10	mV	$V_{CM} = V_{SS}$ (Note 1)
Drift with Temperature	$\Delta V_{OS}/\Delta T$	—	± 10	—	$\mu\text{V}/^{\circ}\text{C}$	$V_{CM} = V_{SS}$
Input Hysteresis Voltage	V_{HYST}	1	3.3	5	mV	$V_{CM} = V_{SS}$ (Note 1)
Drift with Temperature	$\Delta V_{HYST}/\Delta T$	—	6	—	$\mu\text{V}/^{\circ}\text{C}$	$V_{CM} = V_{SS}$
Drift with Temperature	$\Delta V_{HYST}/\Delta T^2$	—	5	—	$\mu\text{V}/^{\circ}\text{C}^2$	$V_{CM} = V_{SS}$
Input Bias Current	I_B	—	1	—	pA	$V_{CM} = V_{SS}$
$T_A = +85^{\circ}\text{C}$	I_B	—	50	—	pA	$V_{CM} = V_{SS}$
$T_A = +125^{\circ}\text{C}$	I_B	—	—	5000	pA	$V_{CM} = V_{SS}$
Input Offset Current	I_{OS}	—	± 1	—	pA	$V_{CM} = V_{SS}$
Common Mode/ Differential Input Impedance	Z_{CM}/Z_{DIFF}	—	$10^{13} 4$	—	ΩpF	

Note 1: The input offset voltage is the center (average) of the input-referred trip points. The input hysteresis is the difference between the input-referred trip points.

- Limit the output current to Absolute Maximum Rating of 30 mA.
- Do not short the output of the **MCP65R46** comparators above $V_{SS} + 10V$.
- The low-power reference voltage pin is designed to drive small capacitive loads. See [Section 4.5.2](#).

MCP65R41/6

DC CHARACTERISTICS (CONTINUED)

Unless otherwise indicated, all limits are specified for: $V_{DD} = +1.8V$ to $+5.5V$, $V_{SS} = GND$, $T_A = +25^{\circ}C$, $V_{IN+} = V_{DD}/2$, $V_{IN-} = V_{SS}$, $R_L = 100\text{ k}\Omega$ to $V_{DD}/2$ (MCP65R41 only), and $R_{Pull-Up} = 2.74\text{ k}\Omega$ to V_{DD} (MCP65R46 only).						
Parameters	Sym	Min	Typ	Max	Units	Conditions
Push Pull Output						
High Level Output Voltage	V_{OH}	$V_{DD}-0.2$	—	—	V	$I_{OUT} = -2\text{ mA}$, $V_{DD} = 5V$
Low Level Output Voltage	V_{OL}	—	—	$V_{SS}+0.2$	V	$I_{OUT} = 2\text{ mA}$, $V_{DD} = 5V$
Short Circuit Current	I_{SC}	—	± 50	—	mA	(Note 2) MCP65R41
	I_{SC}	—	± 1.5	—	mA	(Note 2) MCP65R46
Open Drain Output (MCP65R46)						
Low Level Output Voltage	V_{OL}	—	—	$V_{SS}+0.2$	V	$I_{OUT} = 2\text{ mA}$
Short Circuit Current	I_{SC}	—	± 50	—	mA	
High-Level Output Current	I_{OH}	-100	—	—	nA	$V_{PU} = 10V$
Pull-up Voltage	V_{PU}	1.6	—	10	V	Note 3
Output Pin Capacitance	C_{OUT}	—	8	—	pF	
Reference Voltage Output						
Initial Reference Tolerance	V_{TOL}	-2	± 1	+2	%	$I_{REF} = 0A$, $V_{REF} = 1.21V$ and $2.4V$
	V_{REF}	1.185	1.21	1.234	V	$I_{REF} = 0A$
		2.352	2.4	2.448	V	
Reference Output Current	I_{REF}	—	± 500	—	μA	$V_{TOL} = \pm 2\%$ (maximum)
Drift with Temperature (characterized but not production tested)	$\Delta V_{REF}/\Delta T$	—	27	100	ppm	$V_{REF} = 1.21V$, $V_{DD} = 1.8V$
		—	22	100	ppm	$V_{REF} = 1.21V$, $V_{DD} = 5.5V$
		—	23	100	ppm	$V_{REF} = 2.4V$, $V_{DD} = 5.5V$
Capacitive Load	C_L	—	200	—	pF	Note 4

Note 1: The input offset voltage is the center (average) of the input-referred trip points. The input hysteresis is the difference between the input-referred trip points.

2: Limit the output current to Absolute Maximum Rating of 30 mA.

3: Do not short the output of the **MCP65R46** comparators above $V_{SS} + 10V$.

4: The low-power reference voltage pin is designed to drive small capacitive loads. See [Section 4.5.2](#).

AC CHARACTERISTICS

Unless otherwise indicated, all limits are specified for: $V_{DD} = +1.8V$ to $+5.5V$, $V_{SS} = GND$, $T_A = +25^\circ C$, $V_{IN+} = V_{DD}/2$, Step = 200 mV, Overdrive = 100 mV, $R_L = 100\text{ k}\Omega$ to $V_{DD}/2$ (**MCP65R41** only), $R_{Pull-Up} = 2.74\text{ k}\Omega$ to V_{DD} (**MCP65R46** only), and $C_L = 50\text{ pF}$.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Rise Time	t_R	—	0.85	—	μs	
Fall Time	t_F	—	0.85	—	μs	
Propagation Delay (High-to-Low)	t_{PHL}	—	4	8.0	μs	
Propagation Delay (Low-to-High)	t_{PLH}	—	4	8.0	μs	
Propagation Delay Skew	t_{PDS}	—	± 0.2	—	μs	Note 1
Maximum Toggle Frequency	f_{MAX}	—	160	—	kHz	$V_{DD} = 1.8V$
	f_{MAX}	—	120	—	kHz	$V_{DD} = 5.5V$
Input Noise Voltage	E_N	—	200	—	μV_{P-P}	10 Hz to 100 kHz

Note 1: Propagation Delay Skew is defined as: $t_{PDS} = t_{PLH} - t_{PHL}$.

TEMPERATURE SPECIFICATIONS

Unless otherwise indicated, all limits are specified for: $V_{DD} = +1.8V$ to $+5.5V$ and $V_{SS} = GND$.

Parameters	Symbol	Min	Typ	Max	Units	Conditions
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+125	$^\circ C$	
Operating Temperature Range	T_A	-40	—	+125	$^\circ C$	
Storage Temperature Range	T_A	-65	—	+150	$^\circ C$	
Thermal Package Resistances						
Thermal Resistance, SOT23-6	θ_{JA}	—	190.5	—	$^\circ C/W$	

1.2 Test Circuit Configuration

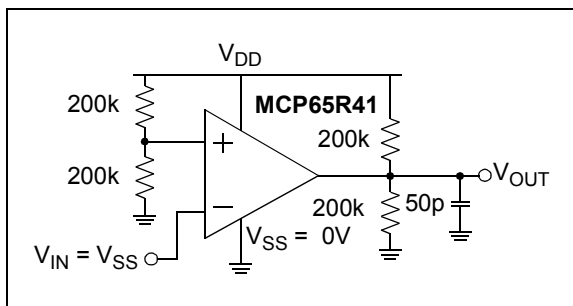


FIGURE 1-1: Test Circuit for the Push-Pull Output Comparators.

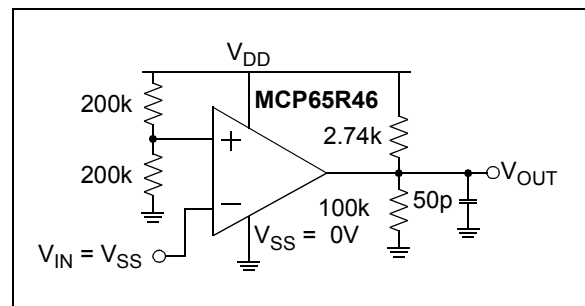


FIGURE 1-2: Test Circuit for the Open-Drain Comparators.

MCP65R41/6

NOTES:

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, $V_{DD} = +1.8V$ to $+5.5V$, $V_{SS} = GND$, $T_A = +25^\circ C$, $V_{IN+} = V_{DD}/2$, $V_{IN-} = GND$, $R_L = 100\text{ k}\Omega$ to $V_{DD}/2$ (**MCP65R41** only), $R_{Pull-Up} = 2.74\text{ k}\Omega$ to $V_{DD}/2$ (**MCP65R46** only) and $C_L = 50\text{ pF}$.

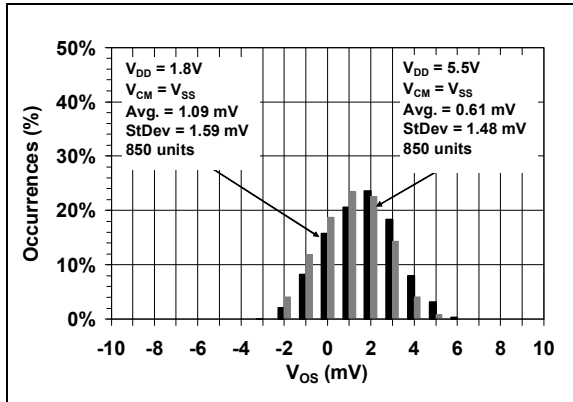


FIGURE 2-1: Input Offset Voltage.

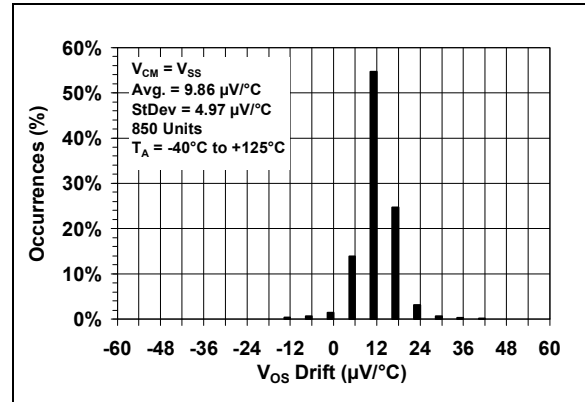


FIGURE 2-4: Input Offset Voltage Drift.

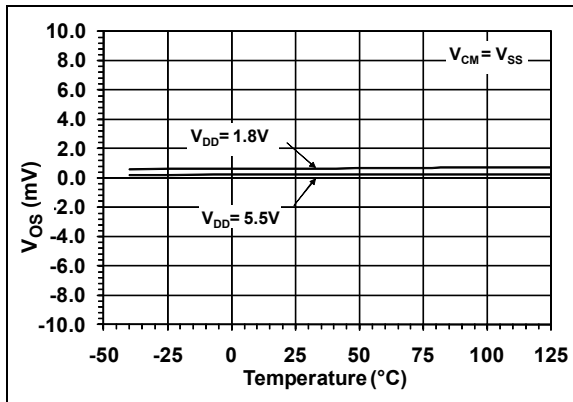


FIGURE 2-2: Input Offset Voltage vs. Temperature.

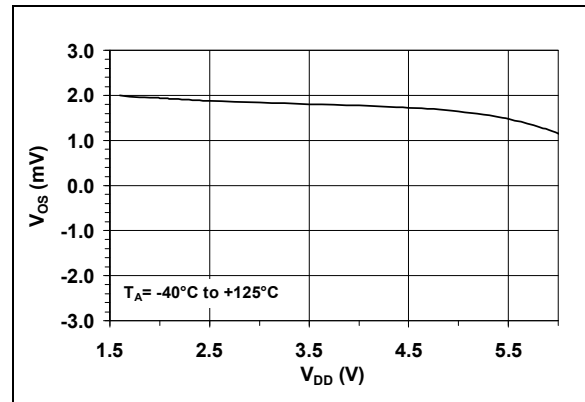


FIGURE 2-5: Input Offset Voltage vs. Supply Voltage vs. Temperature.

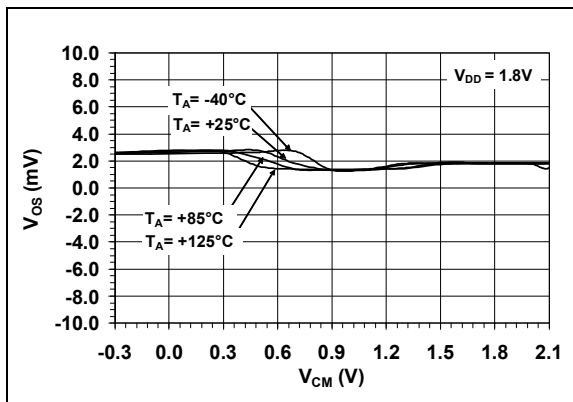


FIGURE 2-3: Input Offset Voltage vs. Common-Mode Input Voltage.

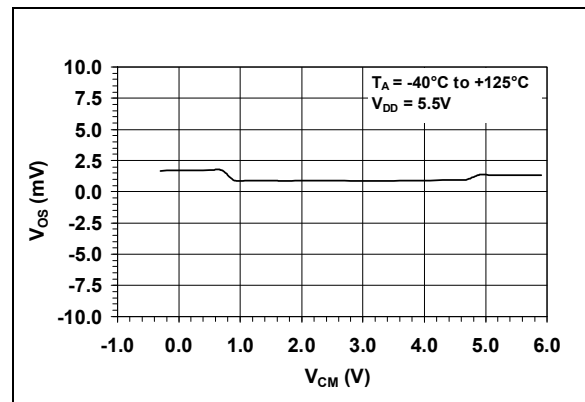


FIGURE 2-6: Input Offset Voltage vs. Common-Mode Input Voltage.

MCP65R41/6

Note: Unless otherwise indicated, $V_{DD} = +1.8V$ to $+5.5V$, $V_{SS} = GND$, $T_A = +25^\circ C$, $V_{IN+} = V_{DD}/2$, $V_{IN-} = GND$, $R_L = 100\text{ k}\Omega$ to $V_{DD}/2$ (**MCP65R41** only), $R_{Pull-Up} = 2.74\text{ k}\Omega$ to $V_{DD}/2$ (**MCP65R46** only) and $C_L = 50\text{ pF}$.

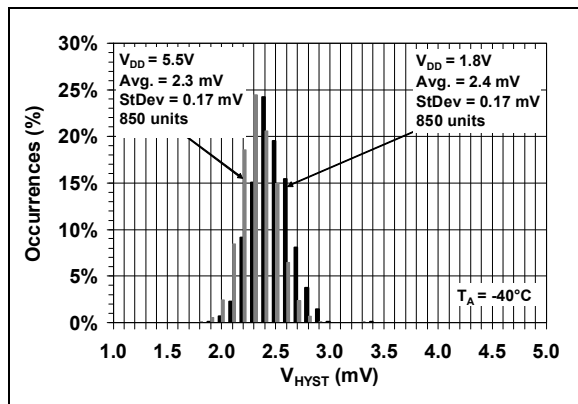


FIGURE 2-7: Input Hysteresis Voltage at $-40^\circ C$.

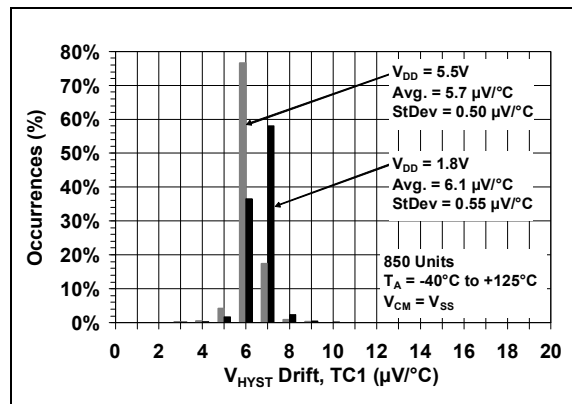


FIGURE 2-10: Input Hysteresis Voltage Drift – Linear Temperature Compensation (TC1).

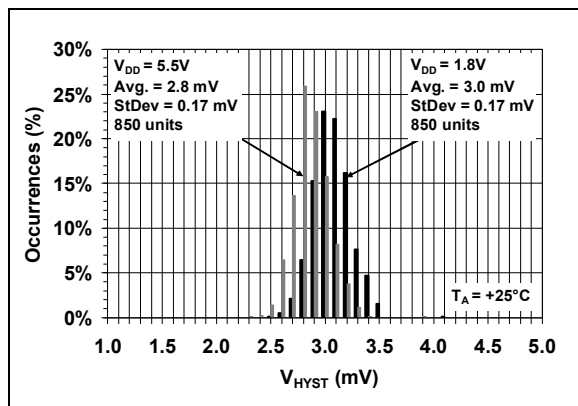


FIGURE 2-8: Input Hysteresis Voltage at $+25^\circ C$.

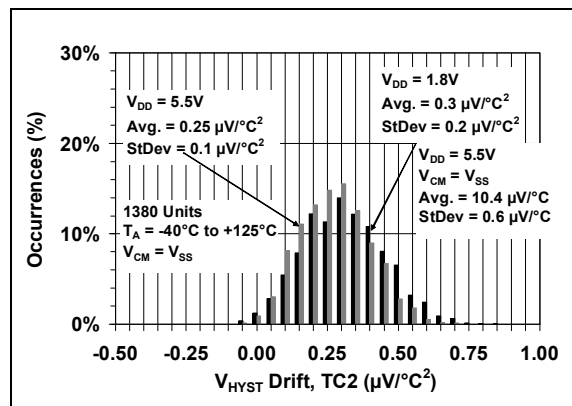


FIGURE 2-11: Input Hysteresis Voltage Drift – Quadratic Temperature Compensation (TC2).

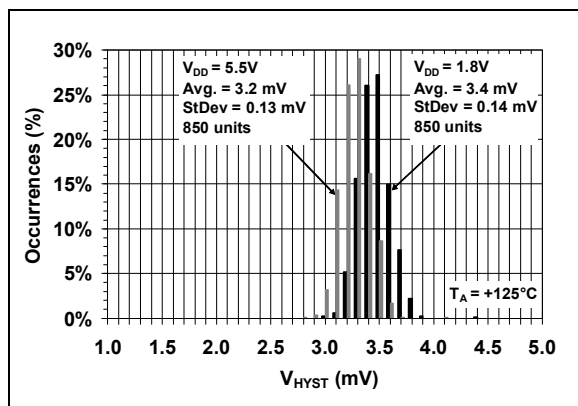


FIGURE 2-9: Input Hysteresis Voltage at $+125^\circ C$.

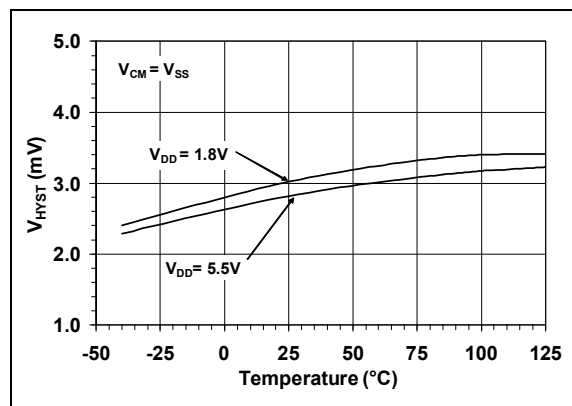


FIGURE 2-12: Input Hysteresis Voltage vs. Temperature.

Note: Unless otherwise indicated, $V_{DD} = +1.8V$ to $+5.5V$, $V_{SS} = GND$, $T_A = +25^\circ C$, $V_{IN+} = V_{DD}/2$, $V_{IN-} = GND$, $R_L = 100\text{ k}\Omega$ to $V_{DD}/2$ (**MCP65R41** only), $R_{Pull-Up} = 2.74\text{ k}\Omega$ to $V_{DD}/2$ (**MCP65R46** only) and $C_L = 50\text{ pF}$.

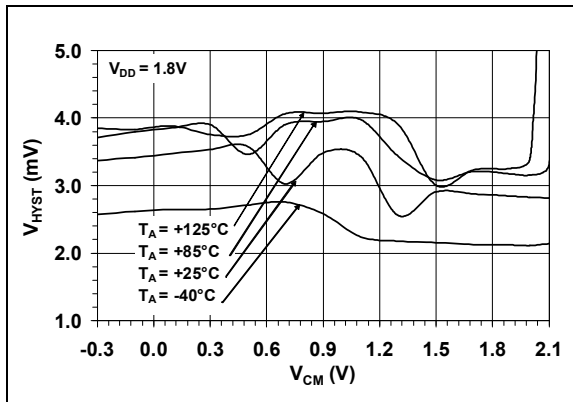


FIGURE 2-13: Input Hysteresis Voltage vs. Common-Mode Input Voltage.

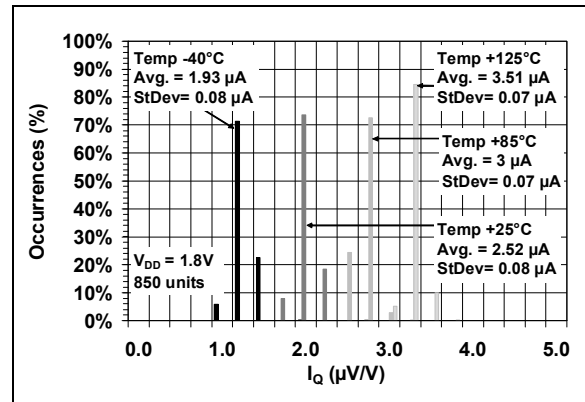


FIGURE 2-16: Quiescent Current.

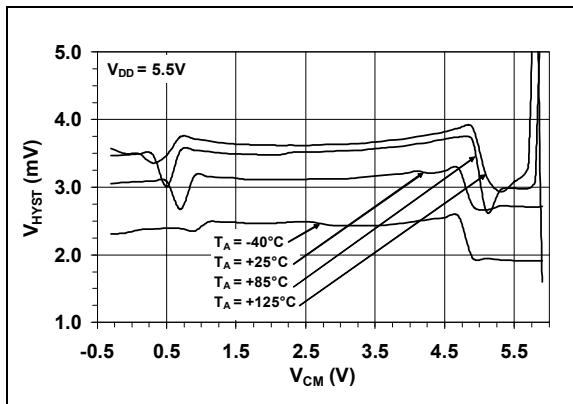


FIGURE 2-14: Input Hysteresis Voltage vs. Common-Mode Input Voltage.

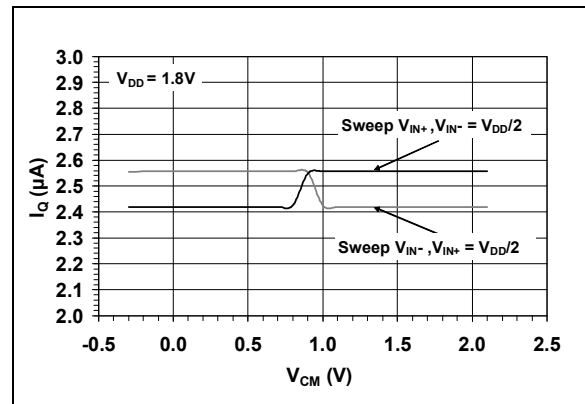


FIGURE 2-17: Quiescent Current vs. Common-Mode Input Voltage.

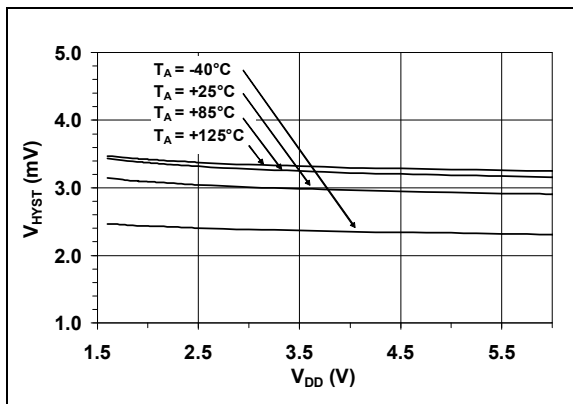


FIGURE 2-15: Input Hysteresis Voltage vs. Supply Voltage vs. Temperature.

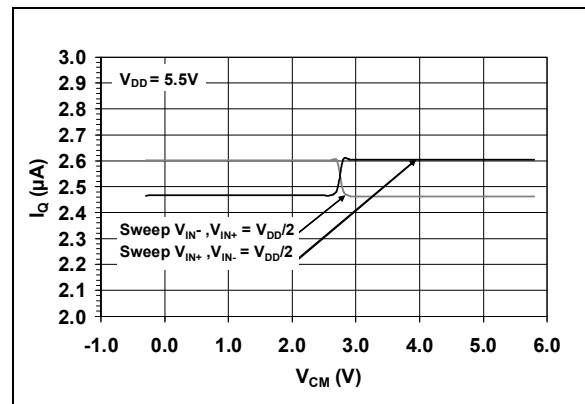


FIGURE 2-18: Quiescent Current vs. Common-Mode Input Voltage.

MCP65R41/6

Note: Unless otherwise indicated, $V_{DD} = +1.8V$ to $+5.5V$, $V_{SS} = GND$, $T_A = +25^\circ C$, $V_{IN+} = V_{DD}/2$, $V_{IN-} = GND$, $R_L = 100\text{ k}\Omega$ to $V_{DD}/2$ (**MCP65R41** only), $R_{Pull-Up} = 2.74\text{ k}\Omega$ to $V_{DD}/2$ (**MCP65R46** only) and $C_L = 50\text{ pF}$.

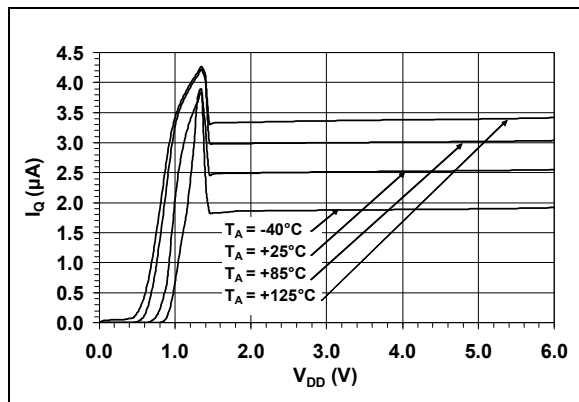


FIGURE 2-19: Quiescent Current vs. Supply Voltage vs. Temperature.

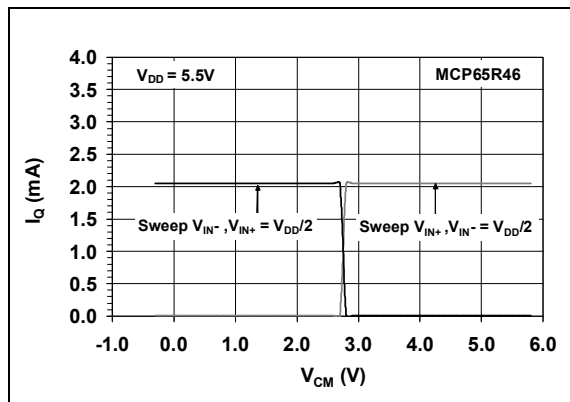


FIGURE 2-22: Quiescent Current vs. Common-Mode Input Voltage.

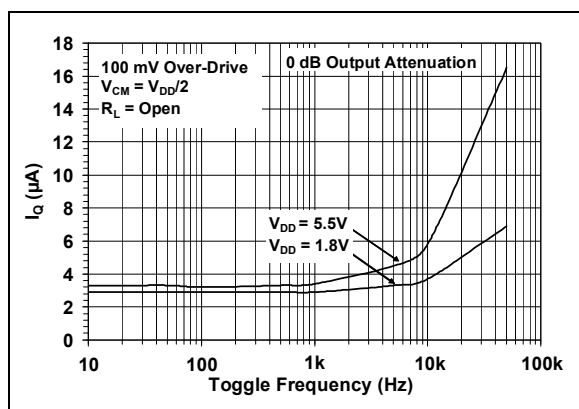


FIGURE 2-20: Quiescent Current vs. Toggle Frequency.

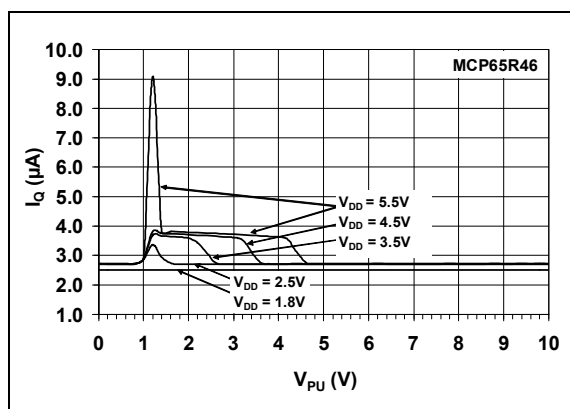


FIGURE 2-23: Quiescent Current vs. Pull-Up Voltage.

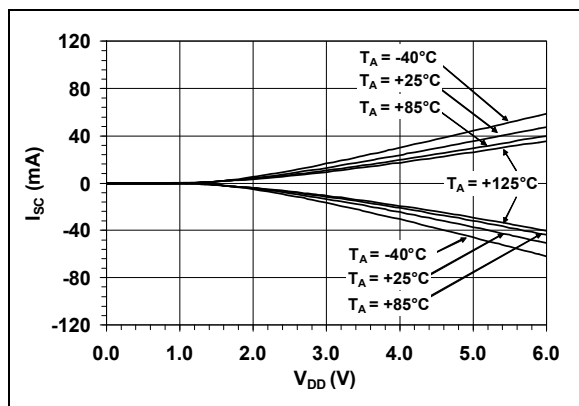


FIGURE 2-21: Short Circuit Current vs. Supply Voltage vs. Temperature.

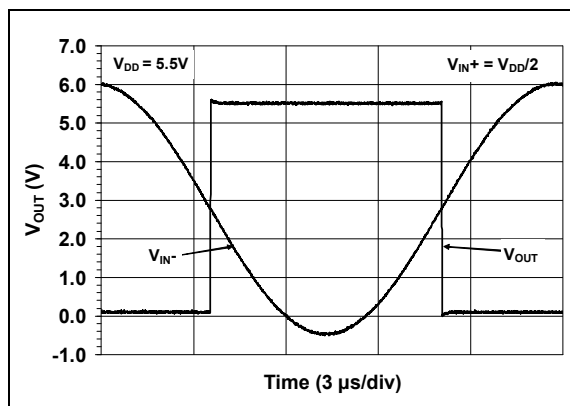


FIGURE 2-24: No Phase Reversal.

Note: Unless otherwise indicated, $V_{DD} = +1.8V$ to $+5.5V$, $V_{SS} = GND$, $T_A = +25^\circ C$, $V_{IN+} = V_{DD}/2$, $V_{IN-} = GND$, $R_L = 100\text{ k}\Omega$ to $V_{DD}/2$ (**MCP65R41** only), $R_{Pull-Up} = 2.74\text{ k}\Omega$ to $V_{DD}/2$ (**MCP65R46** only) and $C_L = 50\text{ pF}$.

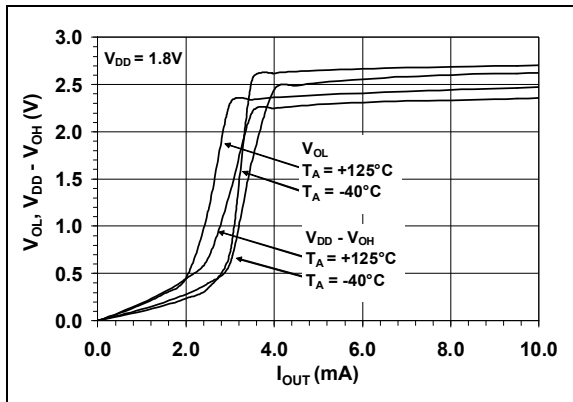


FIGURE 2-25: Output Headroom vs. Output Current.

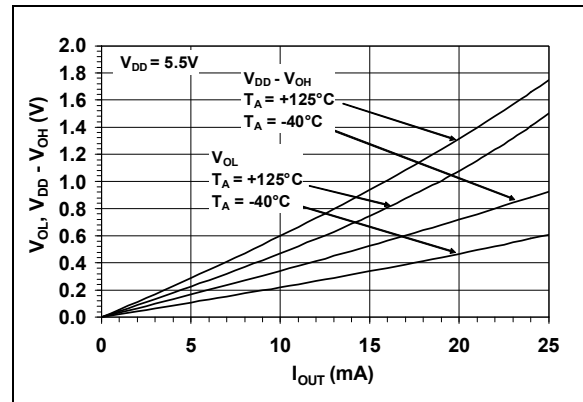


FIGURE 2-28: Output Headroom vs. Output Current.

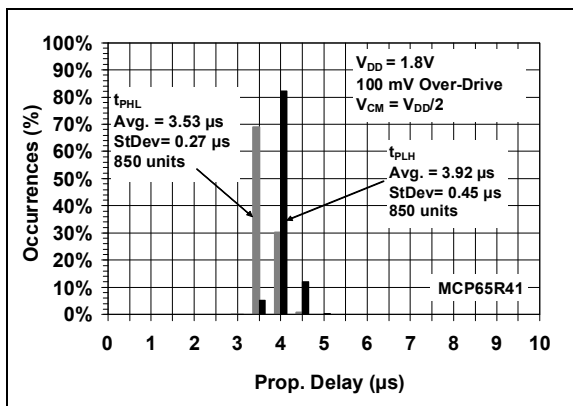


FIGURE 2-26: Low-to-High and High-to-Low Propagation Delays.

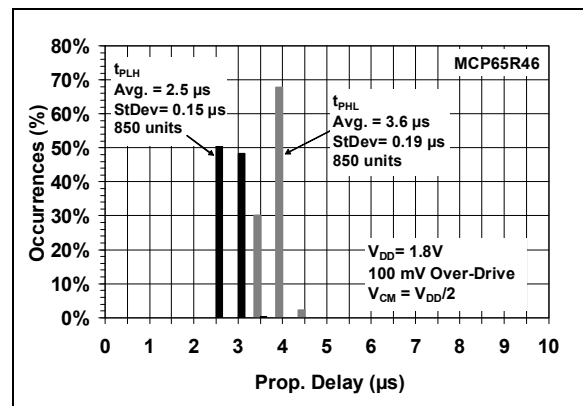


FIGURE 2-29: Low-to-High and High-to-Low Propagation Delays.

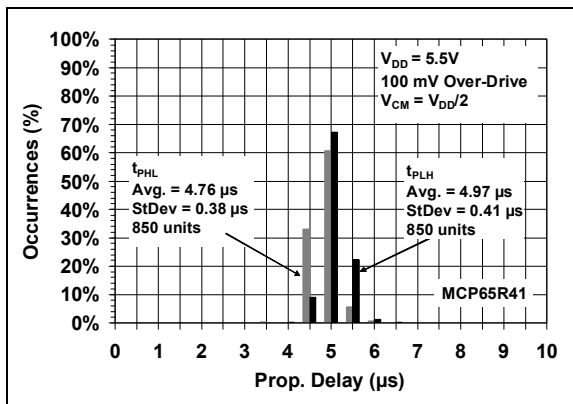


FIGURE 2-27: Low-to-High and High-to-Low Propagation Delays.

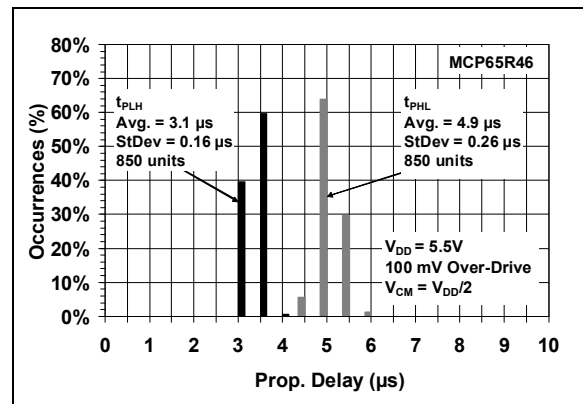


FIGURE 2-30: Low-to-High and High-to-Low Propagation Delays.

MCP65R41/6

Note: Unless otherwise indicated, $V_{DD} = +1.8V$ to $+5.5V$, $V_{SS} = GND$, $T_A = +25^\circ C$, $V_{IN+} = V_{DD}/2$, $V_{IN-} = GND$, $R_L = 100\text{ k}\Omega$ to $V_{DD}/2$ (**MCP65R41** only), $R_{Pull-Up} = 2.74\text{ k}\Omega$ to $V_{DD}/2$ (**MCP65R46** only) and $C_L = 50\text{ pF}$.

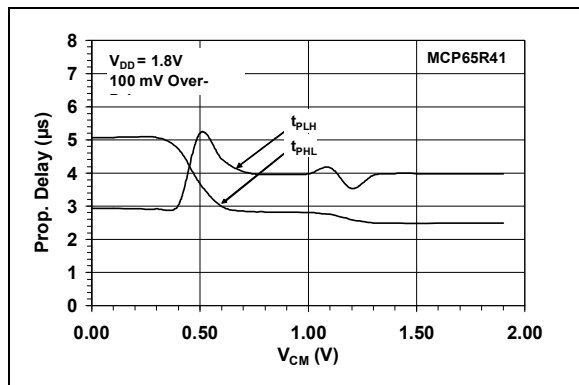


FIGURE 2-31: Propagation Delay vs. Common-Mode Input Voltage.

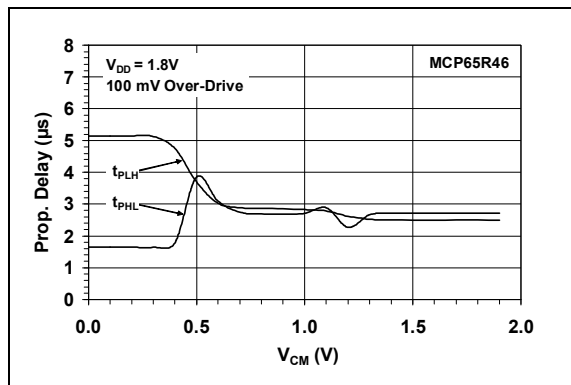


FIGURE 2-34: Propagation Delay vs. Common-Mode Input Voltage.

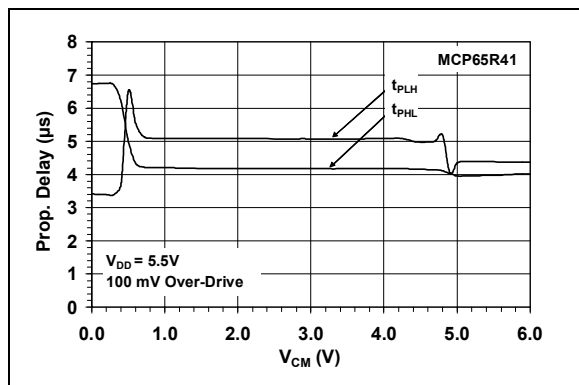


FIGURE 2-32: Propagation Delay vs. Common-Mode Input Voltage.

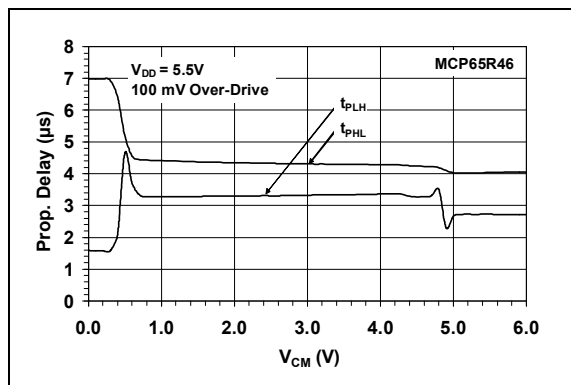


FIGURE 2-35: Propagation Delay vs. Common-Mode Input Voltage.

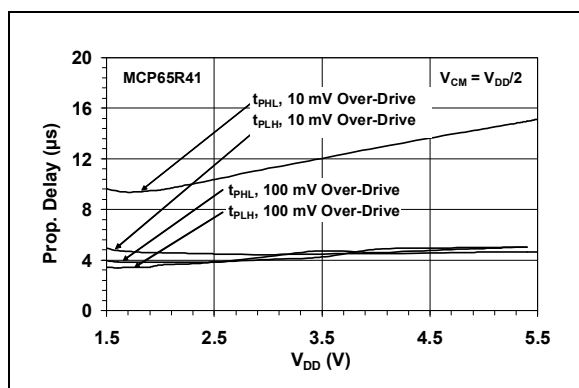


FIGURE 2-33: Propagation Delay vs. Supply Voltage.

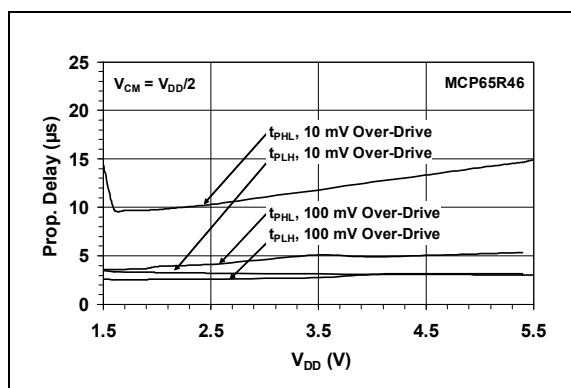


FIGURE 2-36: Propagation Delay vs. Supply Voltage.

Note: Unless otherwise indicated, $V_{DD} = +1.8V$ to $+5.5V$, $V_{SS} = GND$, $T_A = +25^\circ C$, $V_{IN+} = V_{DD}/2$, $V_{IN-} = GND$, $R_L = 100\text{ k}\Omega$ to $V_{DD}/2$ (**MCP65R41** only), $R_{Pull-Up} = 2.74\text{ k}\Omega$ to $V_{DD}/2$ (**MCP65R46** only) and $C_L = 50\text{ pF}$.

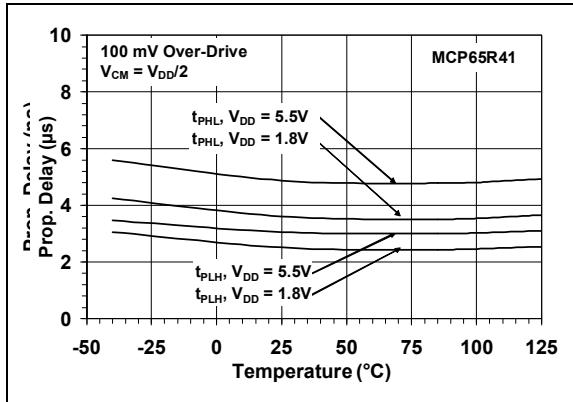


FIGURE 2-37: Propagation Delay vs. Temperature.

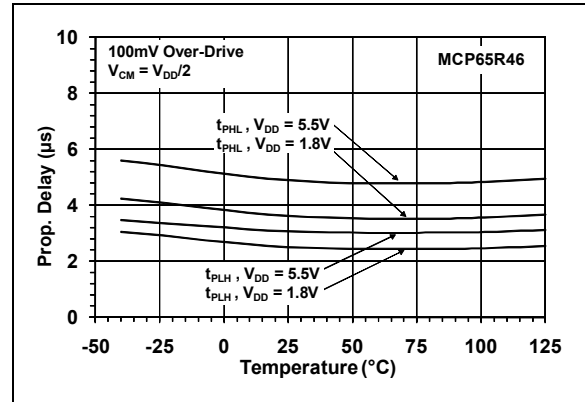


FIGURE 2-40: Propagation Delay vs. Temperature.

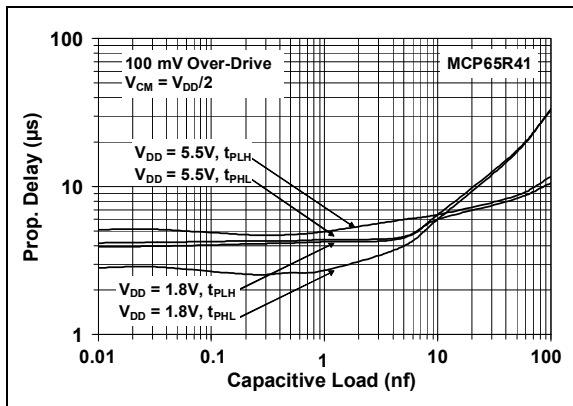


FIGURE 2-38: Propagation Delay vs. Capacitive Load.

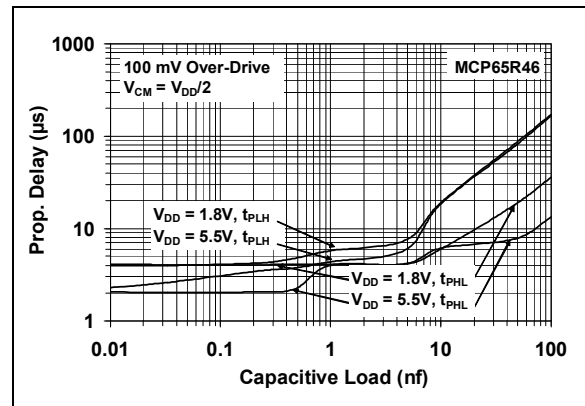


FIGURE 2-41: Propagation Delay vs. Capacitive Load.

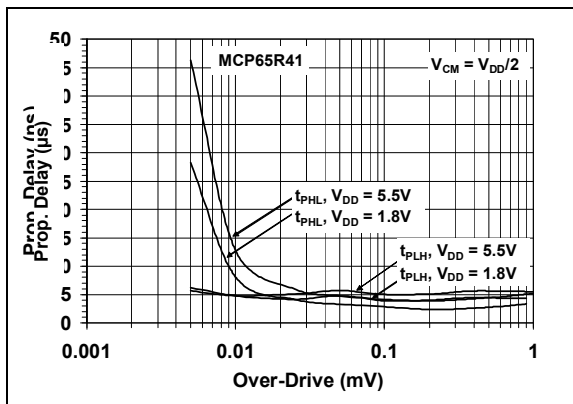


FIGURE 2-39: Propagation Delay vs. Input Over-Drive.

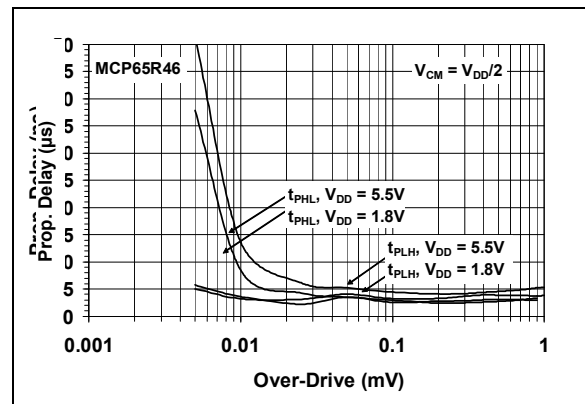


FIGURE 2-42: Propagation Delay vs. Input Over-Drive.

MCP65R41/6

Note: Unless otherwise indicated, $V_{DD} = +1.8V$ to $+5.5V$, $V_{SS} = GND$, $T_A = +25^\circ C$, $V_{IN+} = V_{DD}/2$, $V_{IN-} = GND$, $R_L = 100\text{ k}\Omega$ to $V_{DD}/2$ (**MCP65R41** only), $R_{Pull-Up} = 2.74\text{ k}\Omega$ to $V_{DD}/2$ (**MCP65R46** only) and $C_L = 50\text{ pF}$.

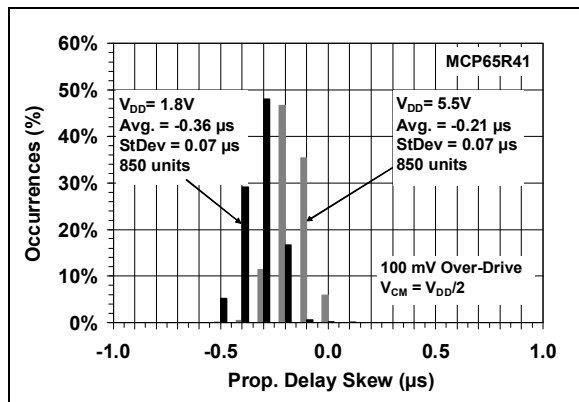


FIGURE 2-43: Propagation Delay Skew.

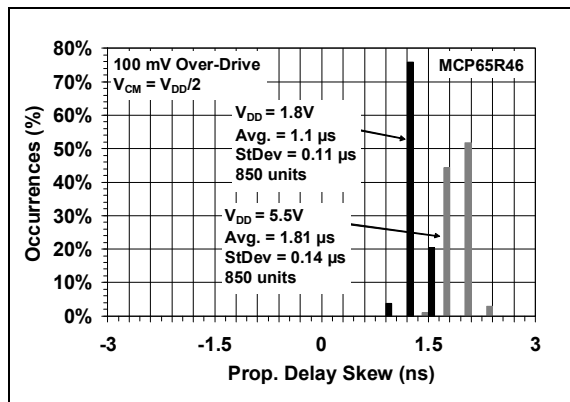


FIGURE 2-46: Propagation Delay Skew.

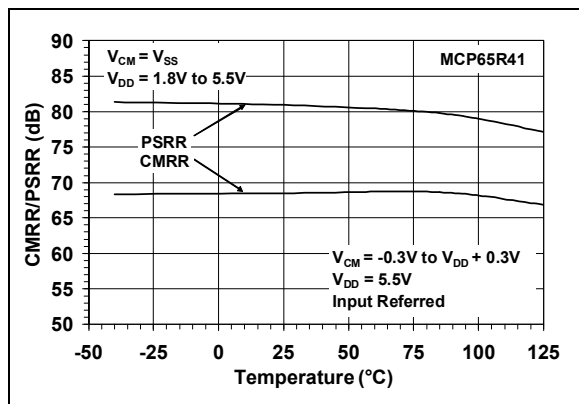


FIGURE 2-44: Common-Mode Rejection Ratio and Power Supply Rejection Ratio vs. Temperature.

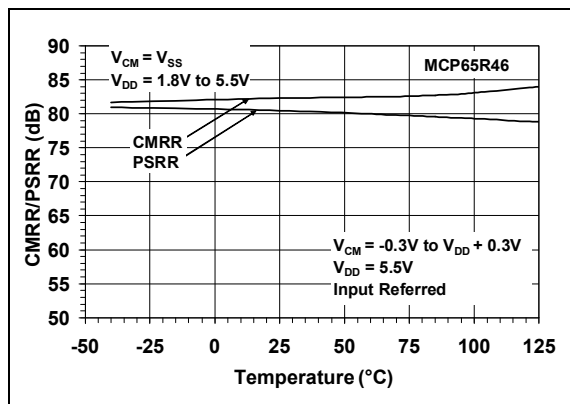


FIGURE 2-47: Common-Mode Rejection Ratio and Power Supply Rejection Ratio vs. Temperature.

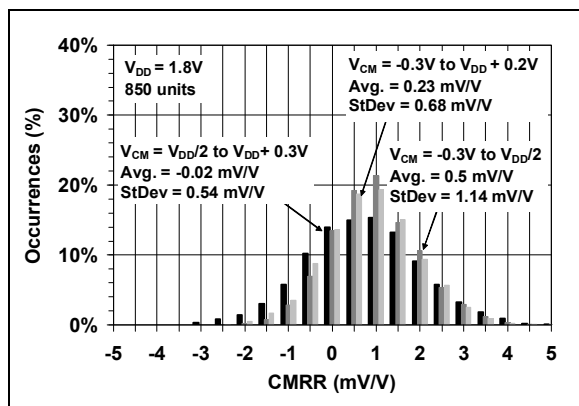


FIGURE 2-45: Common-Mode Rejection Ratio.

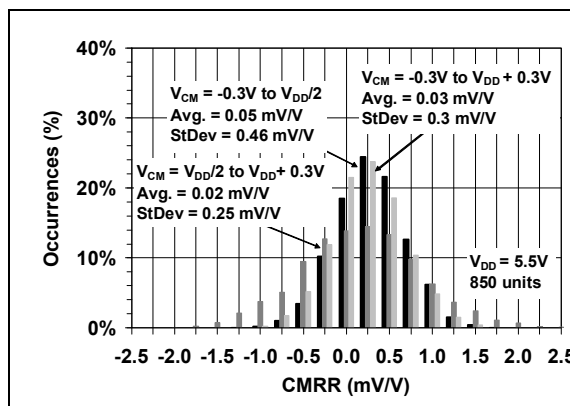


FIGURE 2-48: Common-Mode Rejection Ratio.

Note: Unless otherwise indicated, $V_{DD} = +1.8V$ to $+5.5V$, $V_{SS} = GND$, $T_A = +25^\circ C$, $V_{IN+} = V_{DD}/2$, $V_{IN-} = GND$, $R_L = 100\text{ k}\Omega$ to $V_{DD}/2$ (**MCP65R41** only), $R_{Pull-Up} = 2.74\text{ k}\Omega$ to $V_{DD}/2$ (**MCP65R46** only) and $C_L = 50\text{ pF}$.

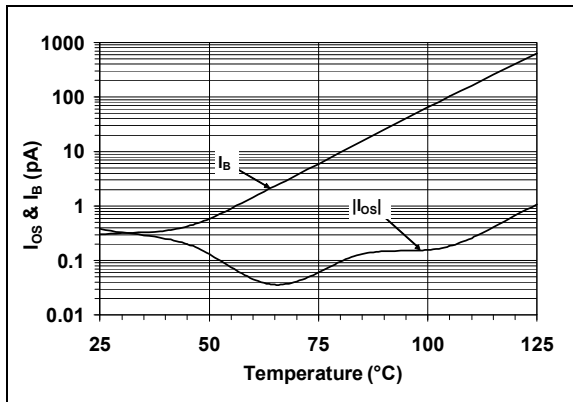


FIGURE 2-49: Input Offset Current and Input Bias Current vs. Temperature.

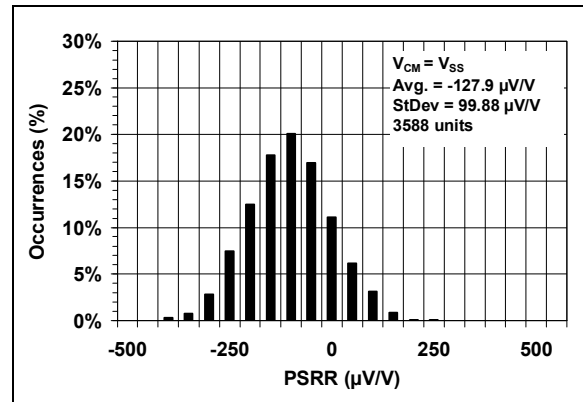


FIGURE 2-52: Power Supply Rejection Ratio.

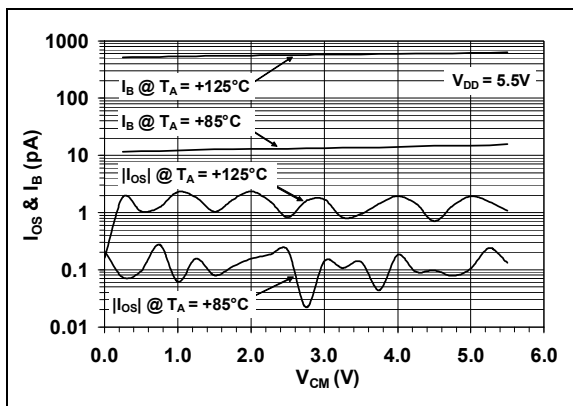


FIGURE 2-50: Input Offset Current and Input Bias Current vs. Common-Mode Input Voltage vs. Temperature.

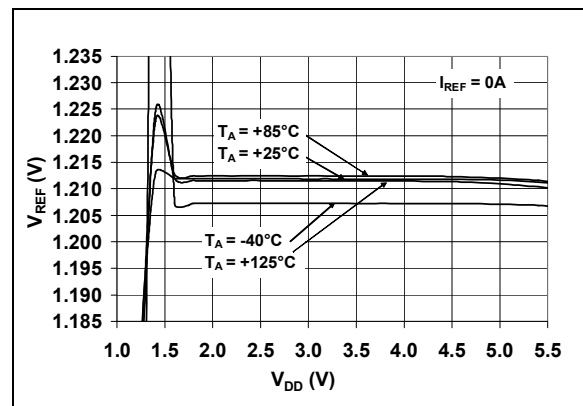


FIGURE 2-53: V_{REF} vs. V_{DD} .

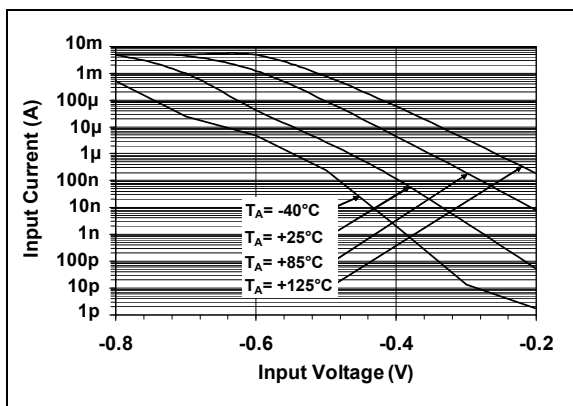


FIGURE 2-51: Input Bias Current vs. Input Voltage vs. Temperature.

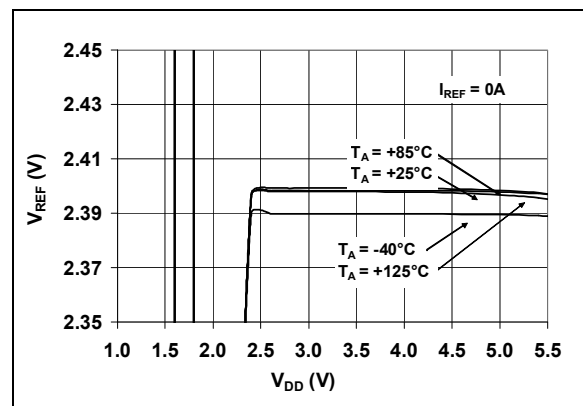


FIGURE 2-54: V_{REF} vs. V_{DD} .

MCP65R41/6

Note: Unless otherwise indicated, $V_{DD} = +1.8V$ to $+5.5V$, $V_{SS} = GND$, $T_A = +25^\circ C$, $V_{IN+} = V_{DD}/2$, $V_{IN-} = GND$, $R_L = 100\text{ k}\Omega$ to $V_{DD}/2$ (**MCP65R41** only), $R_{Pull-Up} = 2.74\text{ k}\Omega$ to $V_{DD}/2$ (**MCP65R46** only) and $C_L = 50\text{ pF}$.

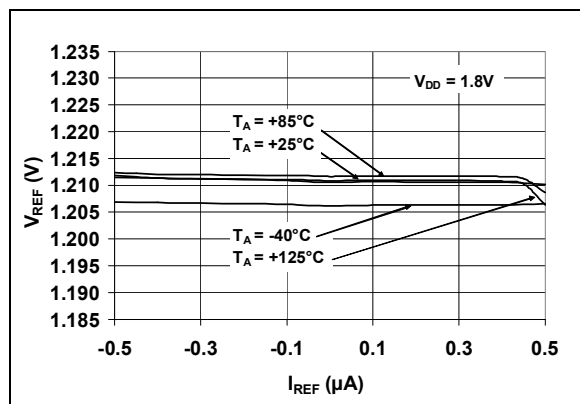


FIGURE 2-55: V_{REF} vs. I_{REF} over Temperature.

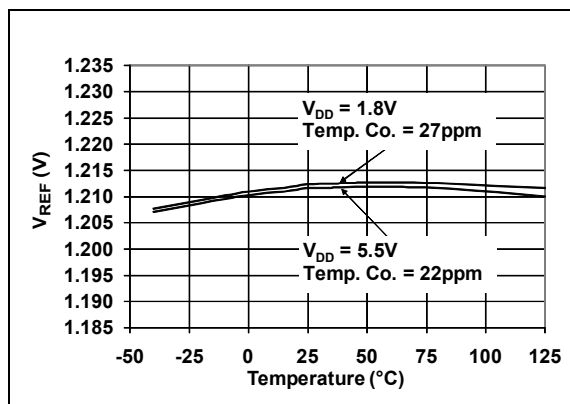


FIGURE 2-58: V_{REF} vs. Temperature.

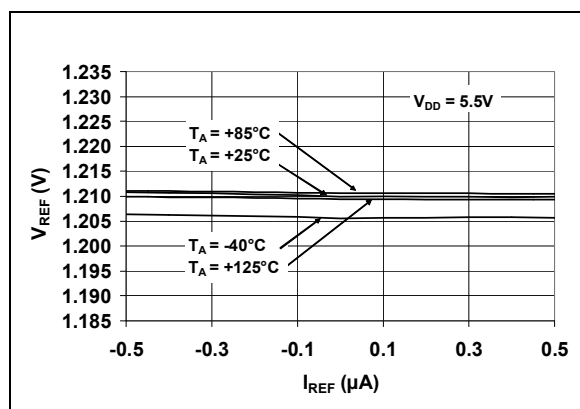


FIGURE 2-56: V_{REF} vs. I_{REF} over Temperature.

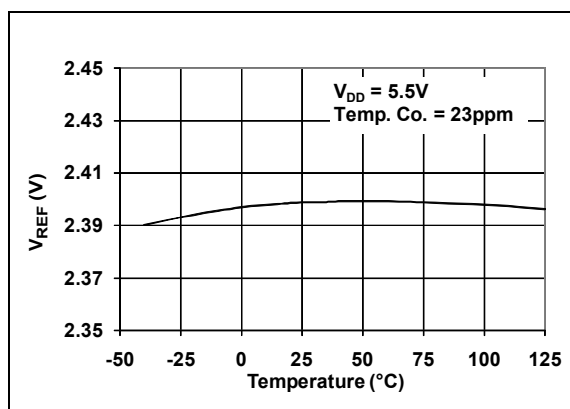


FIGURE 2-59: V_{REF} vs. Temperature.

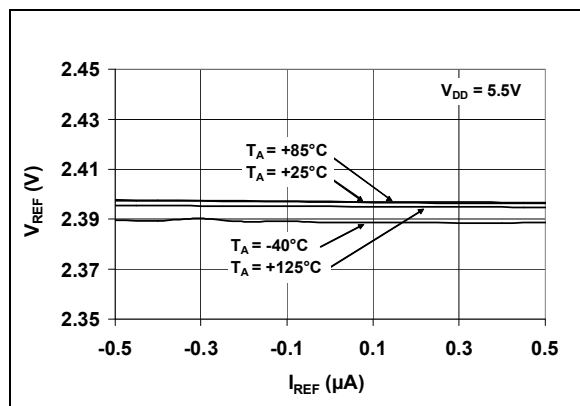


FIGURE 2-57: V_{REF} vs. I_{REF} over Temperature.

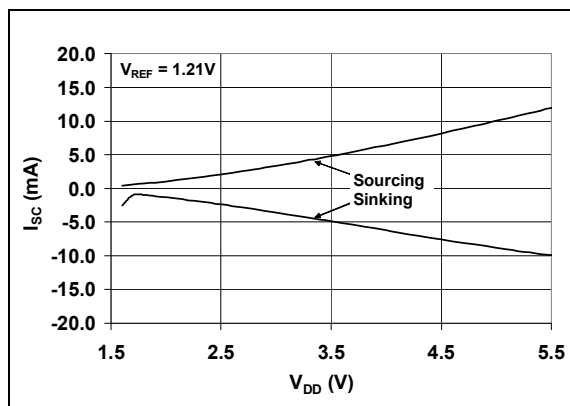


FIGURE 2-60: Short Circuit Current vs. V_{DD} .

Note: Unless otherwise indicated, $V_{DD} = +1.8V$ to $+5.5V$, $V_{SS} = GND$, $T_A = +25^\circ C$, $V_{IN+} = V_{DD}/2$, $V_{IN-} = GND$, $R_L = 100\text{ k}\Omega$ to $V_{DD}/2$ (**MCP65R41** only), $R_{Pull-Up} = 2.74\text{ k}\Omega$ to $V_{DD}/2$ (**MCP65R46** only) and $C_L = 50\text{ pF}$.

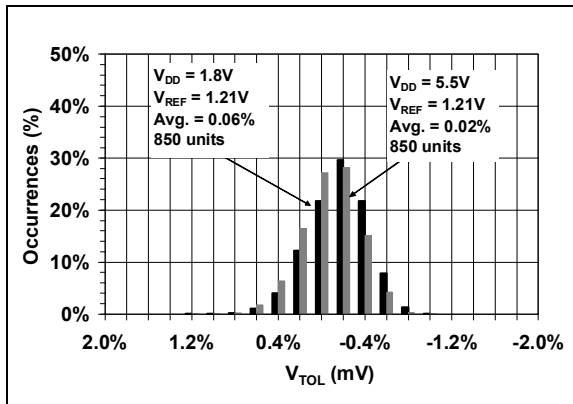


FIGURE 2-61: Reference Voltage Tolerance.

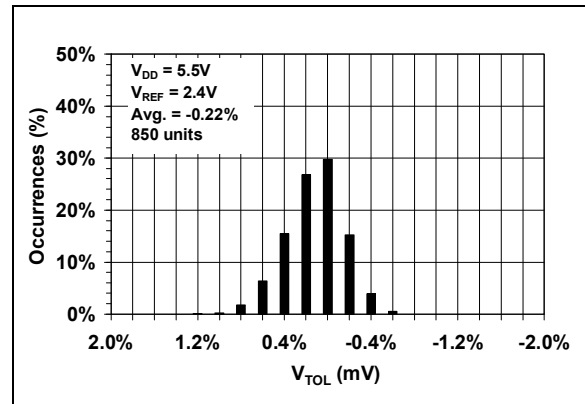


FIGURE 2-62: Reference Voltage Tolerance.

MCP65R41/6

NOTES:

3.0 PIN DESCRIPTIONS

Descriptions of the pins are listed in [Table 3-1](#).

TABLE 3-1: PIN FUNCTION TABLE

MCP65R41/6	Symbol	Description
SOT23-6		
1	OUT	Digital Output
2	V_{SS}	Ground
3	V_{IN+}	Non-inverting Input
4	V_{IN-}	Inverting Input
5	V_{REF}	Reference Voltage Output
6	V_{DD}	Positive Power Supply

3.1 Analog Inputs

The comparator non-inverting and inverting inputs are high-impedance CMOS inputs with low bias currents.

3.2 Digital Outputs

The comparator outputs are CMOS/TTL compatible push-pull and open-drain digital outputs. The push-pull is designed to directly interface to a CMOS/TTL compatible pin while the open-drain output is designed for level shifting and wired-OR interfaces.

3.3 Analog Outputs

The V_{REF} Output pin outputs a reference voltage of 1.21V or 2.4V.

3.4 Power Supply (V_{SS} and V_{DD})

The positive power supply pin (V_{DD}) is 1.8V to 5.5V higher than the negative power supply pin (V_{SS}). For normal operation, the other pins are at voltages between V_{SS} and V_{DD} .

Typically, these parts are used in a single (positive) supply configuration. In this case, V_{SS} is connected to ground and V_{DD} is connected to the supply. V_{DD} will need a local bypass capacitor (typically 0.01 μ F to 0.1 μ F) within 2 mm of the V_{DD} pin. These can share a bulk capacitor with the nearby analog parts (within 100 mm), but it is not required.

MCP65R41/6

NOTES:

4.0 APPLICATIONS INFORMATION

The MCP65R41/6 family of push-pull and open-drain output comparators are fabricated on Microchip's state-of-the-art CMOS process. They are suitable for a wide range of high-speed applications requiring low power consumption.

4.1 Comparator Inputs

4.1.1 NORMAL OPERATION

The input stage of this family of devices uses three differential input stages in parallel: one operates at low input voltages, one at high input voltages, and one at mid input voltages. With this topology, the input voltage range is 0.3V above V_{DD} and 0.3V below V_{SS} , while providing low offset voltage throughout the Common mode range. The input offset voltage is measured at both $V_{SS} - 0.3V$ and $V_{DD} + 0.3V$ to ensure proper operation.

The MCP65R41/6 family has internally-set hysteresis V_{HYST} that is small enough to maintain input offset accuracy, and large enough to eliminate the output chattering caused by the comparator's own input noise voltage E_{NI} . Figure 4-1 depicts this behavior. Input offset voltage (V_{OS}) is the center (average) of the (input-referred) low-high and high-low trip points. Input hysteresis voltage (V_{HYST}) is the difference between the same trip points.

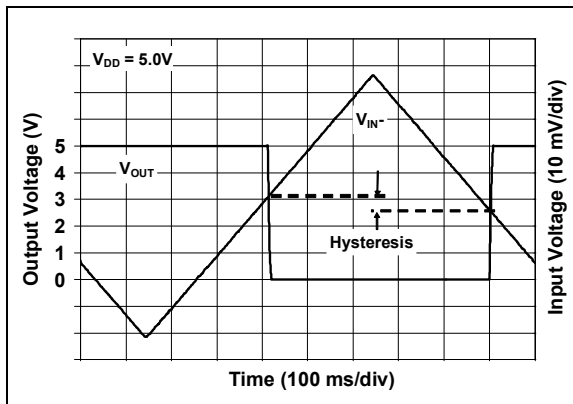


FIGURE 4-1: The MCP65R41/6 Comparators' Internal Hysteresis Eliminates Output Chatter Caused by Input Noise Voltage.

4.1.2 INPUT VOLTAGE AND CURRENT LIMITS

The ESD protection on the inputs can be depicted as shown in Figure 4-2. This structure was chosen to protect the input transistors, and to minimize the input bias current (I_B). The input ESD diodes clamp the inputs when trying to go more than one diode drop below V_{SS} . They also clamp any voltages that go too far above V_{DD} ; their breakdown voltage is high enough to allow a normal operation, and low enough to bypass the ESD events within the specified limits.

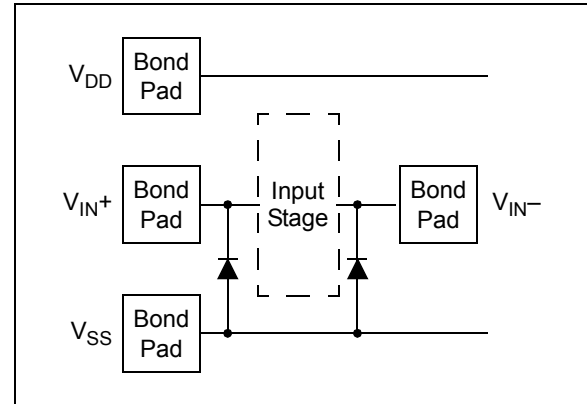


FIGURE 4-2: Simplified Analog Input ESD Structures.

In order to prevent damage and/or improper operation of these comparators, the circuit they are connected to limit the currents (and voltages) at the V_{IN+} and V_{IN-} pins (see **Absolute Maximum Ratings†**). Figure 4-3 shows the recommended approach to protect these inputs. The internal ESD diodes prevent the input pins (V_{IN+} and V_{IN-}) from going too far below ground, and the resistors R_1 and R_2 limit the possible current drawn out of the input pin. Diodes D_1 and D_2 prevent the input pin (V_{IN+} and V_{IN-}) from going too far above V_{DD} . When implemented as shown, resistors R_1 and R_2 also limit the current through D_1 and D_2 .

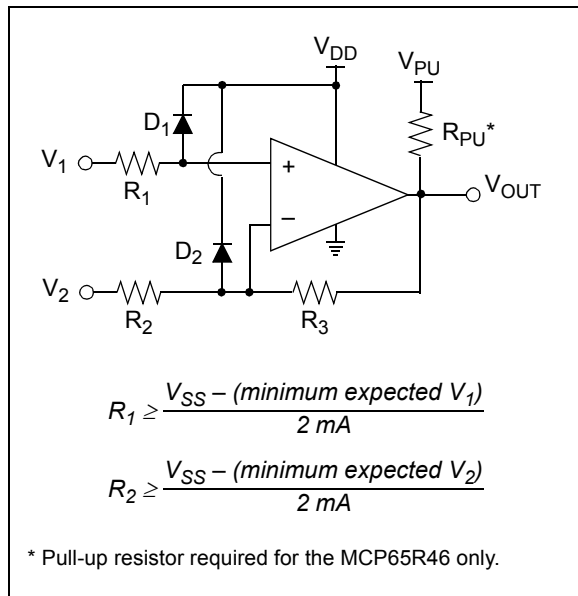


FIGURE 4-3: Protecting the Analog Inputs.

It is also possible to connect the diodes to the left of the resistors R_1 and R_2 . In this case, the currents through the diodes D_1 and D_2 need to be limited by some other mechanism. The resistor then serves as an in-rush current limiter; the DC current into the input pins (V_{IN+} and V_{IN-}) should be very small.

A significant amount of current can flow out of the inputs when the Common mode voltage (V_{CM}) is below ground (V_{SS}); see Figure 4-3. The applications that are high impedance may need to limit the usable voltage range.

4.1.3 PHASE REVERSAL

The MCP65R41/6 comparator family uses CMOS transistors at the input. They are designed to prevent phase inversion when the input pins exceed the supply voltages. Figure 2-3 shows an input voltage exceeding both supplies with no resulting phase inversion.

4.2 Push-Pull Output

The push-pull output is designed to be compatible with CMOS and TTL logic, while the output transistors are configured to give a rail-to-rail output performance. They are driven with circuitry that minimizes any switching current (shoot-through current from supply to supply) when the output is transitioned from high-to-low, or from low-to-high (see Figures 2-18 and 2-19 for more information).

4.3 Externally Set Hysteresis

A greater flexibility in selecting the hysteresis (or the input trip points) is achieved by using external resistors. Hysteresis reduces output chattering when one input is slowly moving past the other. It also helps in systems where it is preferable not to cycle between high and low states too frequently (e.g., air conditioner thermostatic controls). Output chatter also increases the dynamic supply current.

4.3.1 NON-INVERTING CIRCUIT

Figure 4-4 shows a non-inverting circuit for single-supply applications using just two resistors. The resulting hysteresis diagram is shown in Figure 4-5.

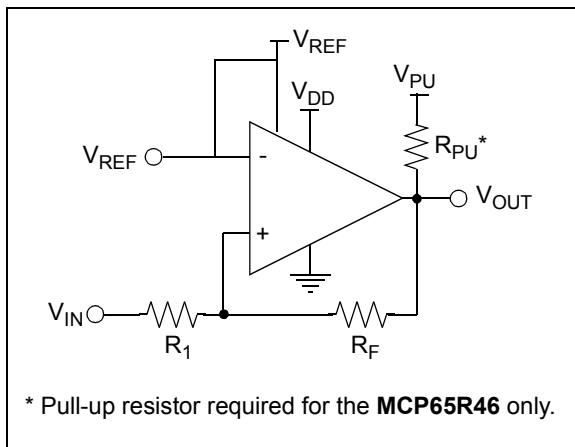


FIGURE 4-4: Non-Inverting Circuit with Hysteresis for Single-Supply.

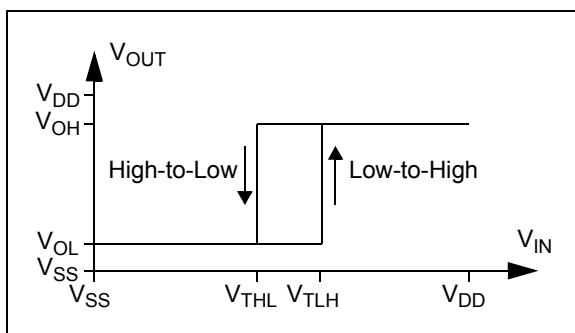


FIGURE 4-5: Hysteresis Diagram for the Non-Inverting Circuit.

The trip points for Figures 4-4 and 4-5 are:

EXAMPLE 4-1:

$$V_{TLH} = V_{REF} \left(1 + \frac{R_1}{R_F} \right) - V_{OL} \left(\frac{R_1}{R_F} \right)$$

$$V_{THL} = V_{REF} \left(1 + \frac{R_1}{R_F} \right) - V_{OH} \left(\frac{R_1}{R_F} \right)$$

Where:

V_{TLH} = trip voltage from low to high

V_{THL} = trip voltage from high to low

4.3.2 INVERTING CIRCUIT

Figure 4-6 shows an inverting circuit for single-supply using three resistors. The resulting hysteresis diagram is shown in Figure 4-7.

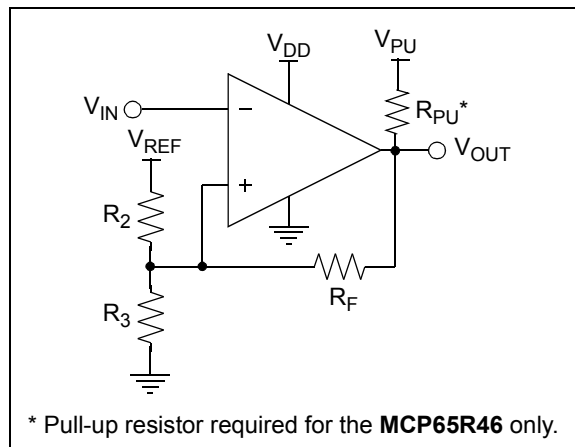


FIGURE 4-6: Inverting Circuit with Hysteresis.

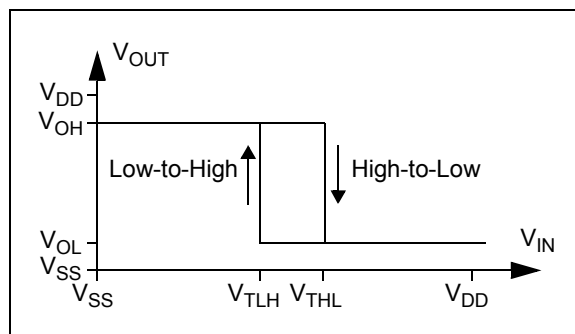


FIGURE 4-7: Hysteresis Diagram for the Inverting Circuit.

MCP65R41/6

To determine the trip voltages (V_{TLH} and V_{THL}) for the circuit shown in Figure 4-6, R_2 and R_3 can be simplified to the Thevenin equivalent circuit with respect to V_{REF} as shown in Figure 4-8:

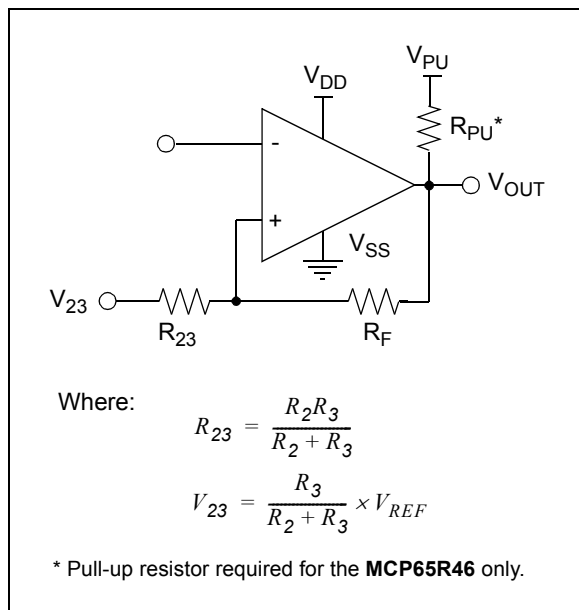


FIGURE 4-8: Thevenin Equivalent Circuit.

By using this simplified circuit, the trip voltage can be calculated using the following equation:

EQUATION 4-1:

$$V_{THL} = V_{OH} \left(\frac{R_{23}}{R_{23} + R_F} \right) + V_{23} \left(\frac{R_F}{R_{23} + R_F} \right)$$

$$V_{TLH} = V_{OL} \left(\frac{R_{23}}{R_{23} + R_F} \right) + V_{23} \left(\frac{R_F}{R_{23} + R_F} \right)$$

Where:

V_{TLH} = trip voltage from low to high

V_{THL} = trip voltage from high to low

Figures 2-25 and 2-28 can be used to determine the typical values for V_{OH} and V_{OL} .

4.4 Bypass Capacitors

With this family of comparators, the power supply pin (V_{DD} for single supply) should have a local bypass capacitor (i.e., 0.01 μ F to 0.1 μ F) within 2 mm for good edge rate performance.

4.5 Capacitive Loads

4.5.1 OUT PIN

Reasonable capacitive loads (i.e., logic gates) have little impact on the propagation delay (see Figure 2-34). The supply current increases with the increasing toggle frequency (Figure 2-22), especially with higher capacitive loads. The output slew rate and propagation delay performance will be reduced with higher capacitive loads.

4.5.2 V_{REF} PIN

The reference output is designed to interface to the comparator input pins, either directly or with some resistive network (e.g., a voltage divider network) with minimal capacitive load. The recommended capacitive load is 200 pF (typical). Capacitive loads greater than 2000 pF may cause the V_{REF} output to oscillate at power up.

4.6 PCB Surface Leakage

In applications where the low input bias current is critical, the Printed Circuit Board (PCB) surface leakage effects need to be considered. Surface leakage is caused by humidity, dust or other type of contamination on the board. Under low humidity conditions, a typical resistance between nearby traces is $10^{12}\Omega$. A 5V difference would cause 5 pA of current to flow. This is greater than the MCP65R41/6 family's bias current at +25°C (1 pA, typical).

The easiest way to reduce the surface leakage is to use a guard ring around the sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin. An example of this type of layout is shown in Figure 4-9.

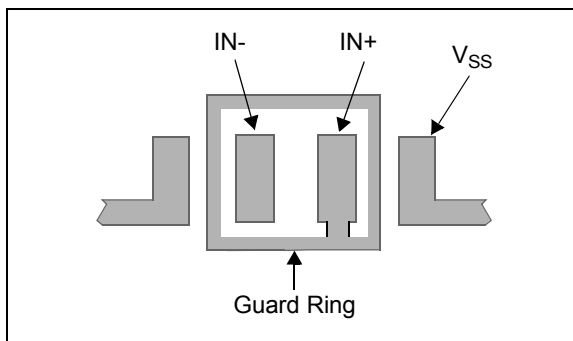


FIGURE 4-9: Example of a Guard Ring Layout for Inverting Circuit.

Use the following steps for an inverting configuration (Figures 4-6):

1. Connect the guard ring to the non-inverting input pin (V_{IN+}). This biases the guard ring to the same reference voltage as the comparator (e.g., $V_{DD}/2$ or ground).
2. Connect the inverting pin (V_{IN-}) to the input pad without touching the guard ring.

Use the following steps for a non-inverting configuration (Figure 4-4):

1. Connect the non-inverting pin (V_{IN+}) to the input pad without touching the guard ring.
2. Connect the guard ring to the inverting input pin (V_{IN-}).

4.7 Typical Applications

4.7.1 PRECISE COMPARATOR

Some applications require a higher DC precision. A simple way to address this need is using an amplifier (such as the MCP6041 – a 600 nA low power and 14 kHz bandwidth op amp) to gain-up the input signal before it reaches the comparator. Figure 4-10 shows an example of this approach, which also level shifts to V_{PU} using the Open-Drain option, the MCP65R46.

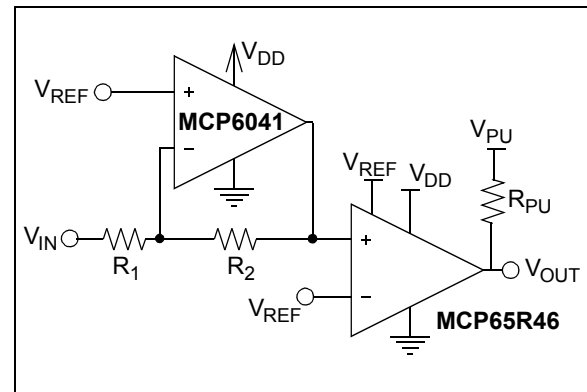


FIGURE 4-10: Precise Inverting Comparator.

4.7.2 BISTABLE MULTI-VIBRATOR

A simple bistable multi-vibrator design is shown in Figure 4-11. V_{REF} needs to be between ground and the maximum comparator internal V_{REF} of 2.4V to achieve oscillation. The output duty cycle changes with V_{REF} .

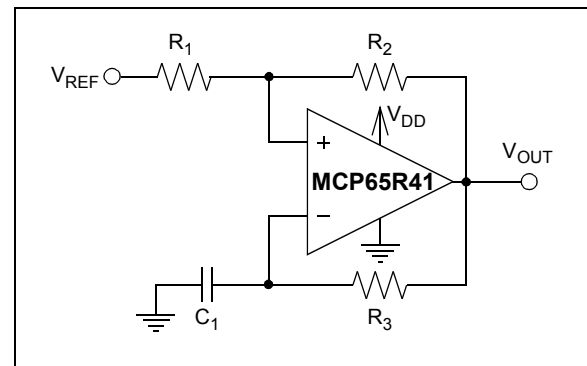


FIGURE 4-11: Bistable Multi-Vibrator.

MCP65R41/6

4.7.3 OVER-TEMPERATURE PROTECTION CIRCUIT

The MCP65R41 device can be used as an over-temperature protection circuit using a thermistor. The 2.4V V_{REF} can be used as stable reference to the thermistor, the alert threshold and hysteresis threshold. This is ideal for battery powered applications, where the change in temperature and output toggle thresholds would remain fixed as battery voltage decays over time.

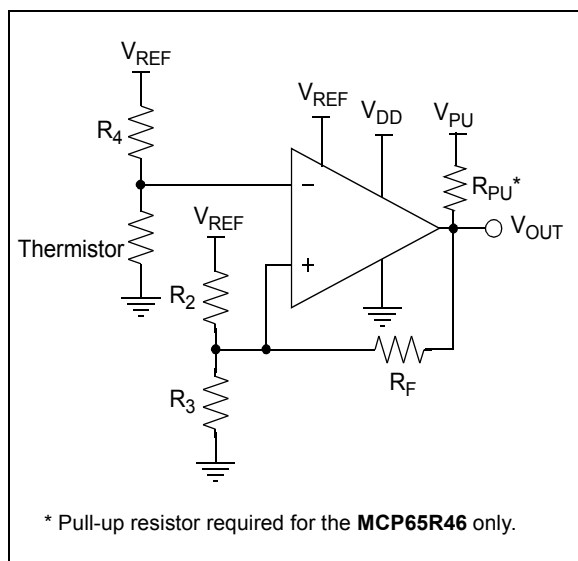
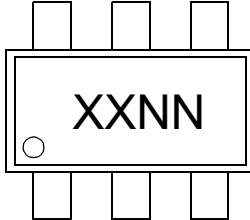


FIGURE 4-12: Over-Temperature Alert Circuit.

5.0 PACKAGING INFORMATION

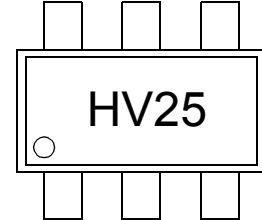
5.1 Package Marking Information

6-Lead SOT-23



Part Number	Code
MCP65R41T-1202E/CHY	HVNN
MCP65R41T-2402E/CHY	HWNN
MCP65R46T-1202E/CHY	HXNN
MCP65R46T-2402E/CHY	HYNN

Example



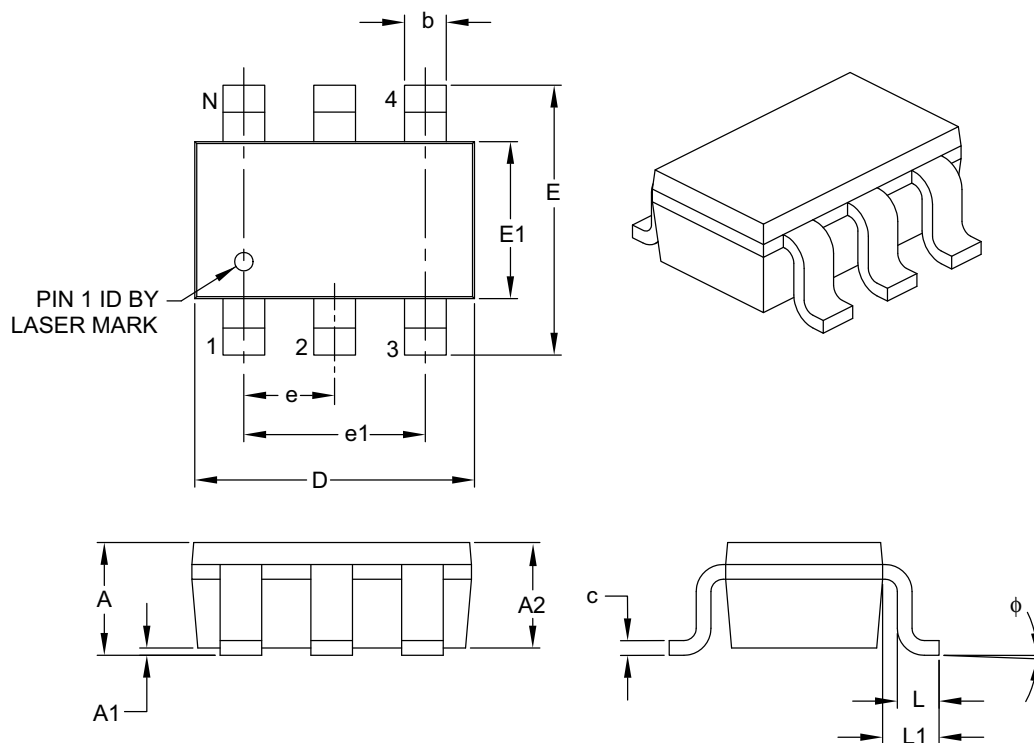
Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

MCP65R41/6

6-Lead Plastic Small Outline Transistor (CHY) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Pins	N	6		
Pitch	e	0.95 BSC		
Outside Lead Pitch	e1	1.90 BSC		
Overall Height	A	0.90	—	1.45
Molded Package Thickness	A2	0.89	—	1.30
Standoff	A1	0.00	—	0.15
Overall Width	E	2.20	—	3.20
Molded Package Width	E1	1.30	—	1.80
Overall Length	D	2.70	—	3.10
Foot Length	L	0.10	—	0.60
Footprint	L1	0.35	—	0.80
Foot Angle	φ	0°	—	30°
Lead Thickness	c	0.08	—	0.26
Lead Width	b	0.20	—	0.51

Notes:

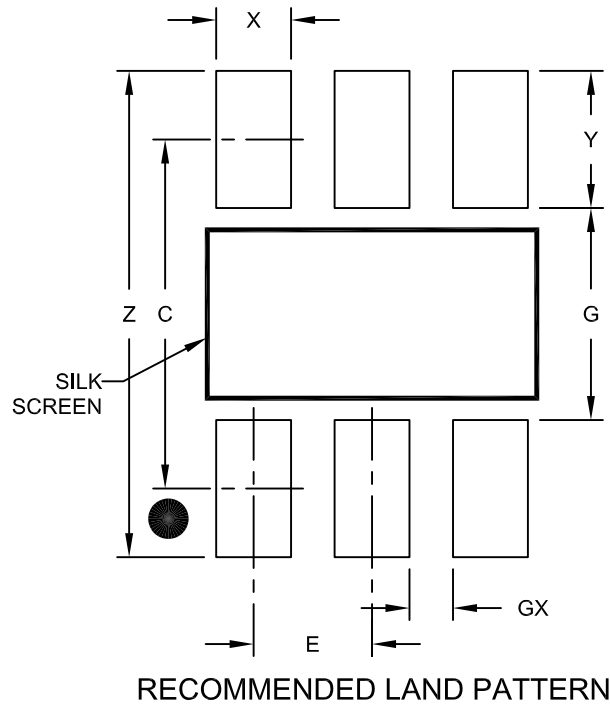
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-028B

6-Lead Plastic Small Outline Transistor (CHY) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	0.95 BSC		
Contact Pad Spacing	C		2.80	
Contact Pad Width (X6)	X			0.60
Contact Pad Length (X6)	Y			1.10
Distance Between Pads	G	1.70		
Distance Between Pads	GX	0.35		
Overall Width	Z			3.90

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2028A

MCP65R41/6

NOTES:

APPENDIX A: REVISION HISTORY

Revision B (September 2011)

The following modification was made to this document:

Updated the DC Characteristics table.

Revision A (December 2010)

Original Release of this Document.

MCP65R41/6

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<u>PART NO.</u>	<u>X</u>	<u>-XX</u>	<u>XX</u>	<u>X</u>	<u>/XX</u>
Device	Tape and	Reference	Reference	Temperature	Package
		Voltage	Tolerance	Range	
Device: MCP65R41T: Push-pull Output Comparator MCP65R46T: Open-drain Output Comparator Reference Voltage: 12 = 1.21V (typical) Initial Reference Voltage 24 = 2.4V (typical) Initial Reference Voltage Reference Tolerance: 02 = 2% Reference Voltage Tolerance Temperature Range: E = -40°C to +125°C (Extended) Package: CHY= Plastic Small Outline Transistor, 6-Lead					
Examples: a) MCP65R41T-1202E/CHY: Push-Pull Output, 1.2VREF, Tape and Reel, 6LD SOT-23 Pkg. b) MCP65R41T-2402E/CHY: Push-Pull Output, 2.4VREF, Tape and Reel, 6LD SOT-23 Pkg. c) MCP65R46T-1202E/CHY: Open-Drain Output, 1.2VREF, Tape and Reel, 6LD SOT-23 Pkg. d) MCP65R46T-2402E/CHY: Open-Drain Output, 2.4VREF, Tape and Reel, 6LD SOT-23 Pkg.					

MCP65R41/6

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights.

Trademarks

The Microchip name and logo, the Microchip logo, dsPIC, KEELOQ, KEELOQ logo, MPLAB, PIC, PICmicro, PICSTART, PIC³² logo, rfPIC and UNI/O are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

FilterLab, Hampshire, HI-TECH C, Linear Active Thermistor, MXDEV, MXLAB, SEEVAL and The Embedded Control Solutions Company are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Analog-for-the-Digital Age, Application Maestro, chipKIT, chipKIT logo, CodeGuard, dsPICDEM, dsPICDEM.net, dsPICworks, dsSPEAK, ECAN, ECONOMONITOR, FanSense, HI-TIDE, In-Circuit Serial Programming, ICSP, Mindi, MiWi, MPASM, MPLAB Certified logo, MPLIB, MPLINK, mTouch, Omniscent Code Generation, PICC, PICC-18, PICDEM, PICDEM.net, PICKit, PICtail, REAL ICE, rfLAB, Select Mode, Total Endurance, TSHARC, UniWinDriver, WiperLock and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

All other trademarks mentioned herein are property of their respective companies.

© 2010-2011, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

 Printed on recycled paper.

ISBN: 978-1-61341-513-9

QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
== ISO/TS 16949:2009 ==

Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

Worldwide Sales and Service

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
<http://www.microchip.com/support>
Web Address:
www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Cleveland
Independence, OH
Tel: 216-447-0464
Fax: 216-447-0643

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Farmington Hills, MI
Tel: 248-538-2250
Fax: 248-538-2260

Indianapolis
Noblesville, IN
Tel: 317-773-8323
Fax: 317-773-5453

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608

Santa Clara
Santa Clara, CA
Tel: 408-961-6444
Fax: 408-961-6445

Toronto
Mississauga, Ontario,
Canada
Tel: 905-673-0699
Fax: 905-673-6509

ASIA/PACIFIC

Asia Pacific Office
Suites 3707-14, 37th Floor
Tower 6, The Gateway
Harbour City, Kowloon
Hong Kong
Tel: 852-2401-1200
Fax: 852-2401-3431

Australia - Sydney
Tel: 61-2-9868-6733
Fax: 61-2-9868-6755

China - Beijing
Tel: 86-10-8569-7000
Fax: 86-10-8528-2104

China - Chengdu
Tel: 86-28-8665-5511
Fax: 86-28-8665-7889

China - Chongqing
Tel: 86-23-8980-9588
Fax: 86-23-8980-9500

China - Hangzhou
Tel: 86-571-2819-3187
Fax: 86-571-2819-3189

China - Hong Kong SAR
Tel: 852-2401-1200
Fax: 852-2401-3431

China - Nanjing
Tel: 86-25-8473-2460
Fax: 86-25-8473-2470

China - Qingdao
Tel: 86-532-8502-7355
Fax: 86-532-8502-7205

China - Shanghai
Tel: 86-21-5407-5533
Fax: 86-21-5407-5066

China - Shenyang
Tel: 86-24-2334-2829
Fax: 86-24-2334-2393

China - Shenzhen
Tel: 86-755-8203-2660
Fax: 86-755-8203-1760

China - Wuhan
Tel: 86-27-5980-5300
Fax: 86-27-5980-5118

China - Xian
Tel: 86-29-8833-7252
Fax: 86-29-8833-7256

China - Xiamen
Tel: 86-592-2388138
Fax: 86-592-2388130

China - Zhuhai
Tel: 86-756-3210040
Fax: 86-756-3210049

ASIA/PACIFIC

India - Bangalore
Tel: 91-80-3090-4444
Fax: 91-80-3090-4123

India - New Delhi
Tel: 91-11-4160-8631
Fax: 91-11-4160-8632

India - Pune
Tel: 91-20-2566-1512
Fax: 91-20-2566-1513

Japan - Yokohama
Tel: 81-45-471- 6166
Fax: 81-45-471-6122

Korea - Daegu
Tel: 82-53-744-4301
Fax: 82-53-744-4302

Korea - Seoul
Tel: 82-2-554-7200
Fax: 82-2-558-5932 or
82-2-558-5934

Malaysia - Kuala Lumpur
Tel: 60-3-6201-9857
Fax: 60-3-6201-9859

Malaysia - Penang
Tel: 60-4-227-8870
Fax: 60-4-227-4068

Philippines - Manila
Tel: 63-2-634-9065
Fax: 63-2-634-9069

Singapore
Tel: 65-6334-8870
Fax: 65-6334-8850

Taiwan - Hsin Chu
Tel: 886-3-5778-366
Fax: 886-3-5770-955

Taiwan - Kaohsiung
Tel: 886-7-536-4818
Fax: 886-7-330-9305

Taiwan - Taipei
Tel: 886-2-2500-6610
Fax: 886-2-2508-0102

Thailand - Bangkok
Tel: 66-2-694-1351
Fax: 66-2-694-1350

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4450-2828
Fax: 45-4485-2829

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

UK - Wokingham
Tel: 44-118-921-5869
Fax: 44-118-921-5820

Данный компонент на территории Российской Федерации

Вы можете приобрести в компании MosChip.

Для оперативного оформления запроса Вам необходимо перейти по данной ссылке:

<http://moschip.ru/get-element>

Вы можете разместить у нас заказ для любого Вашего проекта, будь то серийное производство или разработка единичного прибора.

В нашем ассортименте представлены ведущие мировые производители активных и пассивных электронных компонентов.

Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

Офис по работе с юридическими лицами:

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:

moschip.ru

moschip.ru_4

moschip.ru_6

moschip.ru_9