# 3 µA Comparator with Integrated Reference Voltage

#### Features:

· Factory Set Reference Voltage

- Available Voltage: 1.21V and 2.4V

- Tolerance: ±1% (typical)

Low Quiescent Current: 2.5 µA (typical)

Propagation Delay: 4 µs with 100 mV Overdrive

Input Offset Voltage: ±3mV (typical)

Rail-to-Rail Input: V<sub>SS</sub> - 0.3V to V<sub>DD</sub> + 0.3V

Output Options:

- MCP65R41 → Push-Pull

- MCP65R46 → Open-Drain

Wide Supply Voltage Range: 1.8V to 5.5V

· Packages: SOT23-6

## **Typical Applications:**

· Laptop Computers

· Mobile Phones

· Hand-held Metering Systems

· Hand-held Electronics

RC Timers

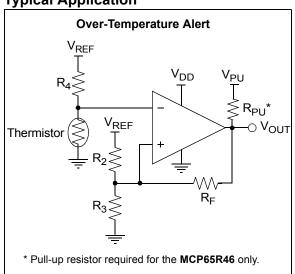
· Alarm and Monitoring Circuits

· Window Comparators

### Design Aids:

- Microchip Advanced Part Selector (MAPS)
- · Analog Demonstration and Evaluation Boards

### Typical Application



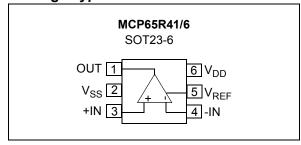
### **Description:**

The Microchip Technology Inc. MCP65R41/6 family of push-pull and open-drain output comparators are offered with integrated reference voltages of 1.21V and 2.4V. This family provides  $\pm 1\%$  (typical) tolerance while consuming 2.5  $\mu A$  (typical) current. These comparators operate with a single-supply voltage as low as 1.8V to 5.5V, which makes them ideal for low cost and/or battery powered applications.

These comparators are optimized for low-power, single-supply applications with greater than rail-to-rail input operation. The output limits supply current surges and dynamic power consumption while switching. The internal input hysteresis eliminates output switching due to internal noise voltage, reducing current draw. The MCP65R41 output interfaces to CMOS/TTL logic. The open-drain output device MCP65R46 can be used as a level-shifter from 1.6V to 10V using a pull-up resistor. It can also be used as a wired-OR logic.

This family of devices is available in the 6-lead SOT-23 package.

### **Package Types**



NOTES:

# 1.0 ELECTRICAL CHARACTERISTICS

### 1.1 Absolute Maximum Ratings†

V <sub>DD</sub> - V <sub>SS</sub>
All other inputs and outputs $V_{SS}$ – 0.3V to $V_{DD}$ + 0.3V
Difference Input voltage V <sub>DD</sub> - V <sub>SS</sub>
Output Short Circuit Current±25 mA
Current at Input Pins±2 mA
Current at Output and Supply Pins±50 mA
Storage temperature65°C to +150°C
Ambient temperature with power applied40°C to +125°C
Junction temperature+150°C
ESD protection on all pins (HBM/MM)≥ 4 kV/200V
ESD protection on MCP65R46 OUT pin (HBM/MM)
≥ 4 kV/175\

**†Notice:** Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

### DC CHARACTERISTICS

Unless otherwise indicated, all limits are specified for:  $V_{DD}$  = +1.8V to +5.5V,  $V_{SS}$  = GND,  $T_A$  = +25°C,  $V_{IN+}$  =  $V_{DD}/2$ ,  $V_{IN-}$  =  $V_{SS}$ ,  $R_L$  = 100 k $\Omega$  to  $V_{DD}/2$  (MCP65R41 only), and  $R_{Pull-Up}$  = 2.74 k $\Omega$  to  $V_{DD}$  (MCP65R46 only).

	1	-			1
Sym	Min	Тур	Max	Units	Conditions
$V_{DD}$	1.8		5.5	V	
IQ	_	2.5	4	μA	I <sub>OUT</sub> = 0
$V_{CMR}$	V <sub>SS</sub> -0.3	_	V <sub>DD</sub> +0.3	V	
CMRR	55	70	l	dB	$V_{CM} = -0.3V \text{ to } 5.3V$
	50	65	1	dB	$V_{CM} = 2.5V \text{ to } 5.3V$
	55	70	_	dB	MCP65R41,
					$V_{CM} = -0.3V \text{ to } 2.5V$
	50	70	_	dB	MCP65R46,
					$V_{CM} = -0.3V \text{ to } 2.5V$
PSRR	63	80		dB	V <sub>CM</sub> = V <sub>SS</sub>
$V_{OS}$	-10	±3	+10	mV	V <sub>CM</sub> = V <sub>SS</sub> (Note 1)
ΔV <sub>OS</sub> /ΔT	_	±10	_	μV/°C	V <sub>CM</sub> = V <sub>SS</sub>
$V_{HYST}$	1	3.3	5	mV	V <sub>CM</sub> = V <sub>SS</sub> (Note 1)
$\Delta V_{HYST}/\Delta T$	_	6	_	μV/°C	V <sub>CM</sub> = V <sub>SS</sub>
$\Delta V_{HYST}/\Delta T^2$	_	5	_	μV/°C <sup>2</sup>	V <sub>CM</sub> = V <sub>SS</sub>
Ι <sub>Β</sub>	_	1	_	pА	$V_{CM} = V_{SS}$
Ι <sub>Β</sub>	_	50	_	pА	V <sub>CM</sub> = V <sub>SS</sub>
I <sub>B</sub>	_	_	5000	рА	V <sub>CM</sub> = V <sub>SS</sub>
I <sub>OS</sub>	_	±1		pА	V <sub>CM</sub> = V <sub>SS</sub>
Z <sub>CM</sub> /Z <sub>DIFF</sub>	_	10 <sup>13</sup>   4		Ω  pF	
	$\begin{array}{c} V_{DD} \\ I_{Q} \\ \\ V_{CMR} \\ CMRR \\ \\ CMRR \\ \\ PSRR \\ V_{OS} \\ \Delta V_{OS}/\Delta T \\ V_{HYST} \\ \Delta V_{HYST}/\Delta T \\ \Delta V_{HYST}/\Delta T^{2} \\ I_{B} \\ I_{B} \\ I_{DS} \\ \\ I_{OS} \\ \end{array}$	V <sub>DD</sub> 1.8 I <sub>Q</sub> —  V <sub>CMR</sub> V <sub>SS</sub> =0.3 CMRR 55 50 55 50 PSRR 63 V <sub>OS</sub> -10 ΔV <sub>OS</sub> /ΔT —  V <sub>HYST</sub> 1 ΔV <sub>HYST</sub> /ΔT —  I <sub>B</sub> —  I <sub>B</sub> —  I <sub>B</sub> —  I <sub>COS</sub> —  Z <sub>CM</sub> /Z <sub>DIFF</sub> —	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	V <sub>DD</sub> 1.8         —         5.5         V           I <sub>Q</sub> —         2.5         4         μA           V <sub>CMR</sub> V <sub>SS</sub> -0.3         —         V <sub>DD</sub> +0.3         V           CMRR         55         70         —         dB           50         65         —         dB           55         70         —         dB           63         80         —         dB           V <sub>OS</sub> -10         ±3         +10         mV           ΔV <sub>OS</sub> /ΔT         —         ±10         —         μV/°C           V <sub>HYST</sub> 1         3.3         5         mV           ΔV <sub>HYST</sub> /ΔT         —         6         —         μV/°C           ΔV <sub>HYST</sub> /ΔT <sup>2</sup> —         5         —         μV/°C           ΔV <sub>HYST</sub> /ΔT <sup>2</sup> —         5         —         μV/°C           ΔI <sub>B</sub> —         1         —         pA           I <sub>B</sub> —         50         —         pA           I <sub>B</sub> —         5000         pA           I <sub>B</sub> —         5000         pA           I <sub>B</sub>

- **Note 1:** The input offset voltage is the center (average) of the input-referred trip points. The input hysteresis is the difference between the input-referred trip points.
  - 2: Limit the output current to Absolute Maximum Rating of 30 mA.
  - 3: Do not short the output of the MCP65R46 comparators above  $V_{SS}$  + 10V.
  - 4: The low-power reference voltage pin is designed to drive small capacitive loads. See Section 4.5.2.

# DC CHARACTERISTICS (CONTINUED)

Unless otherwise indicated, all limits are specified for:  $V_{DD}$  = +1.8V to +5.5V,  $V_{SS}$  = GND,  $T_A$  = +25°C,  $V_{IN+}$  =  $V_{DD}/2$ ,  $V_{IN-} = V_{SS}$ ,  $R_L = 100 \text{ k}\Omega$  to  $V_{DD}/2$  (MCP65R41 only), and  $R_{Pull-Up} = 2.74 \text{ k}\Omega$  to  $V_{DD}$  (MCP65R46 only). **Parameters** Sym Min Max Units **Conditions** Тур **Push Pull Output**  $I_{OUT}$  = -2 mA,  $V_{DD}$  = 5V High Level Output Voltage V  $V_{OH}$  $V_{DD}$ -0.2 V<sub>SS</sub>+0.2 Low Level Output Voltage ٧  $I_{OUT} = 2 \text{ mA}, V_{DD} = 5V$  $V_{OL}$ Short Circuit Current  $I_{SC}$ ±50 mΑ (Note 2) MCP65R41 (Note 2) MCP65R46 ±1.5 mΑ  $I_{SC}$ Open Drain Output (MCP65R46) Low Level Output Voltage  $V_{OL}$ V<sub>SS</sub>+0.2 ٧  $I_{OUT} = 2 \text{ mA}$ **Short Circuit Current**  $I_{SC}$ ±50 mΑ High-Level Output Current -100 nΑ  $V_{PU} = 10V$  $I_{OH}$ Pull-up Voltage ٧ Note 3  $V_{PU}$ 1.6 10 **Output Pin Capacitance** 8 pF C<sub>OUT</sub> Reference Voltage Output -2 % Initial Reference Tolerance +2  $V_{TOL}$  $I_{REF} = 0A$ , +1  $V_{REF} = 1.21V \text{ and } 2.4V$  $V_{REF}$ 1.185 1.21 1.234 ٧  $I_{RFF} = 0A$ 2.448 V 2.352 2.4  $V_{TOL} = \pm 2\%$  (maximum) Reference Output Current ±500 μΑ IREF Drift with Temperature (character-27 100  $V_{REF} = 1.21V, V_{DD} = 1.8V$  $\Delta V_{REF}/\Delta T$ ppm ized but not production tested) 22 100  $V_{REF} = 1.21V, V_{DD} = 5.5V$ ppm 23 100  $V_{REF} = 2.4V, V_{DD} = 5.5V$ ppm

200

2: Limit the output current to Absolute Maximum Rating of 30 mA.

 $C_{l}$ 

- 3: Do not short the output of the MCP65R46 comparators above  $V_{SS}$  + 10V.
- 4: The low-power reference voltage pin is designed to drive small capacitive loads. See Section 4.5.2.

Capacitive Load

Note 4

рF

**Note 1:** The input offset voltage is the center (average) of the input-referred trip points. The input hysteresis is the difference between the input-referred trip points.

### **AC CHARACTERISTICS**

Unless otherwise indicated, all limits are specified for:  $V_{DD}$  = +1.8V to +5.5V,  $V_{SS}$  = GND,  $T_A$  = +25°C,  $V_{IN+}$  =  $V_{DD}/2$ , Step = 200 mV, Overdrive = 100 mV,  $R_L$  = 100 k $\Omega$  to  $V_{DD}/2$  (MCP65R41 only),  $R_{Pull-Up}$  = 2.74 k $\Omega$  to  $V_{DD}$  (MCP65R46 only), and  $R_L$  = 50 pF.

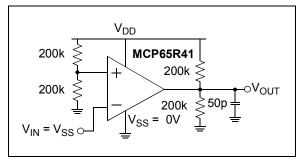
Parameters	Sym	Min	Тур	Max	Units	Conditions
Rise Time	t <sub>R</sub>	_	0.85	_	μs	
Fall Time	t <sub>F</sub>	_	0.85	_	μs	
Propagation Delay (High-to-Low)	t <sub>PHL</sub>	_	4	8.0	μs	
Propagation Delay (Low-to-High)	t <sub>PLH</sub>	_	4	8.0	μs	
Propagation Delay Skew	t <sub>PDS</sub>	_	±0.2	_	μs	Note 1
Maximum Toggle Frequency	f <sub>MAX</sub>	_	160	_	kHz	V <sub>DD</sub> = 1.8V
	f <sub>MAX</sub>	_	120	_	kHz	V <sub>DD</sub> = 5.5V
Input Noise Voltage	E <sub>N</sub>		200	_	$\mu V_{P-P}$	10 Hz to 100 kHz

**Note 1:** Propagation Delay Skew is defined as:  $t_{PDS} = t_{PLH} - t_{PHL}$ .

## **TEMPERATURE SPECIFICATIONS**

Unless otherwise indicated, all limits are specified for: $V_{DD}$ = +1.8V to +5.5V and $V_{SS}$ = GND.						
Parameters	Symbol	Min	Тур	Max	Units	Conditions
Temperature Ranges						
Specified Temperature Range	T <sub>A</sub>	-40	_	+125	°C	
Operating Temperature Range	T <sub>A</sub>	-40	_	+125	°C	
Storage Temperature Range	T <sub>A</sub>	-65	_	+150	°C	
Thermal Package Resistances						
Thermal Resistance, SOT23-6	$\theta_{JA}$	_	190.5	_	°C/W	

# 1.2 Test Circuit Configuration



**FIGURE 1-1:** Test Circuit for the Push-Pull Output Comparators.

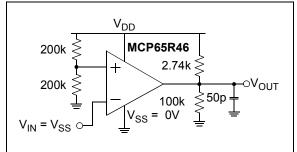


FIGURE 1-2: Test Circuit for the Open-Drain Comparators.

NOTES:

### 2.0 TYPICAL PERFORMANCE CURVES

**Note:** The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

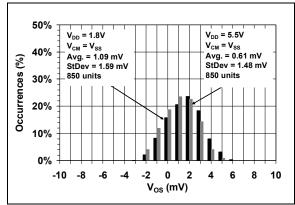


FIGURE 2-1: Input Offset Voltage.

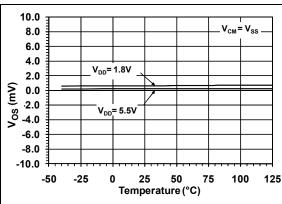


FIGURE 2-2: Input Offset Voltage vs. Temperature.

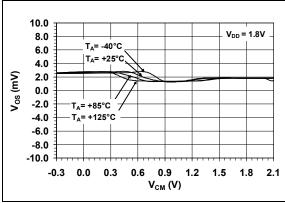


FIGURE 2-3: Input Offset Voltage vs. Common-Mode Input Voltage.

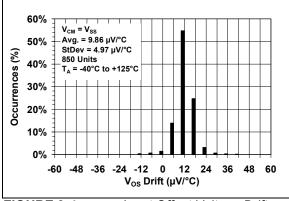


FIGURE 2-4: Input Offset Voltage Drift.

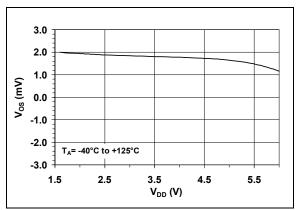


FIGURE 2-5: Input Offset Voltage vs. Supply Voltage vs. Temperature.

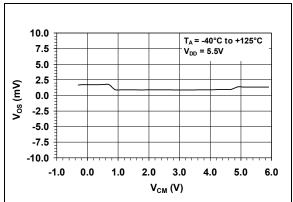
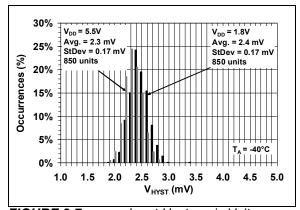
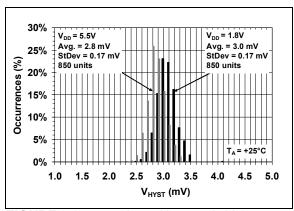


FIGURE 2-6: Input Offset Voltage vs. Common-Mode Input Voltage.



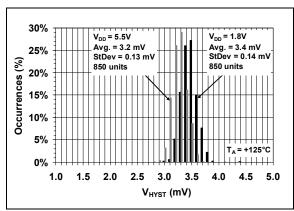
**FIGURE 2-7:** at -40°C.

Input Hysteresis Voltage



**FIGURE 2-8:** at +25°C.

Input Hysteresis Voltage



**FIGURE 2-9:** at +125°C.

Input Hysteresis Voltage

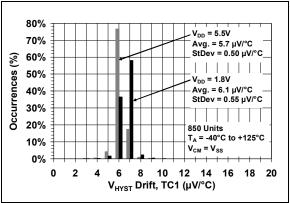
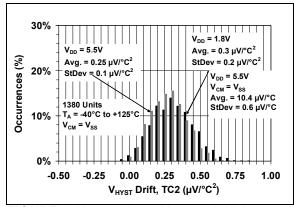


FIGURE 2-10: Input Hysteresis Voltage
Drift – Linear Temperature Compensation (TC1).



**FIGURE 2-11:** Input Hysteresis Voltage Drift – Quadratic Temperature Compensation (TC2).

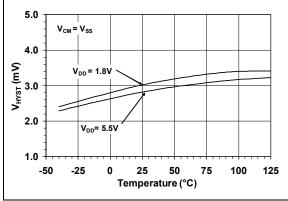


FIGURE 2-12: vs. Temperature.

Input Hysteresis Voltage

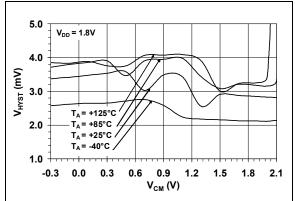


FIGURE 2-13: Input Hysteresis Voltage vs. Common-Mode Input Voltage.

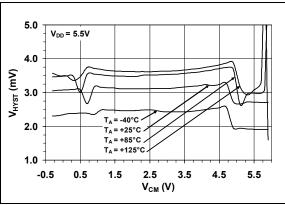
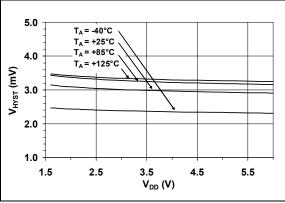


FIGURE 2-14: Input Hysteresis Voltage vs. Common-Mode Input Voltage.



**FIGURE 2-15:** Input Hysteresis Voltage vs. Supply Voltage vs. Temperature.

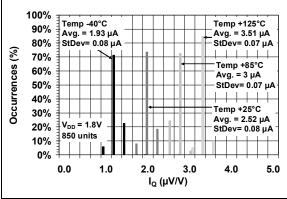
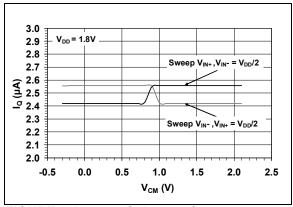


FIGURE 2-16: Quiescent Current.



**FIGURE 2-17:** Quiescent Current vs. Common-Mode Input Voltage.

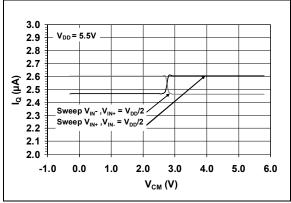


FIGURE 2-18: Quiescent Current vs. Common-Mode Input Voltage.

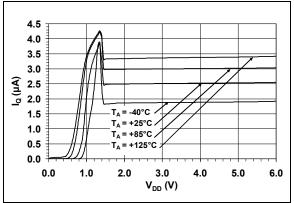


FIGURE 2-19: Quiescent Current vs. Supply Voltage vs. Temperature.

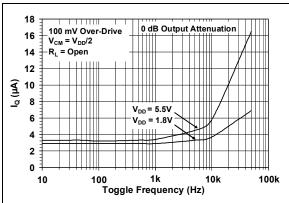


FIGURE 2-20: Quiescent Current vs. Toggle Frequency.

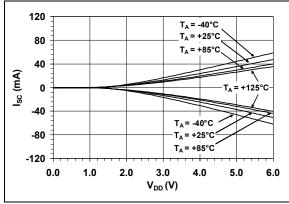


FIGURE 2-21: Short Circuit Current vs. Supply Voltage vs. Temperature.

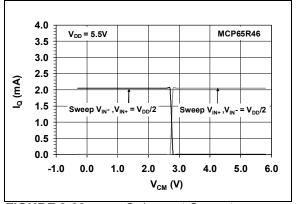


FIGURE 2-22: Quiescent Current vs. Common-Mode Input Voltage.

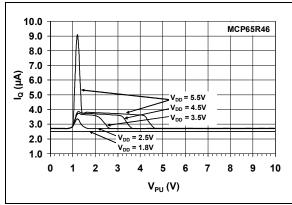


FIGURE 2-23: Quiescent Current vs. Pull-Up Voltage.

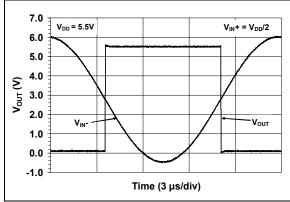
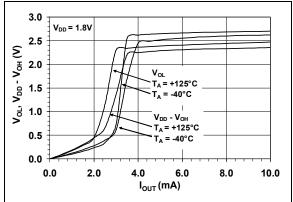


FIGURE 2-24: No Phase Reversal.

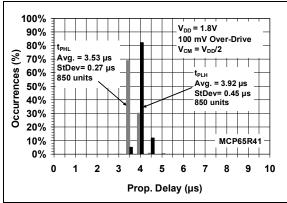
**Note:** Unless otherwise indicated,  $V_{DD}$  = +1.8V to +5.5V,  $V_{SS}$  = GND,  $T_A$  = +25°C,  $V_{IN}$ + =  $V_{DD}$ /2,  $V_{IN}$ - = GND,  $R_L$  = 100 k $\Omega$  to  $V_{DD}/2$  (MCP65R41 only),  $R_{Pull-Up}$  = 2.74 k $\Omega$  to  $V_{DD}/2$  (MCP65R46 only) and  $C_L$  = 50 pF.



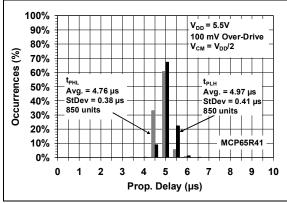
**FIGURE 2-25:** 

Output Headroom vs.

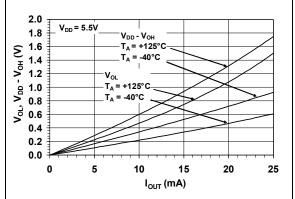
Output Current.



**FIGURE 2-26:** Low-to-High and High-to-Low Propagation Delays.



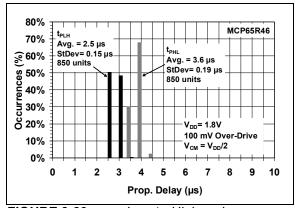
**FIGURE 2-27:** Low-to-High and High-to-Low Propagation Delays.



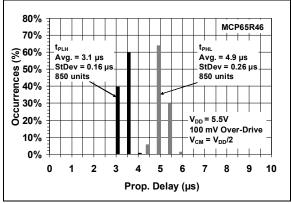
**FIGURE 2-28:** 

Output Headroom vs.

Output Current.



**FIGURE 2-29:** Low-to-High and High-to-Low Propagation Delays.



**FIGURE 2-30:** 

Low-to-High and

High-to-Low Propagation Delays.

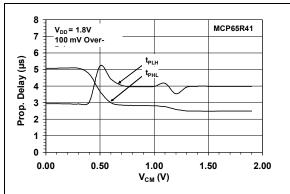


FIGURE 2-31: Propagation Delay vs. Common-Mode Input Voltage.

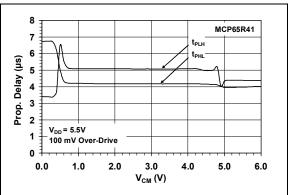
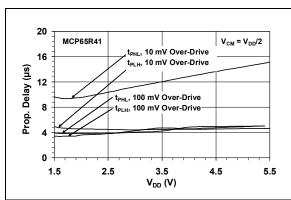


FIGURE 2-32: Propagation Delay vs. Common-Mode Input Voltage.



**FIGURE 2-33:** Propagation Delay vs. Supply Voltage.

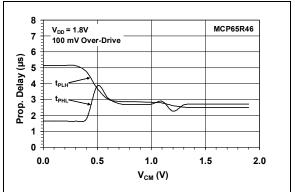


FIGURE 2-34: Propagation Delay vs. Common-Mode Input Voltage.

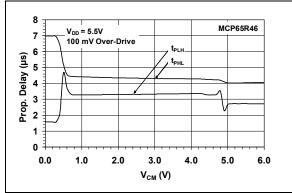


FIGURE 2-35: Propagation Delay vs. Common-Mode Input Voltage.

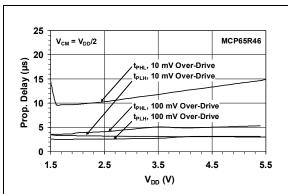
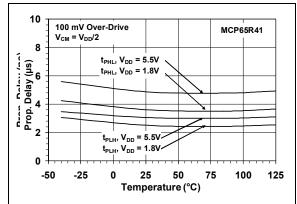


FIGURE 2-36: Propagation Delay vs. Supply Voltage.

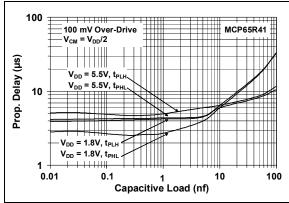
**Note:** Unless otherwise indicated,  $V_{DD}$  = +1.8V to +5.5V,  $V_{SS}$  = GND,  $T_A$  = +25°C,  $V_{IN}$ + =  $V_{DD}$ /2,  $V_{IN}$ - = GND,  $R_L$  = 100 k $\Omega$  to  $V_{DD}/2$  (MCP65R41 only),  $R_{Pull-Up}$  = 2.74 k $\Omega$  to  $V_{DD}/2$  (MCP65R46 only) and  $C_L$  = 50 pF.



**FIGURE 2-37:** 

Propagation Delay vs.

Temperature.



**FIGURE 2-38:** 

Propagation Delay vs.

Capacitive Load.

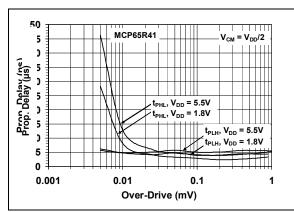
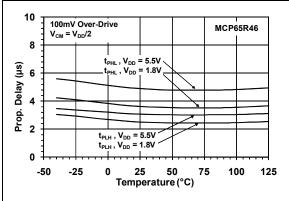


FIGURE 2-39:

Propagation Delay vs.

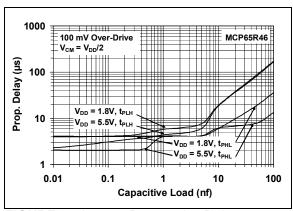
Input Over-Drive.



**FIGURE 2-40:** 

Propagation Delay vs.

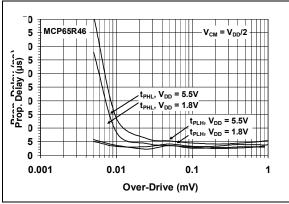
Temperature.



**FIGURE 2-41:** 

Propagation Delay vs.

Capacitive Load.

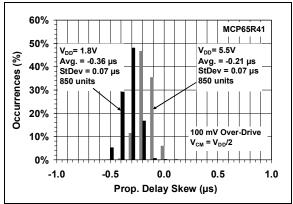


**FIGURE 2-42:** 

Propagation Delay vs.

Input Over-Drive.

**Note:** Unless otherwise indicated,  $V_{DD}$  = +1.8V to +5.5V,  $V_{SS}$  = GND,  $T_A$  = +25°C,  $V_{IN}$ + =  $V_{DD}$ /2,  $V_{IN}$ - = GND,  $R_L$  = 100 k $\Omega$  to  $V_{DD}/2$  (MCP65R41 only),  $R_{Pull-Up}$  = 2.74 k $\Omega$  to  $V_{DD}/2$  (MCP65R46 only) and  $C_L$  = 50 pF.



**FIGURE 2-43:** 

Propagation Delay Skew.

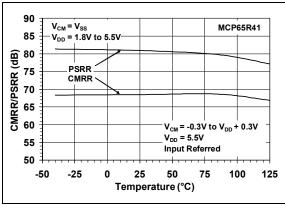


FIGURE 2-44: Common-Mode Rejection Ratio and Power Supply Rejection Ratio vs. Temperature.

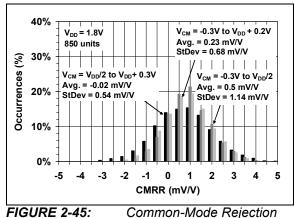
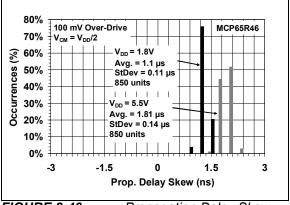


FIGURE 2-45:





**FIGURE 2-46:** 

Propagation Delay Skew.

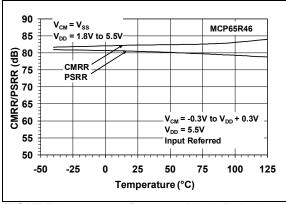
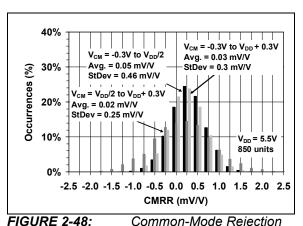


FIGURE 2-47: Common-Mode Rejection Ratio and Power Supply Rejection Ratio vs. Temperature.



Common-Mode Rejection

Ratio.

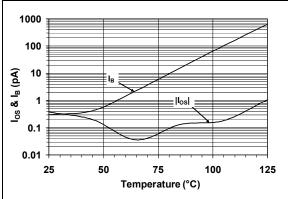


FIGURE 2-49: Input Offset Current and Input Bias Current vs. Temperature.

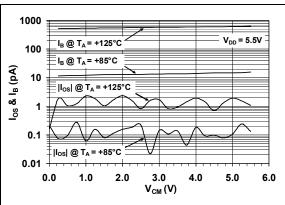


FIGURE 2-50: Input Offset Current and Input Bias Current vs. Common-Mode Input Voltage vs. Temperature.

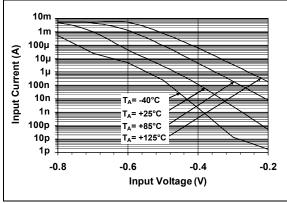


FIGURE 2-51: Input Bias Current vs. Input Voltage vs. Temperature.

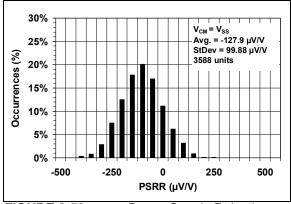


FIGURE 2-52: Power Supply Rejection Ratio.

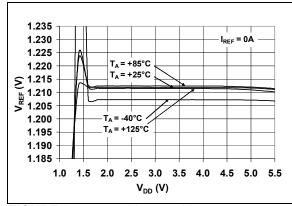


FIGURE 2-53:  $V_{REF}$  vs.  $V_{DD}$ .

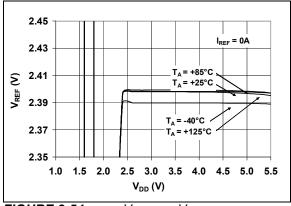


FIGURE 2-54: V<sub>REF</sub> vs. V<sub>DD</sub>.

**Note:** Unless otherwise indicated,  $V_{DD}$  = +1.8V to +5.5V,  $V_{SS}$  = GND,  $T_A$  = +25°C,  $V_{IN}$ + =  $V_{DD}$ /2,  $V_{IN}$ - = GND,  $R_L$  = 100 k $\Omega$  to  $V_{DD}$ /2 (**MCP65R41** only),  $R_{Pull-Up}$  = 2.74 k $\Omega$  to  $V_{DD}$ /2 (**MCP65R46** only) and  $C_L$  = 50 pF.

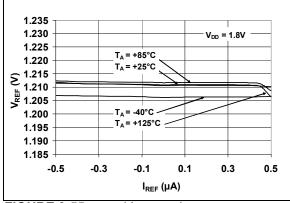
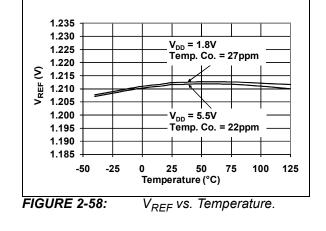


FIGURE 2-55:

V<sub>REF</sub> vs. I<sub>REF</sub> over

Temperature.



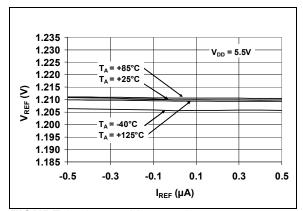


FIGURE 2-56:

V<sub>REF</sub> vs. I<sub>REF</sub> over

Temperature.

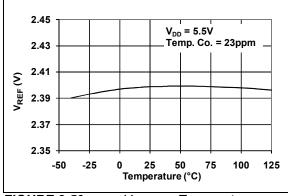


FIGURE 2-59:

V<sub>REF</sub> vs. Temperature.

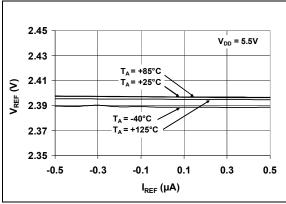
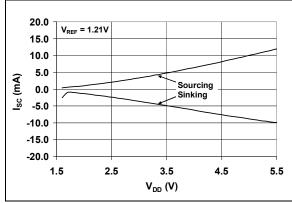


FIGURE 2-57:

V<sub>REF</sub> vs. I<sub>REF</sub> over

Temperature.



**FIGURE 2-60:** 

Short Circuit Current vs.

 $V_{DD}$ .

**Note:** Unless otherwise indicated,  $V_{DD}$  = +1.8V to +5.5V,  $V_{SS}$  = GND,  $T_A$  = +25°C,  $V_{IN}$ + =  $V_{DD}$ /2,  $V_{IN}$ - = GND,  $R_L$  = 100 k $\Omega$  to  $V_{DD}$ /2 (**MCP65R41** only),  $R_{Pull-Up}$  = 2.74 k $\Omega$  to  $V_{DD}$ /2 (**MCP65R46** only) and  $C_L$  = 50 pF.

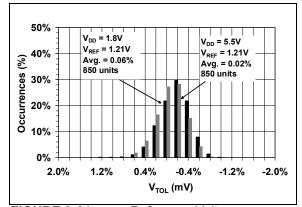
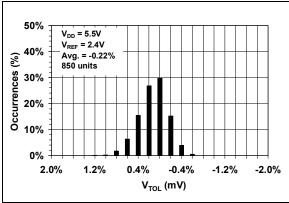


FIGURE 2-61:

Reference Voltage

Tolerance.



**FIGURE 2-62:** 

Reference Voltage

Tolerance.

NOTES:

### 3.0 PIN DESCRIPTIONS

Descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

MCP65R41/6	Compleal	Description		
SOT23-6	- Symbol	Description		
1	OUT	Digital Output		
2	V <sub>SS</sub>	Ground		
3	V <sub>IN</sub> +	Non-inverting Input		
4	V <sub>IN</sub> -	Inverting Input		
5	$V_{REF}$	Reference Voltage Output		
6	$V_{DD}$	Positive Power Supply		

## 3.1 Analog Inputs

The comparator non-inverting and inverting inputs are high-impedance CMOS inputs with low bias currents.

### 3.2 Digital Outputs

The comparator outputs are CMOS/TTL compatible push-pull and open-drain digital outputs. The push-pull is designed to directly interface to a CMOS/TTL compatible pin while the open-drain output is designed for level shifting and wired-OR interfaces.

## 3.3 Analog Outputs

The  $V_{REF}$  Output pin outputs a reference voltage of 1.21V or 2.4V.

# 3.4 Power Supply ( $V_{SS}$ and $V_{DD}$ )

The positive power supply pin ( $V_{DD}$ ) is 1.8V to 5.5V higher than the negative power supply pin ( $V_{SS}$ ). For normal operation, the other pins are at voltages between  $V_{SS}$  and  $V_{DD}$ .

Typically, these parts are used in a single (positive) supply configuration. In this case,  $V_{SS}$  is connected to ground and  $V_{DD}$  is connected to the supply.  $V_{DD}$  will need a local bypass capacitor (typically 0.01  $\mu$ F to 0.1  $\mu$ F) within 2 mm of the  $V_{DD}$  pin. These can share a bulk capacitor with the nearby analog parts (within 100 mm), but it is not required.

NOTES:

### 4.0 APPLICATIONS INFORMATION

The MCP65R41/6 family of push-pull and open-drain output comparators are fabricated on Microchip's state-of-the-art CMOS process. They are suitable for a wide range of high-speed applications requiring low power consumption.

## 4.1 Comparator Inputs

### 4.1.1 NORMAL OPERATION

The input stage of this family of devices uses three differential input stages in parallel: one operates at low input voltages, one at high input voltages, and one at mid input voltages. With this topology, the input voltage range is 0.3V above  $V_{DD}$  and 0.3V below  $V_{SS},$  while providing low offset voltage throughout the Common mode range. The input offset voltage is measured at both  $V_{SS}$  - 0.3V and  $V_{DD}$  + 0.3V to ensure proper operation.

The MCP65R41/6 family has internally-set hysteresis  $V_{HYST}$  that is small enough to maintain input offset accuracy, and large enough to eliminate the output chattering caused by the comparator's own input noise voltage  $E_{NI}$ . Figure 4-1 depicts this behavior. Input offset voltage  $(V_{OS})$  is the center (average) of the (input-referred) low-high and high-low trip points. Input hysteresis voltage  $(V_{HYST})$  is the difference between the same trip points.

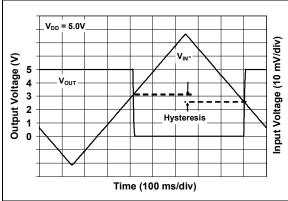


FIGURE 4-1: The MCP65R41/6
Comparators' Internal Hysteresis Eliminates
Output Chatter Caused by Input Noise Voltage.

# 4.1.2 INPUT VOLTAGE AND CURRENT LIMITS

The ESD protection on the inputs can be depicted as shown in Figure 4-2. This structure was chosen to protect the input transistors, and to minimize the input bias current ( $I_B$ ). The input ESD diodes clamp the inputs when trying to go more than one diode drop below  $V_{SS}$ . They also clamp any voltages that go too far above  $V_{DD}$ ; their breakdown voltage is high enough to allow a normal operation, and low enough to bypass the ESD events within the specified limits.

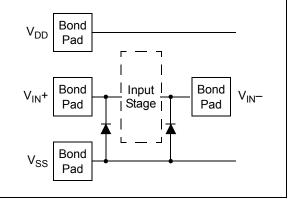


FIGURE 4-2: Simplified Analog Input ESD Structures.

In order to prevent damage and/or improper operation of these comparators, the circuit they are connected to limit the currents (and voltages) at the  $V_{IN}+$  and  $V_{IN}-$  pins (see **Absolute Maximum Ratings†**). Figure 4-3 shows the recommended approach to protect these inputs. The internal ESD diodes prevent the input pins  $(V_{IN}+$  and  $V_{IN}-$ ) from going too far below ground, and the resistors  $R_1$  and  $R_2$  limit the possible current drawn out of the input pin. Diodes  $D_1$  and  $D_2$  prevent the input pin  $(V_{IN}+$  and  $V_{IN}-$ ) from going too far above  $V_{DD}$ . When implemented as shown, resistors  $R_1$  and  $R_2$  also limit the current through  $D_1$  and  $D_2$ .

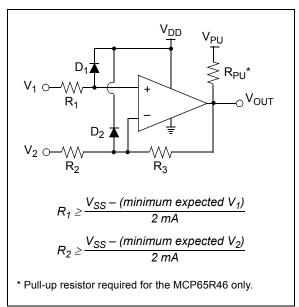


FIGURE 4-3: Protecting the Analog Inputs.

It is also possible to connect the diodes to the left of the resistors  $R_1$  and  $R_2.$  In this case, the currents through the diodes  $D_1$  and  $D_2$  need to be limited by some other mechanism. The resistor then serves as an in-rush current limiter; the DC current into the input pins ( $V_{\text{IN}}+$  and  $V_{\text{IN}}-$ ) should be very small.

A significant amount of current can flow out of the inputs when the Common mode voltage ( $V_{CM}$ ) is below ground ( $V_{SS}$ ); see Figure 4-3. The applications that are high impedance may need to limit the usable voltage range.

### 4.1.3 PHASE REVERSAL

The MCP65R41/6 comparator family uses CMOS transistors at the input. They are designed to prevent phase inversion when the input pins exceed the supply voltages. Figure 2-3 shows an input voltage exceeding both supplies with no resulting phase inversion.

### 4.2 Push-Pull Output

The push-pull output is designed to be compatible with CMOS and TTL logic, while the output transistors are configured to give a rail-to-rail output performance. They are driven with circuitry that minimizes any switching current (shoot-through current from supply to supply) when the output is transitioned from high-to-low, or from low-to-high (see Figures 2-18 and 2-19 for more information).

## 4.3 Externally Set Hysteresis

A greater flexibility in selecting the hysteresis (or the input trip points) is achieved by using external resistors. Hysteresis reduces output chattering when one input is slowly moving past the other. It also helps in systems where it is preferable not to cycle between high and low states too frequently (e.g., air conditioner thermostatic controls). Output chatter also increases the dynamic supply current.

### 4.3.1 NON-INVERTING CIRCUIT

Figure 4-4 shows a non-inverting circuit for single-supply applications using just two resistors. The resulting hysteresis diagram is shown in Figure 4-5.

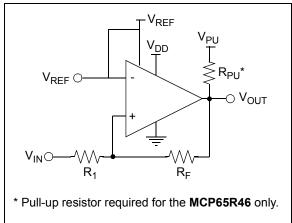
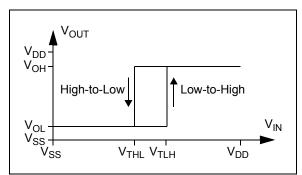


FIGURE 4-4: Non-Inverting Circuit with Hysteresis for Single-Supply.



**FIGURE 4-5:** Hysteresis Diagram for the Non-Inverting Circuit.

The trip points for Figures 4-4 and 4-5 are:

## **EXAMPLE 4-1:**

$$\begin{split} V_{TLH} &= V_{REF} \bigg( I + \frac{R_I}{R_F} \bigg) - V_{OL} \bigg( \frac{R_I}{R_F} \bigg) \\ V_{THL} &= V_{REF} \bigg( I + \frac{R_I}{R_F} \bigg) - V_{OH} \bigg( \frac{R_I}{R_F} \bigg) \end{split}$$

Where:

 $V_{TLH}$  = trip voltage from low to high

 $V_{THL}$  = trip voltage from high to low

### 4.3.2 INVERTING CIRCUIT

Figure 4-6 shows an inverting circuit for single-supply using three resistors. The resulting hysteresis diagram is shown in Figure 4-7.

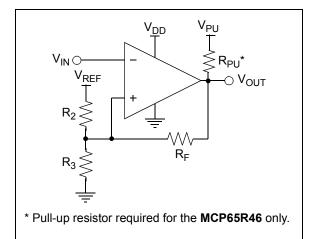


FIGURE 4-6: Inverting Circuit with Hysteresis.

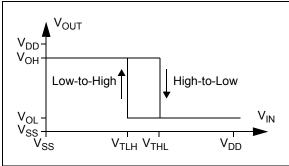


FIGURE 4-7: Hysteresis Diagram for the Inverting Circuit.

To determine the trip voltages ( $V_{TLH}$  and  $V_{THL}$ ) for the circuit shown in Figure 4-6,  $R_2$  and  $R_3$  can be simplified to the Thevenin equivalent circuit with respect to  $V_{REF}$ , as shown in Figure 4-8:

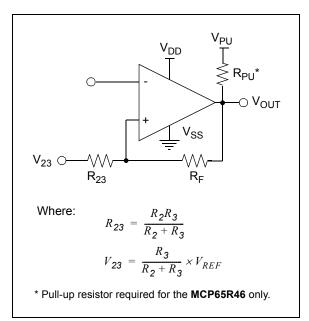


FIGURE 4-8: Thevenin Equivalent Circuit.

By using this simplified circuit, the trip voltage can be calculated using the following equation:

### **EQUATION 4-1:**

$$V_{THL} = V_{OH} \left( \frac{R_{23}}{R_{23} + R_F} \right) + V_{23} \left( \frac{R_F}{R_{23} + R_F} \right)$$

$$V_{TLH} = V_{OL} \left( \frac{R_{23}}{R_{23} + R_F} \right) + V_{23} \left( \frac{R_F}{R_{23} + R_F} \right)$$

Where:

 $V_{TLH}$  = trip voltage from low to high

 $V_{THL}$  = trip voltage from high to low

Figures 2-25 and 2-28 can be used to determine the typical values for  $V_{OH}$  and  $V_{OL}$ .

## 4.4 Bypass Capacitors

With this family of comparators, the power supply pin ( $V_{DD}$  for single supply) should have a local bypass capacitor (i.e., 0.01  $\mu F$  to 0.1  $\mu F$ ) within 2 mm for good edge rate performance.

### 4.5 Capacitive Loads

#### 4.5.1 OUT PIN

Reasonable capacitive loads (i.e., logic gates) have little impact on the propagation delay (see Figure 2-34). The supply current increases with the increasing toggle frequency (Figure 2-22), especially with higher capacitive loads. The output slew rate and propagation delay performance will be reduced with higher capacitive loads.

### 4.5.2 V<sub>REF</sub> PIN

The reference output is designed to interface to the comparator input pins, either directly or with some resistive network (e.g., a voltage divider network) with minimal capacitive load. The recommended capacitive load is 200 pF (typical). Capacitive loads greater than 2000 pF may cause the  $V_{REF}$  output to oscillate at power up.

### 4.6 PCB Surface Leakage

In applications where the low input bias current is critical, the Printed Circuit Board (PCB) surface leakage effects need to be considered. Surface leakage is caused by humidity, dust or other type of contamination on the board. Under low humidity conditions, a typical resistance between nearby traces is  $10^{12}\Omega$ . A 5V difference would cause 5 pA of current to flow. This is greater than the MCP65R41/6 family's bias current at +25°C (1 pA, typical).

The easiest way to reduce the surface leakage is to use a guard ring around the sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin. An example of this type of layout is shown in Figure 4-9.

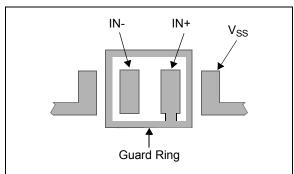


FIGURE 4-9: Example of a Guard Ring Layout for Inverting Circuit.

Use the following steps for an inverting configuration (Figures 4-6):

- Connect the guard ring to the non-inverting input pin (V<sub>IN</sub>+). This biases the guard ring to the same reference voltage as the comparator (e.g., V<sub>DD</sub>/2 or ground).
- Connect the inverting pin (V<sub>IN</sub>-) to the input pad without touching the guard ring.

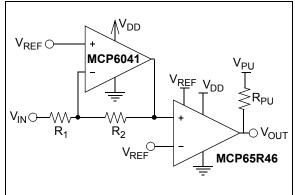
Use the following steps for a non-inverting configuration (Figure 4-4):

- Connect the non-inverting pin (V<sub>IN</sub>+) to the input pad without touching the guard ring.
- 2. Connect the guard ring to the inverting input pin  $(V_{IN}^{-})$ .

## 4.7 Typical Applications

#### 4.7.1 PRECISE COMPARATOR

Some applications require a higher DC precision. A simple way to address this need is using an amplifier (such as the MCP6041 - a 600 nA low power and 14 kHz bandwidth op amp) to gain-up the input signal before it reaches the comparator. Figure 4-10 shows an example of this approach, which also level shifts to  $V_{\rm PLI}$  using the Open-Drain option, the MCP65R46.



**FIGURE 4-10:** Precise Inverting Comparator.

### 4.7.2 BISTABLE MULTI-VIBRATOR

A simple bistable multi-vibrator design is shown in Figure 4-11.  $V_{REF}$  needs to be between ground and the maximum comparator internal  $V_{REF}$  of 2.4V to achieve oscillation. The output duty cycle changes with  $V_{REF}$ .

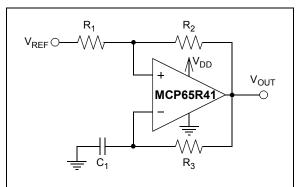
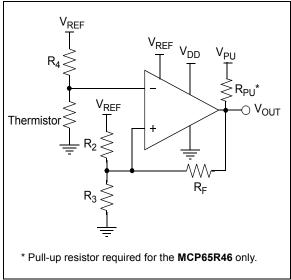


FIGURE 4-11: Bistable Multi-Vibrator.

# 4.7.3 OVER-TEMPERATURE PROTECTION CIRCUIT

The MCP65R41 device can be used as an over-temperature protection circuit using a thermistor. The 2.4V  $V_{REF}$  can be used as stable reference to the thermistor, the alert threshold and hysteresis threshold. This is ideal for battery powered applications, where the change in temperature and output toggle thresholds would remain fixed as battery voltage decays over time.

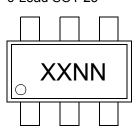


**FIGURE 4-12:** Over-Temperature Alert Circuit.

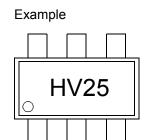
### 5.0 PACKAGING INFORMATION

## 5.1 Package Marking Information





Code
HVNN
HWNN
HXNN
HYNN



**Legend:** XX...X Customer-specific information

Y Year code (last digit of calendar year)
YY Year code (last 2 digits of calendar year)
WW Week code (week of January 1 is week '01')

NNN Alphanumeric traceability code

e3 Pb-free JEDEC designator for Matte Tin (Sn)

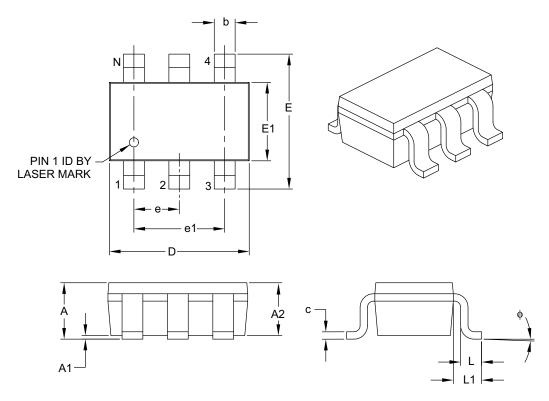
This package is Pb-free. The Pb-free JEDEC designator (e3)

can be found on the outer packaging for this package.

**Note**: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

# 6-Lead Plastic Small Outline Transistor (CHY) [SOT-23]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	MILLIMETERS				
Di	Dimension Limits			MAX	
Number of Pins	N	6			
Pitch	е		0.95 BSC		
Outside Lead Pitch	e1	1.90 BSC			
Overall Height	Α	0.90	_	1.45	
Molded Package Thickness	A2	0.89	_	1.30	
Standoff	A1	0.00	_	0.15	
Overall Width	E	2.20	_	3.20	
Molded Package Width	E1	1.30	_	1.80	
Overall Length	D	2.70	_	3.10	
Foot Length	L	0.10	_	0.60	
Footprint	L1	0.35	_	0.80	
Foot Angle	ф	0°	_	30°	
Lead Thickness	С	0.08	_	0.26	
Lead Width	b	0.20	_	0.51	

### Notes:

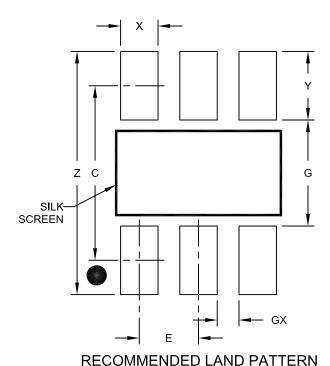
- 1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
- 2. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-028B

# 6-Lead Plastic Small Outline Transistor (CHY) [SOT-23]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



MILLIMETERS Units Dimension Limits MIN NOM MAX Contact Pitch 0.95 BSC Ε Contact Pad Spacing С 2.80 Contact Pad Width (X6) Χ 0.60 Contact Pad Length (X6) Υ 1.10 Distance Between Pads G 1.70 Distance Between Pads GΧ 0.35 Overall Width Z 3.90

### Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2028A

NOTES:

## **APPENDIX A: REVISION HISTORY**

## **Revision B (September 2011)**

The following modification was made to this document: Updated the DC Characteristics table.

# Revision A (December 2010)

Original Release of this Document.

NOTES:

# PRODUCT IDENTIFICATION SYSTEM

 $\underline{\text{To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.}\\$ 

PART NO. X	-XX XX X /XX	Examples:	
Device Tape and	Reference Reference Temperature Package Voltage Tolerance Range	a) MCP65R41T-1202E/CHY:	Push-Pull Output, 1.2VREF, Tape and Reel, 6LD SOT-23 Pkg.
Device:	MCP65R41T: Push-pull Output Comparator MCP65R46T: Open-drain Output Comparator	b) MCP65R41T-2402E/CHY:	Push-Pull Output, 2.4VREF, Tape and Reel, 6LD SOT-23 Pkg.
Reference Voltage:	12 = 1.21V (typical) Initial Reference Voltage 24 = 2.4V (typical) Initial Reference Voltage	c) MCP65R46T-1202E/CHY:	Open-Drain Output, 1.2VREF, Tape and Reel, 6LD SOT-23 Pkg.
Reference Tolerance:	02 = 2% Reference Voltage Tolerance	d) MCP65R46T-2402E/CHY:	Open-Drain Output, 2.4VREF, Tape and Reel, 6LD SOT-23 Pkg.
Temperature Range:	E = -40°C to+125°C(Extended)		522 55 : <b>25</b> F Ng.
Package:	CHY= Plastic Small Outline Transistor, 6-Lead		

NOTES:

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