

# Sound Processor with Built-in 3-band Equalizer

**BD37544FS**

## General Description

BD37544FS is a sound processor with built-in 3-band equalizer for car audio. The functions are stereo input selector (which can switch single and GND isolation), input-gain control, main volume, super bass, 5ch fader volume, LPF/HPF for subwoofer, and mixing input. Moreover, "Advanced switch circuit", which is an original ROHM technology, can reduce various switching noise (ex. No-signal, low frequency like 20Hz & large signal inputs). Also, "Advanced switch" makes control of microcomputer easier, and can construct a high quality car audio system.

## Features

- Reduced switching noise of input gain control, mute, main volume, fader volume, bass, middle, treble, super bass, mixing by using advanced switch circuit.
- Built-in differential input selector that can make various combination of single-ended / differential input.
- Built-in ground isolation amplifier inputs, which is ideal for external stereo input.
- Built-in input gain controller reduces switching noise for volume of a portable audio input.
- Decreased number of external components due to built-in 3-band equalizer filter, LPF for subwoofer, and HPF. It is possible to control Q, G<sub>v</sub>, f<sub>o</sub> of 3-band equalizer and f<sub>c</sub> of LPF/HPF through I<sup>2</sup>C BUS control.
- It is possible to adjust the gain of the bass, middle, and treble up to ±20dB with 1 dB step gain adjustment.
- It is equipped with output terminals for Subwoofer. Moreover, the stereo signal output of the front and rear can also be chosen by the I<sup>2</sup>C BUS control.
- Built-in mixing input and mixing attenuator.
- Energy-saving design resulting in low-current consumption is achieved by utilizing the Bi-CMOS process. It has the advantage in quality over scaling down the power heat control of the internal regulators.
- Input terminals and output terminals are organized and separately laid out to keep the signal flow in one direction which results in simpler and smaller PCB layout.
- It is possible to control the I<sup>2</sup>C BUS by 3.3V / 5V.

## Key Specifications

■ Power Supply Voltage Range:	7.0V to 9.5V
■ Circuit Current (No Signal):	38mA (Typ)
■ Total Harmonic Distortion:	
THD+N1	0.001% (Typ)
THD+N2	0.002% (Typ)
■ Maximum Input Voltage:	2.3Vrms(Typ)
■ Cross-talk Between Selectors:	-100dB(Typ)
■ Volume Control Range:	+15 dB to -79dB
■ Output Noise Voltage:	
V <sub>NO1</sub>	3.8μVrms(Typ)
V <sub>NO2</sub>	4.8μVrms(Typ)
■ Residual Output Noise Voltage:	1.8μVrms(Typ)
■ Operating Temperature Range:	-40°C to +85°C

## Package

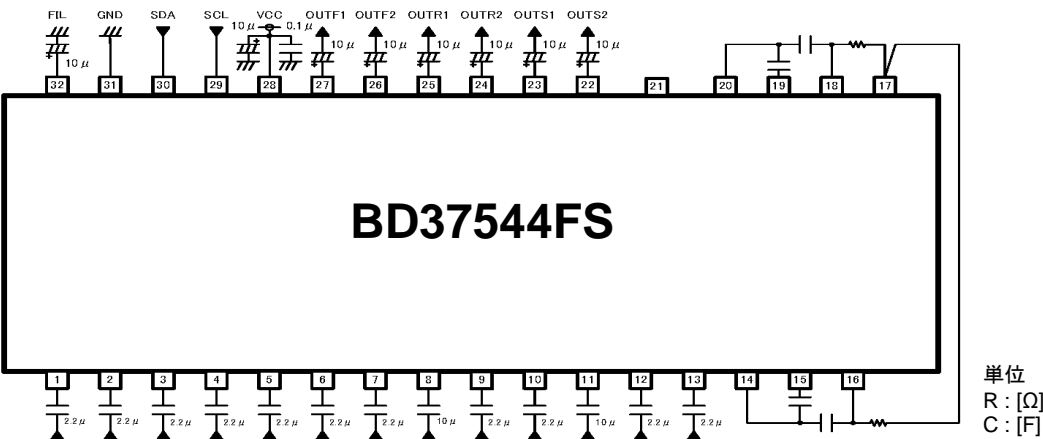
W(Typ) x D(Typ) x H(Max)



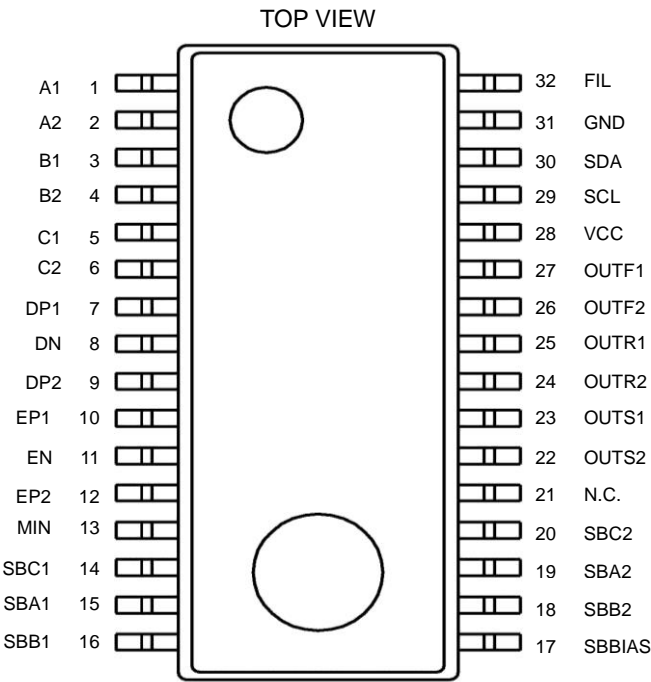
## Applications

It is optimal for car audio systems. It can also be used for audio equipment of mini Compo, micro Compo, TV, etc.

Typical Application Circuit



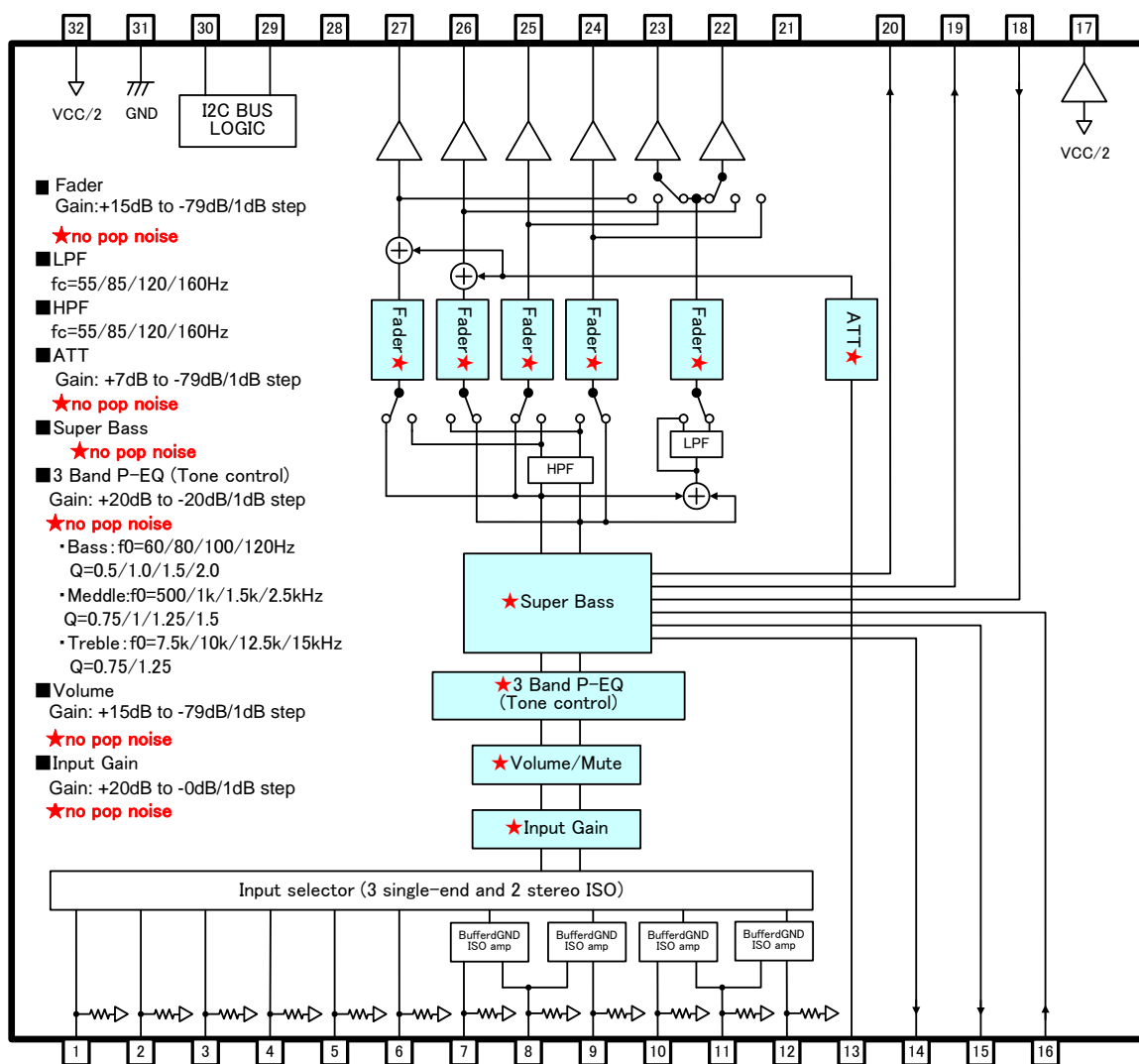
Pin Configuration



Pin Descriptions

Pin No.	Pin Name	Description	Pin No.	Pin Name	Description
1	A1	A input terminal of 1ch	17	SBBIAS	SuperBass bias terminal
2	A2	A input terminal of 2ch	18	SBB2	SuperBass setting terminal of 2ch
3	B1	B input terminal of 1ch	19	SBA2	SuperBass setting terminal of 2ch
4	B2	B input terminal of 2ch	20	SBC2	SuperBass setting terminal of 2ch
5	C1	C input terminal of 1ch	21	N.C.	No connection
6	C2	C input terminal of 2ch	22	OUTS2	Subwoofer output terminal of 2ch
7	DP1	D positive input terminal of 1ch	23	OUTS1	Subwoofer output terminal of 1ch
8	DN	D negative input terminal	24	OUTR2	Rear output terminal of 2ch
9	DP2	D positive input terminal of 2ch	25	OUTR1	Rear output terminal of 1ch
10	EP1	E positive input terminal of 1ch	26	OUTF2	Front output terminal of 2ch
11	EN	E negative input terminal	27	OUTF1	Front output terminal of 1ch
12	EP2	E positive input terminal of 2ch	28	VCC	Power supply terminal
13	MIN	Mixing input terminal	29	SCL	I <sup>2</sup> C Communication clock terminal
14	SBC1	SuperBass setting terminal of 1ch	30	SDA	I <sup>2</sup> C Communication data terminal
15	SBA1	SuperBass setting terminal of 1ch	31	GND	GND terminal
16	SBB1	SuperBass setting terminal of 1ch	32	FIL	VCC/2 terminal

## Block Diagram



## Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Rating	Unit
Power Supply Voltage	V <sub>CC</sub>	10.0	V
Input Voltage	V <sub>IN</sub>	V <sub>CC</sub> +0.3 to GND-0.3	V
Power Dissipation	P <sub>d</sub>	0.95 (Note 1)	W
Storage Temperature	T <sub>stg</sub>	-55 to +150	°C

(Note 1) When mounted on the standard board (70 x 70 x 1.6 mm<sup>3</sup>), derate by 7.6mW/°C for Ta above 25°C.

Thermal resistance  $\theta_{ja}$  = 131.6(°C/W)

Material : A FR4 glass epoxy board(3% or less of copper foil area)

**Caution:** Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

## Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	V <sub>CC</sub>	7.0	-	9.5	V
Temperature	T <sub>opr</sub>	-40	-	+85	°C

## Electrical Characteristics

(Unless specified, Ta=25°C, V<sub>CC</sub>=8.5V, f=1kHz, V<sub>IN</sub>=1Vrms, R<sub>g</sub>=600Ω, R<sub>L</sub>=10kΩ, A1 input, Input gain 0dB, Mute OFF, Volume 0dB, Tone control 0dB, Loudness 0dB, LPF OFF, HPF OFF, Mixing OFF, Fader 0dB)

BLOCK	Parameter	Symbol	Limit			Unit	Conditions
			Min	Typ	Max		
GENERAL	Circuit Current (No Signal)	I <sub>Q</sub>	-	38	48	mA	No signal
	Voltage Gain	G <sub>V</sub>	-1.5	0	+1.5	dB	G <sub>V</sub> =20log(V <sub>OUT</sub> /V <sub>IN</sub> )
	Channel Balance	CB	-1.5	0	+1.5	dB	CB = G <sub>V1</sub> -G <sub>V2</sub>
	Total Harmonic Distortion 1 (FRONT,REAR)	THD+N1	-	0.001	0.05	%	V <sub>OUT</sub> =1Vrms BW=400Hz-30KHz
	Total Harmonic Distortion 2 (SUBWOOFER)	THD+N2	-	0.002	0.05	%	V <sub>OUT</sub> =1Vrms BW=400Hz-30KHz
	Output Noise Voltage 1 (FRONT,REAR) *	V <sub>NO1</sub>	-	3.8	15	μVrms	R <sub>g</sub> = 0Ω BW = IHF-A
	Output Noise Voltage 2 (SUBWOOFER) *	V <sub>NO2</sub>	-	4.8	15	μVrms	R <sub>g</sub> = 0Ω BW = IHF-A
	Residual Output Noise Voltage*	V <sub>NOR</sub>	-	1.8	10	μVrms	Fader = -∞dB R <sub>g</sub> = 0Ω BW = IHF-A
	Cross-talk Between Channels *	CTC	-	-100	-90	dB	R <sub>g</sub> = 0Ω CTC=20log(V <sub>OUT</sub> /V <sub>IN</sub> ) BW = IHF-A
	Ripple Rejection	RR	-	-70	-40	dB	f=1kHz V <sub>RR</sub> =100mVrms RR=20log(V <sub>CC</sub> IN/V <sub>OUT</sub> )
INPUT SELECTOR	Input Impedance(A, B,C)	R <sub>IN_S</sub>	70	100	130	kΩ	
	Input Impedance(D, E)	R <sub>IN_D</sub>	175	250	325	kΩ	
	Maximum Input Voltage	V <sub>IM</sub>	2.1	2.3	-	Vrms	V <sub>IM</sub> at THD+N(V <sub>OUT</sub> )=1 % BW=400Hz-30KHz
	Cross-talk Between Selectors *	CTS	-	-100	-90	dB	R <sub>g</sub> = 0Ω CTS=20log(V <sub>OUT</sub> /V <sub>IN</sub> ) BW = IHF-A
	Common Mode Rejection Ratio*	CMRR	50	65	-	dB	XP1 and XN input XP2 and XN input CMRR=20log(V <sub>IN</sub> /V <sub>OUT</sub> ) BW = IHF-A,[*X...D,E]

## Electrical Characteristics - continued

BLOCK	Parameter	Symbol	Limit			Unit	Conditions
			Min	Typ	Max		
INPUT GAIN	Minimum Input Gain	$G_{IN\_MIN}$	-2	0	+2	dB	Input gain 0dB $V_{IN}=100mV_{rms}$ $G_{IN}=20\log(V_{OUT}/V_{IN})$
	Maximum Input Gain	$G_{IN\_MAX}$	18	20	22	dB	Input gain 20dB $V_{IN}=100mV_{rms}$ $G_{IN}=20\log(V_{OUT}/V_{IN})$
	Gain Set Error	$G_{IN\_ERR}$	-2	0	+2	dB	GAIN=+20dB to +1dB
MUTE	Mute Attenuation *	$G_{MUTE}$	-	-105	-85	dB	Mute ON $G_{MUTE}=20\log(V_{OUT}/V_{IN})$ BW = IHF-A
VOLUME	Maximum Gain	$G_V\_MAX$	13	15	17	dB	Volume = 15dB $V_{IN}=100mV_{rms}$ $G_V=20\log(V_{OUT}/V_{IN})$
	Maximum Attenuation *	$G_V\_MIN$	-	-100	-85	dB	Volume = -∞dB $G_V=20\log(V_{OUT}/V_{IN})$ BW = IHF-A
	Attenuation Set Error 1	$G_V\_ERR1$	-2	0	+2	dB	GAIN & ATT=+15dB to -15dB
	Attenuation Set Error 2	$G_V\_ERR2$	-3	0	+3	dB	ATT=-16dB to -47dB
	Attenuation Set Error 3	$G_V\_ERR3$	-4	0	+4	dB	ATT=-48dB to -79dB
BASS	Maximum Boost Gain	$G_B\_BST$	18	20	22	dB	Gain=+20dB f=100Hz $V_{IN}=100mV_{rms}$ $G_B=20\log(V_{OUT}/V_{IN})$
	Maximum Cut Gain	$G_B\_CUT$	-22	-20	-18	dB	Gain=-20dB f=100Hz $V_{IN}=2V_{rms}$ $G_B=20\log(V_{OUT}/V_{IN})$
	Gain Set Error	$G_B\_ERR$	-2	0	+2	dB	Gain=-20dB to +20dB f=100Hz
MIDDLE	Maximum Boost Gain	$G_M\_BST$	18	20	22	dB	Gain=+20dB f=1kHz $V_{IN}=100mV_{rms}$ $G_M=20\log(V_{OUT}/V_{IN})$
	Maximum Cut Gain	$G_M\_CUT$	-22	-20	-18	dB	Gain=-20dB f=1kHz $V_{IN}=2V_{rms}$ $G_M=20\log(V_{OUT}/V_{IN})$
	Gain Set Error	$G_M\_ERR$	-2	0	+2	dB	Gain=-20dB to +20dB f=1kHz
TREBLE	Maximum Boost Gain	$G_T\_BST$	18	20	22	dB	Gain=+20dB f=10kHz $V_{IN}=100mV_{rms}$ $G_T=20\log(V_{OUT}/V_{IN})$
	Maximum Cut Gain	$G_T\_CUT$	-22	-20	-18	dB	Gain=-20dB f=10kHz $V_{IN}=2V_{rms}$ $G_T=20\log(V_{OUT}/V_{IN})$
	Gain Set Error	$G_T\_ERR$	-2	0	+2	dB	Gain=-20dB to +20dB f=10kHz
MIXING	Input Impedance	$R_{IN\_M}$	19	27	35	kΩ	
	Maximum Input Voltage	$V_{IM\_M}$	2.0	2.2	-	Vrms	$V_{IM}$ at THD+N( $V_{OUT}$ )=1 % BW=400Hz-30KHz
	Maximum Attenuation *	$G_{MX\_MIN}$	-	-100	-85	dB	MIX=OFF $G_{MX}=20\log(V_{OUT}/V_{IN})$ BW=INF-A
	Maximum Gain	$G_{MX\_MAX}$	5	7	9	dB	ATT=+7dB $G_{MX}=20\log(V_{OUT}/V_{IN})$

## Electrical Characteristics - continued

BLOCK	Parameter	Symbol	Limit			Unit	Conditions
			Min	Typ	Max		
FADER / SUBWOOFER	Maximum Boost Gain	$G_{F\_BST}$	13	15	17	dB	Fader=15dB $V_{IN}=100mV_{rms}$ $G_F=20\log(V_{OUT}/V_{IN})$
	Maximum Attenuation *	$G_{F\_MIN}$	-	-100	-90	dB	Fader = $-\infty$ dB $G_F=20\log(V_{OUT}/V_{IN})$ BW = IHF-A
	Gain Set Error	$G_{F\_ERR}$	-2	0	+2	dB	GAIN=+1dB to +15dB
	Attenuation Set Error 1	$G_{F\_ERR1}$	-2	0	+2	dB	ATT=-1dB to -15dB
	Attenuation Set Error 2	$G_{F\_ERR2}$	-3	0	+3	dB	ATT=-16dB to -47dB
	Attenuation Set Error 3	$G_{F\_ERR3}$	-4	0	+4	dB	ATT=-48dB to -79dB
	Output Impedance	$R_{OUT}$	-	-	50	$\Omega$	$V_{IN}=100mV_{rms}$
	Maximum Output Voltage	$V_{OM}$	2	2.2	-	Vrms	THD+N=1 % BW=400Hz-30KHz

VP-9690A(Average value detection, effective value display) filter by Matsushita Communication is used for \* measurement.  
Phase between input / output is same.

## Typical Performance Curves

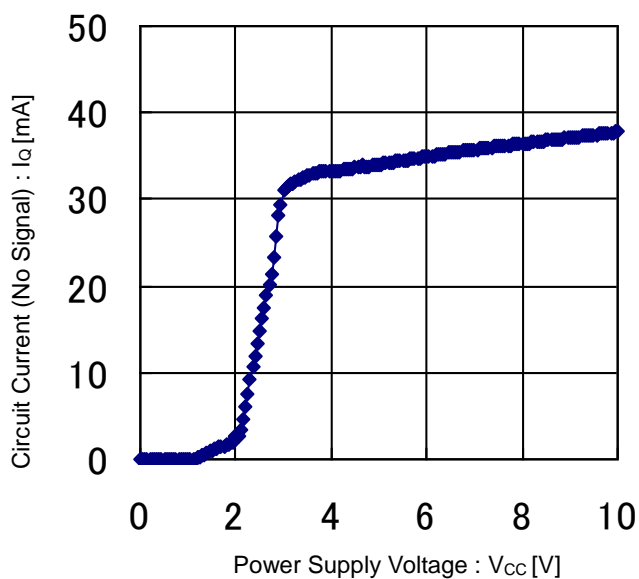


Figure 1. Circuit Current (No Signal) vs Power Supply Voltage

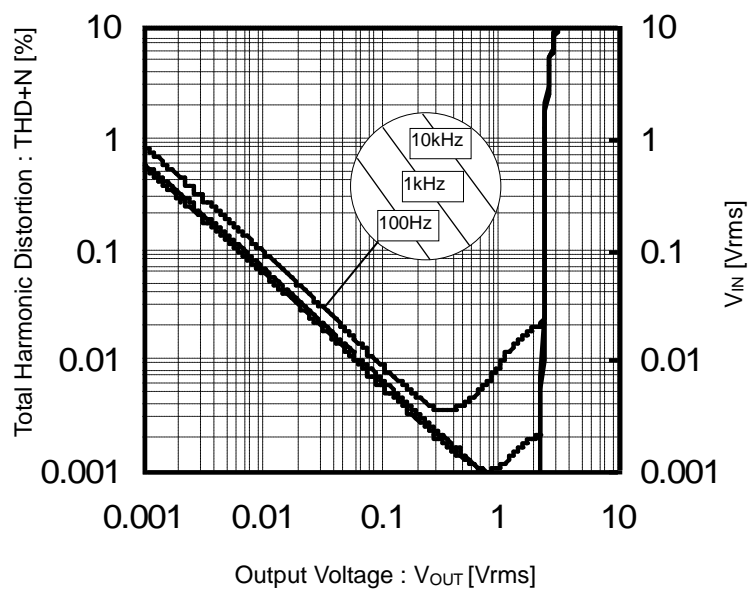


Figure 2. Total Harmonic Distortion vs Output Voltage

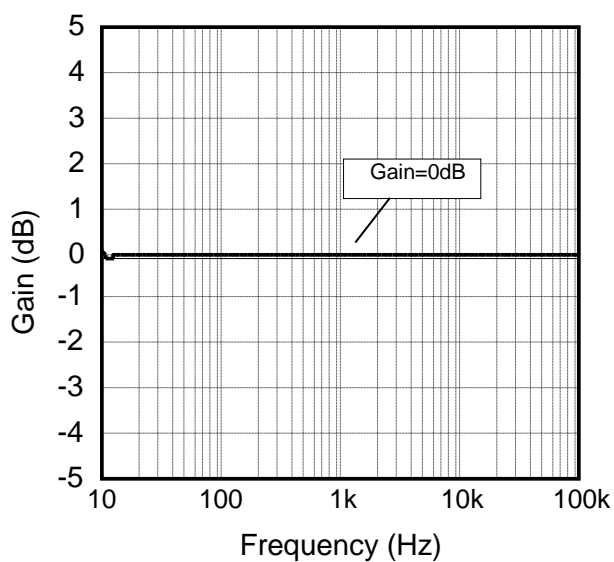


Figure 3. Gain vs Frequency

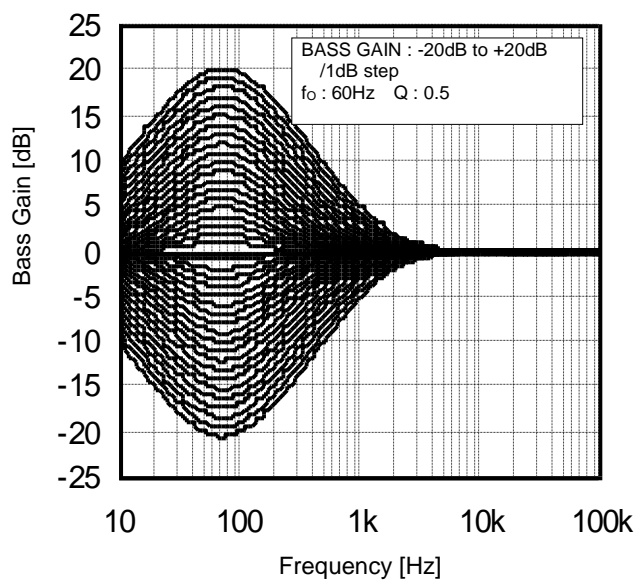


Figure 4. Bass Gain vs Frequency

## Typical Performance Curves – continued

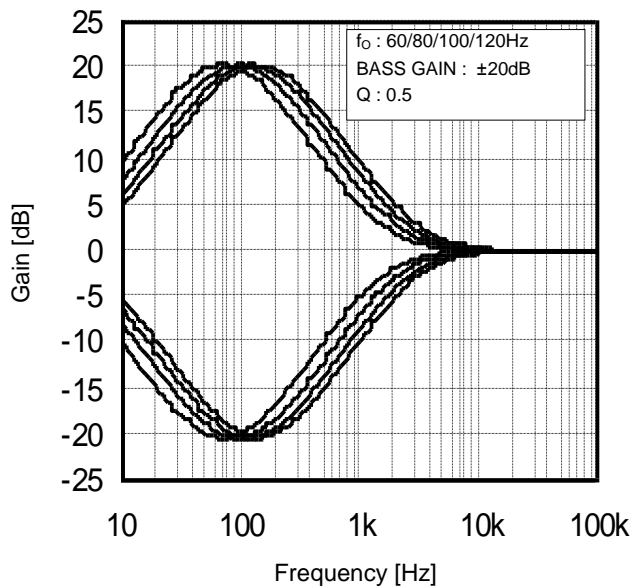
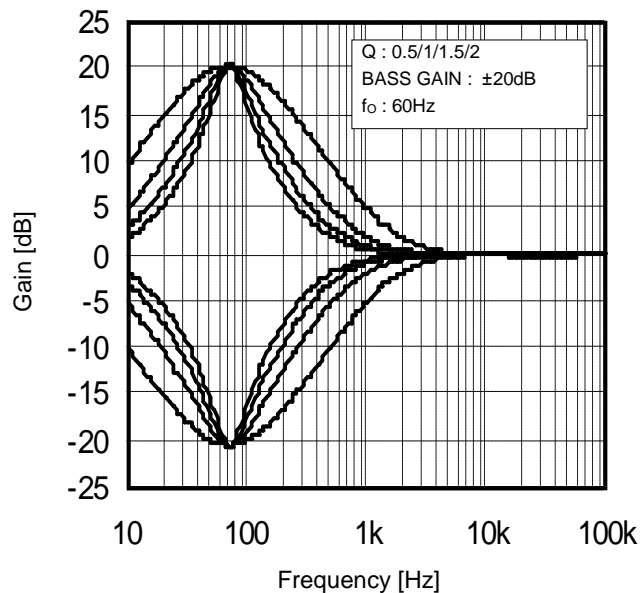
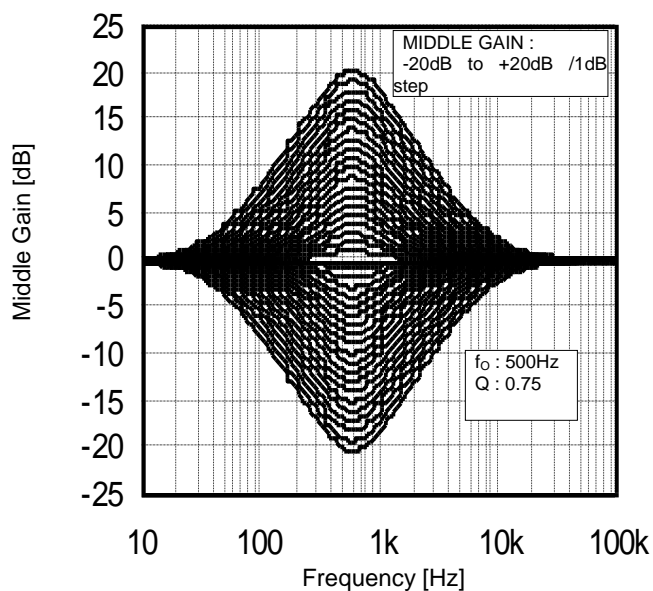
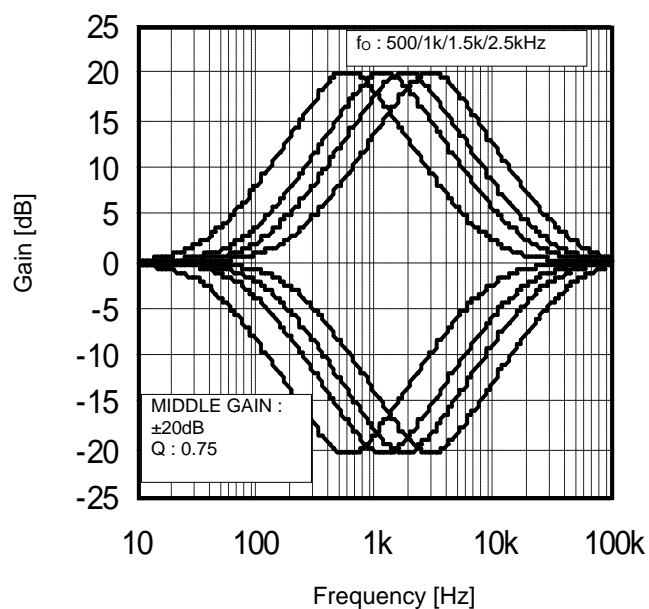
Figure 5. Bass  $f_0$  vs FrequencyFigure 6. Bass  $Q$  vs Frequency

Figure 7. Middle Gain vs Frequency

Figure 8. Middle  $f_0$  vs Frequency

## Typical Performance Curves – continued

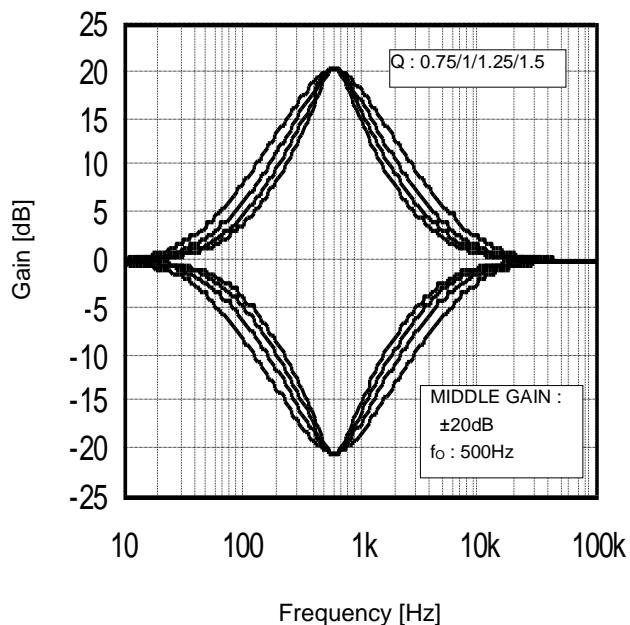


Figure 9. Middle Q vs Frequency

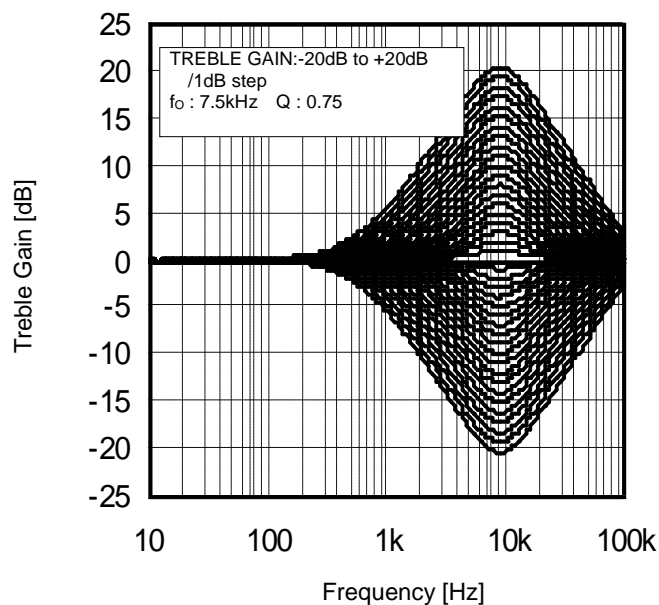


Figure 10. Treble Gain vs Frequency

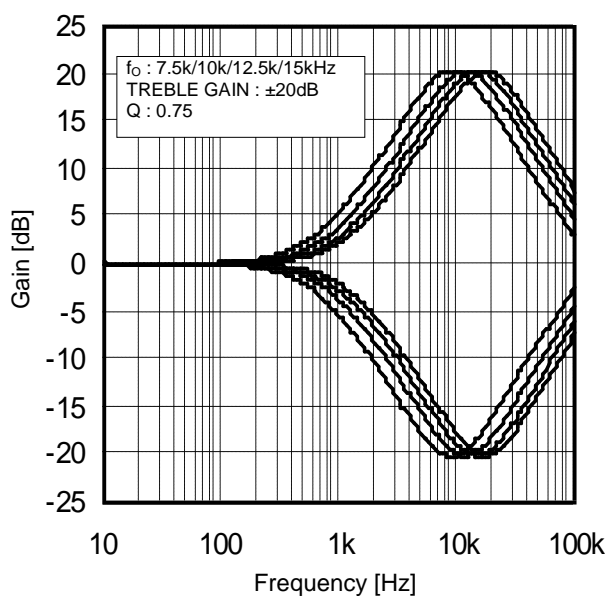


Figure 11. Treble fo vs Frequency

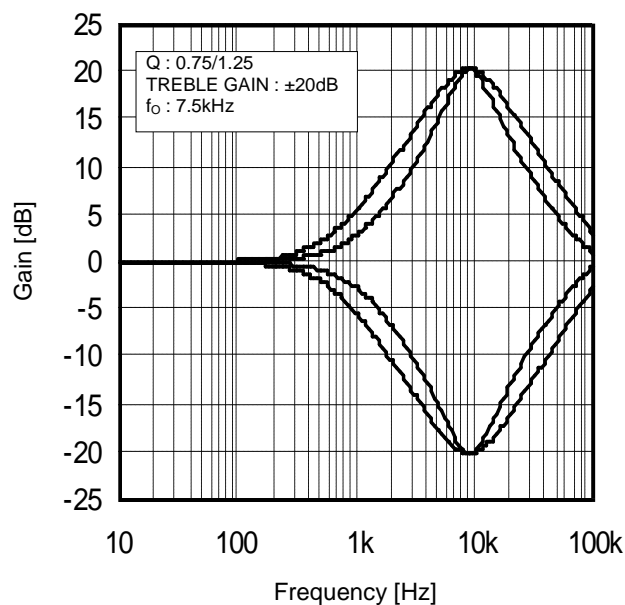


Figure 12. Treble Q vs Frequency

## Typical Performance Curves – continued

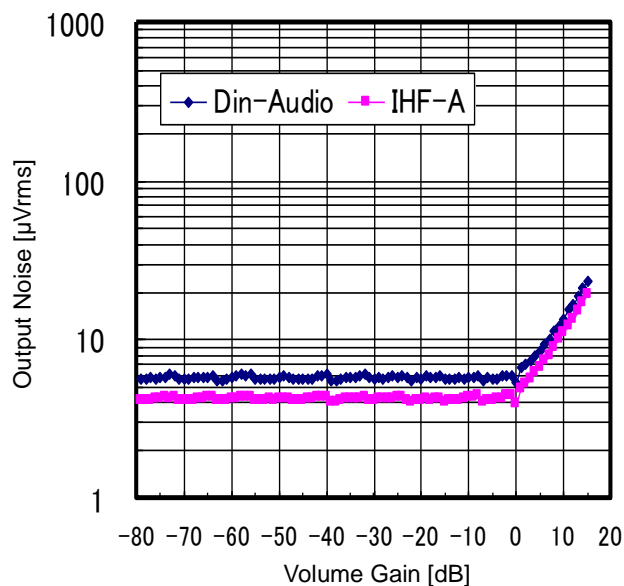


Figure 13. Output Noise vs Volume Gain

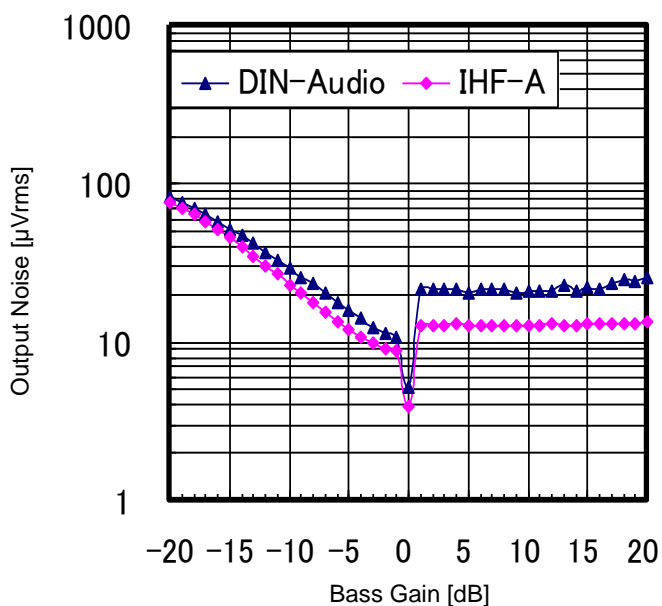


Figure 14. Output Noise vs Bass Gain

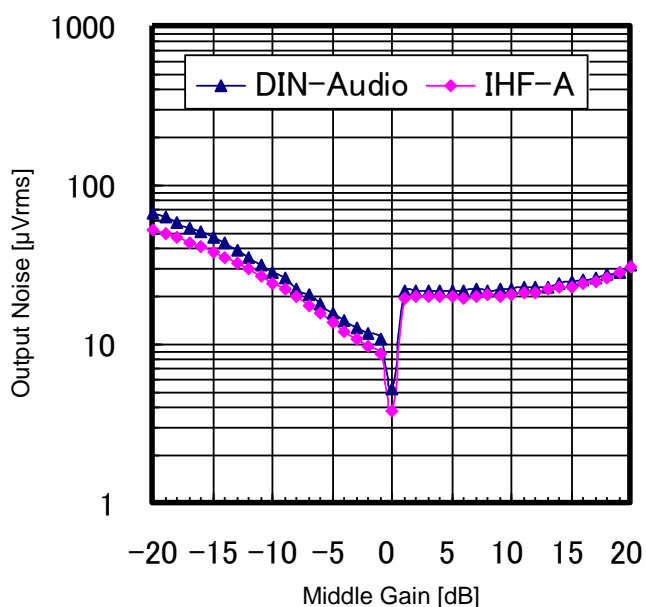


Figure 15. Output Noise vs Middle Gain

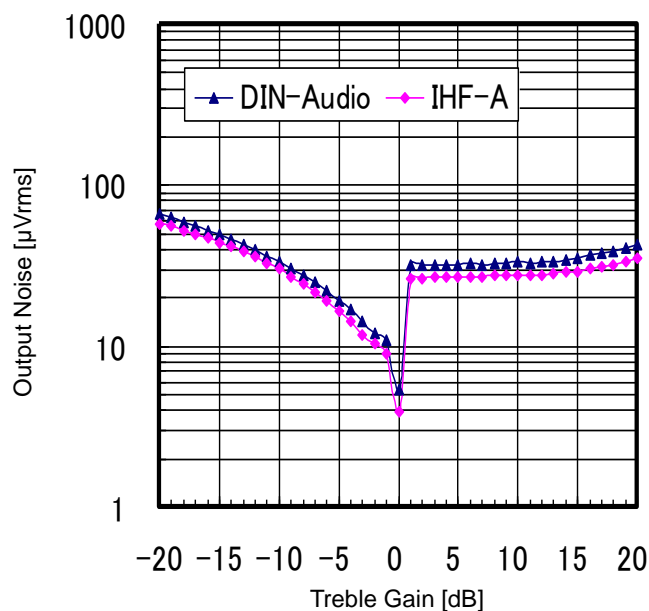


Figure 16. Output Noise vs Treble Gain

Typical Performance Curves – continued

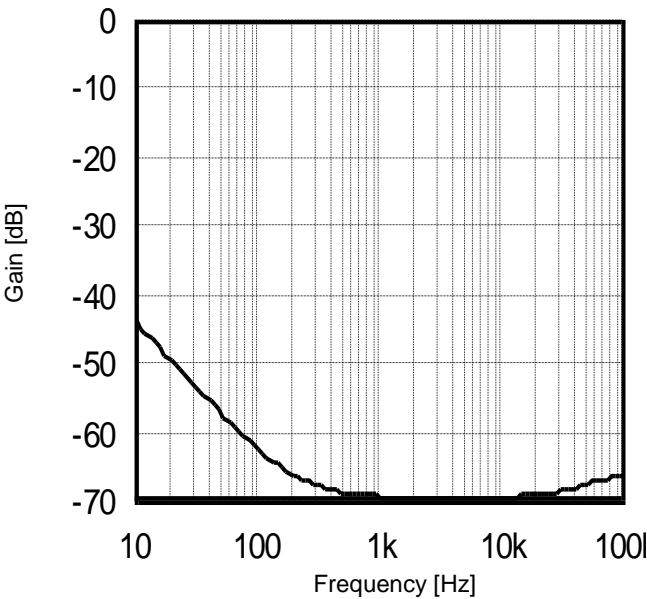


Figure 17. CMRR vs Frequency

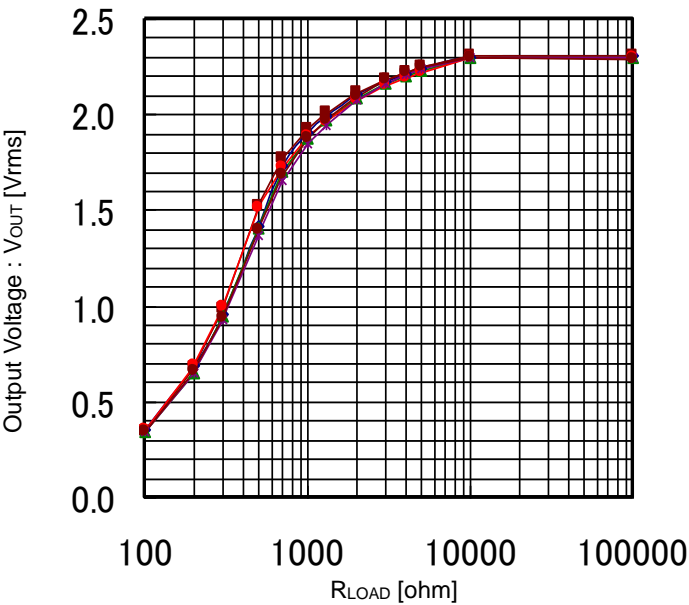


Figure 18. Output Voltage vs R\_LOAD

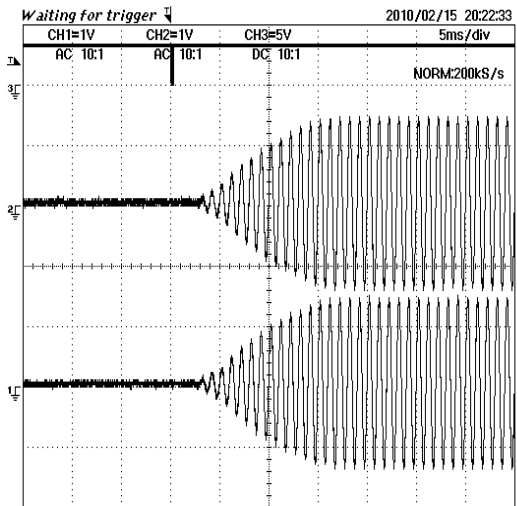


Figure 19. Advanced Switch 1

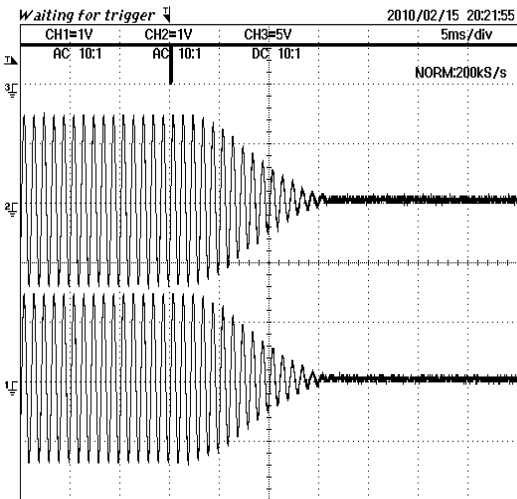


Figure 20. Advanced Switch 2

## Timing Chart

### CONTROL SIGNAL SPECIFICATION

#### (1) Electrical Specifications and Timing for Bus Lines and I/O Stages

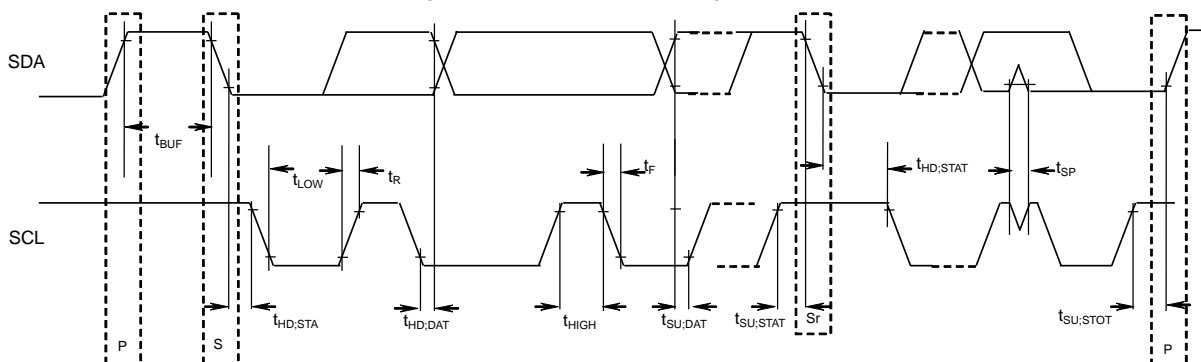


Figure 21. I²C-bus Signal Timing Diagram

Table 1 Characteristics of the SDA and SCL bus lines for I²C-bus devices (Ta=25°C, VCC=8.5V)

	Parameter	Symbol	Fast-mode I²C-bus		Unit
			Min	Max	
1	SCL clock frequency	f <sub>SCL</sub>	0	400	kHz
2	Bus free time between a STOP and START condition	t <sub>BUF</sub>	1.3	-	μs
3	Hold time (repeated) START condition. After this period, the first clock pulse is generated	t <sub>HD,STA</sub>	0.6	-	μs
4	LOW period of the SCL clock	t <sub>LOW</sub>	1.3	-	μs
5	HIGH period of the SCL clock	t <sub>HIGH</sub>	0.6	-	μs
6	Set-up time for a repeated START condition	t <sub>SU,STA</sub>	0.6	-	μs
7	Data hold time:	t <sub>HD,DAT</sub>	0.06 (Note)	-	μs
8	Data set-up time	t <sub>SU,DAT</sub>	120	-	ns
9	Set-up time for STOP condition	t <sub>SU,STO</sub>	0.6	-	μs

All values refer to VIH Min and VIL Max Levels (see Table 2).

(Note) A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the VIH Min of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.

For 7(t<sub>HD,DAT</sub>), 8(t<sub>SU,DAT</sub>), make the setup in which the margin is full.

Table 2 Characteristics of the SDA and SCL I/O stages for I²C-bus devices

	Parameter	Symbol	Fast-mode devices		Unit
			Min	Max	
10	LOW level input voltage:	V <sub>IL</sub>	-0.3	+1	V
11	HIGH level input voltage:	V <sub>IH</sub>	2.3	5	V
12	Pulse width of spikes which must be suppressed by the input filter.	t <sub>SP</sub>	0	50	ns
13	LOW level output voltage: at 3mA sink current	V <sub>OL1</sub>	0	0.4	V
14	Input current each I/O pin with an input voltage between 0.4V and 4.5V.	I <sub>I</sub>	-10	+10	μA

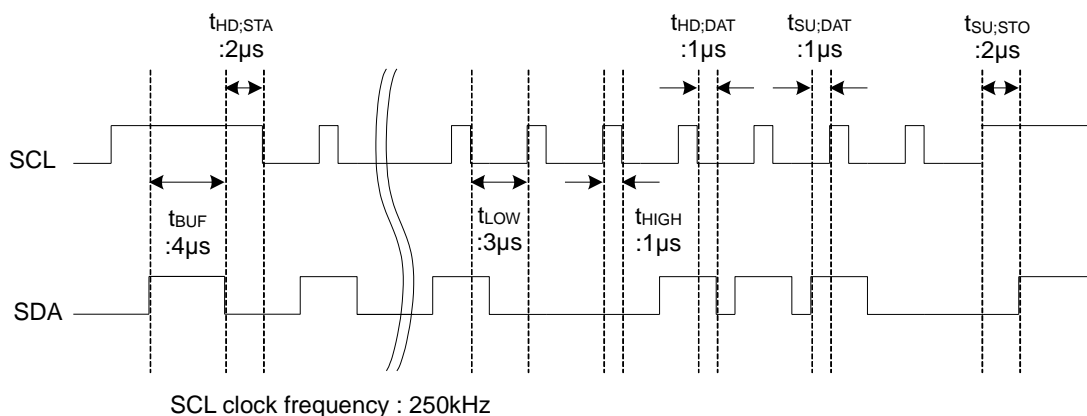


Figure 22. A Command Timing Example in the I²C Data Transmission

(2) I<sup>2</sup>C BUS FORMAT

MSB	LSB	MSB	LSB	MSB	LSB		
S	Slave Address	A	Select Address	A	Data	A	P
1bit	8bit	1bit	8bit	1bit	8bit	1bit	1bit

S = Start condition (Recognition of start bit)

Slave Address = Recognition of slave address. The first 7 bits correspond to the slave address. The least significant bit is "L" which corresponds to write mode.

A = ACKNOWLEDGE bit (Recognition of acknowledgement)

Select Address = Select address corresponding to volume, bass or treble.

Data = Data on every volume and tone.

P = Stop condition (Recognition of stop bit)

(3) I<sup>2</sup>C BUS Interface Protocol

## (a) Basic Format

MSB	LSB	MSB	LSB	MSB	LSB		
S	Slave Address	A	Select Address	A	Data	A	P

## (b) Automatic Increment (Select Address increases (+1) according to the number of data.)

S	Slave Address	A	Select Address	A	Data1	A	Data2	A	...	DataN	A	P			
MSB		LSB		MSB		LSB		MSB		LSB		MSB		LSB	

(Example)

① Data1 shall be set as data of address specified by Select Address.

② Data2 shall be set as data of address specified by Select Address +1.

③ DataN shall be set as data of address specified by Select Address +N-1.

## (c) Configuration Unavailable for Transmission (In this case, only Select Address1 is set.)

MSB	LSB	MSB	LSB	MSB	LSB	MSB	LSB	MSB	LSB	MSB	LSB
S	Slave Address	A	Select Address1	A	Data	A	Select Address 2	A	Data	A	P

(Note) If any data is transmitted as Select Address 2 next to data, it is recognized as data, not as Select Address 2.

(4) Slave Address

MSB							LSB	
A6	A5	A4	A3	A2	A1	A0	R/W	
1	0	0	0	0	0	0	0	80H

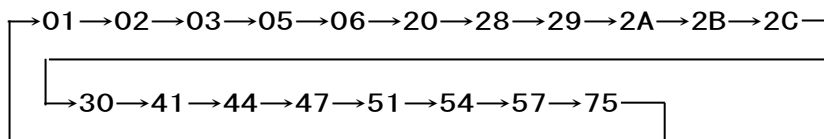
(5) Select Address & Data

Items	Select Address (hex)	MSB		Data						LSB	
		D7	D6	D5	D4	D3	D2	D1	D0		
Initial setup 1	01	Advanced switch ON/OFF	0	Advanced switch time of Input Gain/Volume Tone/Fader/Super Bass Mixing		0	1	Advanced switch time of Mute			
Initial setup 2	02	LPF Phase	0	Subwoofer Output Select		0	Subwoofer LPF f <sub>c</sub>				
Initial setup 3	03	Front HPF Pass	Rear HPF Pass	Front / Rear HPF f <sub>c</sub>			0	1	0		
Input Selector	05	Full-diff Type	0	0	Input selector						
Input gain	06	Mute ON/OFF	0	0	Input Gain						
Volume gain	20	Volume Gain / Attenuation									
Fader 1ch Front	28	Fader Gain / Attenuation									
Fader 2ch Front	29	Fader Gain / Attenuation									
Fader 1ch Rear	2A	Fader Gain / Attenuation									
Fader 2ch Rear	2B	Fader Gain / Attenuation									
Fader Subwoofer	2C	Fader Gain / Attenuation									
Mixing	30	Mixing Gain / Attenuation									
Bass setup	41	0	0	Bass f <sub>0</sub>		0	0	Bass Q			
Middle setup	44	0	0	Middle f <sub>0</sub>		0	0	Middle Q			
Treble setup	47	0	0	Treble f <sub>0</sub>		0	0	0	Treble Q		
Bass gain	51	Bass Boost/Cut	0	0	Bass Gain						
Middle gain	54	Middle Boost/Cut	0	0	Middle Gain						
Treble gain	57	Treble Boost/Cut	0	0	Treble Gain						
Super Bass Gain	75	0	0	0	Super Bass Gain						
System Reset	FE	1	0	0	0	0	0	0	1		

 Advanced switch

## Note

1. The Advanced Switch works in the latch part while changing from one function to another.
2. Upon continuous data transfer, the Select Address rolls over because of the automatic increment function, as shown below.



3. Advanced switch is not used for the function of input selector and subwoofer output select, etc. Therefore, please apply mute on the side when changing these settings.
4. When using mute function of this IC at the time of changing input selector, please switch mute ON/OFF for waiting advanced-mute time.

Select address 01 (hex)

Time	Advanced switch time of Mute							LSB
	D7	D6	D5	D4	D3	D2	D1	D0
0.6msec	Advanced Switch ON/OFF	0	Advanced switch time of Input gain/Volume Tone/Fader/Super Bass/Mixing		0	1	0	0
1.0msec							0	1
1.4msec							1	0
3.2msec							1	1

Time	Advanced switch time of Input gain/Volume/Tone/Fader/Super Bass/Mixing							LSB
	D7	D6	D5	D4	D3	D2	D1	D0
4.7 msec	Advanced Switch ON/OFF	0	0	0	0	1	Advanced switch Time of Mute	
7.1 msec			0	1				
11.2 msec			1	0				
14.4 msec			1	1				

Mode	Advanced switch ON/OFF							LSB
	D7	D6	D5	D4	D3	D2	D1	D0
OFF	0	0	Advanced switch time of Input gain/Volume Tone/Fader/Super Bass/Mixing		0	1	Advanced switch Time of Mute	
ON	1							

Select address 02(hex)

Subwoofer LPF f <sub>c</sub>								
f <sub>c</sub>	MSB						LSB	
	D7	D6	D5	D4	D3	D2	D1	D0
OFF	LPF Phase	0	Subwoofer Output Select		0	0	0	0
55Hz						0	0	1
85Hz						0	1	0
120Hz						0	1	1
160Hz						1	0	0
Prohibition	Other setting							

Mode	Subwoofer Output Select							LSB
	D7	D6	D5	D4	D3	D2	D1	D0
LPF	LPF Phase	0	0	0	0	Subwoofer LPF f <sub>c</sub>		
Front			0	1				
Rear			1	0				
Prohibition			1	1				

Phase	LPF Phase							LSB
	D7	D6	D5	D4	D3	D2	D1	D0
0°	0	0	Subwoofer output select		0	Subwoofer LPF f <sub>c</sub>		
180°	1							

 : Initial condition

Select address 03(hex)

Mode	MSBFront/Rear HPF f <sub>c</sub> LSB							
	D7	D6	D5	D4	D3	D2	D1	D0
55Hz	Front HPF Pass	Rear HPF Pass	0	0	0	0	1	0
85Hz			0	0	1			
120Hz			1	1	0			
160Hz			0	1	0			
Prohibition			Other setting					

Mode	Rear HPF							
	D7	D6	D5	D4	D3	D2	D1	D0
pass	Front HPF Pass	0	Front/Rear HPF f <sub>c</sub>			0	1	0
NOT pass	Pass	1						

Mode	Front HPF							
	D7	D6	D5	D4	D3	D2	D1	D0
pass	0	Rear HPF Pass	Front/Rear HPF f <sub>c</sub>			0	1	0
NOT pass	1							

Select address 05(hex)

Mode	MSB		Input Selector					LSB					
	OUTF1	OUTF2	D7	D6	D5	D4	D3	D2	D1	D0			
A	A1	A2	Full-diff bias type select	0	0	0	0	0	0	0			
B	B1	B2				0	0	0	0	1			
C	C1	C2				0	0	0	1	0			
D single	DP1	DP2				0	0	0	1	1			
E single	EP1	EP2				0	0	1	0	0			
A diff	A1	B1				0	1	1	1	1			
C diff	B2	C2				1	0	0	0	0			
D diff	DP1	DP2				0	0	1	1	0			
E diff	EP1	EP2				0	0	1	1	1			
Input SHORT									0	1	0	0	1
Prohibition									Other setting				

**Input SHORT** : The input impedance of each input terminal is lowered from 100kΩ(Typ) to 6 kΩ(Typ).  
(For quick charge of coupling capacitor)

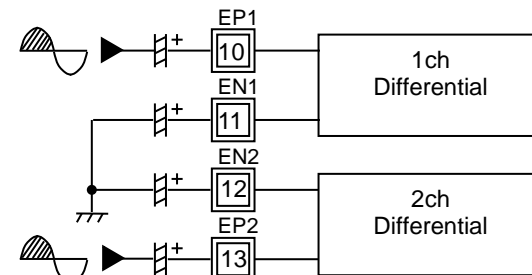
 : Initial condition

Select address 05(hex)

Mode	Full-diff Bias Type Select							LSB
	D7	D6	D5	D4	D3	D2	D1	D0
Negative Input	0	0	0	Input Selector				
Bias	1							

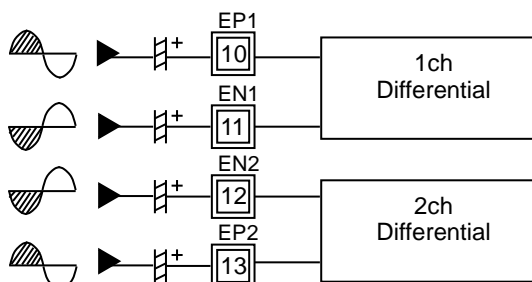
Negative input type

For Ground –isolation type.

1ch  
1ch signal input2ch  
2ch signal input

Bias type

For differential amplifier type

1ch  
1ch signal input2ch  
2ch signal input

Select address 06 (hex)

Select address 00 (hex)								
Gain	MSB			Input Gain				LSB
	D7	D6	D5	D4	D3	D2	D1	D0
0dB	Mute ON/OFF	0	0	0	0	0	0	0
1dB				0	0	0	0	1
2dB				0	0	0	1	0
3dB				0	0	0	1	1
4dB				0	0	1	0	0
5dB				0	0	1	0	1
6dB				0	0	1	1	0
7dB				0	0	1	1	1
8dB				0	1	0	0	0
9dB				0	1	0	0	1
10dB				0	1	0	1	0
11dB				0	1	0	1	1
12dB				0	1	1	0	0
13dB				0	1	1	0	1
14dB				0	1	1	1	0
15dB				0	1	1	1	1
16dB				1	0	0	0	0
17dB				1	0	0	0	1
18dB				1	0	0	1	0
19dB				1	0	0	1	1
20dB	1	0	1	0	0			
Prohibition				1	1	0	1	1
				:	:	:	:	:
				1	1	1	1	1

 : Initial condition

Select address 06 (hex)

Mode	Mute ON/OFF							
	D7	D6	D5	D4	D3	D2	D1	D0
OFF	0	0	0	Input Gain				
ON	1							

Select address 20, 28, 29, 2A, 2B, 2C (hex)

Gain & ATT	Vol, Fader Gain / Attenuation							
	D7	D6	D5	D4	D3	D2	D1	D0
Prohibition	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	1
	:	:	:	:	:	:	:	:
	0	1	1	1	0	0	0	0
15dB	0	1	1	1	0	0	0	1
14dB	0	1	1	1	0	0	1	0
13dB	0	1	1	1	0	0	1	1
:	:	:	:	:	:	:	:	:
-77dB	1	1	0	0	1	1	0	1
-78dB	1	1	0	0	1	1	1	0
-79dB	1	1	0	0	1	1	1	1
Prohibition	1	1	0	1	0	0	0	0
	:	:	:	:	:	:	:	:
	1	1	1	1	1	1	1	0
-∞dB	1	1	1	1	1	1	1	1

Select address 30(hex)

Gain & ATT	Mixing Gain / Attenuation							
	D7	D6	D5	D4	D3	D2	D1	D0
Prohibition	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	1
	:	:	:	:	:	:	:	:
	0	1	1	1	1	0	0	0
7dB	0	1	1	1	1	0	0	1
6dB	0	1	1	1	1	0	1	0
5dB	0	1	1	1	1	0	1	1
:	:	:	:	:	:	:	:	:
-77dB	1	1	0	0	1	1	0	1
-78dB	1	1	0	0	1	1	1	0
-79dB	1	1	0	0	1	1	1	1
Prohibition	1	1	0	1	0	0	0	0
	:	:	:	:	:	:	:	:
	1	1	1	1	1	1	1	0
MIX OFF	1	1	1	1	1	1	1	1

(Note) See the precaution on P30 together, too.

 : Initial condition

Select address 41(hex)

Q factor	MSB		Bass		Q factor		LSB	
	D7	D6	D5	D4	D3	D2	D1	D0
0.5	0	0	Bass fo		0	0	0	0
1.0							0	1
1.5							1	0
2.0							1	1

fo	MSB		Bass		fo		LSB	
	D7	D6	D5	D4	D3	D2	D1	D0
60Hz	0	0	0	0	0	0	Bass Q factor	
80Hz			0	1				
100Hz			1	0				
120Hz			1	1				

Select address 44(hex)

Q factor	MSB		Middle		Q factor		LSB	
	D7	D6	D5	D4	D3	D2	D1	D0
0.75	0	0	Middle fo		0	0	0	0
1.0							0	1
1.25							1	0
1.5							1	1

fo	MSB		Middle		fo		LSB	
	D7	D6	D5	D4	D3	D2	D1	D0
500Hz	0	0	0	0	0	0	Middle Q factor	
1kHz			0	1				
1.5kHz			1	0				
2.5kHz			1	1				

Select address 47 (hex)

Q factor	MSB		Treble		Q factor		LSB	
	D7	D6	D5	D4	D3	D2	D1	D0
0.75	0	0	Treble fo		0	0	0	0
1.25								1


fo	MSB		Treble		fo		LSB	
	D7	D6	D5	D4	D3	D2	D1	D0
7.5kHz	0	0	0	0	0	0	0	Treble Q factor
10kHz			0	1				
12.5kHz			1	0				
15kHz			1	1				

 : Initial condition

Select address 51, 54, 57 (hex)

Gain	MSB		Bass/Middle/Treble Gain					LSB
	D7	D6	D5	D4	D3	D2	D1	D0
0dB	Bass/ Middle/ Treble Boost /cut	0	0	0	0	0	0	0
1dB				0	0	0	0	1
2dB				0	0	0	1	0
3dB				0	0	0	1	1
4dB				0	0	1	0	0
5dB				0	0	1	0	1
6dB				0	0	1	1	0
7dB				0	0	1	1	1
8dB				0	1	0	0	0
9dB				0	1	0	0	1
10dB				0	1	0	1	0
11dB				0	1	0	1	1
12dB				0	1	1	0	0
13dB				0	1	1	0	1
14dB				0	1	1	1	0
15dB				0	1	1	1	1
16dB				1	0	0	0	0
17dB				1	0	0	0	1
18dB				1	0	0	1	0
19dB				1	0	0	1	1
20dB	1	0	1	0	0			
Prohibition	1	0	1	0	1			
	:	:	:	:	:			
	1	1	1	1	1	0		
				1	1	1	1	1

Mode	MSB	Bass/Middle/Treble Boost/Cut						LSB
	D7	D6	D5	D4	D3	D2	D1	D0
Boost	0	0	0	Bass/Middle/Treble Gain				
Cut	1							

 : Initial condition

Select address 75 (hex)

Gain	Super Bass Gain							
	MSB							LSB
	D7	D6	D5	D4	D3	D2	D1	D0
0dB	0	0	0	0	0	0	0	0
1dB				0	0	0	0	1
2dB				0	0	0	1	0
3dB				0	0	0	1	1
4dB				0	0	1	0	0
5dB				0	0	1	0	1
6dB				0	0	1	1	0
7dB				0	0	1	1	1
8dB				0	1	0	0	0
9dB				0	1	0	0	1
10dB				0	1	0	1	0
11dB				0	1	0	1	1
12dB				0	1	1	0	0
13dB				0	1	1	0	1
14dB				0	1	1	1	0
15dB				0	1	1	1	1
16dB				1	0	0	0	0
17dB				1	0	0	0	1
18dB				1	0	0	1	0
19dB				1	0	0	1	1
20dB				1	0	1	0	0
Prohibition				1	0	1	0	1
				:	:	:	:	:
				1	1	1	1	1

(Note) About Super Bass, the above Gain is for in indication purposes. Actual Gain ( $=20\log(V_{OUT}/V_{IN})$ ) is different. Refer to P31 to P34 for the details.

 : Initial condition

#### (6) About Power ON Reset

Built-in IC initialization is made during power ON of the supply voltage. Please send initial data to all addresses at supply voltage on. And please turn ON mute until this initial data is sent.

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Rise Time of VCC	$t_{RISE}$	33	-	-	$\mu\text{sec}$	VCC rise time from 0V to 5V
VCC Voltage of Release Power ON Reset	$V_{POR}$	-	4.1	-	V	

## Application Information

## 1. Function and Specifications

Function	Specifications																	
Input selector	• Stereo input																	
	• Single-End/Differential																	
	(Possible to set the number of single-end/ differential as follows )																	
	<table><tr><td></td><td>Single-End</td><td>Differential</td></tr><tr><td>Mode 1</td><td>0</td><td>4</td></tr><tr><td>Mode 2</td><td>1</td><td>3</td></tr><tr><td>Mode 3</td><td>3</td><td>2</td></tr><tr><td>Mode 4</td><td>4</td><td>1</td></tr><tr><td>Mode 5</td><td>5</td><td>0</td></tr></table>		Single-End	Differential	Mode 1	0	4	Mode 2	1	3	Mode 3	3	2	Mode 4	4	1	Mode 5	5
	Single-End	Differential																
Mode 1	0	4																
Mode 2	1	3																
Mode 3	3	2																
Mode 4	4	1																
Mode 5	5	0																
Table.1 Combination of input selector																		
Input gain	• +20dB to 0dB (1dB step) • Possible to use “Advanced switch” for prevention of switching noise.																	
Mute	• Possible to use “Advanced switch” for prevention of switching noise.																	
Volume	• +15dB to -79dB (1dB step), -∞dB • Possible to use “Advanced switch” for prevention of switching noise.																	
Bass	• +20dB to -20dB (1dB step) • Q=0.5, 1, 1.5, 2 • f <sub>0</sub> =60, 80, 100, 120Hz • Possible to use “Advanced switch” for prevention of switching noise.																	
Middle	• +20dB to -20dB (1dB step) • Q=0.75, 1, 1.25, 1.5 • f <sub>0</sub> =500, 1k, 1.5k 2.5kHz • Possible to use “Advanced switch” for prevention of switching noise.																	
Treble	• +20dB to -20dB (1dB step) • Q=0.75, 1.25 • f <sub>0</sub> =7.5k, 10k, 12.5k, 15kHz • Possible to use “Advanced switch” for prevention of switching noise.																	
Fader	• +15dB to -79dB(1dB step), -∞dB • Possible to use “Advanced switch” for prevention of switching noise.																	
LPF	• f <sub>c</sub> =55/85/120/160Hz, pass • Phase shift (0°/180°)																	
HPF	• f <sub>c</sub> =55/85/120/160Hz, pass																	
Mixing	• Monaural input • +7dBdB to -79dB (1dB step), -∞dB • Possible to use “Advanced switch” for prevention of switching noise.																	
Super Bass	• +20dB to 0dB (1dB step) • Possible to use “Advanced switch” for prevention of switching noise.																	

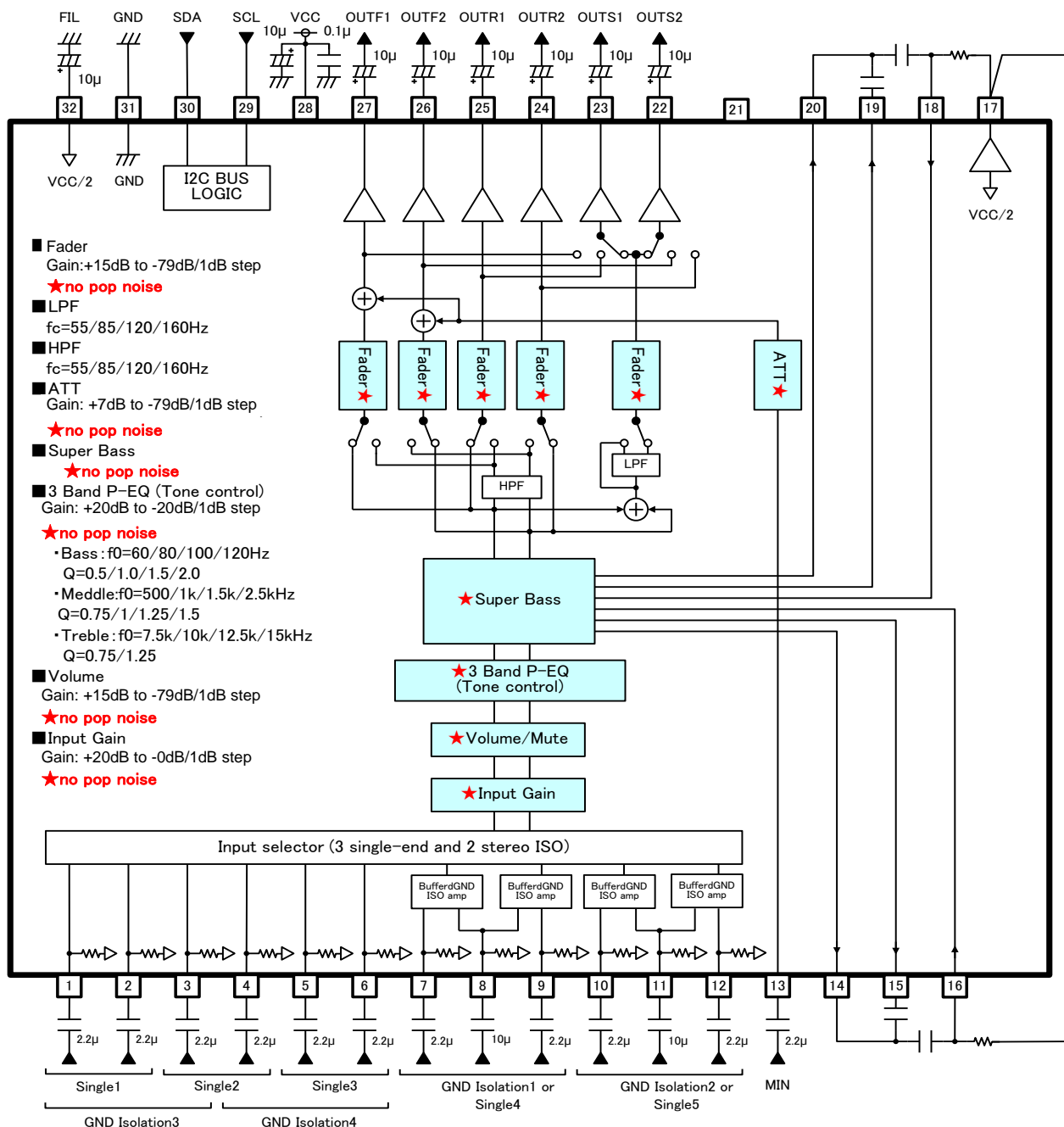
## 2. Volume / Fader Volume / Mixing ATT Attenuation Data

(dB)	D7	D6	D5	D4	D3	D2	D1	D0	(dB)	D7	D6	D5	D4	D3	D2	D1	D0
+15	0	1	1	1	0	0	0	1	-33	1	0	1	0	0	0	0	1
+14	0	1	1	1	0	0	1	0	-34	1	0	1	0	0	0	1	0
+13	0	1	1	1	0	0	1	1	-35	1	0	1	0	0	0	1	1
+12	0	1	1	1	0	1	0	0	-36	1	0	1	0	0	1	0	0
+11	0	1	1	1	0	1	0	1	-37	1	0	1	0	0	1	0	1
+10	0	1	1	1	0	1	1	0	-38	1	0	1	0	0	1	1	0
+9	0	1	1	1	0	1	1	1	-39	1	0	1	0	0	1	1	1
+8	0	1	1	1	1	0	0	0	-40	1	0	1	0	1	0	0	0
+7	0	1	1	1	1	0	0	1	-41	1	0	1	0	1	0	0	1
+6	0	1	1	1	1	0	1	0	-42	1	0	1	0	1	0	1	0
+5	0	1	1	1	1	0	1	1	-43	1	0	1	0	1	0	1	1
+4	0	1	1	1	1	1	0	0	-44	1	0	1	0	1	1	0	0
+3	0	1	1	1	1	1	0	1	-45	1	0	1	0	1	1	0	1
+2	0	1	1	1	1	1	1	0	-46	1	0	1	0	1	1	1	0
+1	0	1	1	1	1	1	1	1	-47	1	0	1	0	1	1	1	1
0	1	0	0	0	0	0	0	0	-48	1	0	1	1	0	0	0	0
-1	1	0	0	0	0	0	0	1	-49	1	0	1	1	0	0	0	1
-2	1	0	0	0	0	0	0	1	-50	1	0	1	1	0	0	1	0
-3	1	0	0	0	0	0	1	1	-51	1	0	1	1	0	0	1	1
-4	1	0	0	0	0	1	0	0	-52	1	0	1	1	0	1	0	0
-5	1	0	0	0	0	1	0	1	-53	1	0	1	1	0	1	0	1
-6	1	0	0	0	0	1	1	0	-54	1	0	1	1	0	1	1	0
-7	1	0	0	0	0	1	1	1	-55	1	0	1	1	0	1	1	1
-8	1	0	0	0	1	0	0	0	-56	1	0	1	1	1	0	0	0
-9	1	0	0	0	1	0	0	1	-57	1	0	1	1	1	0	0	1
-10	1	0	0	0	1	0	1	0	-58	1	0	1	1	1	0	1	0
-11	1	0	0	0	1	0	1	1	-59	1	0	1	1	1	0	1	1
-12	1	0	0	0	1	1	0	0	-60	1	0	1	1	1	1	0	0
-13	1	0	0	0	1	1	0	1	-61	1	0	1	1	1	1	0	1
-14	1	0	0	0	1	1	1	0	-62	1	0	1	1	1	1	1	0
-15	1	0	0	0	1	1	1	1	-63	1	0	1	1	1	1	1	1
-16	1	0	0	1	0	0	0	0	-64	1	1	0	0	0	0	0	0
-17	1	0	0	1	0	0	0	1	-65	1	1	0	0	0	0	0	1
-18	1	0	0	1	0	0	1	0	-66	1	1	0	0	0	0	1	0
-19	1	0	0	1	0	0	1	1	-67	1	1	0	0	0	0	1	1
-20	1	0	0	1	0	1	0	0	-68	1	1	0	0	0	1	0	0
-21	1	0	0	1	0	1	0	1	-69	1	1	0	0	0	1	0	1
-22	1	0	0	1	0	1	1	0	-70	1	1	0	0	0	1	1	0
-23	1	0	0	1	0	1	1	1	-71	1	1	0	0	0	1	1	1
-24	1	0	0	1	1	0	0	0	-72	1	1	0	0	1	0	0	0
-25	1	0	0	1	1	0	0	1	-73	1	1	0	0	1	0	0	1
-26	1	0	0	1	1	0	1	0	-74	1	1	0	0	1	0	1	0
-27	1	0	0	1	1	0	1	1	-75	1	1	0	0	1	0	1	1
-28	1	0	0	1	1	1	0	0	-76	1	1	0	0	1	1	0	0
-29	1	0	0	1	1	1	0	1	-77	1	1	0	0	1	1	0	1
-30	1	0	0	1	1	1	1	0	-78	1	1	0	0	1	1	1	0
-31	1	0	0	1	1	1	1	1	-79	1	1	0	0	1	1	1	1
-32	1	0	1	0	0	0	0	0	-∞	1	1	1	1	1	1	1	1

Adjustable range of mixing ATT is +7dB to -∞dB.

 : Initial condition

## 3. Application Circuit



※About single input 1 to 3 it is possible to change from single input to GND Isolation input 3,4.

※About GND Isolation1 and GND Isolation2, it is possible to change from differential input to single input 4 to 5.

Figure 23. BD37544FS

Unit  
R : [Ω]  
C : [F]

## Notes on wiring

- ① Please connect the decoupling capacitor of the power supply in the shortest possible distance to GND.
- ② GND lines should be one-point connected.
- ③ Wiring pattern of Digital should be away from that of Analog unit and cross-talk should not be acceptable.
- ④ SCL and SDA lines of I<sup>2</sup>C BUS should not be parallel if possible.  
The lines should be shielded, if they are adjacent to each other.
- ⑤ Analog input lines should not be parallel if possible. The lines should be shielded, if they are adjacent.
- ⑥ Please short Pins 15-16, and Pins 18-19 if the Super Bass is not used.

## Power Dissipation

About the thermal design of the IC

Characteristics of an IC have a great deal to do with the temperature at which it is used, and exceeding absolute maximum ratings may degrade and destroy elements. Careful consideration must be given to the heat of the IC from the two standpoints of immediate damage and long-term reliability of operation.

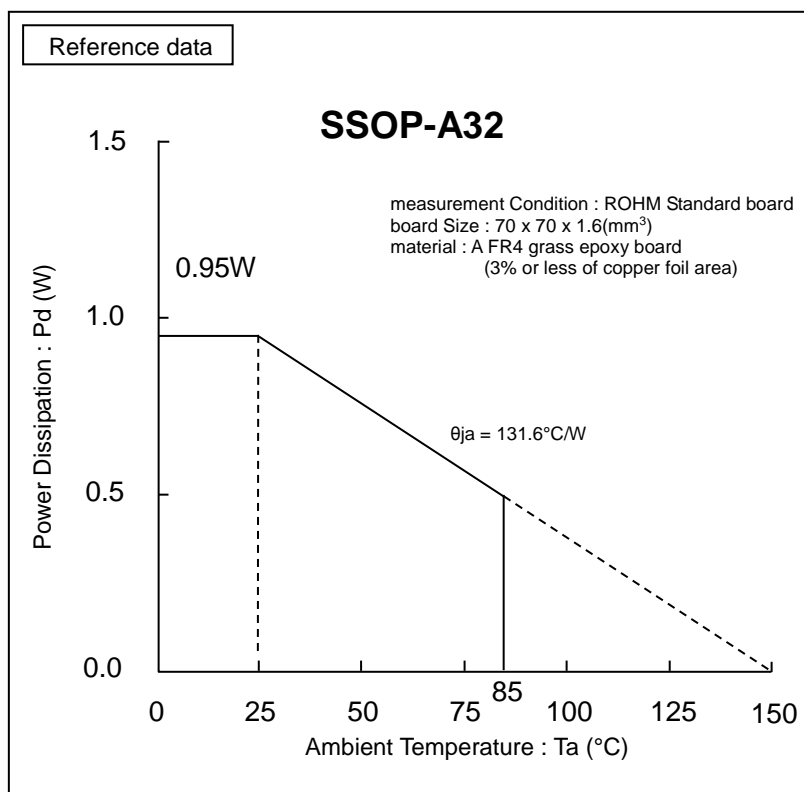


Figure 24. Temperature Derating Curve

(Note) Values are actual measurements and are not guaranteed.

Power dissipation values vary according to the board on which the IC is mounted.

## I/O Equivalent Circuits

Terminal No.	Terminal Name	Terminal Voltage	Equivalent Circuit	Terminal Description
1 2 3 4 5 6	A1 A2 B1 B2 C1 C2	4.25		A terminal for signal input. The input impedance is 100kΩ(Typ).
7 8 9 10 11 12	DP1 DN DP2 EP1 EN EP2	4.25		Input terminal available to ingle/Differential mode. The input impedance is 250kΩ(Typ).
16 18	SBB1 SBB2	-		An input terminal for Super Bass
15 17 19 22 23 24 25 26 27	SBA1 SBBIAS SBA2 OUTS2 OUTS1 OUTR2 OUTR1 OUTF2 OUTF1	4.25		A terminal for Super Bass and fader, Subwoofer output.
14 20	SBC1 SBC2	4.25		An output terminal for Super Bass.

Values in the pin explanation and input/output equivalent circuit are reference values only and are not guaranteed.

## I/O Equivalent Circuits – continued

Terminal No.	Terminal Name	Terminal Voltage	Equivalent Circuit	Terminal Description
28	VCC	8.5		Power supply terminal.
29	SCL	-		A terminal for clock input of I <sup>2</sup> C BUS communication.
30	SDA	-		A terminal for data input of I <sup>2</sup> C BUS communication.
31	GND	0		Ground terminal.
32	FIL	4.25		1/2 VCC terminal. Voltage for reference bias of analog signal system. The simple precharge circuit and simple discharge circuit for an external capacitor are built in.
13	MIN	4.25		A terminal for signal input. The input impedance is 27kΩ(typ).

Values in the pin explanation and input/output equivalent circuit are reference values only and are not guaranteed.

## Operational Notes

### 1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

### 2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

### 3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

### 4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

### 5. Thermal Consideration

Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

### 6. Recommended Operating Conditions

These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

### 7. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

### 8. Operation Under Strong Electromagnetic Field

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

### 9. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

### 10. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

### 11. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

## Operational Notes – continued

## 12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.

When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

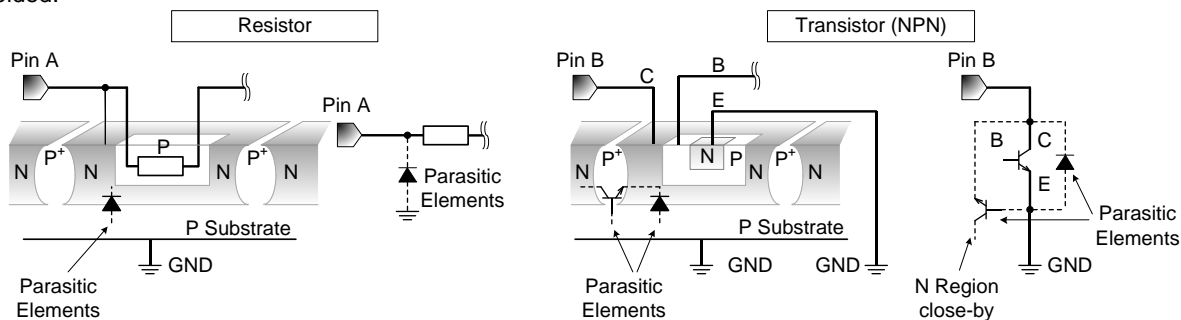
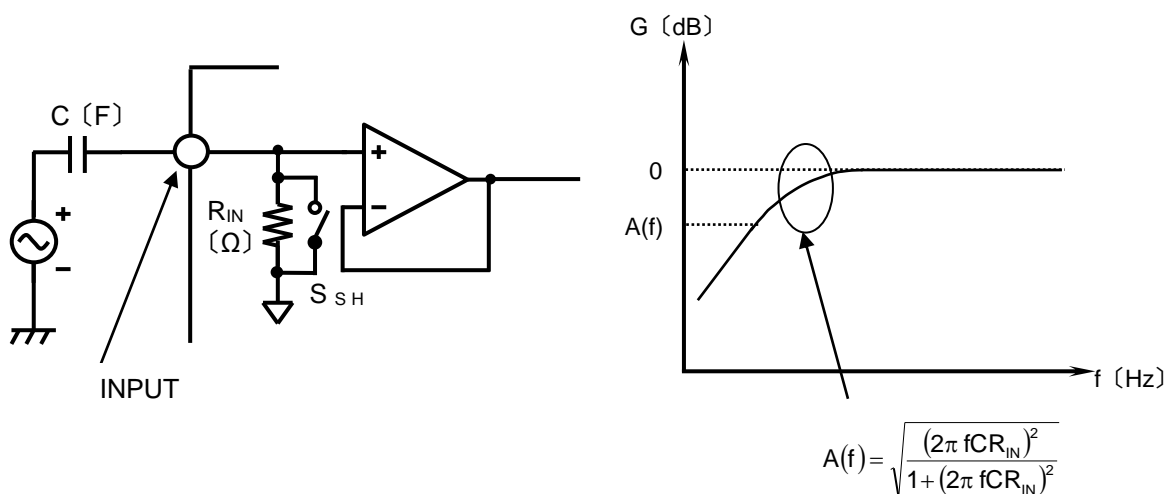


Figure 25. Example of monolithic IC structure

## 13. About Signal Input

## (a) About Input Coupling Capacitor Constant Value

The constant value of input coupling capacitor C(F) is decided with respect to the input impedance  $R_{IN}(\Omega)$  at the input signal terminal of the IC. The first HPF characteristic of RC is composed.



## (b) About the Input Selector SHORT

SHORT mode is the command which makes switch  $S_{SH}$  = ON of input selector part so that the input impedance  $R_{IN}$  of all terminals becomes small. Switch  $S_{SH}$  is OFF when SHORT command is not selected.

The constant time brought about by the small resistance inside and the capacitor outside the LSI becomes small when this command is used. The charge time of the capacitor becomes short. Since SHORT mode turns ON the switch of  $S_{SH}$  and makes it low impedance, please use it at no signal condition.

## Operational Notes – continued

## 14. About MIX

(1) About Specification of Fader  $-\infty$  at MIX ON.

Mix\_signal is added to Main\_signal after Fader\_Gain(+15dB to -79dB) like the figure. When Fader is set at  $-\infty$ , the signal after a MIX signal is added is done with MUTE because the  $-\infty$  circuit of Fader is in the step after the addition circuit

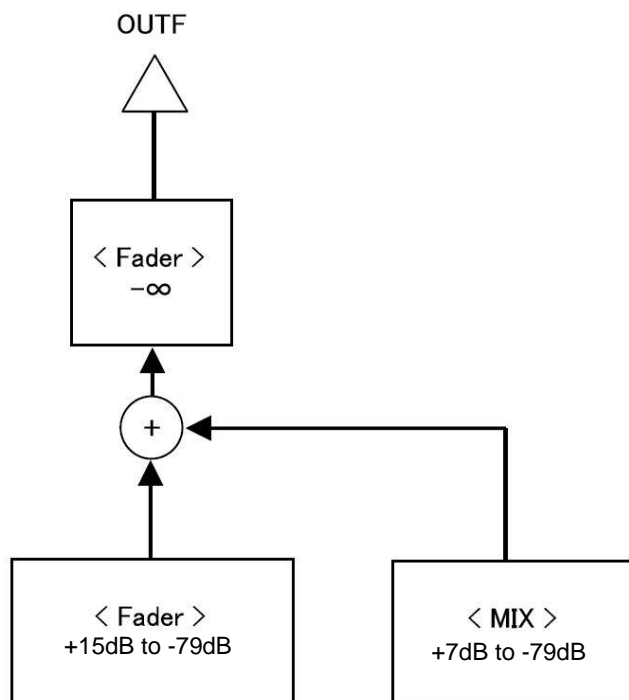


Figure 26. About Front Fader and MIX

## (2) About Advanced Switching of MIX\_Gain/ATT

When advanced switching of MIX\_Gain/ATT works, MIX goes a switching movement that it passes through the state of MIX\_OFF like in B figure below (from current setting of MIX\_Gain/ATT to MIX\_OFF to a target setting of MIX\_Gain/ATT).

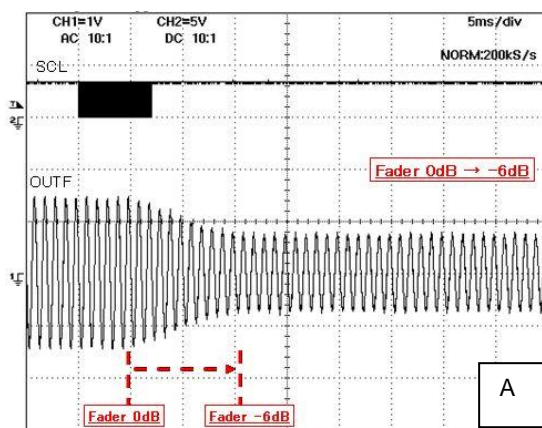
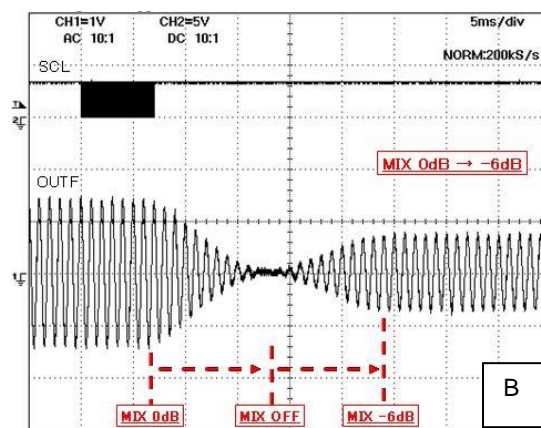
Fader\_Gain/ATT 0dB to -6dB  
advanced switchingMIX\_Gain/ATT 0dB to -6dB  
advanced switching

Figure 27. Advanced Switching Movement when MIX\_Gain/ATT is Changed

## Operational Notes – continued

## 15. About Super Bass Circuit

The (the following Super Bass) which strengthens a low band like the graph below a can be realized by composing an external circuit with the pin 14 to 20 as shown in Figure 28.

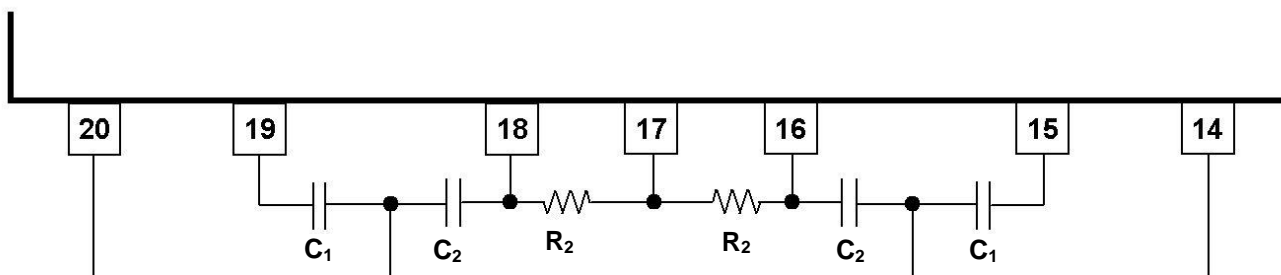


Figure 28. Super Bass circuit

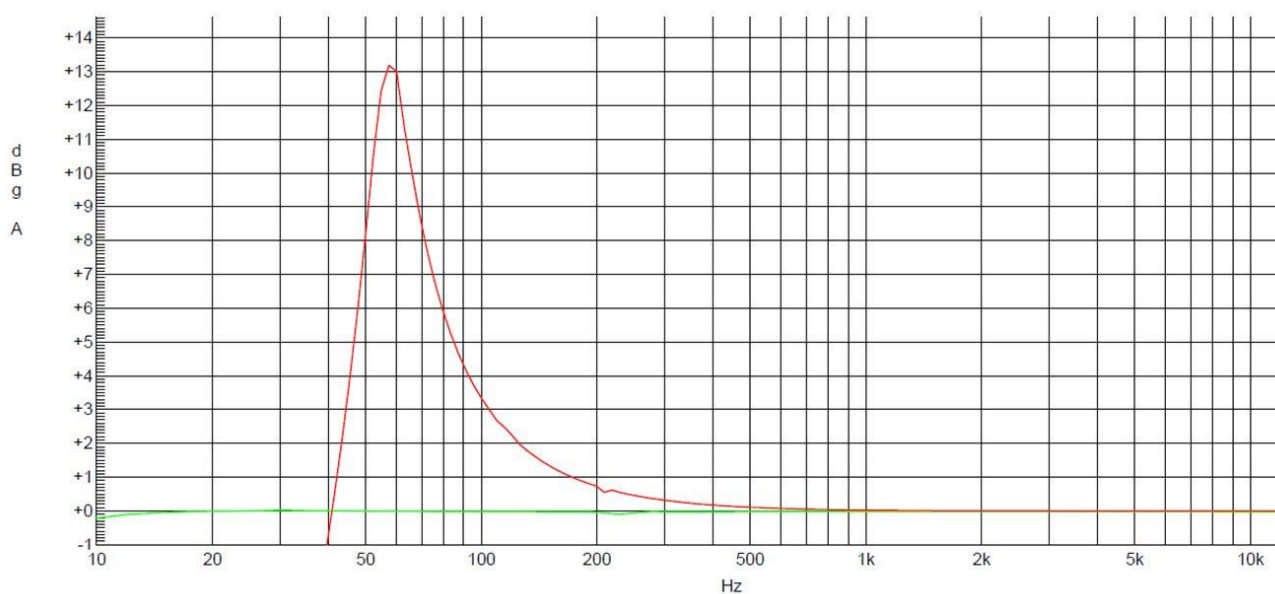


Figure 29. Super Bass Gain vs Frequency

(a) Gain Step Width becomes a Logarithm  
When a setup of Gain is made 0,1,2,3,5,7,11,20dB, it becomes the following (bottom right) character.  
( $C_1=0.047\mu\text{F}$ ,  $C_2=0.1\mu\text{F}$ ,  $R_1=3\text{k}\Omega$ ,  $R_2=560\text{k}\Omega$ )

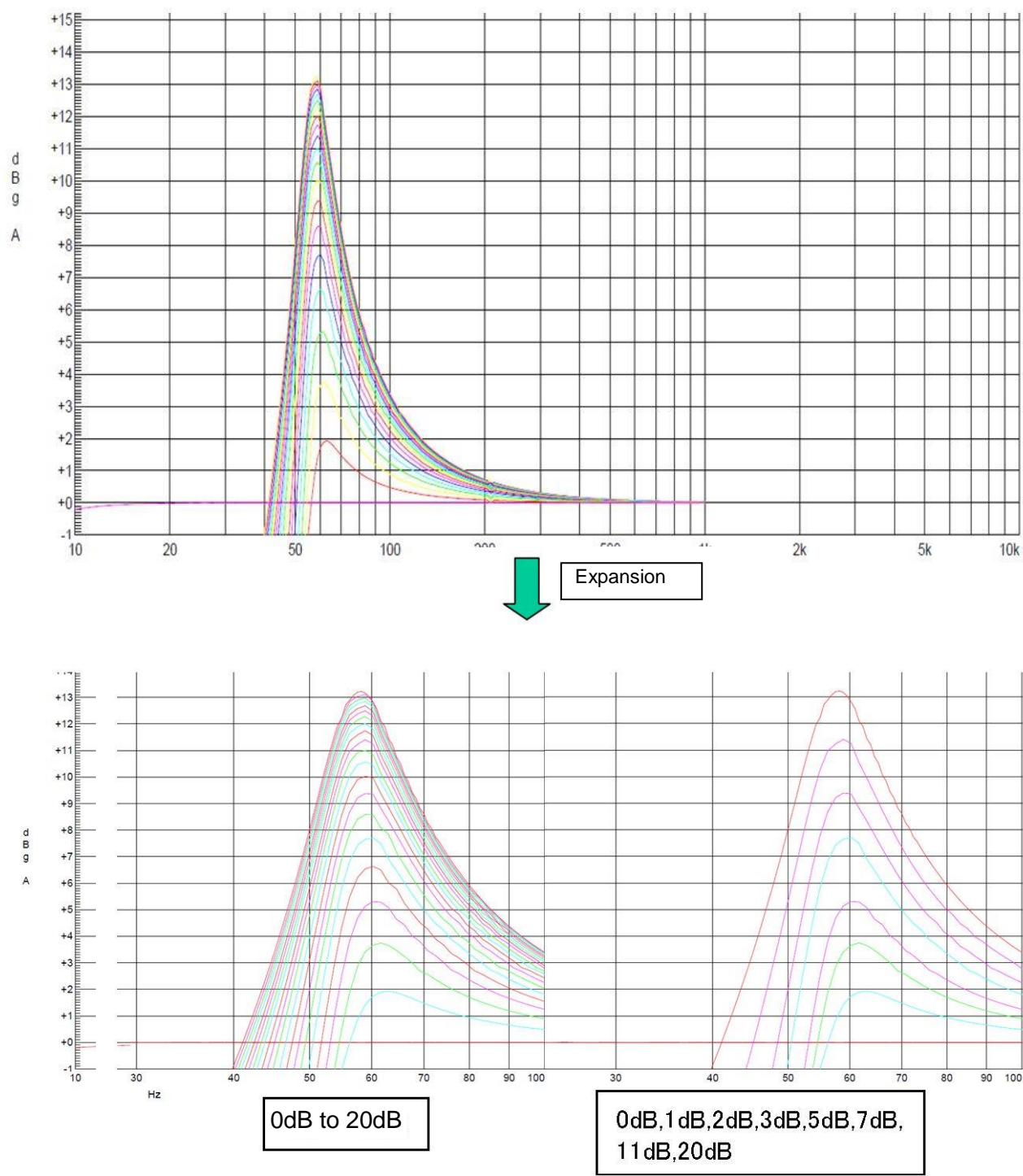
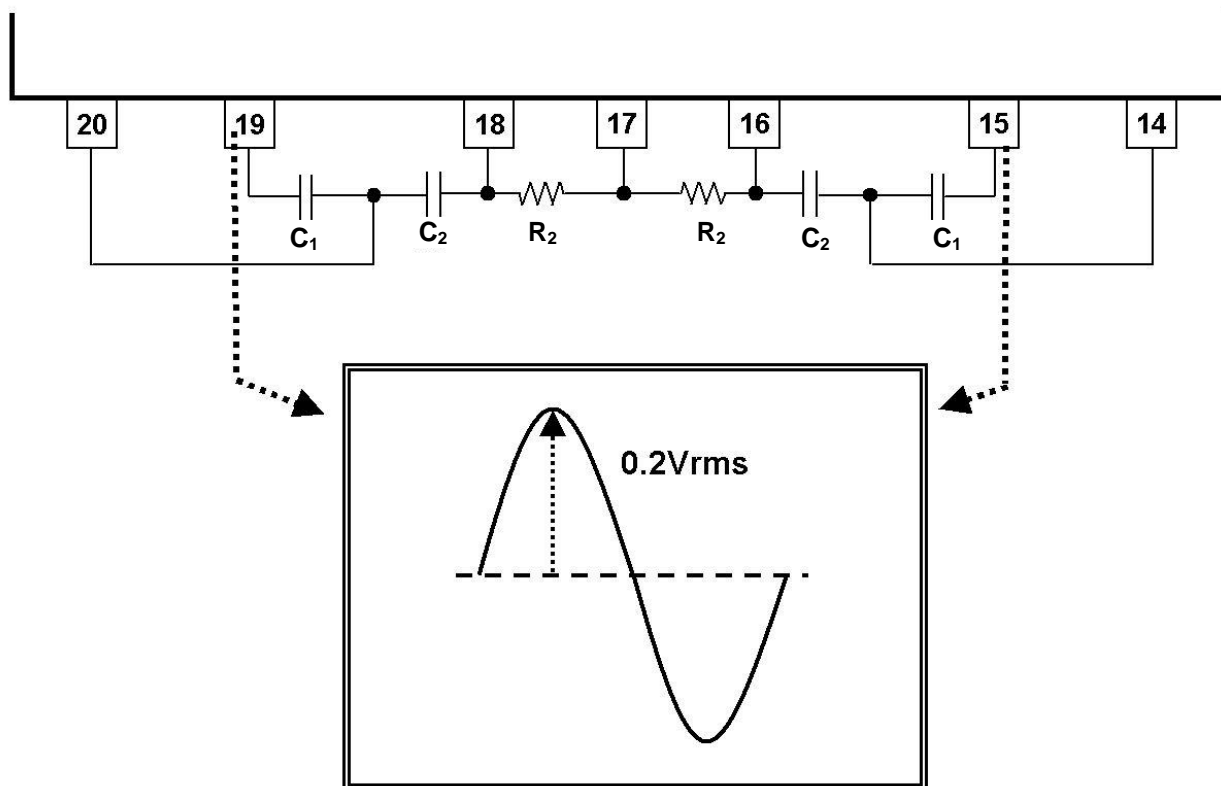


Figure 30. About Gain step of Super Bass

(b) You must take level diagram into consideration so that output may not do a clip

Example ( $C_1=0.047\mu\text{F}$ ,  $C_2=0.1\mu\text{F}$ ,  $R_2=560\text{k}\Omega$ ,  $V_{CC}=8.5\text{V}$ )

To prevent output clipping due to amplification when Super Bass is used, adjust the level diagram with volume until the Tone output level becomes less than  $0.2\text{Vrms}$ .



Please adjust so that the maximum level of the Tone output becomes less than  $0.2\text{Vrms}$ . (at  $V_{CC}=8.5\text{V}$ )

Figure 31. Super Bass Level Diagram

(c) About  $f_0$  and Gain of Super Bass

$f_0$  and Gain of Super Bass deviates due to the deviation of the value of  $C_1$ ,  $C_2$ ,  $R_2$  (Components with the outside),  
 $R_1$  (the resistance built in IC).

Example : Super Bass Gain – frequency characteristic at Dispersion condition of  $C_1, C_2, R_2 \pm 5\%$ ,  $R_1 \pm 30\%$

( $C_1=0.047\mu\text{F}$ ,  $C_2=0.1\mu\text{F}$ ,  $R_1=3\text{kohm}$ ,  $R_2=560\text{kohm}$ , Super Bass Gain=20dB)

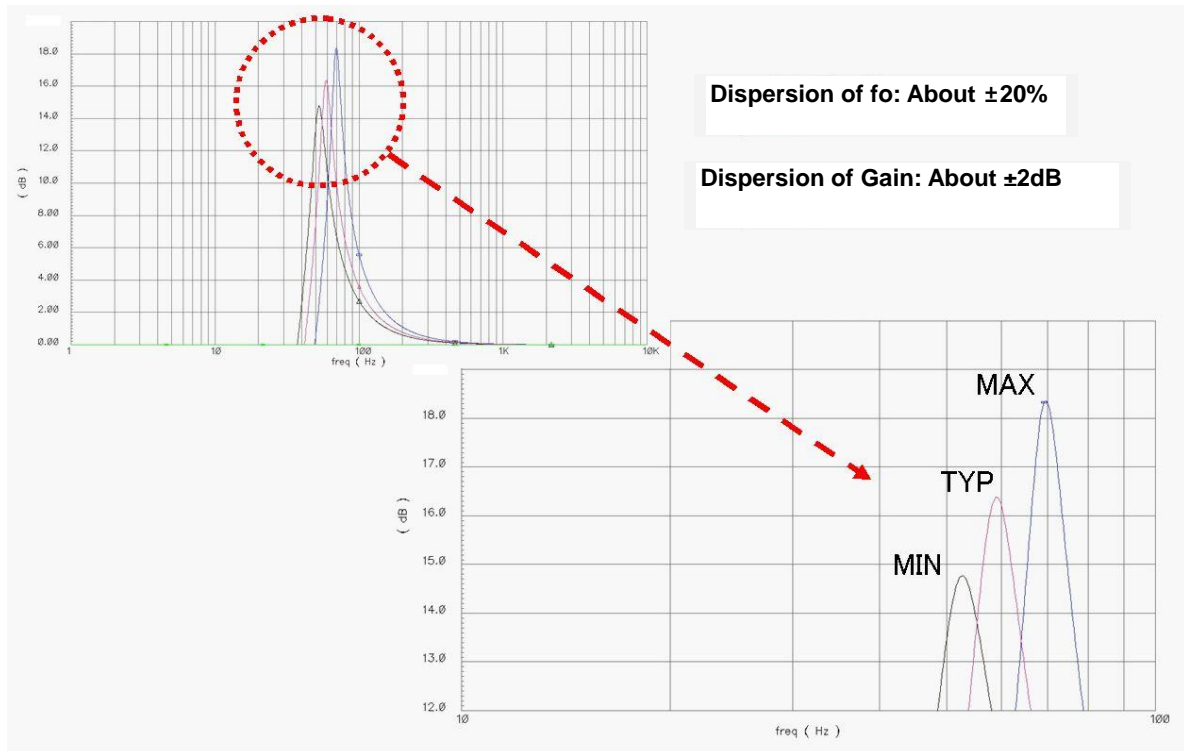
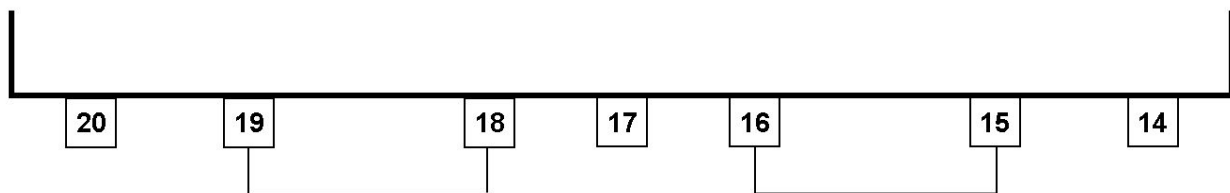


Figure 32. Dispersion of  $f_0$  and Gain of Super Bass

(d) How to Deal with Pins of Super Bass when not used

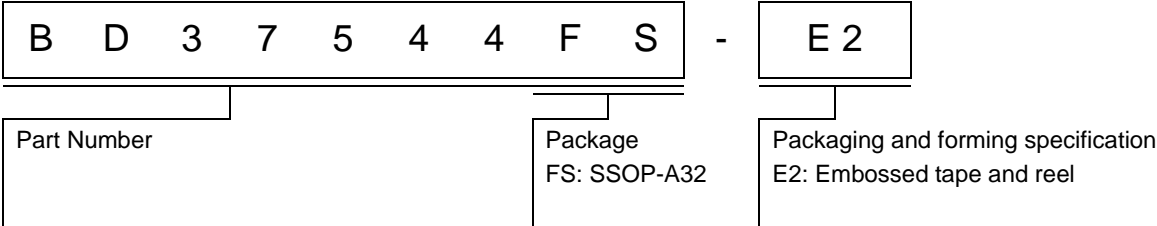
Short Pins 15 to 16, Pins 18 to 19 as shown in Figure 33 when the Super Bass function is not used.



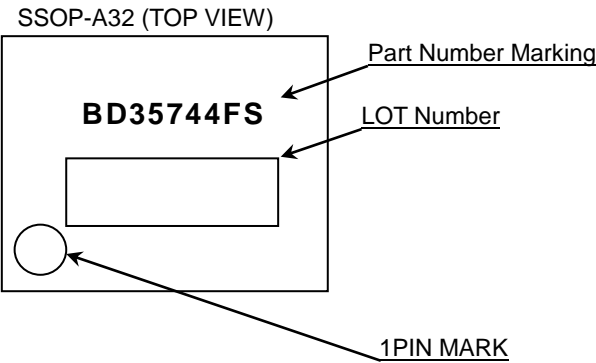
Short Pin 15 to 16, Pin 18 to 19

Figure 33. How to Deal with Pins of Super Bass when not used

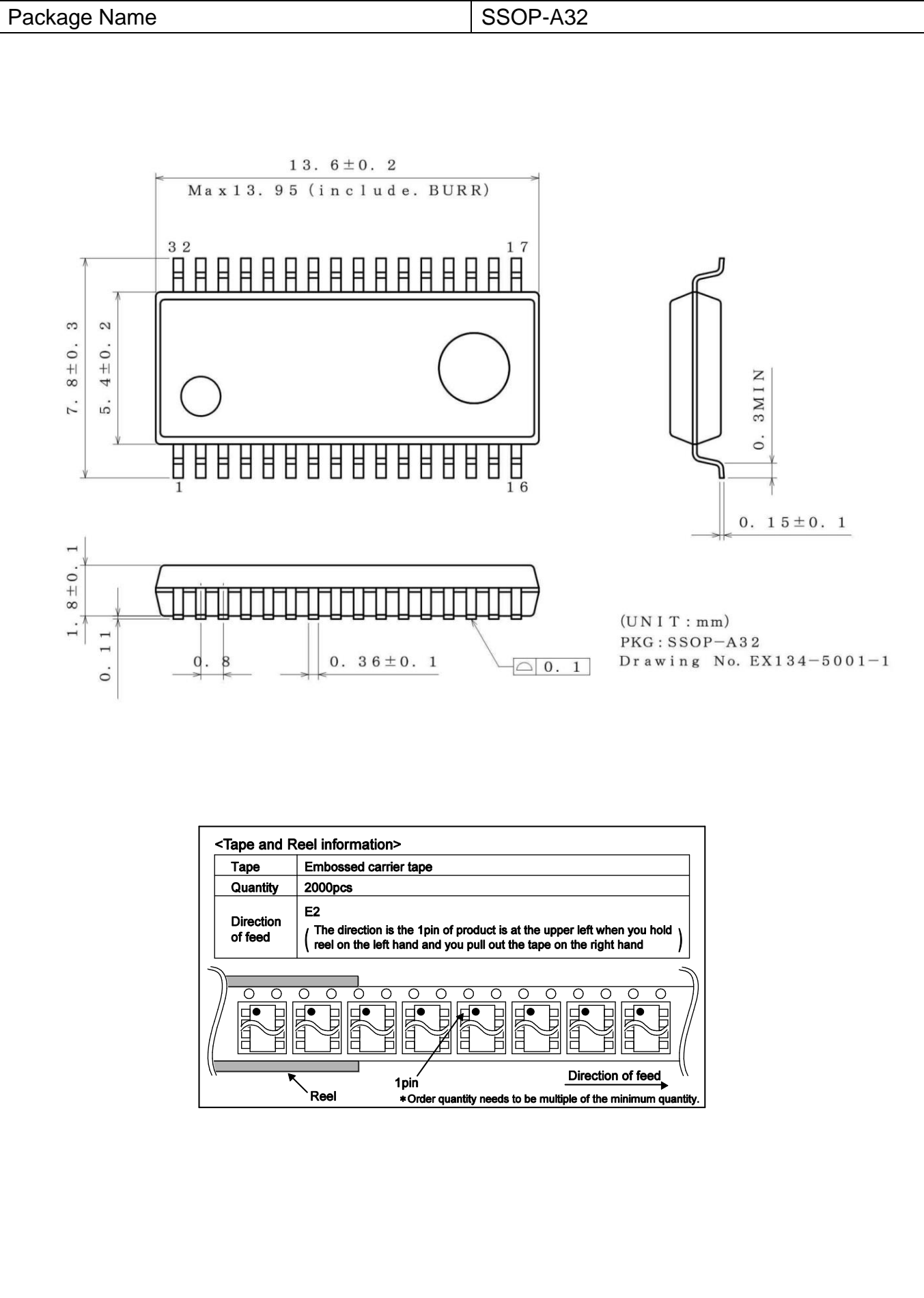
Ordering Information



Marking Diagram



Physical Dimension, Tape and Reel Information



Revision History

Date	Revision	Changes
16.Dec.2015	001	New Release

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