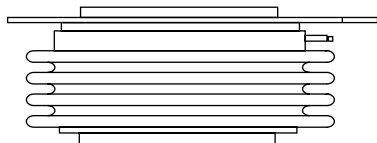


Phase Control Thyristors (Stud Version), 1650 A



A-24 (K-PUK)

FEATURES

- Center amplifying gate
- Metal case with ceramic insulator
- International standard case A-24 (K-PUK)
- High profile hockey PUK
- Compliant to RoHS directive 2002/95/EC
- Designed and qualified for industrial level



RoHS
COMPLIANT

PRODUCT SUMMARY

$I_{T(AV)}$	1650 A
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TYPICAL APPLICATIONS

- DC motor controls
- Controlled DC power supplies
- AC controllers

MAJOR RATINGS AND CHARACTERISTICS

PARAMETER	TEST CONDITIONS	VALUES	UNITS
$I_{T(AV)}$		1650	A
	T_{hs}	55	°C
$I_{T(RMS)}$		3080	A
	T_{hs}	25	°C
I_{TSM}	50 Hz	30 500	A
	60 Hz	32 000	
I^2t	50 Hz	4651	kA ² s
	60 Hz	4250	
V_{DRM}/V_{RRM}		1200 to 2000	V
t_q	Typical	200	µs
T_J		- 40 to 125	°C

ELECTRICAL SPECIFICATIONS

VOLTAGE RATINGS

TYPE NUMBER	VOLTAGE CODE	V_{DRM}/V_{RRM} , MAXIMUM REPETITIVE PEAK AND OFF-STATE VOLTAGE V	V_{RSM} , MAXIMUM NON-REPETITIVE PEAK VOLTAGE V	I_{DRM}/I_{RRM} MAXIMUM AT $T_J = T_J$ MAXIMUM mA
ST1200C..K	12	1200	1300	100
	14	1400	1500	
	16	1600	1700	
	18	1800	1900	
	20	2000	2100	

ABSOLUTE MAXIMUM RATINGS						
PARAMETER	SYMBOL	TEST CONDITIONS			VALUES	UNITS
Maximum average on-state current at heatsink temperature	I _{T(AV)}	180° conduction, half sine wave double side (single side) cooled			1650 (700)	A
					55 (85)	°C
Maximum RMS on-state current	I _{T(RMS)}	DC at 25 °C heatsink temperature double side cooled			3080	A
Maximum peak, one-cycle non-repetitive surge current	I _{TSM}	t = 10 ms	No voltage reapplied	Sinusoidal half wave, initial T _J = T _J maximum	30 500	
		t = 8.3 ms			32 000	
		t = 10 ms	100 % V _{RRM} reapplied		25 700	
		t = 8.3 ms			26 900	
Maximum I ² t for fusing	I ² t	t = 10 ms	No voltage reapplied		4651	kA ² s
		t = 8.3 ms			4250	
		t = 10 ms	100 % V _{RRM} reapplied		3300	
		t = 8.3 ms			3000	
Maximum I ² √t for fusing	I ² √t	t = 0.1 ms to 10 ms, no voltage reapplied			46 510	kA ² √s
Low level value of threshold voltage	V _{T(TO)1}	(16.7 % × π × I _{T(AV)}) < I < π × I _{T(AV)} , T _J = T _J maximum			0.91	V
High level value of threshold voltage	V _{T(TO)2}	(I > π × I _{T(AV)}), T _J = T _J maximum			1.01	
Low level value of on-state slope resistance	r _{t1}	(16.7 % × π × I _{T(AV)}) < I < π × I _{T(AV)} , T _J = T _J maximum			0.21	mΩ
High level value of on-state slope resistance	r _{t2}	(I > π × I _{T(AV)}), T _J = T _J maximum			0.19	
Maximum on-state voltage	V _{TM}	I _p k = 4000 A, T _J = T _J maximum, t _p = 10 ms sine pulse			1.73	V
Maximum holding current	I _H	T _J = 25 °C, anode supply 12 V resistive load			600	mA
Typical latching current	I _L				1000	

SWITCHING				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum non-repetitive rate of rise of turned-on current	di/dt	Gate drive 20 V, 20 Ω, $t_r \leq 1$ μs $T_J = T_J$ maximum, anode voltage ≤ 80 % V_{DRM}	1000	A/μs
Typical delay time	t_d	Gate current 1 A, $di_g/dt = 1$ A/μs $V_d = 0.67$ % V_{DRM} , $T_J = 25$ °C	1.9	μs
Typical turn-off time	t_q	$I_{TM} = 550$ A, $T_J = T_J$ maximum, $di/dt = 40$ A/μs, $V_R = 50$ V, $dV/dt = 20$ V/μs, gate 0 V 100 Ω, $t_p = 500$ μs	200	

BLOCKING				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum critical rate of rise of off-state voltage	dV/dt	$T_J = T_J$ maximum linear to 80 % rated V_{DRM}	500	V/μs
Maximum peak reverse and off-state leakage current	I_{RRM}, I_{DRM}	$T_J = T_J$ maximum, rated V_{DRM}/V_{RRM} applied	100	mA



TRIGGERING						
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES		UNITS
				TYP.	MAX.	
Maximum peak gate power	P _{GM}	T _J = T _J maximum, t _p ≤ 5 ms		16		W
Maximum average gate power	P _{G(AV)}	T _J = T _J maximum, f = 50 Hz, d% = 50		3		
Maximum peak positive gate current	I _{GM}	T _J = T _J maximum, t _p ≤ 5 ms		3.0		A
Maximum peak positive gate voltage	+ V _{GM}			20		V
Maximum peak negative gate voltage	- V _{GM}			5.0		
DC gate current required to trigger	I _{GT}	T _J = - 40 °C	Maximum required gate trigger/ current/voltage are the lowest value which will trigger all units 12 V anode to cathode applied	200	-	mA
		T _J = 25 °C		100	200	
		T _J = 125 °C		50	-	
DC gate voltage required to trigger	V _{GT}	T _J = - 40 °C		1.4	-	V
		T _J = 25 °C		1.1	3.0	
		T _J = 125 °C		0.9	-	
DC gate current not to trigger	I _{GD}	T _J = T _J maximum	Maximum gate current/voltage not to trigger is the maximum value which will not trigger any unit with rated V _{DRM} anode to cathode applied	10		mA
DC gate voltage not to trigger	V _{GD}			0.25		V

THERMAL AND MECHANICAL SPECIFICATIONS					
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS	
Maximum operating junction temperature range	T_J		- 40 to 125	°C	
Maximum storage temperature range	T_{Stg}		- 40 to 150		
Maximum thermal resistance, junction to heatsink	R_{thJ-hs}	DC operation single side cooled	0.042	K/W	
		DC operation double side cooled	0.021		
Maximum thermal resistance, case to heatsink	R_{thC-hs}	DC operation single side cooled	0.006		
		DC operation double side cooled	0.003		
Mounting force, ± 10 %			24 500 (2500)	N (kg)	
Approximate weight			425	g	
Case style		See dimensions - link at the end of datasheet		A-24 (K-PUK)	

ΔR_{thJC} CONDUCTION						
CONDUCTION ANGLE	SINUSOIDAL CONDUCTION		RECTANGULAR CONDUCTION		TEST CONDITIONS	UNITS
	SINGLE SIDE	DOUBLE SIDE	SINGLE SIDE	DOUBLE SIDE		
180°	0.003	0.003	0.002	0.002	T _J = T _J maximum	K/W
120°	0.004	0.004	0.004	0.004		
90°	0.005	0.005	0.005	0.005		
60°	0.007	0.007	0.007	0.007		
30°	0.012	0.012	0.012	0.012		

Note

- The table above shows the increment of thermal resistance R_{thJC} when devices operate at different conduction angles than DC

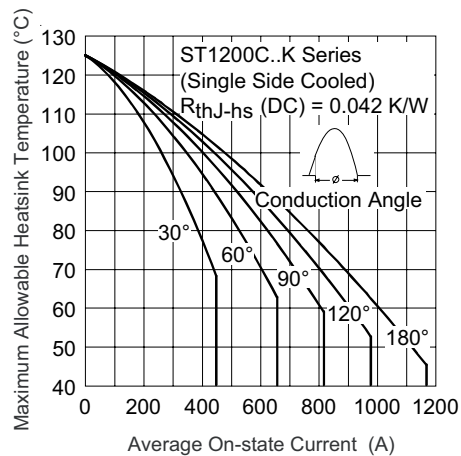


Fig. 1 - Current Ratings Characteristics

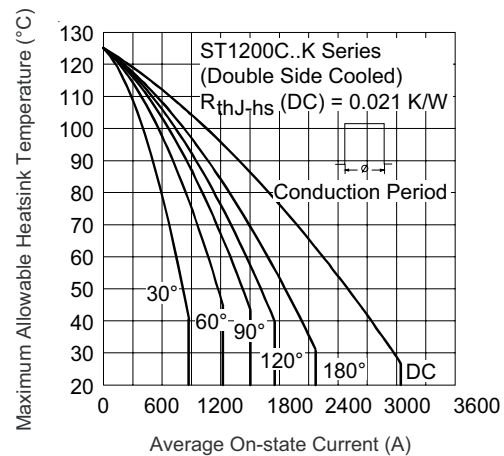


Fig. 4 - Current Ratings Characteristics

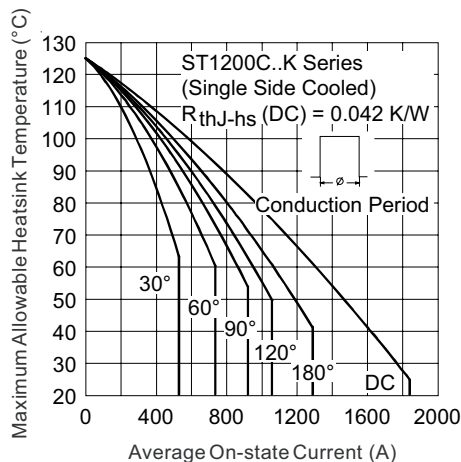


Fig. 2 - Current Ratings Characteristics

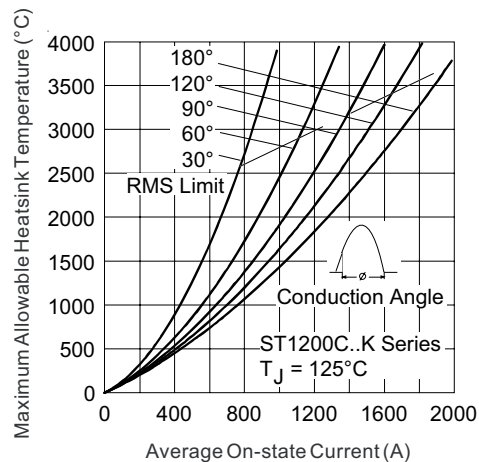


Fig. 5 - On-State Power Loss Characteristics

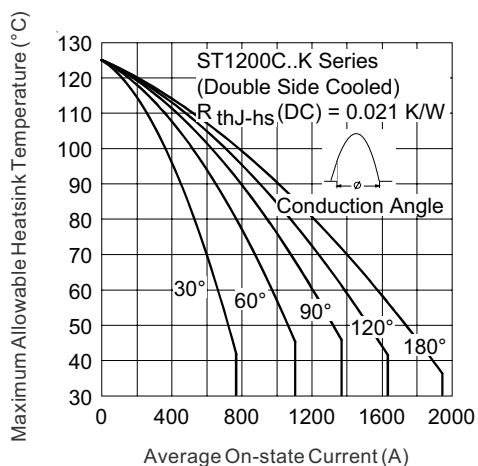


Fig. 3 - Current Ratings Characteristics

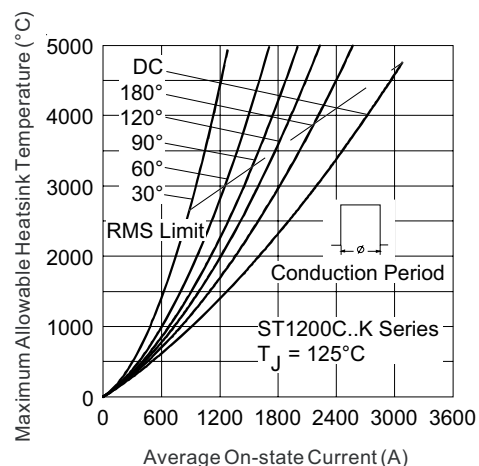


Fig. 6 - On-State Power Loss Characteristics

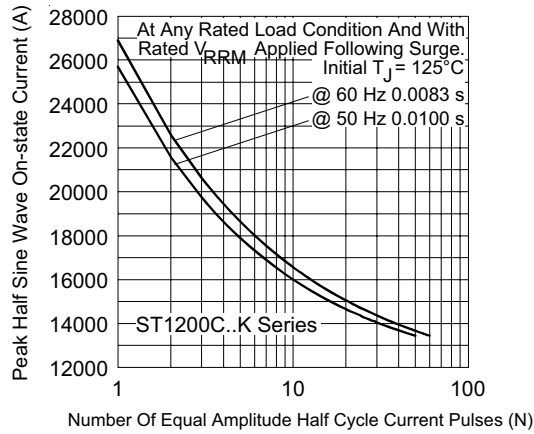


Fig. 7 - Maximum Non-Repetitive Surge Current Single and Double Side Cooled

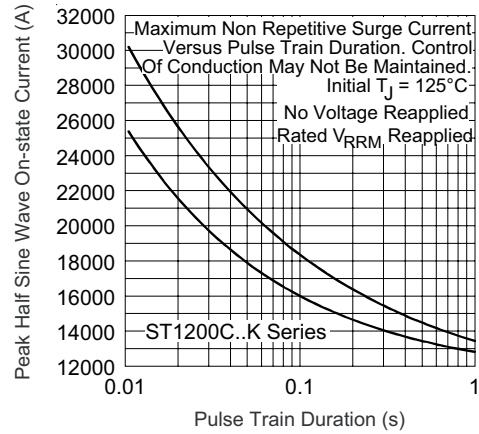


Fig. 8 - Maximum Non-Repetitive Surge Current Single and Double Side Cooled

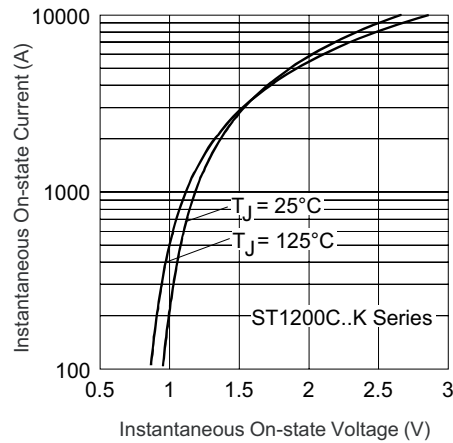


Fig. 9 - On-State Voltage Drop Characteristics

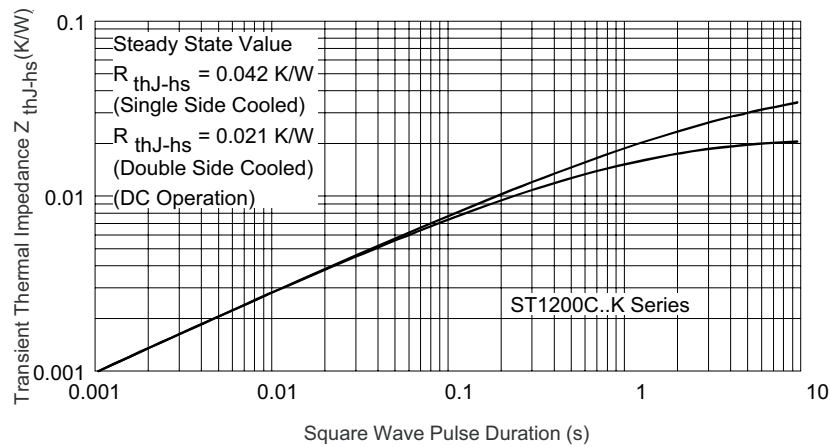


Fig. 10 - Thermal Impedance Z_{thJ-hs} Characteristics

ST1200C..KP Series

Vishay High Power Products Phase Control Thyristors
(Stud Version), 1650 A

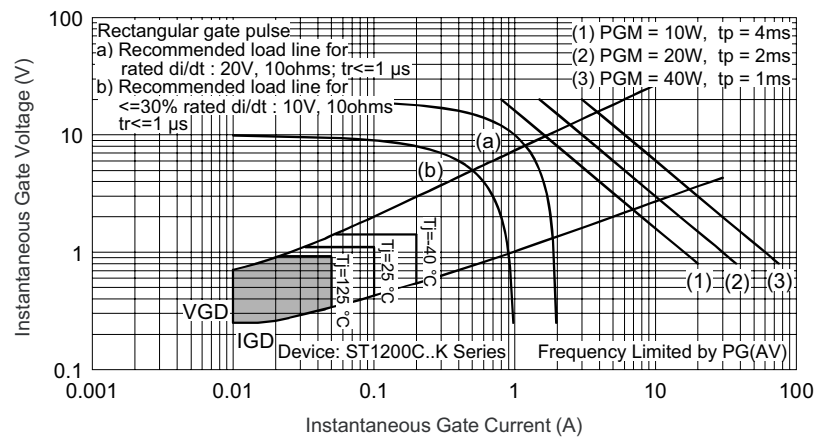


Fig. 11 - Gate Characteristics

ORDERING INFORMATION TABLE

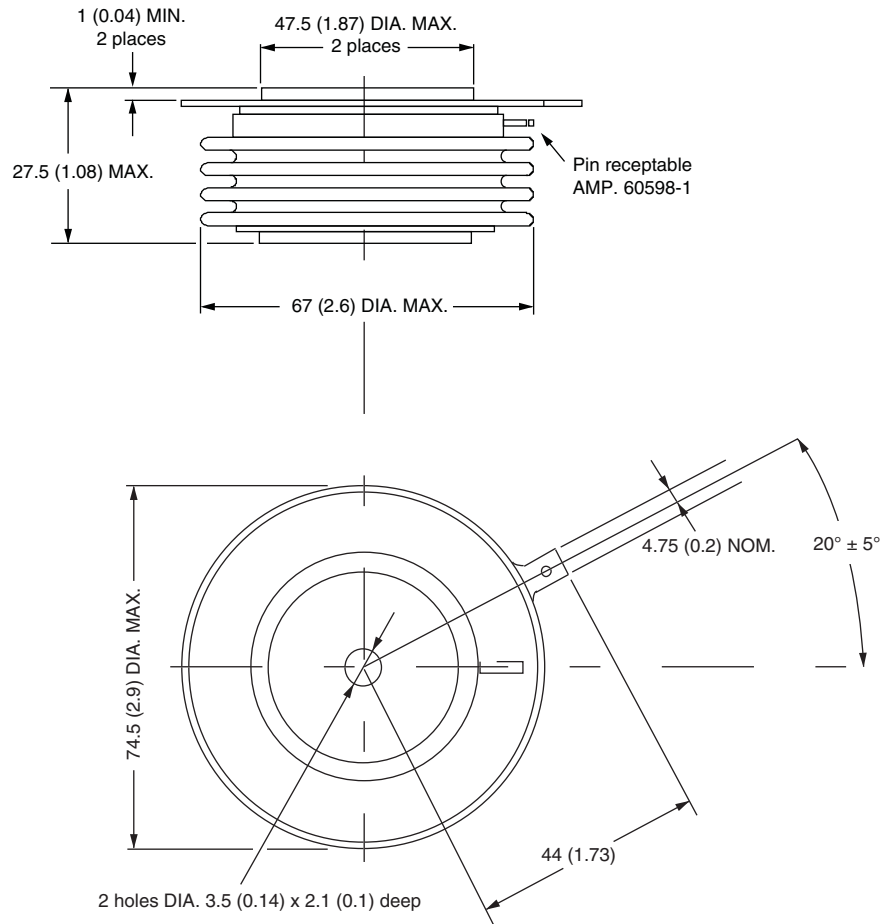
Device code	ST	120	0	C	20	K	1	-	P
	1	2	3	4	5	6	7	8	9
1	- Thyristor								
2	- Essential part number								
3	- 0 = Converter grade								
4	- C = Ceramic PUK								
5	- Voltage code: Code x 100 = V_{RRM} (see Voltage Ratings table)								
6	- K = PUK case A-24 (K-PUK)								
7	- 0 = Eyelet terminals (gate and auxiliary cathode unsoldered leads) 1 = Fast-on terminals (gate and auxiliary cathode unsoldered leads) 2 = Eyelet terminals (gate and auxiliary cathode soldered leads) 3 = Fast-on terminals (gate and auxiliary cathode soldered leads)								
8	- Critical dV/dt: • None = 500 V/ μ s (standard selection) • L = 1000 V/ μ s (special selection)								
9	- P = Lead (Pb)-free								

LINKS TO RELATED DOCUMENTS	
Dimensions	www.vishay.com/doc?95081

A-24 (K-PUK)

DIMENSIONS in millimeters (inches)

Creepage distance: 28.88 (1.137) minimum
Strike distance: 17.99 (0.708) minimum



Quote between upper and lower pole pieces has to be considered after application of mounting force (see thermal and mechanical specification)



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