



P-CHANNEL ENHANCEMENT MODE MOSFET

Product Summary (Typ. @ V_{GS} = -4.5V, T_A = +25°C)

V _{DSS}	R _{DS(on)}	Qg	Q_{gd}	I _D
-8V	8.2mΩ	8.1nC	1.8nC	-10A

Description

This 3^{rd} generation Lateral MOSFET (LD-MOS) is engineered to minimize on-state losses and switch ultra-fast, making it ideal for high-efficiency power transfer. It uses Chip-Scale Package (CSP) to increase power density by combining low thermal impedance with minimal $R_{\text{DS}(on)}$ per footprint area.

Applications

- DC-DC Converters
- Battery Management
- Load Switch

Features

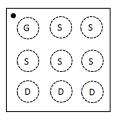
- LD-MOS Technology with the Lowest Figure of Merit:
 - $-R_{DS(on)} = 8.2m\Omega$ to Minimize On-State Losses
 - -Q_q = 8.1nC for Ultra-Fast Switching
- V_{gs(th)} = -0.8V typ. for a Low Turn-On Potential
- CSP with Footprint 1.5mm x 1.5mm
- Height = 0.60mm for Low Profile
- ESD = 6kV HBM Protection of Gate
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- Qualified to AEC-Q101 Standards for High Reliability

Mechanical Data

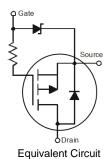
- Case: U-WLB1515-9
- Terminal Connections: See Diagram Below

U-WLB1515-9





Top-View Pin Configuration



Ordering Information (Note 4)

Part Number	Case	Packaging
DMP1011UCB9-7	U-WLB1515-9	3,000/Tape & Reel

Notes:

- 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
- 2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free
- 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
- 4. For packaging details, go to our website at http://www.diodes.com/products/packages.html.

Marking Information

U-WLB1515-9

NX YM $\begin{array}{l} NX = Product\ Type\ Marking\ Code \\ YM = Date\ Code\ Marking \\ Y\ or\ \overline{Y} = Year\ (ex:\ B = 2014) \\ M\ or\ M = Month\ (ex:\ 9 = September) \end{array}$

Date Code Key

Year	2012	2	2013		2014	20	15	2016		2017	2	2018
Code	Z		Α		В	(D		Е		F
Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	0	N	D



Characteristic		Symbol	Value	Units	
Drain-Source Voltage		V _{DSS}	-8	V	
Gate-Source Voltage			V _{GSS}	-6	V
Continuous Drain Current (Note 5) V _{GS} = -4.5V	Steady State	T _A = +25°C T _A = +70°C	I _D	-10 -8	А
Continuous Drain Current (Note 6) $V_{GS} = -4.5V$ Steady $T_A = +25^{\circ}C$ State $T_A = +70^{\circ}C$			I _D	-7.4 -6.0	А
Pulsed Drain Current (Pulse duration 10µs, duty cy	rcle ≤1%)		I _{DM}	-50	Α
Continuous Source Pin Current (Note 6)			Is	-2	_
Pulsed Source Pin Current (Pulse duration 10µs, d	uty cycle ≤	Ism	-15	_	
Continuous Gate Current			I _G	-0.5	Α

Thermal Characteristics (@TA = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Units
Total Power Dissipation (Note 5)	P _D	0.89	W
Total Power Dissipation (Note 6)	P _D	1.57	W
Thermal Resistance, Junction to Ambient (Note 5)	R _{0JA}	+142.1	°C/W
Thermal Resistance, Junction to Ambient (Note 6)	R _{0JA}	+80.5	°C/W
Operating and Storage Temperature Range	T _J , T _{STG}	-55 to +150	°C

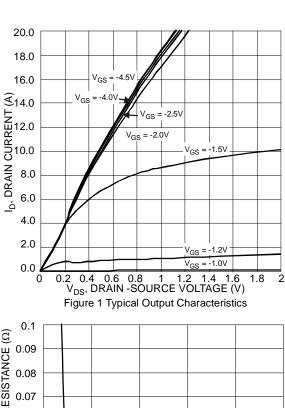
Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

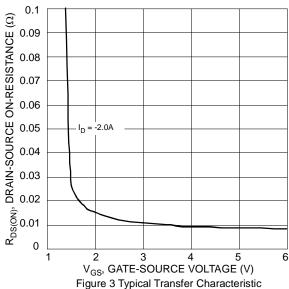
Characteristic	Symbol	Min	Тур	Max	Unit	Test Condition	
OFF CHARACTERISTICS (Note 7)							
Drain-Source Breakdown Voltage	BV _{DSS}	-8	_	l	V	$V_{GS} = 0V, I_D = -250\mu A$	
Gate to Source Voltage	BV _{SGS}	-6	_	-	V	$V_{DS} = 0V, I_{D} = -250\mu A$	
Zero Gate Voltage Drain Current @T _C = +25°C	IDSS	_	_	-1	μA	$V_{DS} = -4.0V, V_{GS} = 0V$	
Gate-Source Leakage	I _{GSS}	_	_	-100	nA	$V_{GS} = -4.0V, V_{DS} = 0V$	
ON CHARACTERISTICS (Note 7)							
Gate Threshold Voltage	V _{GS(th)}	-0.4	-0.8	-1.1	V	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$	
			8.2	10		$V_{GS} = -4.5V, I_{D} = -2A$	
Static Drain-Source On-Resistance	R _{DS (ON)}	_	10	13	mΩ	$V_{GS} = -3.0V, I_D = -2A$	
			11	14		$V_{GS} = -2.5V$, $I_D = -2A$	
Forward Transfer Admittance	Y _{fs}	_	16.8		S	$V_{DS} = -4V, I_{D} = -2A$	
Diode Forward Voltage (Note 6)	V_{SD}	_	-0.7	-1	V	$V_{GS} = 0V, I_{S} = -2A$	
Reverse Recovery Charge	Qrr	_	6.3	_	nC	$V_{dd} = -5V, I_F = -2A,$	
Reverse Recovery Time	t _{rr}	_	18.5	_	ns	di/dt = 200A/µs	
DYNAMIC CHARACTERISTICS (Note 8)							
Input Capacitance	Ciss	_	817	1,060	pF	\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\	
Output Capacitance	Coss	_	595	770	pF	$V_{DS} = -4V, V_{GS} = 0V,$ f = 1.0MHz	
Reverse Transfer Capacitance	Crss	_	269	350	pF	1 – 1.01/11/12	
Series Gate Resistance	R_{G}	_	1.9	_	Ω	$V_{DS} = 0V, V_{GS} = 0V, f = 1.0MHz$	
Total Gate Charge (4.5V)	Qg	_	8.1	10.5	nC	V 45V V 4V	
Gate-Source Charge	Q_{gs}	_	0.9	_	nC	$V_{GS} = -4.5V, V_{DS} = -4V,$ $I_{D} = -2A$	
Gate-Drain Charge	Q_{gd}	_	1.8		nC	I _D = -2A	
Turn-On Delay Time	t _{D(on)}	_	6.2	10	ns		
Turn-On Rise Time	t _r	_	22.6	_	ns	$V_{DD} = -4V, V_{GS} = -4.5V,$	
Turn-Off Delay Time	t _{D(off)}	_	30.1	48	ns	$I_{DS} = -2A$, $R_G = 10\Omega$,	
Turn-Off Fall Time	t _f	_	22.7	_	ns		

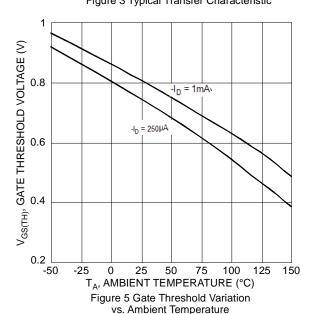
Notes:

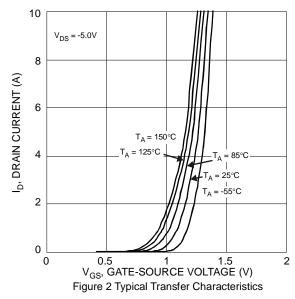
- 5. Device mounted on FR-4 PCB with minimum recommended pad layout.
- 6. Device mounted on FR4 material with 1-inch² (6.45cm²), 2oz (0.071mm thick) Cu.
- 7. Short duration pulse test used to minimize self-heating effect. 8. Guaranteed by design. Not subject to production testing.

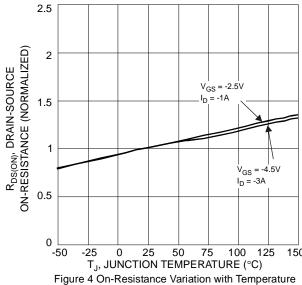












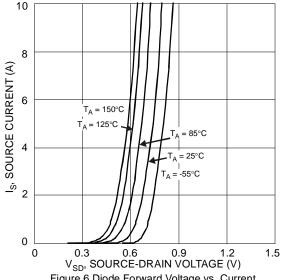
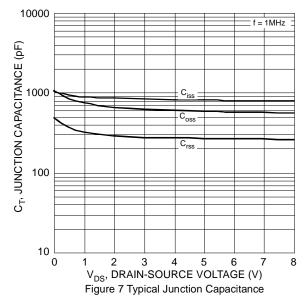
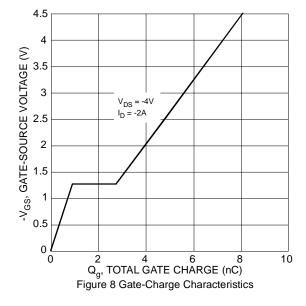
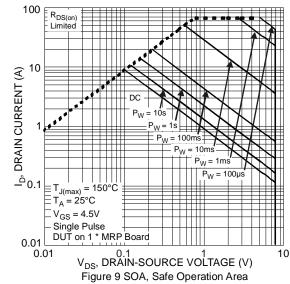


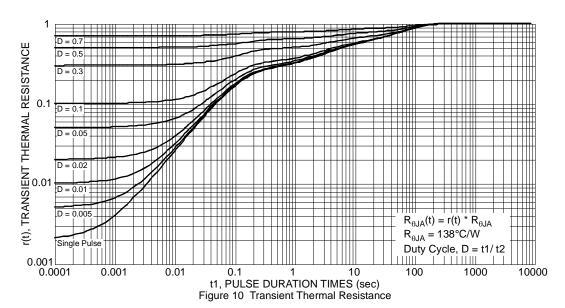
Figure 6 Diode Forward Voltage vs. Current







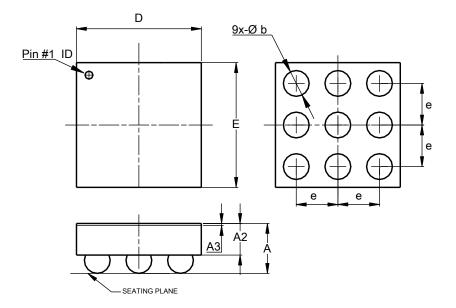






Package Outline Dimensions

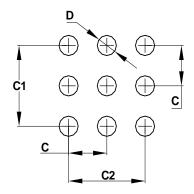
Please see AP02002 at http://www.diodes.com/datasheets/ap02002.pdf for the latest version.



U-WLB1515-9						
Dim	Min	Max	Тур			
Α	-	0.60	-			
A2	-	0.36	0.36			
А3	0.020	0.030	0.025			
b	0.22	0.32	0.27			
D	1.47	1.50	1.49			
Е	1.47	1.50	1.49			
е	-	-	0.50			
All Dimensions in mm						

Suggested Pad Layout

Please see AP02001 at http://www.diodes.com/datasheets/ap02001.pdf for the latest version.



Dimensions	Value (in mm)
С	0.50
C1	1.00
C2	1.00
D	0.25



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