TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

# TC74ACT245P, TC74ACT245F, TC74ACT245FT TC74ACT640P, TC74ACT640F, TC74ACT640FT

Octal Bus Transceiver

TC74ACT245P/F/FT 3-State,

Non-Inverting

TC74ACT640P/F/FT 3-State, Inverting

The TC74ACT245 and 640 are advanced high speed CMOS OCTAL BUS TRANSCEIVERs fabricated with silicon gate and double-layer metal wiring C<sup>2</sup>MOS technology.

They achieve the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

These devices may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.

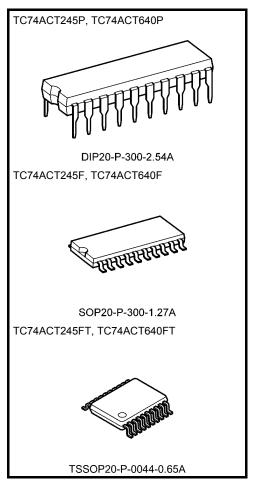
They are intended for two-way asynchronous communication between data busses. The direction of data transmission is determined by the level of the DIR input.

The enable input ( $\overline{\rm G}$  ) can be used to disable the device so that the busses are effectively isolated.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

## Features (Note 1) (Note 2)

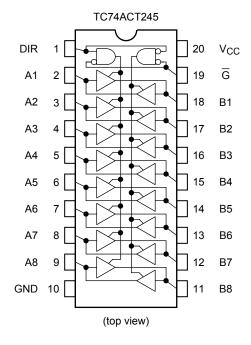
- High speed:  $t_{pd} = 4.7$  ns (typ.) at  $V_{CC} = 5$  V
- Low power dissipation:  $I_{CC} = 8 \mu A \text{ (max)}$  at  $Ta = 25^{\circ}C$
- · Compatible with TTL outputs
  - $V_{IL} = 0.8 \text{ V (max)}, V_{IH} = 2.0 \text{ V (min)}$
- · Symmetrical output impedance
  - $|I_{OH}| = I_{OL} = 24 \text{ mA (min)}$
  - Capability of driving 50  $\Omega$  transmission lines.
- $\bullet \quad \text{Balanced propagation delays: } t_{\text{pLH}} \simeq t_{\text{pHL}}$
- Pin and function compatible with 74F245/640
  - Note 1: Do not apply a signal to any bus terminal when it is in the output mode. Damage may result.
  - Note 2: All floating (high impedance) bus terminals must have their input levels fixed by means of pull up or pull down resistors.

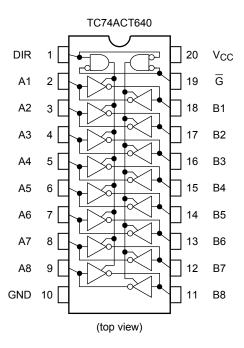


Weight

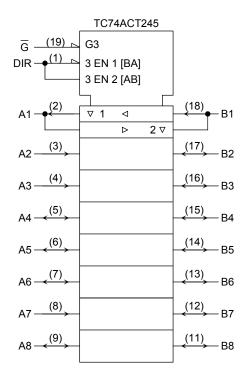
DIP20-P-300-2.54A : 1.30 g (typ.) SOP20-P-300-1.27A : 0.22 g (typ.) TSSOP20-P-0044-0.65A : 0.08 g (typ.)

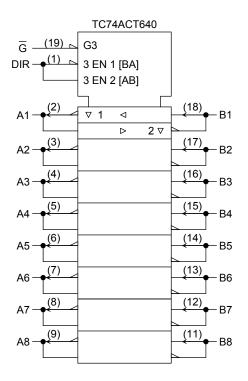
## **Pin Assignment**





## **IEC Logic Symbol**





#### **Truth Table**

Inputs		Fun	ction	Outputs			
G	DIR	A Bus	B Bus	ACT245	ACT640		
L	L	Output	Input	A = B	A = B		
L	Н	Input	Output	B = A	$B = \overline{A}$		
Н	Х	2	<u> </u>	Z	Z		

X: Don't care

Z: High impedance

## **Absolute Maximum Ratings (Note 1)**

Characteristics	Symbol	Rating	Unit
Supply voltage range	V <sub>CC</sub>	−0.5 to 7.0	V
DC input voltage	V <sub>IN</sub>	-0.5 to V <sub>CC</sub> + 0.5	V
DC output voltage	V <sub>OUT</sub>	-0.5 to V <sub>CC</sub> + 0.5	V
Input diode current	I <sub>IK</sub>	±20	mA
Output diode current	lok	±50	mA
DC output current	lout	±50	mA
DC V <sub>CC</sub> /ground current	Icc	±200	mA
Power dissipation	PD	500 (DIP) (Note 2)/180 (SOP/TSSOP)	mW
Storage temperature	T <sub>stg</sub>	−65 to 150	°C

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: 500 mW in the range of Ta =  $-40^{\circ}$ C to 65°C. From Ta = 65°C to 85°C a derating factor of -10 mW/°C should be applied up to 300 mW.

#### **Operating Range (Note)**

Characteristics	Symbol	Rating	Unit
Supply voltage	V <sub>CC</sub>	4.5 to 5.5	V
Input voltage	V <sub>IN</sub>	0 to V <sub>CC</sub>	V
Output voltage	V <sub>OUT</sub>	0 to V <sub>CC</sub>	V
Operating temperature	T <sub>opr</sub>	−40 to 85	°C
Input rise and fall time	dt/dV	0 to 10	ns/V

Note: The operating range is required to ensure the normal operation of the device. Unused inputs and bus inputs must be tied to either  $V_{CC}$  or GND. Please connect both bus inputs and the bus outputs with  $V_{CC}$  or GND when the I/O of the bus terminal changes by the function. In this case, please note that the output is not short-circuited.

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## **Electrical Characteristics**

### **DC Characteristics**

Characteristics	Symbol	Test Condition V <sub>CC</sub> (V)			Ta = 25°C			Ta = −40 to 85°C		Unit	
	- <b>,</b>				V <sub>CC</sub> (V)	Min	Тур.	Max	Min	Max	
High-level input voltage	V <sub>IH</sub>	_			4.5 to 5.5	2.0	_	_	2.0	_	V
Low-level input voltage	V <sub>IL</sub>	_		4.5 to 5.5	_	_	0.8	_	0.8	V	
High-level output voltage	Voн	VIN	I <sub>OH</sub> = -50 μA		4.5	4.4	4.5	_	4.4	_	
		= V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = −24 mA		4.5	3.94	_	_	3.80	_	V
0			I <sub>OH</sub> = −75 mA	(Note)	5.5		_	_	3.85	_	
	V <sub>OL</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 50 μA		4.5	_	0.0	0.1	_	0.1	
Low-level output voltage			$I_{OL}$ = 24 mA		4.5	_	_	0.36	_	0.44	V
			I <sub>OL</sub> = 75 mA	(Note)	5.5		_	_	_	1.65	
3-state output off-state current	I <sub>OZ</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>OUT</sub> = V <sub>CC</sub> or GND		5.5	-	_	±0.5	_	±5.0	μΑ	
Input leakage current	I <sub>IN</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND			5.5	-	_	±0.1	_	±1.0	μΑ
Quiescent supply current	Icc	$V_{IN} = V_{C}$	V <sub>IN</sub> = V <sub>CC</sub> or GND			_	_	8.0	_	80.0	μA
	Ic	Per input: V <sub>IN</sub> = 3.4 V Other input: V <sub>CC</sub> or GND			5.5	ı	_	1.35	_	1.5	mA

Note: This spec indicates the capability of driving 50  $\Omega$  transmission lines.

One output should be tested at a time for a 10 ms maximum duration.



## AC Characteristics (C<sub>L</sub> = 50 pF, R<sub>L</sub> = 500 $\Omega$ , input: $t_r$ = $t_f$ = 3 ns)

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = −40 to 85°C		Unit
	- <b>,</b>		V <sub>CC</sub> (V)	Min	Тур.	Max	Min	Max	
Propagation delay	t <sub>pLH</sub>		5.0 ± 0.5		5.0	8.0	1.0	9.0	ns
time (Note 2)	$t_{pHL}$	_	5.0 ± 0.5	_	5.0	0.0	1.0	9.0	115
Propagation delay	$t_{pLH}$		5.0 ± 0.5	_	5.7	8.5	1.0	9.5	ns
time (Note 3)	$t_{pHL}$	_							
Output enable time	$t_{pZL}$		5.0 ± 0.5	_	7.3	12.3	1.0	14.0	ns
Output enable time	t <sub>pZH</sub>	_	3.0 1 0.3		7.5	12.5	1.0	14.0	113
Output disable time	$t_{pLZ}$	_	5.0 ± 0.5	1	6.3	9.7	1.0	11.0	ns
Output disable time	t <sub>pHZ</sub>								113
Input capacitance	C <sub>IN</sub>	DIR, G		_	5	10	1	10	pF
Bus input capacitance	C <sub>I/O</sub>	A <sub>n</sub> , Bn		_	13	_	_	_	pF
Power dissipation	C <sub>PD</sub>	TC74ACT245		_	38	_	_	_	nΕ
capacitance	(Note 1)	TC74ACT640		_	43	_	_	_	pF

Note 1: C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

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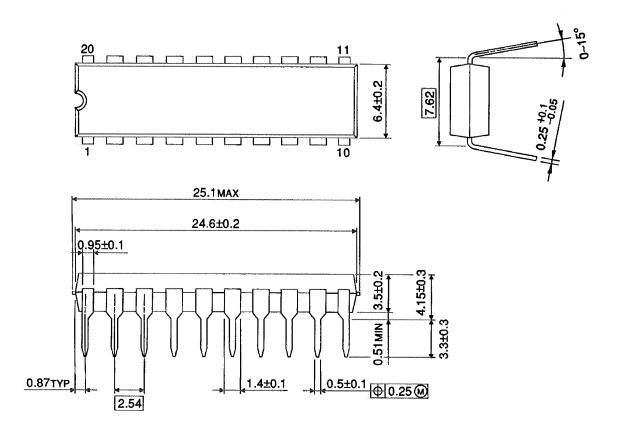
Average operating current can be obtained by the equation:

 $I_{CC (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 (per bit)$ 

Note 2: For TC74ACT245 only Note 3: For TC74ACT640 only

## **Package Dimensions**

DIP20-P-300-2.54A Unit: mm

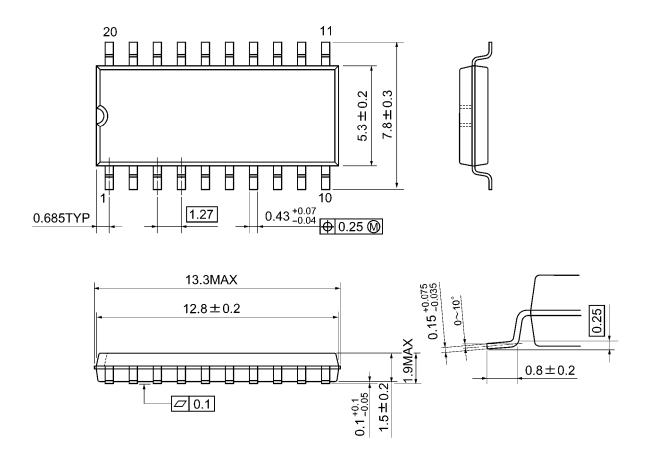


Weight: 1.30 g (typ.)



## **Package Dimensions**

SOP20-P-300-1.27A Unit: mm

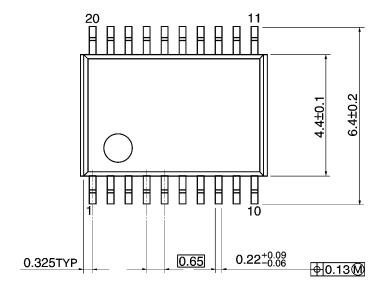


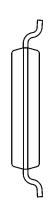
Weight: 0.22 g (typ.)

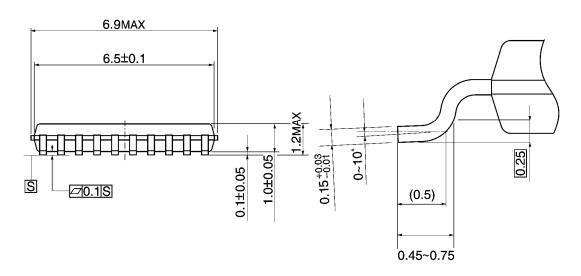
## **Package Dimensions**

TSSOP20-P-0044-0.65A

Unit: mm







Weight: 0.08 g (typ.)

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