



BUK768R3-60E

N-channel TrenchMOS standard level FET

13 July 2012

Product data sheet

1. Product profile

1.1 General description

Standard level N-channel MOSFET in a SOT404 package using TrenchMOS technology. This product has been designed and qualified to AEC Q101 standard for use in high performance automotive applications.

1.2 Features and benefits

- AEC Q101 compliant
- Repetitive avalanche rated
- Suitable for thermally demanding environments due to 175 °C rating
- True standard level gate with VGS(th) rating of greater than 1V at 175 °C

1.3 Applications

- 12 V Automotive systems
- Motors, lamps and solenoid control
- Start-Stop micro-hybrid applications
- Transmission control
- Ultra high performance power switching

1.4 Quick reference data

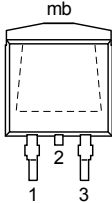
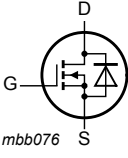
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V _{DS}	drain-source voltage	T _J ≥ 25 °C; T _J ≤ 175 °C		-	-	60	V
I _D	drain current	V _{GS} = 10 V; T _{mb} = 25 °C; Fig. 1	[1]	-	-	75	A
P _{tot}	total power dissipation	T _{mb} = 25 °C; Fig. 2		-	-	137	W
Static characteristics							
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 20 A; T _J = 25 °C; Fig. 11		-	5.9	8.3	mΩ
Dynamic characteristics							
Q _{GD}	gate-drain charge	I _D = 20 A; V _{DS} = 48 V; V _{GS} = 10 V; Fig. 14		-	14.6	-	nC

[1] Continuous current is limited by package.

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 D2PAK (SOT404)	 mbb076
2	D	drain		
3	S	source		
mb	D	mounting base; connected to drain		

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK768R3-60E	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

4. Limiting values

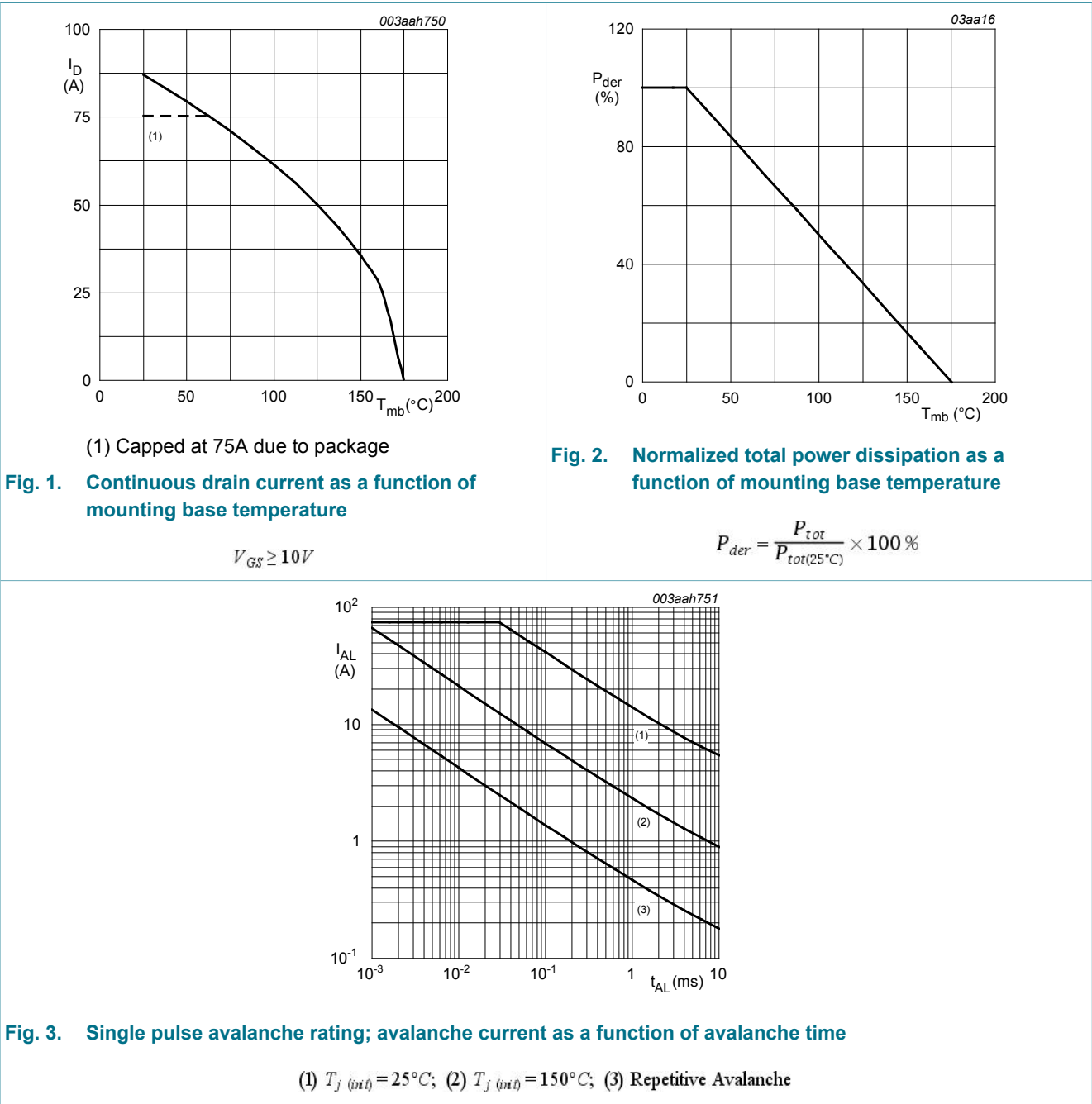
Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$		-	60	V
V_{DGR}	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$		-	60	V
V_{GS}	gate-source voltage	$T_j = 25\text{ °C}$		-20	20	V
I_D	drain current	$T_{mb} = 25\text{ °C}$; $V_{GS} = 10\text{ V}$; Fig. 1	[1]	-	75	A
		$T_{mb} = 100\text{ °C}$; $V_{GS} = 10\text{ V}$; Fig. 1		-	61.5	A
I_{DM}	peak drain current	$T_{mb} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$; Fig. 4		-	349	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 2		-	137	W
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C
Source-drain diode						
I_S	source current	$T_{mb} = 25\text{ °C}$	[1]	-	75	A
I_{SM}	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$		-	349	A

Symbol	Parameter	Conditions		Min	Max	Unit
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 75\text{ A}$; $V_{sup} \leq 60\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 60\text{ V}$; $T_{j(init)} = 25\text{ }^\circ\text{C}$; unclamped; Fig. 3	[2][3]	-	86	mJ

- [1] Continuous current is limited by package.
- [2] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
- [3] Refer to application note AN10273 for further information.



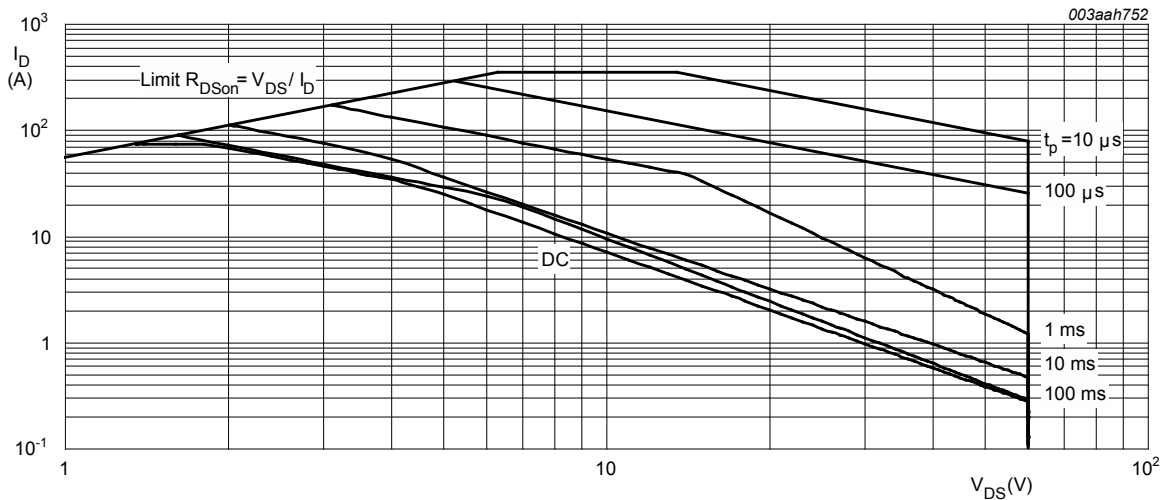


Fig. 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$T_{mb} = 25^{\circ}C$; I_{DM} is a single pulse

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	-	1.09	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	minimum footprint ; mounted on a printed-circuit board	-	50	-	K/W

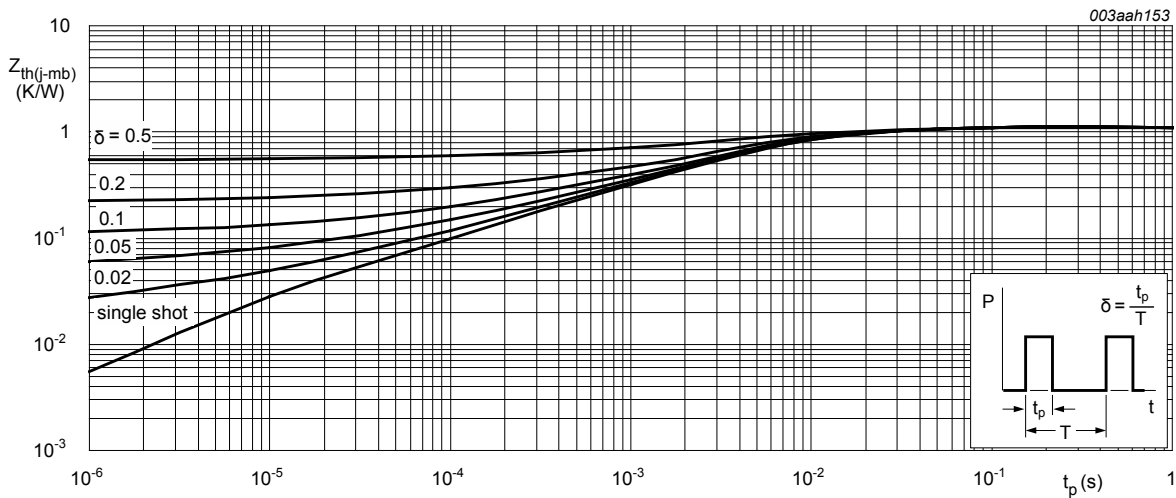


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 250 μA; V _{GS} = 0 V; T _j = 25 °C		60	-	-	V
		I _D = 250 μA; V _{GS} = 0 V; T _j = -55 °C		54	-	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} = V _{GS} ; T _j = 25 °C; Fig. 9; Fig. 10		2.4	3	4	V
		I _D = 1 mA; V _{DS} = V _{GS} ; T _j = 175 °C; Fig. 9		1	-	-	V
		I _D = 1 mA; V _{DS} = V _{GS} ; T _j = -55 °C; Fig. 9		-	-	4.5	V
I _{DSS}	drain leakage current	V _{DS} = 60 V; V _{GS} = 0 V; T _j = 25 °C		-	0.04	1	μA
		V _{DS} = 60 V; V _{GS} = 0 V; T _j = 175 °C		-	-	500	μA
I _{GSS}	gate leakage current	V _{GS} = 20 V; V _{DS} = 0 V; T _j = 25 °C		-	2	100	nA
		V _{GS} = -20 V; V _{DS} = 0 V; T _j = 25 °C		-	2	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 20 A; T _j = 25 °C; Fig. 11		-	5.9	8.3	mΩ
		V _{GS} = 10 V; I _D = 20 A; T _j = 175 °C; Fig. 11; Fig. 12		-	-	18	mΩ
Dynamic characteristics							
Q _{G(tot)}	total gate charge	I _D = 20 A; V _{DS} = 48 V; V _{GS} = 10 V; Fig. 13; Fig. 14		-	43.1	-	nC
Q _{GS}	gate-source charge	I _D = 20 A; V _{DS} = 48 V; V _{GS} = 10 V; Fig. 14		-	10.9	-	nC
Q _{GD}	gate-drain charge			-	14.6	-	nC
C _{iss}	input capacitance	V _{GS} = 0 V; V _{DS} = 25 V; f = 1 MHz; T _j = 25 °C; Fig. 15		-	2188	2920	pF
C _{oss}	output capacitance			-	319	383	pF
C _{rss}	reverse transfer capacitance			-	205	281	pF
t _{d(on)}	turn-on delay time	V _{DS} = 45 V; R _L = 2 Ω; V _{GS} = 10 V; R _{G(ext)} = 5 Ω		-	14	-	ns
t _r	rise time			-	27	-	ns
t _{d(off)}	turn-off delay time			-	27	-	ns
t _f	fall time			-	27	-	ns
L _D	internal drain inductance	from upper edge of mounting base to centre of die		-	2.5	-	nH
L _S	internal source inductance	measured from source lead to source bond pad		-	7.5	-	nH

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 20\text{ A}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ °C}$; Fig. 16	-	0.84	1.2	V
t_{rr}	reverse recovery time	$I_S = 20\text{ A}$; $di_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$;	-	27	-	ns
Q_r	recovered charge	$V_{DS} = 25\text{ V}$	-	24	-	nC

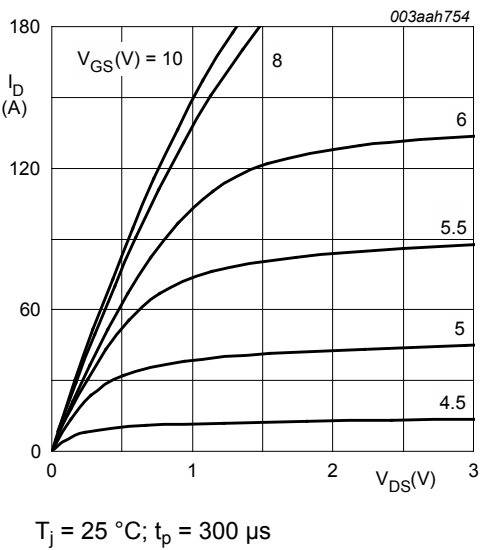


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

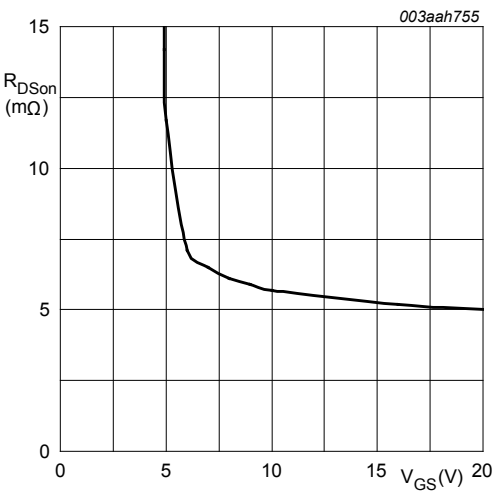


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

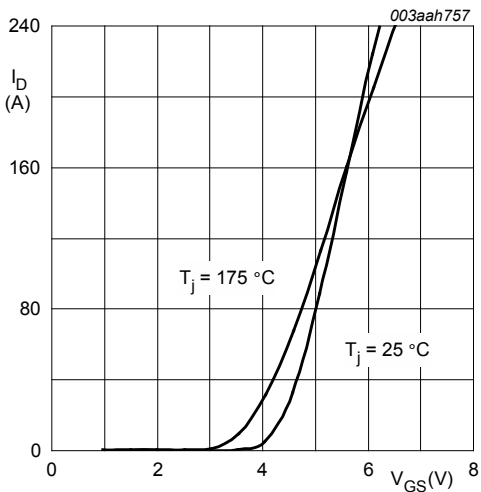


Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values

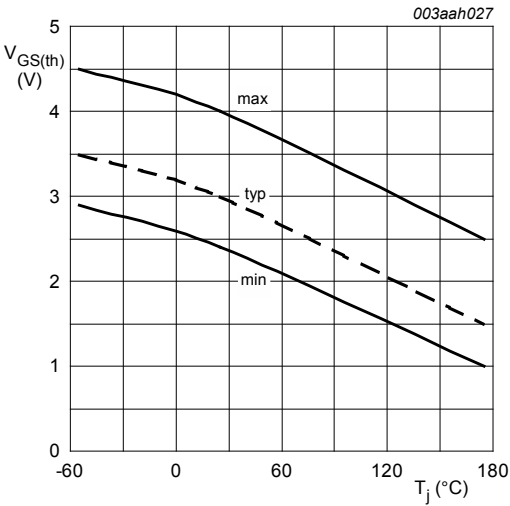


Fig. 9. Gate-source threshold voltage as a function of junction temperature

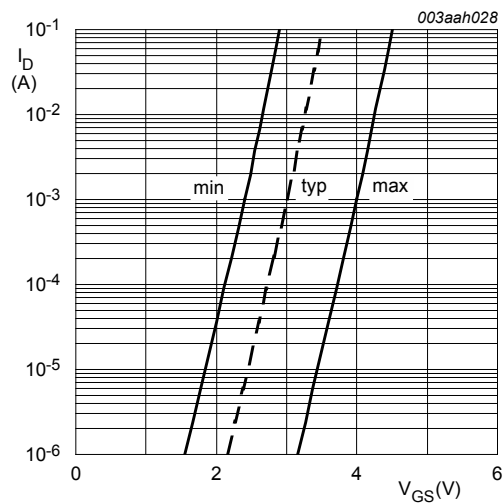


Fig. 10. Sub-threshold drain current as a function of gate-source voltage

$T_j = 25^{\circ}\text{C}; V_{DS} = 5\text{V}$

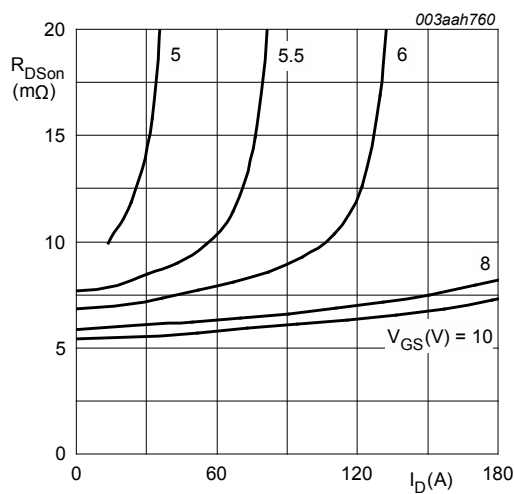


Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

$T_j = 25^{\circ}\text{C}; t_p = 300\text{ }\mu\text{s}$

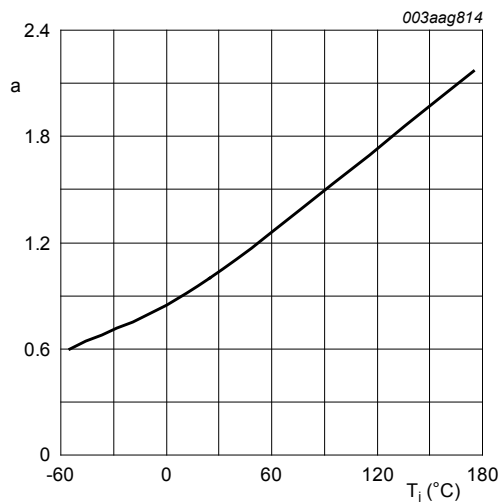


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}\text{C})}}$$

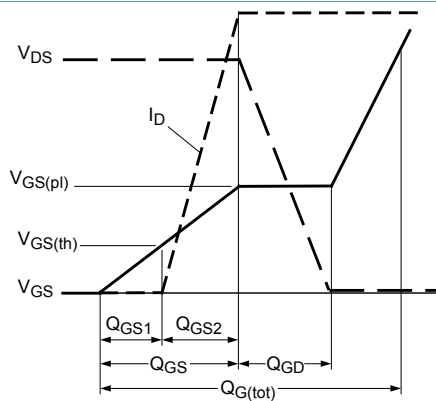


Fig. 13. Gate charge waveform definitions

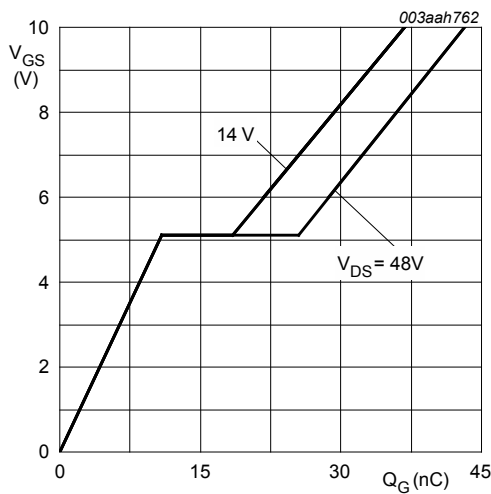


Fig. 14. Gate-source voltage as a function of gate charge; typical values

$T_j = 25^{\circ}\text{C}; I_D = 20\text{ A}$

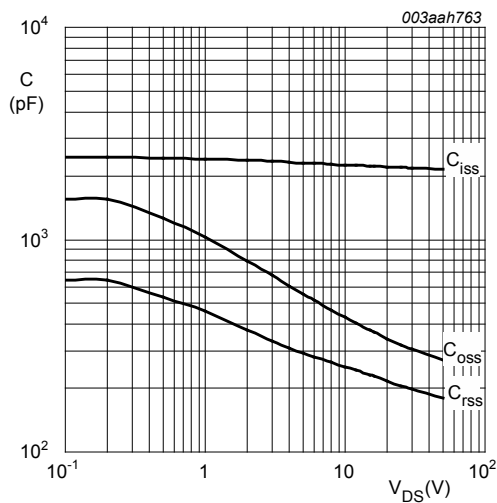


Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$V_{GS} = 0\text{ V}; f = 1\text{ MHz}$

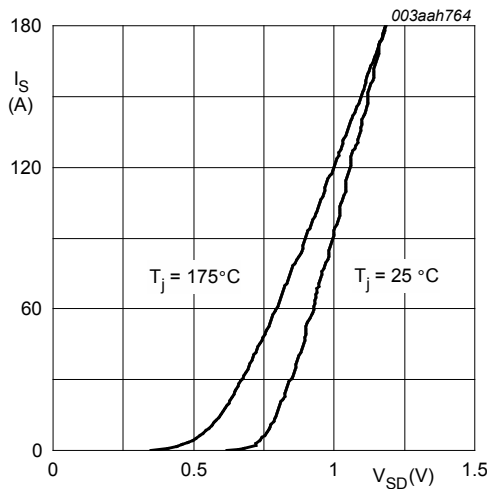


Fig. 16. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

$V_{GS} = 0\text{ V}$

7. Package outline

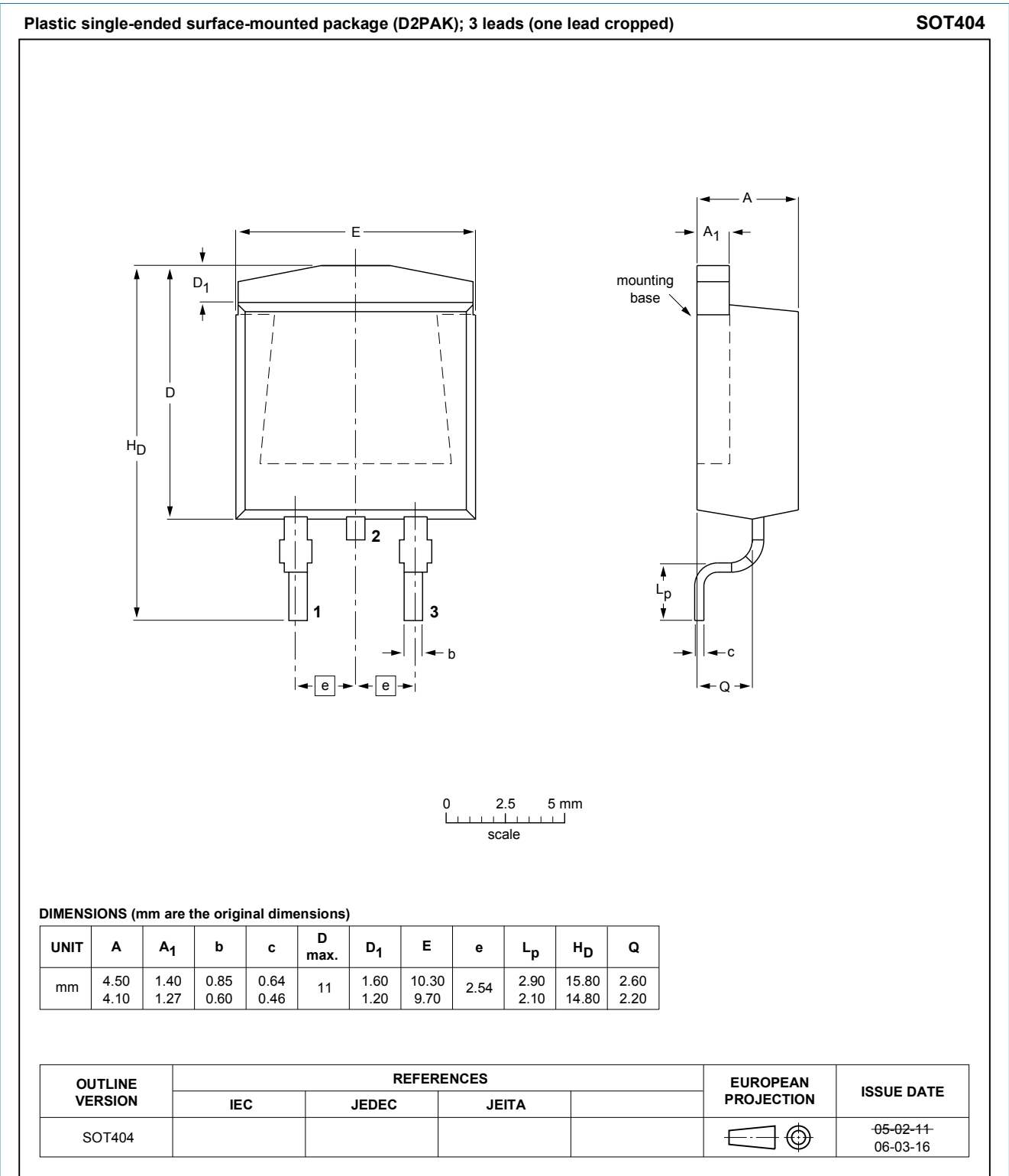


Fig. 17. D2PAK (SOT404)

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Офис по работе с юридическими лицами:

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

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