

# PYTHON 480

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## PYTHON 0.48 Megapixel Global Shutter CMOS Image Sensor



**ON Semiconductor®**

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### FEATURES

- 808 x 608 Active Pixels, 1/3.6" Optical Format
- 4.8  $\mu\text{m}$  x 4.8  $\mu\text{m}$  Low Noise Global Shutter Pixels with In-pixel CDS
- Monochrome (SN, SP), Color (SE, SF)
- Wide CRA Options (SP, SF)
- Frame Rate up to 120 fps at Full Resolution
- On-chip 10-bit Analog-to-Digital Converter (ADC)
- 10-bit Output Mode
- One Low Voltage Differential Signaling (LVDS) High Speed Serial Output or Parallel CMOS Output
- Random Programmable Region of Interest (ROI) Readout
- Serial Peripheral Interface (SPI)
- Automatic Exposure Control (AEC)
- Phase Locked Loop (PLL)
- Dual Power Supply (3.3 V and 1.8 V)
- $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  Operational Temperature Range
- 67 pin CSP
- 265 mW / 226 mW Power Dissipation (LVDS 120 fps / 60 fps)
- These Devices are Pb-Free and are RoHS Compliant

### APPLICATIONS

- Machine Vision
- Motion Monitoring
- Security
- Bar Code Scanning

### DESCRIPTION

The PYTHON 480 image sensor utilizes high sensitivity 4.8  $\mu\text{m}$  x 4.8  $\mu\text{m}$  pixels that support low noise “pipelined” and “triggered” global shutter readout modes. In global shutter mode, the sensors support correlated double sampling (CDS) readout, reducing noise and increasing dynamic range.

The image sensors have on-chip programmable gain amplifiers and 10-bit A/D converters. The integration time and gain parameters can be reconfigured without any visible image artifact. Optionally the on-chip automatic exposure control loop (AEC) controls these parameters dynamically. The image’s black level is either calibrated automatically or can be adjusted by a user programmable offset.

A high level of programmability using a four wire serial peripheral interface enables the user to read out specific regions of interest. Up to four regions can be programmed, achieving even higher frame rates.

The image data interface consists of one LVDS data lane, facilitating frame rate up to 120 frames per second. A separate synchronization channel containing payload information is provided to facilitate the image reconstruction at the receiving end. The device also provides a parallel CMOS output interface at the same frame rate.

The PYTHON 480 is packaged in a 67-pin CSP package and is available in monochrome and Bayer color configurations with standard and wide CRA options.

# PYTHON 480

## ORDERING INFORMATION

| Part Number       | Description                            | MPQ | Package     |
|-------------------|--|-----|-------------|
| NOIP1SN0480A-STI  | 0.48 MegaPixel, Monochrome, CRA 1.65   | 100 | 67-ball CSP |
| NOIP1SE0480A-STI  | 0.48 MegaPixel, Bayer Color, CRA 1.65  |     |             |
| NOIP1SP0480A-STI  | 0.48 MegaPixel, Monochrome, CRA 23.59  |     |             |
| NOIP1SF0480A-STI  | 0.48 MegaPixel, Bayer Color, CRA 23.59 |     |             |
| NOIP1SN0480A-STI1 | 0.48 MegaPixel, Monochrome, CRA 1.65   | 10  |             |
| NOIP1SE0480A-STI1 | 0.48 MegaPixel, Bayer Color, CRA 1.65  |     |             |
| NOIP1SP0480A-STI1 | 0.48 MegaPixel, Monochrome, CRA 23.59  |     |             |
| NOIP1SF0480A-STI1 | 0.48 MegaPixel, Bayer Color, CRA 23.59 |     |             |

NOTE: More details on the part coding can be found at [http://www.onsemi.com/pub\\_link/Collateral/TND310-D.PDF](http://www.onsemi.com/pub_link/Collateral/TND310-D.PDF)

## PRODUCTION MARK

| Part Number           | 10-Digit Package Mark |
|-----------------------|-----------------------|
| NOIP1SN0480A-STI/STI1 | SN480 YM NNN          |
| NOIP1SE0480A-STI/STI1 | SE480 YM NNN          |
| NOIP1SP0480A-STI/STI1 | SP480 YM NNN          |
| NOIP1SF0480A-STI/STI1 | SF480 YM NNN          |

where Y is 1-digit year, M is the 1-digit month, NNN is the 3-digit serial number for wafer identification

# PYTHON 480

## SPECIFICATIONS

### Key Specifications

**Table 1. GENERAL SPECIFICATIONS**

| Parameter         | Specification   |
|-------------------|---|
| Pixel type        | In-pixel CDS. Global shutter pixel architecture   |
| Shutter type      | Pipelined and triggered global shutter  |
| Frame rate        | up to 120fps (Full Frame readout)   |
| Master clock      | LVDS Mode:<br>68 MHz when PLL is used,<br>340 MHz (10-bit) / 272 MHz (8-bit)<br>when PLL is not used<br>CMOS Mode: 68 MHz |
| Windowing         | 4 Randomly programmable windows.<br>Normal, sub-sampled and binned<br>readout modes                                       |
| ADC resolution    | 10-bit  |
| LVDS outputs      | data + sync + clock   |
| CMOS outputs      | 10-bit parallel output, frame_valid,<br>line_valid, clock   |
| Data rate         | LVDS Mode:<br>1 x 680 Mbps (10-bit)<br>CMOS Mode: 68 MHz  |
| Power dissipation | LVDS mode: 265 mW,<br>CMOS mode: 226 mW   |
| Package type      | 67-pin CSP  |

NOTE: All numbers listed are for 1x gain condition unless otherwise noted.

**Table 2. ELECTRO-OPTICAL SPECIFICATIONS**

| Parameter                         | Specification  |
|-----------------------------------|--|
| Active pixels                     | 808 (H) x 608 (V)  |
| Pixel size                        | 4.8 $\mu\text{m}$ x 4.8 $\mu\text{m}$                      |
| Conversion gain                   | 0.096 LSB10/e <sup>-</sup><br>140 $\mu\text{V}/\text{e}^-$ |
| Dark temporal noise               | < 11 e <sup>-</sup>  |
| Responsivity at 550 nm            | 7.7 V/lux.s  |
| Parasitic Light Sensitivity (PLS) | <1/6300  |
| Full Well Charge                  | 10000 e <sup>-</sup>                                       |
| Quantum Efficiency at 550 nm      | 56%  |
| Pixel FPN                         | < 1.0 LSB10  |
| PRNU                              | < 1%   |
| MTF                               | 62% @ 535 nm – X-dir & Y-dir                               |
| PSNL at 20°C                      | 200 LSB10/s, 2000 e <sup>-</sup> /s                        |
| Dark signal at 20°C               | 5 e <sup>-</sup> /s, 0.5 LSB10/s                           |
| Dynamic Range                     | > 59 dB  |
| Signal to Noise Ratio (SNR max)   | 40 dB  |

NOTE: All numbers listed are for 1x analog gain condition unless otherwise noted.

**Table 3. RECOMMENDED OPERATING RATINGS** (Note 1)

| Symbol         | Description                 | Min | Max | Unit |
|----------------|-----------------------------|-----|-----|------|
| T <sub>J</sub> | Operating temperature range | -40 | 85  | °C   |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

1. Performance parameters may degrade above 60°C.

**Table 4. ABSOLUTE MAXIMUM RATINGS** (Note 4)

| Symbol                        | Parameter                               | Min  | Max | Unit |
|-------------------------------|---|------|-----|------|
| ABS (1.8 V supply group)      | ABS rating for 1.8 V supply group       | -0.5 | 2.2 | V    |
| ABS (3.3 V supply group)      | ABS rating for 3.3 V supply group       | -0.5 | 3.8 | V    |
| T <sub>S</sub>                | ABS storage temperature range           | -40  | 150 | °C   |
|                               | ABS storage humidity range at 85°C      |      | 85  | %RH  |
| Electrostatic discharge (ESD) | Human Body Model (HBM): JS-001          | 2000 |     | V    |
|                               | Charged Device Model (CDM): JESD22-C101 | 500  |     |      |
| LU                            | Latch-up: JESD-78                       | 100  |     | mA   |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. The ADC is 11-bit, down-scaled to 10-bit. The PYTHON uses a larger word-length internally to provide 10-bit on the output.

3. Operating ratings are conditions in which operation of the device is intended to be functional.

4. ON Semiconductor recommends that customers become familiar with, and follow the procedures in JEDEC Standard JESD625-A. Refer to Application Note AN52561. Long term exposure toward the maximum storage temperature will accelerate color filter degradation.

# PYTHON 480

**Table 5. ELECTRICAL SPECIFICATIONS**

**Boldface limits apply for  $T_J = T_{MIN}$  to  $T_{MAX}$ , all other limits  $T_J = +30^\circ\text{C}$ .** (Notes 5, 6, 7, 8)

| Parameter  | Description   | Min          | Typ  | Max         | Unit |
|--|---|--------------|------|-------------|------|
| <b>Power Supply Parameters – LVDS</b>  |   |              |      |             |      |
| (NOTE: All ground pins (gnd_18, gnd_33, gnd_colpc) should be connected to an external 0 V ground reference.) |   |              |      |             |      |
| vdd_33   | Supply voltage, 3.3 V                                     | <b>3.2</b>   | 3.3  | <b>3.4</b>  | V    |
| Idd_33   | Current consumption 3.3 V supply                          |              | 48   |             | mA   |
| vdd_18   | Supply voltage, 1.8 V                                     | <b>1.7</b>   | 1.8  | <b>1.9</b>  | V    |
| Idd_18   | Current consumption 1.8 V supply                          |              | 59   |             | mA   |
| vdd_pix  | Supply voltage, pixel                                     | <b>3.25</b>  | 3.3  | <b>3.35</b> | V    |
| Idd_pix  | Current consumption pixel supply                          |              | 0.04 |             | mA   |
| Ptot   | Total power consumption at vdd_33 = 3.3 V, vdd_18 = 1.8 V |              | 265  |             | mW   |
| Pstby_lp   | Power consumption in low power standby mode               |              | < 1  |             | mW   |
| Popt   | Power consumption at lower pixel rates                    | Configurable |      |             |      |

**Power Supply Parameters – CMOS**

|          |   |              |      |             |    |
|----------|---|--------------|------|-------------|----|
| vdd_33   | Supply voltage, 3.3 V                       | <b>3.2</b>   | 3.3  | <b>3.4</b>  | V  |
| Idd_33   | Current consumption 3.3 V supply            |              | 48   |             | mA |
| vdd_18   | Supply voltage, 1.8 V                       | <b>1.7</b>   | 1.8  | <b>1.9</b>  | V  |
| Idd_18   | Current consumption 1.8 V supply            |              | 37   |             | mA |
| vdd_pix  | Supply voltage, pixel                       | <b>3.25</b>  | 3.3  | <b>3.35</b> | V  |
| Idd_pix  | Current consumption pixel supply            |              | 0.04 |             | mA |
| Ptot     | Total power consumption                     |              | 226  |             | mW |
| Pstby_lp | Power consumption in low power standby mode |              | < 1  |             | mW |
| Popt     | Power consumption at lower pixel rates      | Configurable |      |             |    |

**I/O – LVDS (EIA/TIA-644): Conforming to standard/additional specifications and deviations listed**

|           |   |     |      |     |      |
|-----------|---|-----|------|-----|------|
| fserdata  | Data rate on data channels<br>DDR signaling – 1 data channel, 1 synchronization channel |     |      | 680 | Mbps |
| fserclock | Clock rate of output clock<br>Clock output for mesochronous signaling                   |     |      | 340 | MHz  |
| Vicm      | LVDS input common mode level  | 0.3 | 1.25 | 1.8 | V    |
| Tccsk     | Channel to channel skew (Training pattern allows per channel skew correction)           |     | 50   |     | ps   |

**I/O – CMOS 1.8 V Signal levels (Note 9)**

|          |   |      |  |     |      |
|----------|---|------|--|-----|------|
| fpardata | Data rate on parallel channels (10-bit) |      |  | 68  | Mbps |
| ViL      | CMOS input low level                    | -0.2 |  | 0.8 | V    |
| ViH      | CMOS input high level                   | 1.2  |  | 3.6 | V    |

**Electrical Interface – LVDS**

|     |                                    |  |     |  |     |
|-----|------------------------------------|--|-----|--|-----|
| fin | Input clock rate when PLL used     |  | 68  |  | MHz |
|     | Input clock rate when PLL not used |  | 340 |  |     |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. All parameters are characterized for DC conditions after thermal equilibrium is established.

6. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is recommended that normal precautions be taken to avoid application of any voltages higher than the maximum rated voltages to this high impedance circuit.

7. Minimum and maximum limits are guaranteed through test and design.

8. Refer to ACSPYTHON480 available at the Image Sensor Portal for detailed acceptance criteria specifications.

9. CMOS inputs are compatible with 3.3 V signal levels.

10. Longer integration times are possible, but with possible image quality trade-offs.

11. Data is clocked on the rising edge of the output clock. This can be changed to the falling edge by register 130[8]

# PYTHON 480

**Table 5. ELECTRICAL SPECIFICATIONS** (continued)

**Boldface limits apply for  $T_J = T_{MIN}$  to  $T_{MAX}$ , all other limits  $T_J = +30^\circ\text{C}$ .** (Notes 5, 6, 7, 8)

| Parameter                          | Description                             | Min | Typ | Max | Unit |
|------------------------------------|---|-----|-----|-----|------|
| <b>Electrical Interface – LVDS</b> |   |     |     |     |      |
| tidc                               | Input clock duty cycle when PLL used    | 45  | 50  | 55  | %    |
| ratspi<br>(= fin/fspi)             | 10-bit, PLL used (fin = 68 MHz)         | 6   |     |     |      |
|                                    | 10-bit, LVDS input used (fin = 340 MHz) | 30  |     |     |      |

**Electrical Interface – CMOS**

|                        |                                    |           |     |     |     |
|------------------------|------------------------------------|-----------|-----|-----|-----|
| Cout                   | Output load (only capacitive load) |           |     | 10  | pF  |
| Tr                     | Output Rise Time                   | 2.5       | 4.5 | 6.5 | ns  |
| Tf                     | Output Fall Time                   | 2         | 3.5 | 5   | ns  |
| fin                    | Input clock rate                   | <b>68</b> |     |     | MHz |
| tidc                   | Input clock Duty Cycle             | 45        | 50  | 55  | %   |
| ratspi<br>(= fin/fspi) | 10-bit (fin = 68 MHz)              | 6         |     |     |     |
| todc                   | CLK_OUT duty cycle                 | 40        | 50  | 60  | %   |
| t <sub>CD</sub>        | CLK_OUT to DOUTx (Note 11)         |           |     | 4   | ns  |
| t <sub>CFH</sub>       | CLK_OUT to FRAME_VALID HIGH        |           |     | 4   | ns  |
| t <sub>CFL</sub>       | CLK_OUT to FRAME_VALID LOW         |           |     | 4   | ns  |
| t <sub>CLH</sub>       | CLK_OUT to LINE_VALID HIGH         |           |     | 4   | ns  |
| t <sub>CLL</sub>       | CLK_OUT to LINE_VALID LOW          |           |     | 4   | ns  |

**Frame Specifications – LVDS**

|         |  |       |  |                  |        |
|---------|--|-------|--|------------------|--------|
| T_int   | Integration Time range                           | 0.035 |  | 100<br>(Note 10) | ms     |
| fps     | Frame rate at full resolution (800 x 600 pixels) |       |  | 120              | fps    |
| fps_roi | Frame rate at 640 x 480 pixels resolution        |       |  | 180              | fps    |
| fpix    | Pixel rate                                       |       |  | 68               | Mpix/s |

**Frame Specifications – CMOS**

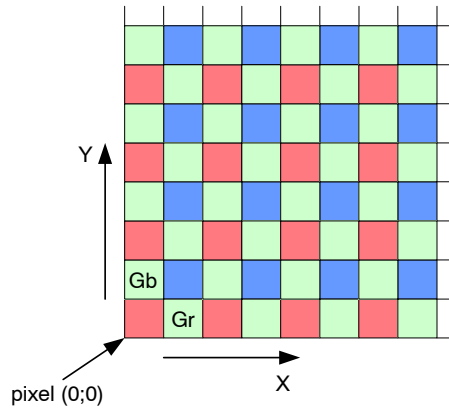
|     |  |  |     |  |     |
|-----|--|--|-----|--|-----|
| fps | Frame rate at full resolution (800 x 600 pixels) |  | 120 |  | fps |
|-----|--|--|-----|--|-----|

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. All parameters are characterized for DC conditions after thermal equilibrium is established.
6. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is recommended that normal precautions be taken to avoid application of any voltages higher than the maximum rated voltages to this high impedance circuit.
7. Minimum and maximum limits are guaranteed through test and design.
8. Refer to ACSPYTHON480 available at the Image Sensor Portal for detailed acceptance criteria specifications.
9. CMOS inputs are compatible with 3.3 V signal levels.
10. Longer integration times are possible, but with possible image quality trade-offs.
11. Data is clocked on the rising edge of the output clock. This can be changed to the falling edge by register 130[8]

**Color Filter Array**

The sensor is processed with a Bayer RGB color pattern as shown in Figure 1. Pixel (0,0) has a red filter situated to the bottom left.



**Figure 1. Color Filter Array for the Pixel Array**

**Quantum Efficiency**



**Figure 2. Quantum Efficiency Curve for Mono and Color**

**Ray Angle and Microlens Array Information**

An array of microlenses is placed over the CMOS pixel array in order to improve the absolute responsivity of the photodiodes. The combined microlens array and pixel array has two important properties:

1. Angular dependency of photoresponse of a pixel

The photoresponse of a pixel with microlens in the center of the array to a fixed optical power with varied incidence angle is as plotted in Figure 3, where definitions of angles  $\phi_x$  and  $\phi_y$  are as described by Figure 4.

2. Microlens shift across array and CRA

The microlens array is fabricated with a slightly smaller pitch than the array of photodiodes. This difference in pitch creates a varying degree of shift of a pixel's microlens with regards to its photodiode. A shift in microlens position

versus photodiode position will cause a tilted angle of peak photoresponse, here denoted Chief Ray Angle (CRA). Microlenses and photodiodes are aligned with 0 shift and CRA in the center of the array, while the shift and CRA increases radially towards its edges, as illustrated by Figure 5.

The purpose of the shifted microlenses is to improve the uniformity of photoresponse when camera lenses with a finite exit pupil distance are used. The CRA varies nearly linearly with distance from the center as illustrated in Figure 6, with a corner CRA of approximately 1.65 degrees. This edge CRA is matching a lens with exit pupil distance of ~ 60 mm.

Another CRA option targeting 23.59 degrees is available for both mono and color versions. The corresponding curves for this version is shown in figures 8 and 9.



Note that the photoresponse peaks near normal incidence for center pixels.

**Figure 3. Central Pixel Photoresponse to a Fixed Optical Power with Incidence Angle varied along  $\phi_x$  and  $\phi_y$  (Low CRA Version)**



Figure 4. Definition of Angles used in Figure 3.



The Center Axes of the Microlens and the Photodiode Coincide for the Center Pixels. For the Edge Pixels, there is a Shift between the Axes of the Microlens and the Photodiode causing a Peak Response Incidence Angle (CRA) that deviates from the Normal of the Pixel Array.

Figure 5. Principles of Microlens Shift



Figure 6. Variation of Peak Responsivity Angle (CRA) as a Function of Distance from the Center of the Array (Low CRA Version)



PYTHON 480



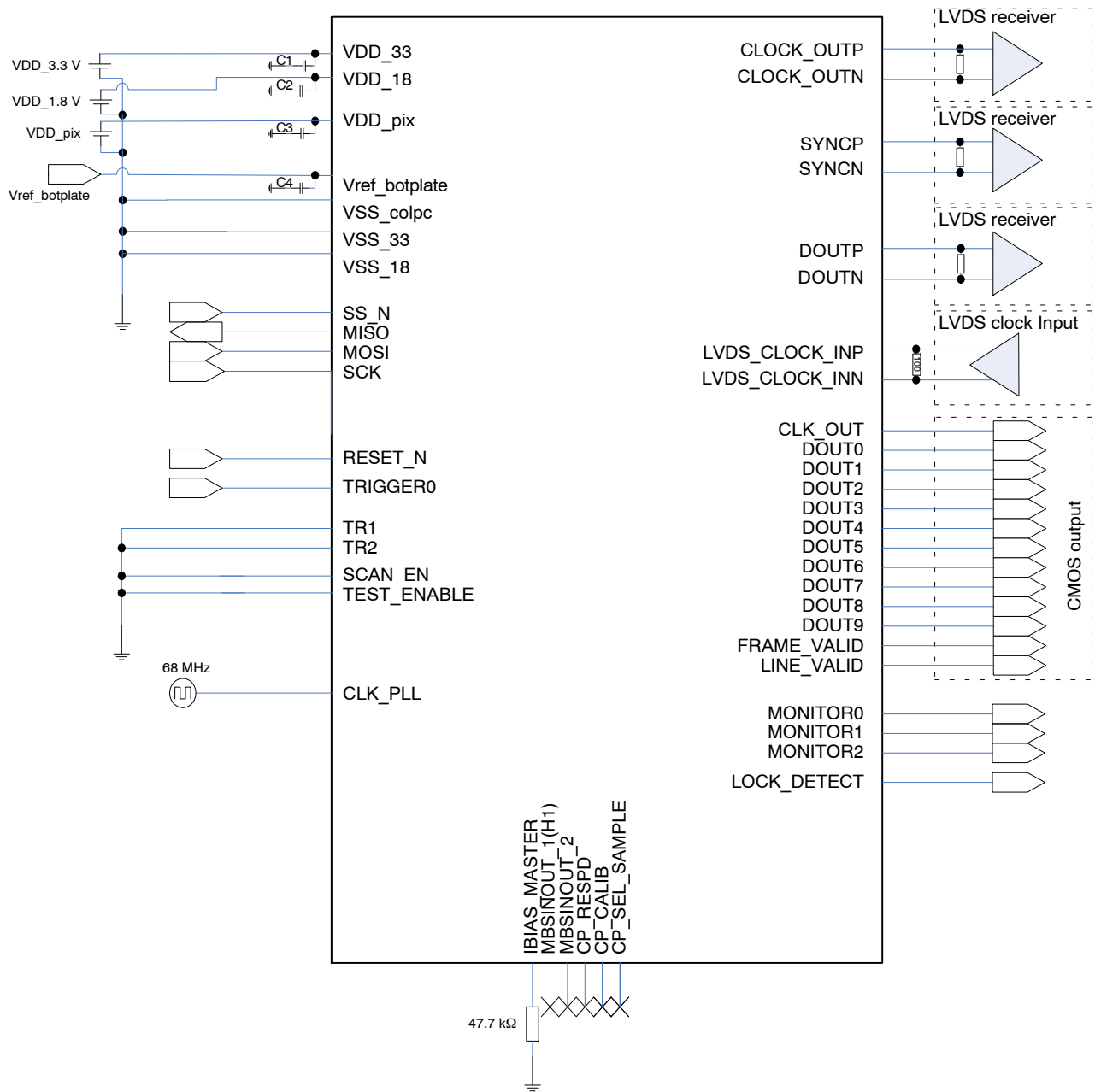
Note that the photoresponse peaks near normal incidence for center pixels.

Figure 7. Central Pixel Photoresponse to a Fixed Optical Power with Incidence Angle varied along  $\phi_x$  and  $\phi_y$  (High CRA Version)



Figure 8. Variation of Peak Responsivity Angle (CRA) as a Function of Distance from the Center of the Array (High CRA Version)

# PYTHON 480



## NOTES:

- Vref\_botplate power needs to allow source and sink; load is < 20 mA
- vdd\_pix is 3.3 V low noise power supply. Verify tolerance allowed in Table 5.
- Place low inductance bypass capacitors as close as possible to all power pins (10  $\mu$ F and 100 nF)
- LVDS lines: Route the differential output traces close together to maximize common-mode rejection with the 100  $\Omega$  termination resistor close to the receiver. User should pay attention to printed circuit board (PCB) trace lengths to minimize any delay skew.

**Figure 9. Typical Application Diagram**

# PYTHON 480

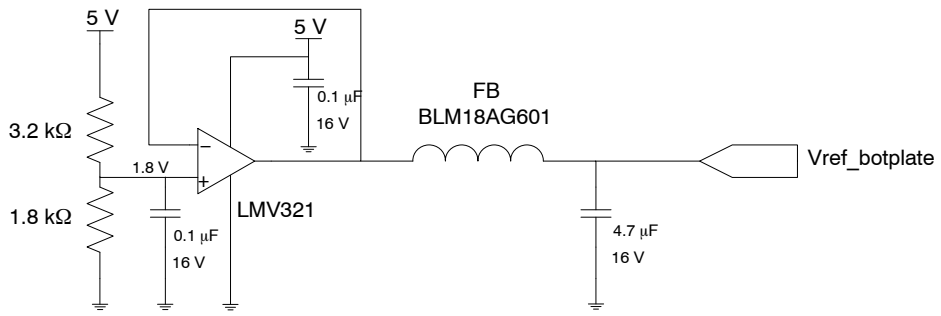


Figure 10. Recommended Circuit for Vref\_botplate Signal Generation

OVERVIEW

Figure 11 gives an overview of the major functional blocks of the sensor.



Figure 11. Block Diagram

**Image Core**

The image core consists of:

- Pixel Array
- Address Decoders and Row Drivers
- Pixel Biasing

The PYTHON 480 pixel array contains 808 (H) x 608 (V) readout pixels with a pixel pitch of 4.8  $\mu\text{m}$ , inclusive of 8 pixel rows and 8 pixel columns at every side to allow for reprocessing or color reconstruction. The sensors use in-pixel CDS architecture, which makes it possible to achieve a low noise read out of the pixel array in global shutter mode with CDS.

The function of the row drivers is to access the image array line by line, or all lines together, to reset or read the pixel data. The row drivers are controlled by the on-chip sequencer and can access the pixel array.

The pixel biasing block guarantees that the data on a pixel is transferred properly to the column multiplexer when the row drivers select a pixel line for readout.

**Phase Locked Loop**

The PLL accepts a (low speed) clock and generates the required high speed clock. Input clock frequency is 68 MHz.

### LVDS Clock Receiver

The LVDS clock receiver receives an LVDS clock signal and distributes the required clocks to the sensor.

Input clock frequency is 340 MHz. The clock input needs to be terminated with a 100  $\Omega$  resistor.

### Column Multiplexer

All pixels of one image row are stored in the column sample-and-hold (S/H) stages. These stages store both the reset and integrated signal levels.

The data stored in the column S/H stages is read out through 2 parallel differential outputs operating at a frequency of 34 MHz. At this stage, the reset signal and integrated signal values are transferred into an FPN-corrected differential signal. A programmable gain of 1x, 2x, or 3.5x can be applied to the signal. The column multiplexer also supports read-1-skip-1 and read-2-skip-2 mode. Enabling this mode increases the frame rate, with a decrease in resolution but same field of view.

### Bias Generator

The bias generator generates all required reference voltages and bias currents used on chip. An external resistor of 47 k $\Omega$ , connected between pin IBIAS\_MASTER and gnd\_33, is required for the bias generator to operate properly.

### Analog Front End

The AFE contains 2 channels, each containing a PGA and a 10-bit ADC.

For each of the 2 channels, a pipelined 10-bit ADC is used to convert the analog image data into a digital signal, which is delivered to the data formatting block. A black calibration loop is implemented to ensure that the black level is mapped to match the correct ADC input level.

### Data Formatting

The data block receives data from two ADCs and multiplexes this data to one data stream. A cyclic redundancy check (CRC) code is calculated on the passing data.

A frame synchronization data block transmits synchronization codes such as frame start, line start, frame end, and line end indications.

The data block calculates a CRC once per line for every channel. This CRC code can be used for error detection at the receiving end.

### Serializer and LVDS Interface (LVDS Mode only)

The serializer and LVDS interface block receives the formatted data from the data formatting block. This data is serialized and transmitted by the LVDS 340 MHz output driver.

The maximum output data rate is 680 Mbps per channel.

In addition to the LVDS data outputs, two extra LVDS outputs are available. One of these outputs carries the output clock, which is skew aligned to the output data channels. The second LVDS output contains frame format synchronization codes to serve system-level image reconstruction.

### CMOS Interface

Frame synchronization information is communicated by means of frame and line valid strobes. Both CMOS and LVDS outputs are active at the same time. LVDS channels can be powered down through SPI control when using the CMOS outputs.

### Sequencer

The sequencer:

- Controls the image core. Starts and stops integration and control pixel readout.
- Operates the sensor in master or slave mode.
- Applies the window settings. Organizes readouts so that only the configured windows are read.
- Controls the column multiplexer and analog core. Applies gain settings and subsampling modes at the correct time, without corrupting image data.
- Starts up the sensor correctly when leaving standby mode.

### Automatic Exposure Control

The AEC block implements a control system to modulate the exposure of an image. Both integration time and gains are controlled by this block to target a predefined illumination level.

OPERATING MODES

**Global Shutter Mode**

The PYTHON 480 operates in pipelined or triggered global shuttering modes. In this mode, light integration takes place on all pixels in parallel, although subsequent readout is sequential. Figure 12 shows the integration and readout sequence for the global shutter. All pixels are light sensitive at the same period of time. The whole pixel core is reset

simultaneously and after the integration time all pixel values are sampled together on the storage node inside each pixel. The pixel core is read out line by line after integration. Note that the integration and readout can occur in parallel or sequentially. The integration starts at a certain period, relative to the frame start.



Figure 12. Global Shutter Operation

**Pipelined Global Shutter Mode**

In pipelined global shutter mode, the integration and readout are done in parallel. Images are continuously read and integration of frame N is ongoing during readout of the previous frame N-1. The readout of every frame starts with a Frame Overhead Time (FOT), during which the analog value on the pixel diode is transferred to the pixel memory element. After the FOT, the sensor is read out line per line and the readout of each line is preceded by the Row

Overhead Time (ROT). Figure 13 shows the exposure and readout time line in pipelined global shutter mode.

*Master Mode*

In this mode, the integration time is set through the register interface and the sensor integrates and reads out the images autonomously. The sensor acquires images without any user interaction.

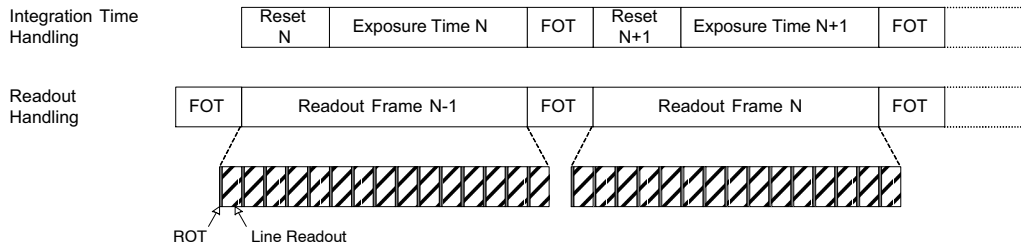


Figure 13. Integration and Readout for Pipelined Shutter

*Slave Mode*

The slave mode adds more manual control to the sensor. The integration time registers are ignored in this mode and the integration time is instead controlled by an external pin. As soon as the control pin is asserted, the pixel array goes out

of reset and integration starts. The integration continues until the user or system deasserts the external pin. Upon a falling edge of the trigger input, the image is sampled and the readout begins. Figure 14 shows the relation between the external trigger signal and the exposure/readout timing.



Figure 14. Pipelined Shutter Operated in Slave Mode

**Triggered Global Shutter Mode**

In this mode, manual intervention is required to control both the integration time and the start of readout. After the integration time, indicated by a user controlled pin, the image core is read out. After this sequence, the sensor goes to an idle mode until a new user action is detected.

The three main differences with the pipelined global shutter mode are:

- Upon user action, one single image is read.
- Normally, integration and readout are done sequentially. However, the user can control the sensor in such a way that two consecutive batches are overlapping, that is, having concurrent integration and readout.
- Integration and readout is under user control through an external pin.

This mode requires manual intervention for every frame. The pixel array is kept in reset state until requested.

The triggered global mode can also be controlled in a master or in a slave mode.

*Master Mode*

In this mode, a rising edge on the synchronization pin is used to trigger the start of integration and readout. The integration time is defined by a register setting. The sensor autonomously integrates during this predefined time, after which the FOT starts and the image array is readout sequentially. A falling edge on the synchronization pin does not have any impact on the readout or integration and subsequent frames are started again for each rising edge. Figure 15 shows the relation between the external trigger signal and the exposure/readout timing.

If a rising edge is applied on the external trigger before the exposure time and FOT of the previous frame is complete, it is ignored by the sensor.



Figure 15. Triggered Shutter Operated in Master Mode

*Slave Mode*

Integration time control is identical to the pipelined shutter slave mode. An external synchronization pin controls the start of integration. When it is de-asserted, the

FOT starts. The analog value on the pixel diode is transferred to the pixel memory element and the image readout can start. A request for a new frame is started when the synchronization pin is asserted again.

SENSOR OPERATION

Flowchart

Figure 16 shows the sensor operation flowchart. The sensor has six different 'states'. Every state is indicated with the oval circle. These states are Power off, Low power standby, Standby (1), Standby (2), Idle, Running.



Figure 16. Sensor Operation Flowchart



**Sensor States**

**Low Power Standby**

In low power standby state, all power supplies are on, but internally every block is disabled. No internal clock is running (PLL / LVDS clock receiver is disabled).

Only a subset of the SPI registers is active for read/write in order to be able to configure clock settings and leave the low power standby state. The only SPI registers that should be touched are the ones required for the ‘Enable Clock Management’ action described in Enable Clock Management – Part 1 on page NO TAG

**Standby (1)**

In standby state, the PLL/LVDS clock receiver is running, but the derived logic clock signal is not enabled.

**Standby (2)**

In standby state, the derived logic clock signal is running. All SPI registers are active, meaning that all SPI registers can be accessed for read or write operations. All other blocks are disabled.

**Idle**

In the idle state, all internal blocks are enabled, except the sequencer block. The sensor is ready to start grabbing images as soon as the sequencer block is enabled.

**Running**

In running state, the sensor is enabled and grabbing images. The sensor can be operated in global master/slave modes.

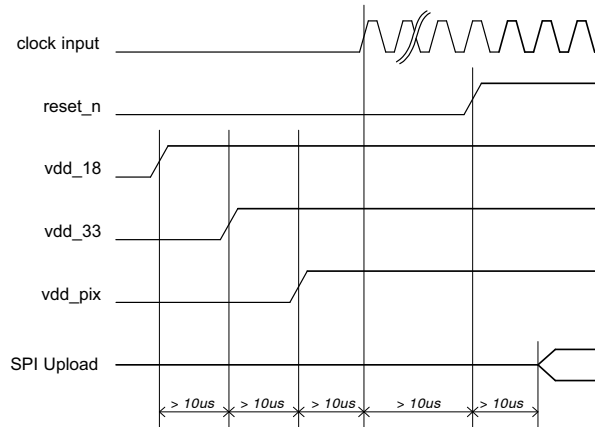
**User Actions: Power Up Functional Mode Sequences**

**Power Up Sequence**

Figure 17 shows the power up sequence of the sensor. The figure indicates that the first supply to ramp-up is the vdd\_18 supply, followed by vdd\_33 and vdd\_pix respectively. It is important to comply with the described sequence. Any other supply ramping sequence may lead to high current peaks and, as consequence, a failure of the sensor power up.

The clock input should start running when all supplies are stabilized. When the clock frequency is stable, the reset\_n signal can be de-asserted. After a wait period of 10 μs, the power up sequence is finished and the first SPI upload can be initiated.

NOTE: The ‘clock input’ can be LVDS clock input (lvds\_clock\_inn/p) in case the PLL is bypassed.



**Figure 17. Power Up Sequence**

**Enable Clock Management**

The ‘Enable Clock Management’ action configures the clock management blocks and activates the clock generation and distribution circuits in a pre-defined way. First, a set of clock settings must be uploaded through the SPI register. These settings are dependent on the desired operation mode of the sensor.

The SPI uploads that need to be executed to configure the sensor for LVDS 10-bit serial mode, with the PLL, as well as all other supported modes are available to customers under NDA at the ON Semiconductor Image Sensor Portal: <https://www.onsemi.com/PowerSolutions/myon/erCispFolder.do>

In the serial modes, if the PLL is not used, the LVDS clock input must be running.

**Use of Phase Locked Loop**

If PLL is used, the PLL is started after the upload of the SPI registers. The PLL requires (dependent on the settings) some time to generate a stable output clock. A lock detect circuit detects if the clock is stable. When complete, this is flagged in a status register.

Check the PLL\_lock flag 24[0] by reading the SPI register. When the flag is set, the ‘Enable Clock Management’ action can be continued. When PLL is not used, this step can be bypassed as shown in Figure 16 on page 16.

**Required Register Upload**

In this phase, the ‘reserved’ register settings are uploaded through the SPI register. Different settings are not allowed and may cause the sensor to malfunction. The required uploads can be downloaded from the MyON website.

**Soft Power Up**

During the soft power up action, the internal blocks are enabled and prepared to start processing the image data stream. This action exists of a set of SPI uploads.

**Enable Sequencer**

During the ‘Enable Sequencer’ action, the frame grabbing sequencer is enabled. The sensor starts grabbing images in the configured operation mode. Refer to Sensor States on page 17.

The ‘Enable Sequencer’ action consists of enabling bit 192[0].

**User Actions: Functional Modes to Power Down Sequences**

**Disable Sequencer**

During the ‘Disable Sequencer’ action, the frame grabbing sequencer is stopped. The sensor stops grabbing images and returns to the idle mode.

The ‘Disable Sequencer’ action consists of disabling bit 192[0].

**Soft Power Down**

During the soft power down action, the internal blocks are disabled and the sensor is put in standby state to reduce the current dissipation. This action exists of a set of SPI uploads.

**Disable Clock Management**

The ‘Disable Clock Management’ action stops the internal clocking to further decrease the power dissipation.

**Power Down Sequence**

Figure 18 illustrates the timing diagram of the preferred power down sequence. It is important that the sensor is in reset before the clock input stops running. Otherwise, the internal PLL becomes unstable and the sensor gets into an unknown state. This can cause high peak currents.

The same applies for the ramp down of the power supplies. The preferred order to ramp down the supplies is first vdd\_pix, second vdd\_33, and finally vdd\_18. Any other sequence can cause high peak currents.

NOTE: The ‘clock input’ can be the LVDS clock input (lvds\_clock\_inn/p) in case the PLL is bypassed.



**Figure 18. Power Down Sequence**

**Sensor Reconfiguration**

During the standby, idle, or running state several sensor parameters can be reconfigured.

- **Frame Rate and Exposure Time:** Frame rate and exposure time changes can occur during standby, idle, and running states by modifying registers 199 to 203. Refer to page 30–32 for more information.
- **Signal Path Gain:** Signal path gain changes can occur during standby, idle, and running states by modifying registers 204/205. Refer to page 37 for more information.
- **Windowing:** Changes with respect to windowing can occur during standby, idle, and running states. Refer to Multiple Window Readout on page 26 for more information.
- **Subsampling:** Changes of the subsampling mode can occur during standby, idle, and running states by modifying register 192. Refer to Subsampling on page 27 for more information.
- **Shutter Mode:** The shutter mode can only be changed during standby or idle mode by modifying register 192. Reconfiguring the shutter mode during running state is not supported.

**Sensor Configuration**

This device contains multiple configuration registers. Some of these registers can only be configured while the sensor is not acquiring images (while register 192[0] = 0), while others can be configured while the sensor is acquiring images. For the latter category of registers, it is possible to distinguish the register set that can cause corrupted images (limited number of images containing visible artifacts) from the set of registers that are not causing corrupted images.

These three categories are described here.

**Static Readout Parameters**

Some registers are only modified when the sensor is not acquiring images. Reconfiguration of these registers while images are acquired can cause corrupted frames or even interrupt the image acquisition. Therefore, it is recommended to modify these static configurations while the sequencer is disabled (register 192[0] = 0). The registers shown in Table 6 should not be reconfigured during image acquisition. A specific configuration sequence applies for these registers. Refer to the operation flow and startup description.

**Table 6. STATIC READOUT PARAMETERS**

| Group                    | Addresses | Description   |
|--------------------------|-----------|---|
| Clock generator          | 32        | Configure according to recommendation   |
| Image core               | 40        | Configure according to recommendation   |
| AFE                      | 48        | Configure according to recommendation   |
| Bias                     | 64–71     | Configure according to recommendation   |
| LVDS                     | 112       | Configure according to recommendation   |
| Sequencer mode selection | 192 [5:4] | Operation modes are: <ul style="list-style-type: none"> <li>• triggered_mode</li> <li>• slave_mode</li> </ul> |
| All reserved registers   |           | Keep reserved registers to their default state, unless otherwise described in the recommendation              |

**Dynamic Configuration Potentially Causing Image Artifacts**

The category of registers as shown in Table 7 consists of configurations that do not interrupt the image acquisition process, but may lead to one or more corrupted images during and after the reconfiguration. A corrupted image is an

image containing visible artifacts. A typical example of a corrupted image is an image which is not uniformly exposed.

The effect is transient in nature and the new configuration is applied after the transient effect.

**Table 7. DYNAMIC CONFIGURATION POTENTIALLY CAUSING IMAGE ARTIFACTS**

| Group                         | Addresses            | Description   |
|-------------------------------|----------------------|---|
| Black level configuration     | 128–129<br>197[12:8] | reconfiguration of these registers may have an impact on the black-level calibration algorithm. The effect is a transient number of images with incorrect black level compensation. |
| Sync codes                    | 129[13]<br>116–126   | Incorrect sync codes may be generated during the frame in which these registers are modified.   |
| Datablock test configurations | 144                  | Modification of these registers may generate incorrect test patterns during a transient frame.  |

**Dynamic Readout Parameters**

It is possible to reconfigure the sensor while it is acquiring images. Frame related parameters are internally resynchronized to frame boundaries, such that the modified parameter does not affect a frame that has already started. However, there can be restrictions to some registers as

shown in Table 8. Some reconfiguration may lead to one frame being blanked. This happens when the modification requires more than one frame to settle. The image is blanked out and training patterns are transmitted on the data and sync channels.

**Table 8. DYNAMIC READOUT PARAMETERS**

| Group                    | Addresses      | Description   |
|--------------------------|----------------|---|
| Subsampling              | 192[7]         | Subsampling is synchronized to a new frame start.   |
| ROI configuration        | 195<br>256–265 | A ROI switch is only detected when a new window is selected as the active window (reconfiguration of register 195). reconfiguration of the ROI dimension of the active window does not lead to a frame blank and can cause a corrupted image. |
| Exposure reconfiguration | 199–203        | Exposure reconfiguration does not cause artifact. However, a latency of one frame is observed unless <code>reg_seq_exposure_sync_mode</code> is set to '1' in triggered global mode (master).   |
| Gain reconfiguration     | 204–205        | Gains are synchronized at the start of a new frame. Optionally, one frame latency can be incorporated to align the gain updates to the exposure updates (refer to register 204[13] – <code>gain_lat_comp</code> ).                            |

**Freezing Active Configurations**

Though the readout parameters are synchronized to frame boundaries, an update of multiple registers can still lead to a transient effect in the subsequent images, as some configurations require multiple register uploads. For example, to reconfigure the exposure time in master global mode, both the `fr_length` and exposure registers need to be updated. Internally, the sensor synchronizes these configurations to frame boundaries, but it is still possible that the reconfiguration of multiple registers spans over two or even more frames. To avoid inconsistent combinations, the active configurations can be frozen while altering the SPI registers by disabling synchronization for the corresponding functionality before reconfiguration. When all registers are uploaded, re-enable the synchronization. The sensor's sequencer then updates its active set of

registers and uses them for the coming frames. Freezing of the active set of registers can be programmed in the `sync_configuration` registers, which can be found at the SPI address 206.

Figure 19 shows a reconfiguration that does not use the `sync_configuration` option. As depicted, new SPI configurations are synchronized to frame boundaries.

Figure 20 shows the usage of the `sync_configuration` settings. Before uploading a set of registers, the corresponding `sync_configuration` is de-asserted. After the upload is completed, the `sync_configuration` is asserted again and the sensor resynchronizes its set of registers to the coming frame boundaries. As seen in the figure, this ensures that the uploads performed at the end of frame N+2 and the start of frame N+3 become active in the same frame (frame N+4).



**Figure 19. Frame Synchronization of Configurations (no freezing)**

# PYTHON 480



**Figure 20. reconfiguration Using Sync\_configuration**

NOTE: SPI updates are not taken into account while sync\_configuration is inactive. The active configuration is frozen for the sensor. Table 9 lists the several sync\_configuration possibilities along with the respective registers being frozen.

**Table 9. ALTERNATE SYNC CONFIGURATIONS**

| Group            | Affected Registers                  | Description   |
|------------------|-------------------------------------|---|
| sync_black_lines | black_lines                         | Update of black line configuration is not synchronized at start of frame when '0'. The sensor continues with its previous configurations.   |
| sync_dummy_lines | dummy_lines                         | Update of dummy line configuration is not synchronized at start of frame when '0'. The sensor continues with its previous configurations.   |
| sync_exposure    | mult_timer<br>fr_length<br>exposure | Update of exposure configurations is not synchronized at start of frame when '0'. The sensor continues with its previous configurations.  |
| sync_gain        | mux_gainsw<br>afe_gain<br>db_gain   | Update of gain configurations is not synchronized at start of frame when '0'. The sensor continues with its previous configurations.  |
| sync_roi         | roi_active0[3:0]<br>subsampling     | Update of active ROI configurations is not synchronized at start of frame when '0'. The sensor continues with its previous configurations.<br><b>Note:</b> The window configurations themselves are not frozen. reconfiguration of active windows is not gated by this setting. |

## Window Configuration

Up to 4 windows can be defined in global shutter mode (pipelined or triggered). The windows are defined by registers 256 to 265. Each window can be activated or deactivated separately using register 195. It is possible to reconfigure the inactive windows while the sensor is acquiring images.

Switching between predefined windows is achieved by activation of the respective windows. This way a minimum number of registers need to be uploaded when it is necessary to switch between two or more sets of windows. As an example of this, scanning the scene at higher frame rates using multiple windows and switching to full frame capture when the object is tracked. Switching between the two modes only requires an upload of one register.

## Black Calibration

The sensor automatically calibrates the black level for each frame. Therefore, the device generates a configurable number of electrical black lines at the start of each frame. The desired black level in the resulting output interface can be configured and is not necessarily targeted to '0'. Configuring the target to a higher level yields some information on the left side of the black level distribution, while the other end of the distribution tail is clipped to '0' when setting the black level target to '0'.

The black level is calibrated for the 2 columns contained in one kernel. This implies 2 black level offsets are generated and applied to the corresponding columns. Configurable parameters for the black-level algorithm are listed in Table 10.

Table 10. CONFIGURABLE PARAMETERS FOR BLACK LEVEL ALGORITHM

| Group                                   | Addresses            | Description  |
|---|----------------------|--|
| <b>Black Line Generation</b>            |                      |  |
| 197[7:0]                                | black_lines          | This register configures the number of black lines that are generated at the start of a frame. At least one black line must be generated. The maximum number is 255.<br><b>Note:</b> When the automatic black-level calibration algorithm is enabled, make sure that this register is configured properly to produce sufficient black pixels for the black-level filtering. The number of black pixels generated per line is dependent on the operation mode and window configurations:<br>Each black line contains 404 kernels.   |
| 197[12:8]                               | gate_first_line      | A number of black lines are blanked out when a value different from 0 is configured. These blanked out lines are not used for black calibration. It is recommended to enable this functionality, because the first line can have a different behavior caused by boundary effects.  |
| <b>Black Value Filtering</b>            |                      |  |
| 129[0]                                  | auto_blackcal_enable | Internal black-level calibration functionality is enabled when set to '1'. Required black level offset compensation is calculated on the black samples and applied to all image pixels. When set to '0', the automatic black-level calibration functionality is disabled. It is possible to apply an offset compensation to the image pixels, which is defined by the registers 129[10:1].<br><b>Note:</b> Black sample pixels are not compensated; the raw data is sent out to provide external statistics and, optionally, calibrations.   |
| 129[9:1]                                | blackcal_offset      | Black calibration offset that is added or subtracted to each regular pixel value when auto_blackcal_enable is set to '0'. The sign of the offset is determined by register 129[10] (blackcal_offset_dec).<br><b>Note:</b> All channels use the same offset compensation when automatic black calibration is disabled. The calculated black calibration factors are frozen when this register is set to 0x1FF (all-'1') in auto calibration mode. Any value different from 0x1FF re-enables the black calibration algorithm. This freezing option can be used to prevent eventual frame to frame jitter on the black level as the correction factors are recalculated every frame. It is recommended to enable the black calibration regularly to compensate for temperature changes.   |
| 129[10]                                 | blackcal_offset_dec  | Sign of blackcal_offset. If set to '0', the black calibration offset is added to each pixel. If set to '1', the black calibration offset is subtracted from each pixel.<br>This register is not used when auto_blackcal_enable is set to '1'.  |
| 128[10:8]                               | black_samples        | The black samples are low-pass filtered before being used for black level calculation. The more samples are taken into account, the more accurate the calibration, but more samples require more black lines, which in turn affects the frame rate.<br>The effective number of samples taken into account for filtering is 2 <sup>black_samples</sup> .<br><b>Note:</b> An error is reported by the device if more samples than available are requested (refer to register 136).   |
| <b>Black Level Filtering Monitoring</b> |                      |  |
| 136                                     | blackcal_error0      | An error is reported by the device if there are requests for more samples than are available (each bit corresponding to one data path). The black level is not compensated correctly if one of the channels indicates an error. There are three possible methods to overcome this situation and to perform a correct offset compensation: <ul style="list-style-type: none"> <li>• Increase the number of black lines such that enough samples are generated at the cost of increasing frame time (refer to register 197).</li> <li>• Relax the black calibration filtering at the cost of less accurate black level determination (refer to register 128).</li> <li>• Disable automatic black level calibration and provide the offset via SPI register upload. Note that the black level can drift in function of the temperature. It is thus recommended to perform the offset calibration periodically to avoid this drift.</li> </ul> |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

**Serial Peripheral Interface**

The sensor configuration registers are accessed through an SPI. The SPI consists of four wires:

- sck: Serial Clock
- ss\_n: Active Low Slave Select
- mosi: Master Out, Slave In, or Serial Data In
- miso: Master In, Slave Out, or Serial Data Out

The SPI is synchronous to the clock provided by the master (sck) and asynchronous to the sensor’s system clock. When the master wants to write or read a sensor’s register, it selects the chip by pulling down the Slave Select line (ss\_n). When selected, data is sent serially and synchronous to the SPI clock (sck).

Figure 21 shows the communication protocol for read and write accesses of the SPI registers. The PYTHON 480 image sensors use 9-bit addresses and 16-bit data words.

Data driven by the system is colored blue in Figure 21, while data driven by the sensor is colored yellow. The data in grey indicates high-Z periods on the miso interface. Red markers indicate sampling points for the sensor (mosi sampling); green markers indicate sampling points for the system (miso sampling during read operations).

The access sequence is:

3. Select the sensor for read or write by pulling down the ss\_n line.
4. One SPI clock cycle after selecting the sensor, the 9-bit data is transferred, most significant bit first.

The sck clock is passed through to the sensor as indicated in Figure 21. The sensor samples this data on a rising edge of the sck clock (mosi needs to be driven by the system on the falling edge of the sck clock).

5. The tenth bit sent by the master indicates the type of transfer: high for a write command, low for a read command.
6. Data transmission:
  - For write commands, the master continues sending the 16-bit data, most significant bit first.
  - For read commands, the sensor returns the requested address on the miso pin, most significant bit first. The miso pin must be sampled by the system on the falling edge of sck (assuming nominal system clock frequency and maximum 10 MHz SPI frequency).
7. When data transmission is complete, the system deselects the sensor one clock period after the last bit transmission by pulling ss\_n high.

Note that the maximum frequency for the SPI interface scales with the input clock frequency, bit depth and LVDS output multiplexing as described in Table 5.

Consecutive SPI commands can be issued by leaving at least two SPI clock periods between two register uploads. Deselect the chip between the SPI uploads by pulling the ss\_n pin high.



**Figure 21. SPI Read and Write Timing Diagram**



Table 11. SPI TIMING REQUIREMENTS

| Group   | Addresses   | Description | Units |
|---------|---|-------------|-------|
| tsck    | sck clock period  | 100 (*)     | ns    |
| tssck   | ss_n low to sck rising edge   | tsck        | ns    |
| tsckss  | sck falling edge to ss_n high   | tsck        | ns    |
| ts_mosi | Required setup time for mosi  | 20          | ns    |
| th_mosi | Required hold time for mosi   | 20          | ns    |
| ts_miso | Setup time for miso   | tsck/2-10   | ns    |
| th_miso | Hold time for miso  | tsck/2-20   | ns    |
| tspi    | Minimal time between two consecutive SPI accesses (not shown in figure) | 2 x tsck    | ns    |

\*Value indicated is for nominal operation. The maximum SPI clock frequency depends on the sensor configuration (operation mode, input clock). tsck is defined as  $1/f_{SPI}$ . See text for more information on SPI clock frequency restrictions.

### IMAGE SENSOR TIMING AND READOUT

The following sections describe the configurations for single slope reset mechanism. Extra integration time registers are available.

#### Pipelined Global Shutter (Master)

The integration time is controlled by the registers `fr_length[15:0]` and `exposure[15:0]`. The `mult_timer` configuration defines the granularity of the registers `reset_length` and `exposure`. It is read as number of system clock cycles (14.706 ns nominal at 68 MHz).

The exposure control for (Pipelined) Global Master mode is depicted in Figure 22.

The pixel values are transferred to the storage node during FOT, after which all photo diodes are reset. The reset state remains active for a certain time, defined by the `reset_length` and `mult_timer` registers, as shown in the figure. Note that meanwhile the image array is read out line by line. After this reset period, the global photodiode reset condition is abandoned. This indicates the start of the integration or

exposure time. The length of the exposure time is defined by the registers `exposure` and `mult_timer`.

NOTE: The start of the exposure time is synchronized to the start of a new line (during ROT) if the exposure period starts during a frame readout. As a consequence, the effective time during which the image core is in a reset state is extended to the start of a new line.

- Make sure that the sum of the reset time and exposure time exceeds the time required to readout all lines. If this is not the case, the exposure time is extended until all (active) lines are read out.
- Alternatively, it is possible to specify the frame time and exposure time. The sensor automatically calculates the required reset time. This mode is enabled by the `fr_mode` register. The frame time is specified in the register `fr_length`.



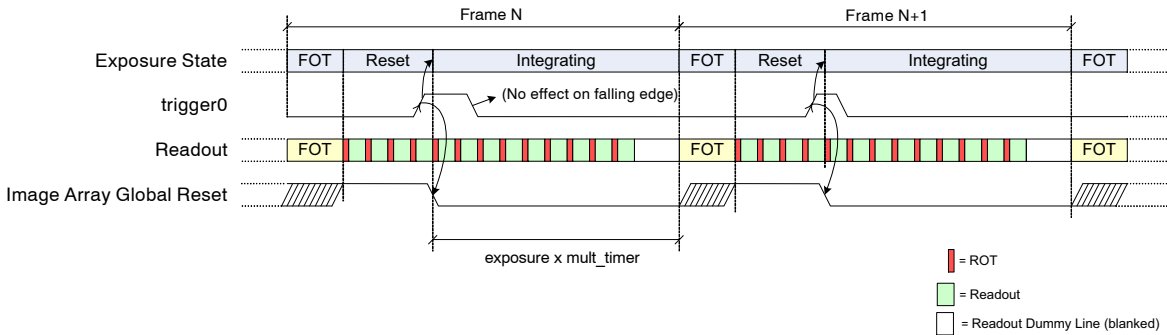
Figure 22. Integration Control for (Pipelined) Global Shutter Mode (Master)



**Triggered Global Shutter (Master)**

In master triggered global mode, the start of integration time is controlled by a rising edge on the trigger0 pin. The exposure or integration time is defined by the registers

exposure and mult\_timer, as in the master pipelined global mode. The fr\_length configuration is not used. This operation is graphically shown in Figure 23.



**Figure 23. Exposure Time Control in Triggered Shutter Mode (Master)**

Notes:

- The falling edge on the trigger pin does not have any impact. Note however the trigger must be asserted for at least 100 ns.
- The start of the exposure time is synchronized to the start of a new line (during ROT) if the exposure period starts during a frame readout. As a consequence, the effective time during which the image core is in a reset state is extended to the start of a new line.
- If the exposure timer expires before the end of readout, the exposure time is extended until the end of the last active line.
- The trigger pin needs to be kept low during the FOT. The monitor pins can be used as a feedback to the FPGA/controller (eg. use monitor0, indicating the very first line when monitor\_select = 0x5 – a new trigger can be initiated after a rising edge on monitor0).

the pixel storage node and readout of the image array. In other words, the high time of the trigger pin indicates the integration time, the period of the trigger pin indicates the frame time.

The use of the trigger during slave mode is shown in Figure 24.

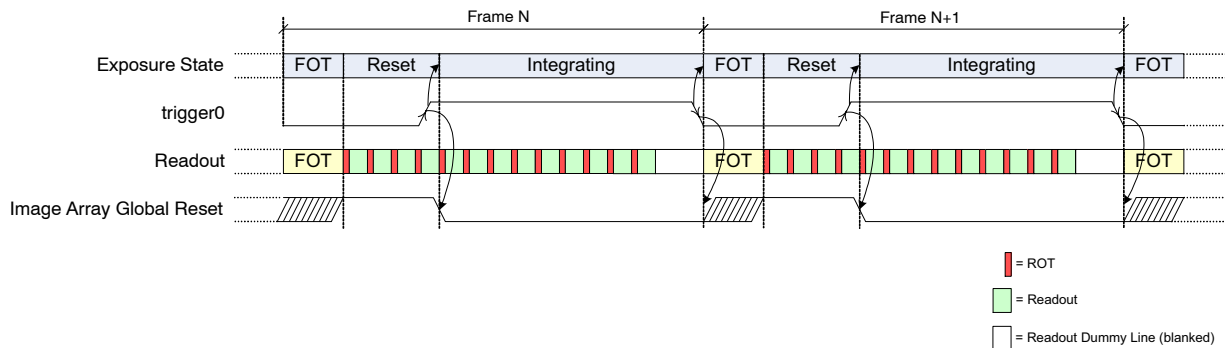
Notes:

- The registers exposure, fr\_length, and mult\_timer are not used in this mode.
- The start of exposure time is synchronized to the start of a new line (during ROT) if the exposure period starts during a frame readout. As a consequence, the effective time during which the image core is in a reset state is extended to the start of a new line.
- If the trigger is de-asserted before the end of readout, the exposure time is extended until the end of the last active line.
- The trigger pin needs to be kept low during the FOT. The monitor pins can be used as a feedback to the FPGA/controller (eg. use monitor0, indicating the very first line when monitor\_select = 0x5 – a new trigger can be initiated after a rising edge on monitor0).

**Triggered Global Shutter (Slave)**

Exposure or integration time is fully controlled by means of the trigger pin in slave mode. The registers fr\_length, exposure and mult\_timer are ignored by the sensor.

A rising edge on the trigger pin indicates the start of the exposure time, while a falling edge initiates the transfer to



**Figure 24. Exposure Time Control in Global-Slave Mode**

ADDITIONAL FEATURES

**Multiple Window Readout**

The PYTHON 480 image sensors support multiple window readout, which means that only the user-selected Regions Of Interest (ROI) are read out. This allows limiting data output for every frame, which in turn allows increasing the frame rate. Up to four ROIs can be configured.

**Window Configuration**

Figure 25 shows the four parameters defining a region of interest (ROI).



**Figure 25. Region of Interest Configuration**

- **x-start[8:0]**  
x-start defines the x-starting point of the desired window. The sensor reads out 2 pixels in one single clock cycle. As a consequence, the granularity for configuring the x-start position is also 2 pixels for no sub sampling. The value configured in the x-start register is multiplied by 2 to find the corresponding column in the pixel array.
- **x-end[8:0]**  
This register defines the window end point on the x-axis. Similar to x-start, the granularity for this configuration is one kernel. x-end needs to be larger than x-start.
- **y-start[9:0]**  
The starting line of the readout window. The granularity of this setting is one line, except with color sensors where it needs to be an even number.
- **y-end[9:0]**  
The end line of the readout window. y-end must be configured larger than y-start. This setting has the same granularity as the y-start configuration.

Up to four windows can be defined, possibly (partially) overlapping, as illustrated in Figure 26.

**NOTE:** The least significant configuration bits for x and y parameters are located in separate registers (refer to registers 264–265). One may decide not to reconfigure these bits, in which case the configuration granularity becomes 4 pixels for both x- and y-configurations.



**Figure 26. Overlapping Multiple Window Configuration**

The sequencer analyses each line that need to be read out for multiple windows.

**Restrictions**

The following restrictions for each line are assumed for the user configuration:

- Windows are ordered from left to right, based on their x-start address:

$$x\_start\_roi(i) \leq x\_start\_roi(j) \text{ AND}$$

$$x\_end\_roi(i) \leq x\_end\_roi(j)$$

Where  $j > i$

**Processing Multiple Windows**

The sequencer control block houses two sets of counters to construct the image frame. As previously described, the y-counter indicates the line that needs to be read out and is incremented at the end of each line. For the start of the frame, it is initialized to the y-start address of the first window and it runs until the y-end address of the last window to be read out. The last window is configured by the configuration registers and it is not necessarily window #3.

The x-counter starts counting from the x-start address of the window with the lowest ID which is active on the addressed line. Only windows for which the current y-address is enclosed are taken into account for scanning. Other windows are skipped.

Figure 27 illustrates a practical example of a configuration with four windows. The current position of the read pointer (ys) is indicated by a red line crossing the image array. For this position of the read pointer, three windows need to be read out. The initial start position for the x-kernel pointer is the x-start configuration of ROI0. Kernels are scanned up to the ROI2 x-end position. From there, the x-pointer jumps to the next window, which is ROI3 in this illustration. When reaching ROI3's x-end position, the read pointer is incremented to the next line and xs is reinitialized to the starting position of ROI0.



Figure 27. Scanning the Image Array with Four Windows

Notes:

- The starting point for the readout pointer at the start of a frame is the y-start position of the first active window.
- The read pointer is not necessarily incremented by one, but depending on the configuration, it can jump in y-direction. In Figure 27, this is the case when reaching the end of ROI0 where the read pointer jumps to the y-start position of ROI1
- The x-pointer starting position is equal to the x-start configuration of the first active window on the current line addressed. This window is not necessarily window #0.
- The x-pointer is not necessarily incremented by one each cycle. At the end of a window it can jump to the start of the next window.
- Each window can be activated separately. There is no restriction on which window and how many of the 4 windows are active.

**Subsampling**

Subsampling is used to reduce the image resolution. This allows increasing the frame rate. Two subsampling modes are supported: for monochrome sensors (LVDS/CMOS) and color sensors (LVDS/CMOS).

**Monochrome Sensors**

For monochrome sensors, the read-1-skip-1 subsampling scheme is used. Subsampling occurs both in x- and y- direction.

**Color Sensors**

For color sensors, the read-2-skip-2 subsampling scheme is used. Subsampling occurs both in x- and y- direction. Figure 28 shows which pixels are read and which ones are skipped.

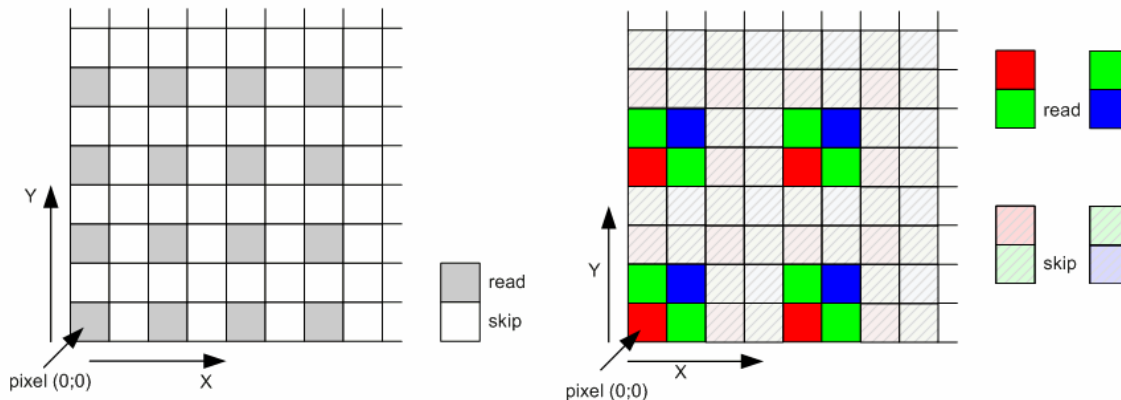


Figure 28. Subsampling Scheme for Monochrome and Color Sensors

**Reverse Readout**

Reverse readout in y-direction can be done by toggling reverse\_y (reg 194[8]). The reference for y\_start and y\_end pointers is reversed.

Reverse readout in x-direction can be done by toggling reverse\_x (reg 194[9]).

**Black Reference**

The sensor reads out one or more black lines at the start of every new frame. The number of black lines to be generated is programmable and is minimal equal to 1. The length of the black lines depends on the operation mode. The sensor always reads out the entire line (404 kernels), independent of window configurations.

The black references are used to perform black calibration and offset compensation in the data channels. The raw black pixel data is transmitted over the usual output interface, while the regular image data is compensated (can be bypassed).

On the output interface, black lines can be seen as a separate window, however without Frame Start and Ends (only Line Start/End). The Sync code following the Line Start and Line End indications (“window ID”) contains the active window number, which is 0. Black reference data is classified by a BL code.

**Reference Lines**

The sensor optionally reads out one or more reference lines after the black lines. The number of reference lines to be generated is programmable. No reference lines shall be generated when set to 0. As for the black lines, the length of the reference lines depends on the operation mode.

The reference lines are not used internally in the sensor. The ROT for these lines can be configured such that these lines contain particular reference data, such as a grey level, in order to perform PRNU correction off-chip. Reference

lines are indicated on the output interface by means of a dedicated Sync pattern (REF).

The black calibration block can be configured to either perform black level correction and compression or not. In the latter case, the LSB is discarded from the ADC word.

Optionally, the black level calibration processor can be configured to transmit the average black level on the reference lines. In this mode, the reference pixel data are replaced by the average black level, as calculated by the black calibration block. Channel differences can easily be observed in this mode (See register `reg_db_ref_bcal_enable`).

**Signal Path Gain**

**Analog Gain Stages**

Referring to Table 12, three gain settings are available in the analog data path to apply gain to the analog signal before it is digitized. The gain amplifier can apply a gain of approximately 1x to 3.5x to the analog signal.

The moment a gain reconfiguration is applied and becomes valid can be controlled by the `gain_lat_comp` configuration.

With ‘`gain_lat_comp`’ set to ‘0’, the new gain configurations are applied from the very next frame.

With ‘`gain_lat_comp`’ set to ‘1’, the new gain settings are postponed by one extra frame. This feature is useful when exposure time and gain are reconfigured together, as an exposure time update always has one frame latency.

**Table 12. SIGNAL PATH GAIN STAGES**

| Address   | Gain Setting | Gain Stage 1 (204[4:0]) | Gain Stage 2 (204[12:5]) | Overall Gain |
|-----------|--------------|-------------------------|--------------------------|--------------|
| 204[12:0] | 0x00E1       | 1                       | 1                        | 1            |
| 204[12:0] | 0x00E4       | 2                       | 1                        | 2            |
| 204[12:0] | 0x0024       | 2                       | 1.75                     | 3.5          |

NOTE: The sensor performance specifications are tested at unity gain. Analog gain above 2x affects noise performance. All other gains settings shown in this table are tested for sensor functionality only.

**Digital Gain Stage**

The digital gain stage allows fine gain adjustments on the digitized samples. The gain configuration is an absolute 5.7

unsigned number (5 digits before and 7 digits after the decimal point).

**Automatic Exposure Control**

The exposure control mechanism has the shape of a general feedback control system. Figure 29 shows the high level block diagram of the exposure control loop.



**Figure 29. Automatic Exposure Control Loop**

Three main blocks can be distinguished:

- The **statistics block** compares the average of the current image’s samples to the configured target value for the average illumination of all pixels
- The relative gain change request from the statistics block is filtered through the **AEC Filter block** in the time domain (low pass filter) before being integrated. The output of the filter is the total requested gain in the complete signal path.
- The **enforcer block** accepts the total requested gain and distributes this gain over the integration time and gain stages (both analog and digital)

The automatic exposure control loop is enabled by asserting the `aec_enable` configuration in register 160.

**AEC Statistics Block**

The statistics block calculates the average illumination of the current image. Based on the difference between the calculated illumination and the target illumination the statistics block requests a relative gain change.

*Statistics Subsampling and Windowing*

For average calculation, the statistics block will sub-sample the current image or windows by taking every fourth sample into account. Note that only the pixels read out through the active windows are visible for the AEC. In the case where multiple windows are active, the samples will be selected from the total samples. Samples contained in a region covered by multiple (overlapping) window will be taken into account only once.

It is possible to define an AEC specific sub-window on which the AEC will calculate its average. For instance, the sensor can be configured to read out a larger frame, while the illumination is measured on a smaller region of interest, e.g. center weighted as shown in Table 13.

**Table 13. AEC SAMPLE SELECTION**

| Register | Name                        | Description  |
|----------|-----------------------------|--|
| 192[10]  | <code>roi_aec_enable</code> | When 0x0, all active windows are selected for statistics calculation. When 0x1, the AEC samples are selected from the active pixels contained in the region of interest defined by <code>roi_aec</code>  |
| 253-255  | <code>roi_aec</code>        | These registers define a window from which the AEC samples will be selected when <code>roi_aec_enable</code> is asserted. Configuration is similar to the regular region of interests. The intersection of this window with the active windows define the selected pixels. It is important that this window at least overlaps with one or more active windows. |

*Target Illumination*

The target illumination value is configured by means of register *desired\_intensity* as shown in Table 14.

**Table 14. AEC TARGET ILLUMINATION CONFIGURATION**

| Register | Name              | Description                              |
|----------|-------------------|--|
| 161[9:0] | desired_intensity | Target intensity value, on 10-bit scale. |

*Color Sensor*

The weight of each color can be configured for color sensors by means of scale factors. Note these scale factor are only used to calculate the statistics in order to compensate for (off-chip) white balancing and/or color matrices. The pixel values itself are not modified.

The scale factors are configured as 3.7 unsigned numbers (0x80 = unity). Refer to Table 15 for color scale factors. For mono sensors, configure these factors to their default value.

**Table 15. COLOR SCALE FACTORS**

| Register | Name                | Description                            |
|----------|---------------------|--|
| 162[9:0] | red_scale_factor    | Red scale factor for AEC statistics    |
| 163[9:0] | green1_scale_factor | Green1 scale factor for AEC statistics |
| 164[9:0] | green2_scale_factor | Green2 scale factor for AEC statistics |
| 165[9:0] | blue_scale_factor   | Blue scale factor for AEC statistics   |

**AEC Filter Block**

The filter block low-pass filters the gain change requests received from the statistics block.

The filter can be restarted by asserting the *restart\_filter* configuration of register 160.

**AEC Enforcer Block**

The enforcer block calculates the four different gain parameters, based on the required total gain, thereby respecting a specific hierarchy in those configurations. Some (digital) hysteresis is added so that the (analog) sensor settings don't need to change too often.

*Exposure Control Parameters*

The several gain parameters are described below, in the order in which these are controlled by the AEC for large adjustments. Small adjustments are regulated by digital gain only.

- Exposure Time

The exposure is the time between the global image array reset de-assertion and the pixel charge transfer. The granularity of the integration time steps is configured by the *mult\_timer* register.

NOTE: The *exposure\_time* register is ignored when the AEC is enabled. The register *fr\_length* defines the frame time and needs to be configured accordingly.

- Analog Gain

The sensor has two analog gain stages, configurable independently from each other. Typically the AEC shall only regulate the first stage.

- Digital Gain

The last gain stage is a gain applied on the digitized samples. The digital gain is represented by a 5.7 unsigned number (i.e. 7 bits after the decimal point). While the analog gain steps are coarse, the digital gain stage makes it possible to achieve very fine adjustments.

**AEC Control Range**

The control range for each of the exposure parameters can be pre-programmed in the sensor. Table 16 lists the relevant registers.

**Table 16. MINIMUM AND MAXIMUM EXPOSURE CONTROL PARAMETERS**

| Register  | Name             | Description   |
|-----------|------------------|---|
| 168[15:0] | min_exposure     | Lower bound for the integration time applied by the AEC   |
| 169[1:0]  | min_mux_gain     | Lower bound for the first stage analog amplifier. This stage has two configurations with the following approximative gains:<br>0x1 = 1x<br>0x4 = 2x             |
| 169[3:2]  | min_afe_gain     | Lower bound for the second stage analog amplifier. This stage has two configurations with the following approximative gain settings:<br>0x7 = 1x<br>0x1 = 1.75x |
| 169[15:4] | min_digital_gain | Lower bound for the digital gain stage. This configuration specifies the effective gain in 5.7 unsigned format  |
| 170[15:0] | max_exposure     | Upper bound for the integration time applied by the AEC   |
| 171[1:0]  | max_mux_gain     | Upper bound for the first stage analog amplifier. This stage has two configurations with the following approximative gains:<br>0x1 = 1x<br>0x4 = 2x             |
| 171[3:2]  | max_afe_gain     | Upper bound for the second stage analog amplifier. This stage has two configurations with the following approximative gain settings:<br>0x7 = 1x<br>0x1 = 1.75x |
| 171[15:4] | max_digital_gain | Upper bound for the digital gain stage. This configuration specifies the effective gain in 5.7 unsigned format  |

**AEC Update Frequency**

As an integration time update has a latency of one frame, the exposure control parameters are evaluated and updated every other frame.

Note: The gain update latency must be postpone to match the integration time latency. This is done by asserting the *gain\_lat\_comp* register on address 204[13].

**Exposure Control Status Registers**

Configured integration and gain parameters are reported to the user by means of status registers. The sensor provides two levels of reporting: the status registers reported in the AEC address space are updated once the parameters are recalculated and requested to the internal sequencer. The status registers residing in the sequencer's address space on the other hand are updated once these parameters are taking effect on the image readout. Refer to Table 17 reflecting the AEC and Sequencer Status registers.

**Table 17. EXPOSURE CONTROL STATUS REGISTERS**

| Register             | Name         | Description  |
|----------------------|--------------|--|
| AEC Status Registers |              |  |
| 184[15:0]            | total_pixels | Total number of pixels taken into account for the AEC statistics.                                    |
| 186[9:0]             | average      | Calculated average illumination level for the current frame.   |
| 187[15:0]            | exposure     | AEC calculated exposure. Note: this parameter is updated at the frame end.                           |
| 188[1:0]             | mux_gain     | AEC calculated analog gain (1 <sup>st</sup> stage) Note: this parameter is updated at the frame end. |
| 188[3:2]             | afe_gain     | AEC calculated analog gain (2 <sup>nd</sup> stage) Note: this parameter is updated at the frame end. |
| 188[15:4]            | digital_gain | AEC calculated digital gain (5.7 unsigned format) Note: this parameter is updated at the frame end.  |



**Mode Changes and Frame Blanking**

Dynamically reconfiguring the sensor may lead to corrupted or non-uniformly exposed frames. For some reconfigurations, the sensor automatically blanks out the image data during one frame. Frame blanking is

summarized in the following table for the sensor's image related modes.

NOTE: Major mode switching (i.e. switching between master, triggered or slave mode) must be performed while the sequencer is disabled (reg\_seq\_enable = 0x0).

**Table 18. DYNAMIC SENSOR RECONFIGURATION AND FRAME BLANKING**

| Configuration                     | Corrupted Frame   | Blanked Out Frame | Notes  |
|-----------------------------------|---|-------------------|--|
| <b>Shutter Mode and Operation</b> |   |                   |  |
| triggered_mode                    | Do not reconfigure while the sensor is acquiring images. Disable image acquisition by setting reg_seq_enable = 0x0. |                   |  |
| slave_mode                        | Do not reconfigure while the sensor is acquiring images. Disable image acquisition by setting reg_seq_enable = 0x0. |                   |  |
| subsampling                       | Enabling: No<br>Disabling: Yes  | Configurable      | Configurable with blank_subsampling_ss register.   |
| <b>Frame Timing</b>               |   |                   |  |
| black_lines                       | No  | No                |  |
| <b>Exposure Control</b>           |   |                   |  |
| mult_timer                        | No  | No                | Latency is 1 frame   |
| fr_length                         | No  | No                | Latency is 1 frame   |
| exposure                          | No  | No                | Latency is 1 frame   |
| <b>Gain</b>                       |   |                   |  |
| mux_gainsw                        | No  | No                | Latency configurable by means of gain_lat_comp register  |
| afe_gain                          | No  | No                | Latency configurable by means of gain_lat_comp register.   |
| db_gain                           | No  | No                | Latency configurable by means of gain_lat_comp register.   |
| <b>Window/ROI</b>                 |   |                   |  |
| roi_active                        | See Note  | No                | Windows containing lines previously not read out may lead to corrupted frames.   |
| roi*_configuration*               | See Note  | No                | Reconfiguring the windows by means of roi*_configuration* may lead to corrupted frames when configured close to frame boundaries. It is recommended to (re)configure an inactive window and switch the roi_active register. See Notes on roi_active. |
| <b>Black Calibration</b>          |   |                   |  |
| black_samples                     | No  | No                | If configured within range of configured black lines   |
| auto_blackcal_enable              | See Note  | No                | Manual correction factors become instantly active when auto_blackcal_enable is deasserted during operation.  |
| blackcal_offset                   | See Note  | No                | Manual blackcal_offset updates are instantly active.   |
| <b>CRC Calculation</b>            |   |                   |  |
| crc_seed                          | No  | No                | Impacts the transmitted CRC  |
| <b>Sync Channel</b>               |   |                   |  |
| bl_0                              | No  | No                | Impacts the Sync channel information, not the Data channels.   |
| img_0                             | No  | No                | Impacts the Sync channel information, not the Data channels.   |
| crc_0                             | No  | No                | Impacts the Sync channel information, not the Data channels.   |
| tr_0                              | No  | No                | Impacts the Sync channel information, not the Data channels.   |



**Monitor Pins**

The internal sequencer has two monitor outputs (Pin 44 and Pin 45) that can be used to communicate the internal

states from the sequencer. A three-bit register configures the assignment of the pins as shown in Table 19.

**Table 19. MONITOR SELECT**

| Monitor Select | Monitor Output                               | Description  |
|----------------|--|--|
| 0x0            | monitor0: '0'                                | No information is provided on the output pins. All outputs are driven to logic '0' |
|                | monitor1: '0'                                |  |
|                | monitor2: '0'                                |  |
| 0x1            | monitor0: Integration time indication        | High during integration  |
|                | monitor1: ROT indication                     | High when ROT is active, low outside ROT   |
|                | monitor2: Dummy line indication              | High during dummy lines, low during all other lines                                |
| 0x2            | monitor0: Integration time indication        | High during integration  |
|                | monitor1: N/A                                | N/A  |
|                | monitor2: N/A                                | N/A  |
| 0x3            | monitor0: Start of X-readout                 | Pulse indicating the start of X-readout  |
|                | monitor1: Black line indication              | High during black lines, low during all other lines                                |
|                | monitor2: Dummy line indication              | High during dummy lines, low during all other lines                                |
| 0x4            | monitor0: Frame start                        | Pulse indicating the start of a new frame  |
|                | monitor1: Start of ROT                       | Pulse indicating the start of ROT  |
|                | monitor2: Start of X-readout                 | Pulse indicating the start of X-readout  |
| 0x5            | monitor0: First line indication              | High during the first line of each frame, low for all others                       |
|                | monitor1: Start of ROT indication            | Pulse indicating the start of ROT  |
|                | monitor2: ROT inactive                       | Low when ROT is active, high outside ROT   |
| 0x6            | monitor0: ROT indication                     | High when ROT is active, low outside ROT   |
|                | monitor1: Start of X-readout                 | Pulse indicating the start of X-readout  |
|                | monitor2: X-readout inactive                 | Low during X-readout, high outside X-readout                                       |
| 0x7            | monitor0: Start of X-readout for black lines | Pulse indicating the start of X-readout for black lines                            |
|                | monitor1: Start of X-readout for image lines | Pulse indicating the start of X-readout for image lines                            |
|                | monitor2: Start of X-readout for dummy lines | Pulse indicating the start of X-readout for dummy lines                            |

**Sequences of Frame Acquisition with Different Configurations**

Frame dependent configurations require multiple contexts, which are sync'ed upon a start of a new frame. The following configurations are context switchable:

- FOT program
- ROT programs (only for regular ROT in Global Shutter Mode (no muxing for black reference ROT programs))
- Integration Time
- Gain (both digital and analog)
- Active ROI Configuration (not the window configuration themselves)

When enabled, the sequencer shall automatically select one set of parameters for the even frames and the other set of parameters for the odd frames.

This operation mode is enabled by means of the `reg_seq_sequence` register and can be used in global shutter modes.

The configurations used for even odd frames are summarized in Table 20.

When the sequenced readout is not enabled, the first set of configurations ('Even configurations') is applicable. The second set ('Odd configurations') is ignored by the sequencer.

**Table 20. ODD/EVEN CONFIGURATION**

| Configuration            | Even Frames                      | Odd Frames                       |
|--------------------------|----------------------------------|----------------------------------|
| Integration Time         | <code>reg_seq_exposure0</code>   | <code>reg_seq_exposure1</code>   |
| FR Length                | <code>reg_seq_fr_length0</code>  | <code>reg_seq_fr_length1</code>  |
| Mult Timer               | <code>reg_seq_mult_timer0</code> | <code>reg_seq_mult_timer1</code> |
| Gain Stage 1             | <code>reg_seq_mux_gainsw0</code> | <code>reg_seq_mux_gainsw1</code> |
| Gain Stage 2             | <code>reg_seq_afe_gain0</code>   | <code>reg_seq_afe_gain1</code>   |
| Digital Gain             | <code>reg_seq_db_gain0</code>    | <code>reg_seq_db_gain1</code>    |
| ROI Active Configuration | <code>reg_seq_roi_active0</code> | <code>reg_seq_roi_active1</code> |

## DATA OUTPUT FORMAT

The PYTHON 480 image sensor can be configured in LVDS output mode, which includes one LVDS output channel together with an LVDS clock output and an LVDS synchronization output channel. The PYTHON 480 is also configurable in a CMOS output configuration, which includes a 10-bit parallel CMOS output together with a CMOS clock output and 'frame valid' and 'line valid' CMOS output signals.

### LVDS Interface Mode

#### LVDS Output Channels

The image data output occurs through one LVDS data channel where a synchronization LVDS channel and an LVDS output clock signal synchronizes the data.

The one data channel is used to output the image data only. The sync channel transmits information about the data sent over the data channel (includes codes indicating black pixels, normal pixels, and CRC codes).

#### Frame Format

The frame format is explained by example of the readout of two (overlapping) windows as shown in Figure 30(a).

The readout of a frame occurs on a line-by-line basis. The read pointer goes from left to right, bottom to top.

Figure 30 indicates that, after the FOT is completed, the sensor reads out a number of black lines for black calibration purposes. After these black lines, the windows are processed. First a number of lines which only includes

information of 'ROI 0' are sent out, starting at position  $y0\_start$ . When the line at position  $y1\_start$  is reached, a number of lines containing data of 'ROI 0' and 'ROI 1' are sent out, until the line position of  $y0\_end$  is reached. From there on, only data of 'ROI 1' appears on the data output channels until line position  $y1\_end$  is reached

During read out of the image data over the data channels, the sync channel sends out frame synchronization codes which give information related to the image data that is sent over the four data output channels.

Each line of a window starts with a Line Start (LS) indication and ends with a Line End (LE) indication. The line start of the first line is replaced by a Frame Start (FS); the line end of the last line is replaced with a Frame End indication (FE). Each such frame synchronization code is followed by a window ID (range 0 to 7). For overlapping windows, the line synchronization codes of the overlapping windows with lower IDs are not sent out (as shown in the illustration: no LE/FE is transmitted for the overlapping part of window 0).

**NOTE:** In Figure 30, only Frame Start and Frame End Sync words are indicated in (b). CRC codes are also omitted from the figure.

For additional information on the synchronization codes, refer to Application Note AND5001.



Figure 30. LVDS Mode: Frame Sync Codes

Figure 31 shows the detail of a black line readout during global or full-frame readout.



Figure 31. LVDS Mode: Time Line for Black Line Readout

Figure 32 shows shows the details of the readout of a number of lines for single window readout, at the beginning of the frame.



**Figure 32. LVDS Mode: Time Line for Single Window Readout (at the start of a frame)**

Figure 33 shows the detail of the readout of a number of lines for readout of two overlapping windows.



**Figure 33. LVDS Mode: Time Line Showing the Readout of Two Overlapping Windows**

**Frame Synchronization**

Table 21 shows the structure of the frame synchronization code. Note that the table shows the default data word (configurable). If more than one window is active at the

same time, the sync channel transmits the frame synchronization codes of the window with highest index only.

**Table 21. FRAME SYNCHRONIZATION CODE DETAILS**

| Sync Word Bit Position | Register Address | Default Value | Description  |
|------------------------|------------------|---------------|--|
| 9:7                    | N/A              | 0x4           | Frame Sequence Start (FSS). Only sent out when reg_seq_fss_enable is asserted.   |
| 9:7                    | N/A              | 0x7           | Frame Sequence End (FSE). Only sent out when reg_seq_fse_enable is asserted.   |
| 9:7                    | N/A              | 0x5           | Frame start indication   |
| 9:7                    | N/A              | 0x6           | Frame end indication   |
| 9:7                    | N/A              | 0x1           | Line start indication  |
| 9:7                    | N/A              | 0x2           | Line end indication  |
| 6:0                    | 117[6:0]         | 0x2A          | These bits indicate that the received sync word is a frame synchronization code. The value is programmable by a register setting |

• Window Identification

Frame synchronization codes are always followed by a 3-bit window identification (bits 2:0). This is an integer number, ranging from 0 to 7, indicating the active window. If more than one window is active for the current cycle, the highest window ID is transmitted.

• Data Classification Codes

For the remaining cycles, the sync channel indicates the type of data sent through the data links: black pixel data (BL), image data (IMG), or training pattern (TR). These codes are programmable by a register setting. The default values are listed in Table 22.

**Table 22. SYNCHRONIZATION CHANNEL DEFAULT IDENTIFICATION CODE VALUES**

| Sync Word Bit Position | Register Address | Default Value | Description  |
|------------------------|------------------|---------------|--|
| 9:0                    | 118 [9:0]        | 0x015         | Black pixel data (BL). This data is not part of the image. The black pixel data is used internally to correct channel offsets. |
| 9:0                    | 119 [9:0]        | 0x035         | Valid pixel data (IMG). The data on the data output channels is valid pixel data (part of the image).                          |
| 9:0                    | 125 [9:0]        | 0x059         | CRC value. The data on the data output channels is the CRC code of the finished image data line.                               |
| 9:0                    | 126 [9:0]        | 0x3A6         | Training pattern (TR). The sync channel sends out the training pattern which can be programmed by a register setting.          |

**Training Patterns on Data Channels**

During idle periods, the data channels transmit training patterns, indicated on the sync channel by a TR code. These

training patterns are configurable independent of the training code on the sync channel as shown in Table 23.

**Table 23. TRAINING CODE ON SYNC CHANNEL IN**

| Sync Word Bit Position | Register Address | Default Value | Description   |
|------------------------|------------------|---------------|---|
| [9:0]                  | 116 [9:0]        | 0x3A6         | Data channel training pattern. The data output channels send out the training pattern, which can be programmed by a register setting. The default value of the training pattern is 0x3A6, which is identical to the training pattern indication code on the sync channel. |

**Cyclic Redundancy Code**

At the end of each line, a CRC code is calculated to allow error detection at the receiving end. Each data channel transmits a CRC code to protect the data words sent during the previous cycles. Idle and training patterns are not included in the calculation.

The sync channel is not protected. A special character (CRC indication) is transmitted whenever the data channels send their respective CRC code.

The polynomial is  $x^{10} + x^9 + x^6 + x^3 + x^2 + x + 1$ . The CRC encoder is seeded at the start of a new line and updated for every (valid) data word received. The CRC seed is configurable using the `crc_seed` register. When '0', the CRC is seeded by all-'0'; when '1' it is seeded with all-'1'.

NOTE: The CRC is calculated for every line. This implies that the CRC code can protect lines from multiple windows.

**Data Order: LVDS Interface Version**

To read out the image data through the output channel, the pixel array is organized in kernels. The kernel size is two pixels in x-direction by one pixel in y-direction. Figure 34

indicates how the kernels are organized. The first kernel (kernel [0, 0]) is located in the bottom left corner. The pixel data is transmitted in order. The figures in the following paragraphs represent the data order for a non-mirrored readout (i.e. left-to-right readout).



**Figure 34. Kernel Organization in Pixel Array (Top View)**

- Subsampling disabled

Figure 35 shows how a kernel is read out. The pixels are transferred in order, or in ascending order for normal readout and descending order for mirrored readout.



Figure 35. P1-SN/SE/FN: Data Output Order when Subsampling is Disabled

- Subsampling on Monochrome Sensor

During subsampling on a monochrome sensor, every other pixel is read out and the lines are read in a read-1-skip-1 manner. To read out the image data with subsampling enabled on a monochrome sensor, two

neighboring kernels are combined to a single kernel of 4 pixels in the x-direction and one pixel in the y-direction. Only the pixels at the even pixel positions inside that kernel are read out.

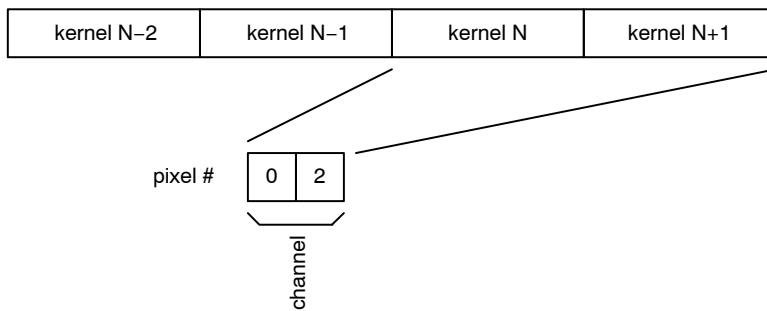


Figure 36. Data Output Order in Subsampling Mode on a Monochrome Sensor

- Subsampling on Color Sensor

During subsampling on a color sensor, lines are read in a read-2-skip-2 manner. To read out the image data with subsampling enabled on a color sensor, two neighboring

kernels are combined to a single kernel of 4 pixels in the x-direction and one pixel in the y-direction. Only the pixels 0 and 1 are read out.

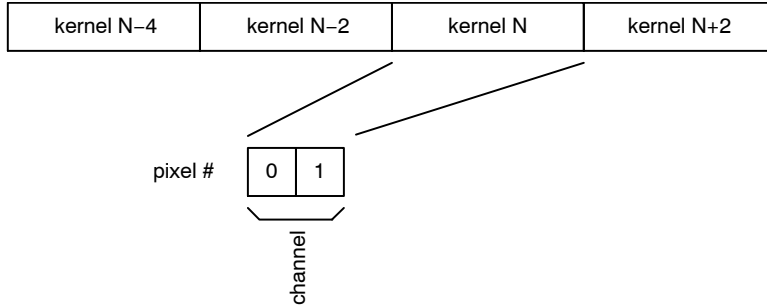


Figure 37. Data Output Order for the LVDS Output Channel in Subsampling Mode on a Color Sensor

**CMOS Interface Mode**

**CMOS Output Signals**

The image data output occurs through a single 10-bit parallel CMOS data output. A CMOS clock output, ‘frame valid’ and ‘line valid’ signal synchronizes the output data.

No windowing information is sent out by the sensor.

**Frame Format**

Frame timing is indicated by means of two signals: frame\_valid and line\_valid.

- The frame\_valid indication is asserted at the start of a new frame and remains asserted until the last line of the frame is completely transmitted.

- The line\_valid indication serves the following needs:
  - ♦ While the line\_valid indication is asserted, the data channels contain valid pixel data.
  - ♦ The line valid communicates frame timing as it is asserted at the start of each line and it is de-asserted at the end of the line. Low periods indicate the idle time between lines (ROT).
  - ♦ The data channels transmit the calculated CRC code after each line. This can be detected as the data words right after the falling edge of the line valid.



Figure 38. CMOS Mode: Frame Timing Indication

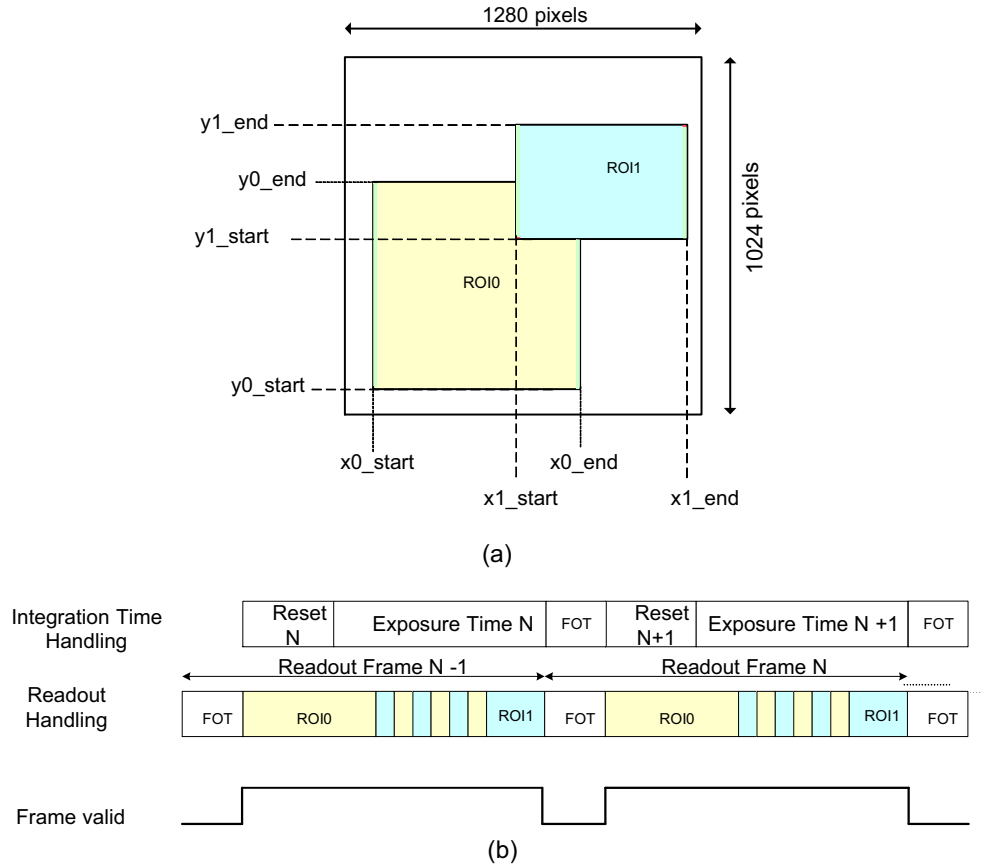


## PYTHON 480

The frame format is explained with an example of the readout of two (overlapping) windows as shown in Figure 39 (a).

The readout of a frame occurs on a line-by-line basis. The read pointer goes from left to right, bottom to top. Figure 39 (a) and (b) indicate that, after the FOT is finished, a number of lines which include information of 'ROI 0' are sent out,

starting at position  $y0\_start$ . When the line at position  $y1\_start$  is reached, a number of lines containing data of 'ROI 0' and 'ROI 1' are sent out, until the line position of  $y0\_end$  is reached. Then, only data of 'ROI 1' appears on the data output until line position  $y1\_end$  is reached. The `line_valid` strobe is not shown in Figure 39.



**Figure 39. CMOS Mode: Frame Format to Read Out Image Data**

### Black Lines

Black pixel data is also sent through the data channels. To distinguish these pixels from the regular image data, it is

possible to 'mute' the frame and/or line valid indications for the black lines. Refer to Table 24 for black line, `frame_valid` and `line_valid` settings.

**Table 24. BLACK LINE FRAME\_VALID AND LINE\_VALID SETTINGS**

| <code>bl_frame_valid_enable</code> | <code>bl_line_valid_enable</code> | Description  |
|------------------------------------|-----------------------------------|--|
| 0x1                                | 0x1                               | The black lines are handled similar to normal image lines. The frame valid indication is asserted before the first black line and the line valid indication is asserted for every valid (black) pixel.   |
| 0x1                                | 0x0                               | The frame valid indication is asserted before the first black line, but the line valid indication is not asserted for the black lines. The line valid indication indicates the valid image pixels only. This mode is useful when one does not use the black pixels and when the frame valid indication needs to be asserted some time before the first image lines (for example, to precondition ISP pipelines). |
| 0x0                                | 0x1                               | In this mode, the black pixel data is clearly unambiguously indicated by the line valid indication, while the decoding of the real image data is simplified.   |
| 0x0                                | 0x0                               | Black lines are not indicated and frame and line valid strobes remain de-asserted. Note however that the data channels contains the black pixel data and CRC codes (Training patterns are interrupted).  |

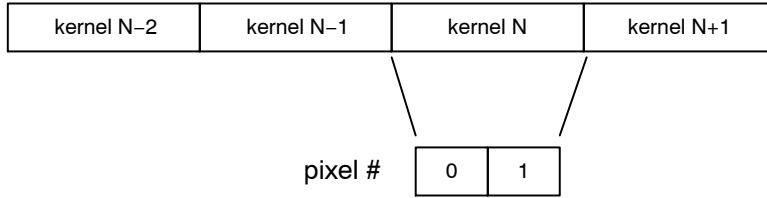
**Data order: CMOS Interface Mode**

To read out the image data through the parallel CMOS output, the pixel array is divided in kernels. The kernel size is two pixels in x-direction by one pixel in y-direction. Figure 34 on page 38 indicates how the kernels are organized.

The pixel data is transmitted in order. The figures in the following paragraphs represent the data order for a non-mirrored readout (i.e. left-to-right readout).

• No Subsampling

Figure 40 shows the pixel sequence of a kernel which is read out over the single CMOS output channel. The pixels are transmitted in order or ascending for a normal readout and descending for a mirrored readout.

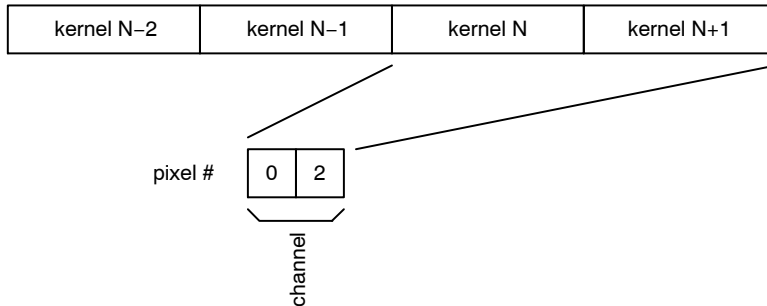


**Figure 40. CMOS Mode: Data Output Order without Subsampling**

• Subsampling On Monochrome Sensor

To read out the image data with subsampling enabled on a monochrome sensor, two neighboring kernels are combined to a single kernel of 4 pixels in the x-direction and

one pixel in the y-direction. Only the pixels at the even pixel positions inside that kernel are read out. Figure 41 shows the data order.

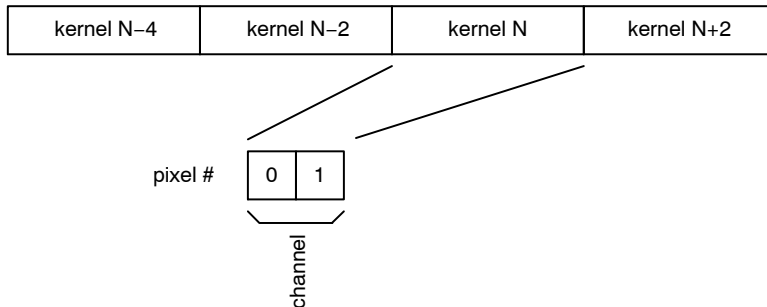


**Figure 41. CMOS Mode: Data Output Order with Subsampling on a Monochrome Sensor**

• Subsampling On Color Sensor

To read out the image data with subsampling enabled on a color sensor, two neighboring kernels are combined to a

single kernel of 4 pixels in the x-direction and one pixel in the y-direction. Figure 42 shows the data order.



**Figure 42. CMOS Mode: Data Output Order with Subsampling on a Color Sensor**

# PYTHON 480

## REGISTER MAP

**Table 25. REGISTER MAP**

| Address Offset                           | Address | Bit Field | Register Name       | Default (Hex) | Default | Description   | Type   |
|--|---------|-----------|---------------------|---------------|---------|---|--------|
| <b>Chip ID [Block Offset: 0]</b>         |         |           |                     |               |         |   |        |
| 0  | 0       |           | chip_id             | 0x5004        | 20484   | Chip ID   | Status |
|  |         | [15:0]    | id                  | 0x5004        | 20484   | Chip ID   |        |
| 1  | 1       |           | reserved            | 0x0000        | 0       | Reserved  | Status |
|  |         | [3:0]     | reserved            | 0x0           | 0       | Reserved  |        |
|  |         | [9:8]     | Resolution          | 0x0           | 0       | Chip Resolution   |        |
|  |         | [11:10]   | reserved            | 0x0           | 0       | Reserved  |        |
| 2  | 2       |           | chip_configuration  | 0x0000        | 0       | Chip General Configuration  | RW     |
|  |         | [0]       | color               | 0x0           | 0       | Color/Monochrome Configuration<br>'0': Monochrome<br>'1': Color       |        |
|  |         | [1]       | reserved            | 0x0           | 0       | Reserved  |        |
|  |         | [15:2]    | reserved            | 0x0           | 0       | Reserved  |        |
| <b>Reset Generator [Block Offset: 8]</b> |         |           |                     |               |         |   |        |
| 0  | 8       |           | soft_reset_pll      | 0x0099        | 153     | PLL Soft Reset Configuration  | RW     |
|  |         | [3:0]     | pll_soft_reset      | 0x9           | 9       | PLL Reset<br>0x9: Soft Reset State<br>others: Operational             |        |
|  |         | [7:4]     | pll_lock_soft_reset | 0x9           | 9       | PLL Lock Detect Reset<br>0x9: Soft Reset State<br>others: Operational |        |
| 1  | 9       |           | soft_reset_cgen     | 0x0009        | 9       | Clock Generator Soft Reset  | RW     |
|  |         | [3:0]     | cgen_soft_reset     | 0x9           | 9       | Clock Generator Reset<br>0x9: Soft Reset State<br>others: Operational |        |
| 2  | 10      |           | soft_reset_analog   | 0x0999        | 2457    | Analog Block Soft Reset   | RW     |
|  |         | [3:0]     | mux_soft_reset      | 0x9           | 9       | Column MUX Reset<br>0x9: Soft Reset State<br>others: Operational      |        |
|  |         | [7:4]     | afe_soft_reset      | 0x9           | 9       | AFE Reset<br>0x9: Soft Reset State<br>others: Operational             |        |
|  |         | [11:8]    | ser_soft_reset      | 0x9           | 9       | Serializer Reset<br>0x9: Soft Reset State<br>others: Operational      |        |
| <b>PLL [Block Offset: 16]</b>            |         |           |                     |               |         |   |        |
| 0  | 16      |           | power_down          | 0x0004        | 4       | PLL Configuration   | RW     |
|  |         | [0]       | pwd_n               | 0x0           | 0       | PLL Power Down<br>'0': Power Down,<br>'1': Operational                |        |
|  |         | [1]       | enable              | 0x0           | 0       | PLL Enable<br>'0': disabled,<br>'1': enabled                          |        |
|  |         | [2]       | bypass              | 0x1           | 1       | PLL Bypass<br>'0': PLL Active,<br>'1': PLL Bypassed                   |        |
| 1  | 17      |           | reserved            | 0x2113        | 8467    | Reserved  | RW     |
|  |         | [7:0]     | reserved            | 0x13          | 19      | Reserved  |        |
|  |         | [12:8]    | reserved            | 0x1           | 1       | Reserved  |        |
|  |         | [14:13]   | reserved            | 0x1           | 1       | Reserved  |        |

# PYTHON 480

**Table 25. REGISTER MAP** (continued)

| Address Offset                              | Address | Bit Field | Register Name      | Default (Hex) | Default | Description   | Type   |
|---|---------|-----------|--------------------|---------------|---------|---|--------|
| <b>I/O [Block Offset: 20]</b>               |         |           |                    |               |         |   |        |
| 0   | 20      |           | config1            | 0x0000        | 0       | IO Configuration  | RW     |
|   |         | [0]       | clock_in_pwd_n     | 0x0           | 0       | Power down Clock Input  |        |
|   |         | [9:8]     | reserved           | 0x0           | 0       | Reserved  |        |
|   |         | [10]      | reserved           | 0x0           | 0       | Reserved  |        |
| <b>PLL Lock Detector [Block Offset: 24]</b> |         |           |                    |               |         |   |        |
| 0   | 24      |           | pll_lock           | 0x0000        | 0       | PLL Lock Indication   | Status |
|   |         | [0]       | lock               | 0x0           | 0       | PLL Lock Indication   |        |
| 2   | 26      |           | reserved           | 0x2280        | 8832    | Reserved  | RW     |
|   |         | [7:0]     | reserved           | 0x80          | 128     | Reserved  |        |
|   |         | [10:8]    | reserved           | 0x2           | 2       | Reserved  |        |
|   |         | [14:12]   | reserved           | 0x2           | 2       | Reserved  |        |
| 3   | 27      |           | reserved           | 0x3D2D        | 15661   | Reserved  | RW     |
|   |         | [7:0]     | reserved           | 0x2D          | 45      | Reserved  |        |
|   |         | [15:8]    | reserved           | 0x3D          | 61      | Reserved  |        |
| <b>Clock Generator [Block Offset: 32]</b>   |         |           |                    |               |         |   |        |
| 0   | 32      |           | config0            | 0x2014        | 8212    | Clock Generator Configuration   | RW     |
|   |         | [0]       | enable_analog      | 0x0           | 0       | Enable analogue clocks<br>'0': disabled,<br>'1': enabled                              |        |
|   |         | [1]       | enable_log         | 0x0           | 0       | Enable logic clock<br>'0': disabled,<br>'1': enabled                                  |        |
|   |         | [2]       | select_pll         | 0x1           | 1       | Input Clock Selection<br>'0': Select LVDS clock input,<br>'1': Select PLL clock input |        |
|   |         | [3]       | adc_mode           | 0x0           | 0       | Set operation mode of CGEN block<br>'0': divide by 5 mode (10-bit mode)               |        |
|   |         | [4]       | enable_clkgate     | 0x1           | 1       | Clock gate on master distribution<br>'0': Clock active<br>'1': Clock inactive (gated) |        |
|   |         | [11:8]    | reserved           | 0x0           | 0       | Reserved  |        |
|   |         | [14:12]   | reserved           | 0x2           | 2       | Reserved  |        |
| <b>General Logic [Block Offset: 34]</b>     |         |           |                    |               |         |   |        |
| 0   | 34      |           | config0            | 0x0000        | 0       | Clock Generator Configuration   | RW     |
|   |         | [0]       | enable             | 0x0           | 0       | Logic General Enable Configuration<br>'0': Disable<br>'1': Enable                     |        |
| 0   | 38      |           | reserved           | 0x0000        | 0       | Reserved  | RW     |
|   |         | [15:0]    | reserved           | 0x0000        | 0       | Reserved  |        |
| <b>Image Core [Block Offset: 40]</b>        |         |           |                    |               |         |   |        |
| 0   | 40      |           | image_core_config0 | 0x0000        | 0       | Image Core Configuration  | RW     |
|   |         | [0]       | imc_pwd_n          | 0x0           | 0       | Image Core Power Down<br>'0': powered down,<br>'1': powered up                        |        |
|   |         | [1]       | mux_pwd_n          | 0x0           | 0       | Column Multiplexer Power Down<br>'0': powered down,<br>'1': powered up                |        |
|   |         | [2]       | colbias_enable     | 0x0           | 0       | Bias Enable<br>'0': disabled<br>'1': enabled  |        |
| 1   | 41      |           | image_core_config1 | 0x085A        | 2138    | Image Core Configuration  | RW     |

# PYTHON 480

**Table 25. REGISTER MAP** (continued)

| Address Offset | Address | Bit Field | Register Name | Default (Hex) | Default | Description | Type |
|----------------|---------|-----------|---------------|---------------|---------|-------------|------|
|                |         | [3:0]     | reserved      | 0xA           | 10      | Reserved    |      |
|                |         | [7:4]     | reserved      | 0x5           | 5       | Reserved    |      |
|                |         | [10:8]    | reserved      | 0x0           | 0       | Reserved    |      |
|                |         | [12:11]   | reserved      | 0x1           | 1       | Reserved    |      |
|                |         | [13]      | reserved      | 0x0           | 0       | Reserved    |      |
|                |         | [14]      | reserved      | 0x0           | 0       | Reserved    |      |
|                |         | [15]      | reserved      | 0x0           | 0       | Reserved    |      |
| 2              | 42      |           | reserved      | 0x0003        | 3       | Reserved    | RW   |
|                |         | [0]       | reserved      | 0x1           | 1       | Reserved    |      |
|                |         | [1]       | reserved      | 0x1           | 1       | Reserved    |      |
|                |         | [6:4]     | reserved      | 0x0           | 0       | Reserved    |      |
|                |         | [10:8]    | reserved      | 0x0           | 0       | Reserved    |      |
|                |         | [15:12]   | reserved      | 0x0           | 0       | Reserved    |      |
| 3              | 43      |           | reserved      | 0x0508        | 1288    | Reserved    | RW   |
|                |         | [0]       | reserved      | 0x0           | 0       | Reserved    |      |
|                |         | [1]       | reserved      | 0x0           | 0       | Reserved    |      |
|                |         | [2]       | reserved      | 0x0           | 0       | Reserved    |      |
|                |         | [3]       | reserved      | 0x1           | 1       | Reserved    |      |
|                |         | [6:4]     | reserved      | 0x0           | 0       | Reserved    |      |
|                |         | [7]       | reserved      | 0x0           | 0       | Reserved    |      |
|                |         | [11:8]    | reserved      | 0x5           | 5       | Reserved    |      |
|                |         | [15:12]   | reserved      | 0x0           | 0       | Reserved    |      |

**AFE [Block Offset: 48]**

|   |    |     |            |        |   |   |    |
|---|----|-----|------------|--------|---|---|----|
| 0 | 48 |     | power_down | 0x0000 | 0 | AFE Configuration   | RW |
|   |    | [0] | pwd_n      | 0x0    | 0 | Power down for AFE's<br>'0': powered down,<br>'1': powered up |    |

**Bias [Block Offset: 64]**

|   |    |         |               |        |       |  |    |
|---|----|---------|---------------|--------|-------|--|----|
| 0 | 64 |         | power_down    | 0x0000 | 0     | Bias Power Down Configuration  | RW |
|   |    | [0]     | pwd_n         | 0x0    | 0     | Power down bandgap<br>'0': powered down,<br>'1': powered up                      |    |
| 1 | 65 |         | configuration | 0xF8CB | 63691 | Bias Configuration   | RW |
|   |    | [0]     | extres        | 0x1    | 1     | External Resistor Selection<br>'0': internal resistor,<br>'1': external resistor |    |
|   |    | [3:1]   | reserved      | 0x5    | 5     | Reserved   |    |
|   |    | [7:4]   | reserved      | 0xC    | 12    | Reserved   |    |
|   |    | [11:8]  | reserved      | 0x8    | 8     | Reserved   |    |
|   |    | [15:12] | reserved      | 0xF    | 15    | Reserved   |    |
| 2 | 66 |         | reserved      | 0x53C8 | 21448 | Reserved   | RW |
|   |    | [3:0]   | reserved      | 0x8    | 8     | Reserved   |    |
|   |    | [7:4]   | reserved      | 0xC    | 12    | Reserved   |    |
|   |    | [14:8]  | reserved      | 0x53   | 83    | Reserved   |    |
| 3 | 67 |         | reserved      | 0x8788 | 34696 | Reserved   | RW |
|   |    | [3:0]   | reserved      | 0x8    | 8     | Reserved   |    |
|   |    | [7:4]   | reserved      | 0x8    | 8     | Reserved   |    |

# PYTHON 480

**Table 25. REGISTER MAP** (continued)

| Address Offset | Address | Bit Field | Register Name | Default (Hex) | Default | Description             | Type |
|----------------|---------|-----------|---------------|---------------|---------|-------------------------|------|
|                |         | [11:8]    | reserved      | 0x7           | 7       | Reserved                |      |
|                |         | [15:12]   | reserved      | 0x8           | 8       | Reserved                |      |
| 4              | 68      |           | lvds_bias     | 0x0085        | 133     | LVDS Bias Configuration | RW   |
|                |         | [3:0]     | lvds_ibias    | 0x5           | 5       | LVDS Ibias              |      |
|                |         | [7:4]     | lvds_iref     | 0x8           | 8       | LVDS Iref               |      |
| 5              | 69      |           | reserved      | 0x0088        | 2184    | Reserved                | RW   |
|                |         | [3:0]     | reserved      | 0x8           | 8       | Reserved                |      |
|                |         | [7:4]     | reserved      | 0x8           | 8       | Reserved                |      |
|                |         | [11:8]    | reserved      | 0x8           | 8       | Reserved                |      |
| 6              | 70      |           | reserved      | 0x4111        | 16657   | Reserved                | RW   |
|                |         | [3:0]     | reserved      | 0x1           | 1       | Reserved                |      |
|                |         | [7:4]     | reserved      | 0x1           | 1       | Reserved                |      |
|                |         | [11:8]    | reserved      | 0x1           | 1       | Reserved                |      |
|                |         | [15:12]   | reserved      | 0x4           | 4       | Reserved                |      |
| 7              | 71      |           | reserved      | 0x9788        | 38792   | Reserved                | RW   |
|                |         | [15:0]    | reserved      | 0x9788        | 38792   | Reserved                |      |

**Charge Pump [Block Offset: 72]**

|   |    |         |               |        |       |                           |    |
|---|----|---------|---------------|--------|-------|---------------------------|----|
| 0 | 72 |         | configuration | 0x3330 | 13104 | Charge Pump Configuration | RW |
|   |    | [0]     | reserved      | 0x0    | 0     | Reserved                  |    |
|   |    | [1]     | reserved      | 0x0    | 0     | Reserved                  |    |
|   |    | [2]     | reserved      | 0x0    | 0     | Reserved                  |    |
|   |    | [6:4]   | reserved      | 0x3    | 3     | Reserved                  |    |
|   |    | [10:8]  | reserved      | 0x3    | 3     | Reserved                  |    |
|   |    | [14:12] | reserved      | 0x3    | 3     | Reserved                  |    |
| 0 | 80 |         | reserved      | 0x0000 | 0     | Reserved                  | RW |
|   |    | [1:0]   | reserved      | 0x0    | 0     | Reserved                  |    |
|   |    | [3:2]   | reserved      | 0x0    | 0     | Reserved                  |    |
|   |    | [5:4]   | reserved      | 0x0    | 0     | Reserved                  |    |
|   |    | [7:6]   | reserved      | 0x0    | 0     | Reserved                  |    |
|   |    | [9:8]   | reserved      | 0x0    | 0     | Reserved                  |    |
| 1 | 81 |         | reserved      | 0x8881 | 34945 | Reserved                  | RW |
|   |    | [15:0]  | reserved      | 0x8881 | 34945 | Reserved                  |    |

**Temperature Sensor [Block Offset: 96]**

|   |     |        |          |        |   |                                  |        |
|---|-----|--------|----------|--------|---|----------------------------------|--------|
| 0 | 96  |        | enable   | 0x0000 | 0 | Temperature Sensor Configuration | RW     |
|   |     | [0]    | reserved | 0x0    | 0 | Reserved                         |        |
|   |     | [1]    | reserved | 0x0    | 0 | Reserved                         |        |
|   |     | [2]    | reserved | 0x0    | 0 | Reserved                         |        |
|   |     | [3]    | reserved | 0x0    | 0 | Reserved                         |        |
|   |     | [4]    | reserved | 0x0    | 0 | Reserved                         |        |
|   |     | [5]    | reserved | 0x0    | 0 | Reserved                         |        |
|   |     | [13:8] | offset   | 0x0    | 0 | Temperature Offset (signed)      |        |
| 1 | 97  |        | temp     | 0x0000 | 0 | Temperature Sensor Status        | Status |
|   |     | [7:0]  | temp     | 0x00   | 0 | Temperature Readout              |        |
| 0 | 104 |        | reserved | 0x0000 | 0 | Reserved                         | RW     |

# PYTHON 480

**Table 25. REGISTER MAP** (continued)

| Address Offset | Address | Bit Field | Register Name | Default (Hex) | Default | Description | Type |
|----------------|---------|-----------|---------------|---------------|---------|-------------|------|
|                |         | [15:0]    | reserved      | 0x0           | 0       | Reserved    |      |
| 1              | 105     |           | reserved      | 0x0000        | 0       | Reserved    | RW   |
|                |         | [1:0]     | reserved      | 0x0           | 0       | Reserved    |      |
|                |         | [5:2]     | reserved      | 0x0           | 0       | Reserved    |      |
|                |         | [7]       | reserved      | 0x0           | 0       | Reserved    |      |
|                |         | [9:8]     | reserved      | 0x0           | 0       | Reserved    |      |
|                |         | [13:10]   | reserved      | 0x0           | 0       | Reserved    |      |
|                |         | [15]      | reserved      | 0x0           | 0       | Reserved    |      |
| 2              | 106     |           | reserved      | 0x0000        | 0       | Reserved    | RW   |
|                |         | [15:0]    | reserved      | 0x0000        | 0       | Reserved    |      |
| 3              | 107     |           | reserved      | 0x0000        | 0       | Reserved    | RW   |
|                |         | [10:0]    | reserved      | 0x0000        | 0       | Reserved    |      |

**Serializers/LVDS/IO [Block Offset: 112]**

|   |     |     |                 |        |   |  |    |
|---|-----|-----|-----------------|--------|---|--|----|
| 0 | 112 |     | power_down      | 0x0000 | 0 | LVDS Power Down Configuration  | RW |
|   |     | [0] | clock_out_pwd_n | 0x0    | 0 | Power down for Clock Output.<br>'0': powered down,<br>'1': powered up              |    |
|   |     | [1] | sync_pwd_n      | 0x0    | 0 | Power down for Sync channel<br>'0': powered down,<br>'1': powered up               |    |
|   |     | [2] | data_pwd_n      | 0x0    | 0 | Power down for data channels (4 channels)<br>'0': powered down,<br>'1': powered up |    |

**Sync Words [Block Offset: 116]**

|    |     |       |                 |        |     |   |    |
|----|-----|-------|-----------------|--------|-----|---|----|
| 4  | 116 |       | trainingpattern | 0x03A6 | 934 | Data Formatting - Training Pattern  | RW |
|    |     | [9:0] | trainingpattern | 0x3A6  | 934 | Training pattern sent on Data channels during idle mode. This data is used to perform word alignment on the LVDS data channels. |    |
| 5  | 117 |       | sync_code0      | 0x002A | 42  | LVDS Power Down Configuration   | RW |
|    |     | [6:0] | frame_sync_0    | 0x02A  | 42  | Frame Sync Code LSBs - Even kernels   |    |
| 6  | 118 |       | sync_code1      | 0x0015 | 21  | Data Formatting - BL Indication   | RW |
|    |     | [9:0] | bl_0            | 0x015  | 21  | Black Pixel Identification Sync Code - Even kernels   |    |
| 7  | 119 |       | sync_code2      | 0x0035 | 53  | Data Formatting - IMG Indication  | RW |
|    |     | [9:0] | img_0           | 0x035  | 53  | Valid Pixel Identification Sync Code - Even kernels   |    |
| 8  | 120 |       | sync_code3      | 0x0025 | 37  | Data Formatting - IMG Indication  | RW |
|    |     | [9:0] | ref_0           | 0x025  | 37  | Reference Pixel Identification Sync Code - Even kernels   |    |
| 9  | 121 |       | sync_code4      | 0x002A | 42  | LVDS Power Down Configuration   | RW |
|    |     | [6:0] | frame_sync_1    | 0x02A  | 42  | Frame Sync Code LSBs - Odd kernels  |    |
| 10 | 122 |       | sync_code5      | 0x0015 | 21  | Data Formatting - BL Indication   | RW |
|    |     | [9:0] | bl_1            | 0x015  | 21  | Black Pixel Identification Sync Code - Odd kernels  |    |
| 11 | 123 |       | sync_code6      | 0x0035 | 53  | Data Formatting - IMG Indication  | RW |
|    |     | [9:0] | img_1           | 0x035  | 53  | Valid Pixel Identification Sync Code - Odd kernels  |    |
| 12 | 124 |       | sync_code7      | 0x0025 | 37  | Data Formatting - IMG Indication  | RW |
|    |     | [9:0] | ref_1           | 0x025  | 37  | Reference Pixel Identification Sync Code - Odd kernels  |    |

# PYTHON 480

**Table 25. REGISTER MAP** (continued)

| Address Offset | Address | Bit Field | Register Name | Default (Hex) | Default | Description                             | Type |
|----------------|---------|-----------|---------------|---------------|---------|---|------|
| 13             | 125     |           | sync_code8    | 0x0059        | 89      | Data Formatting - CRC Indication        | RW   |
|                |         | [9:0]     | crc           | 0x059         | 89      | CRC Value Identification Sync Code      |      |
| 14             | 126     |           | sync_code9    | 0x03A6        | 934     | Data Formatting - TR Indication         | RW   |
|                |         | [9:0]     | tr            | 0x3A6         | 934     | Training Value Identification Sync Code |      |
| 15             | 127     |           | reserved      | 0x02AA        | 682     | Reserved                                | RW   |
|                |         | [9:0]     | reserved      | 0x2AA         | 682     | Reserved                                |      |

**Data Block [Block Offset: 128]**

|   |     |         |                        |        |       |  |    |
|---|-----|---------|------------------------|--------|-------|--|----|
| 0 | 128 |         | blackcal               | 0x4714 | 18196 | Black Calibration Configuration  | RW |
|   |     | [7:0]   | black_offset           | 0x014  | 20    | Desired black level at output  |    |
|   |     | [10:8]  | black_samples          | 0x7    | 7     | Black pixels taken into account for black calibration.<br>Total samples = 2**black_samples   |    |
|   |     | [14:11] | reserved               | 0x8    | 8     | Reserved   |    |
|   |     | [15]    | crc_seed               | 0x0    | 0     | CRC Seed<br>'0': All-0<br>'1': All-1   |    |
| 1 | 129 |         | general_configuration  | 0x0001 | 1     | Black Calibration and Data Formatting Configuration  | RW |
|   |     | [0]     | auto_blackcal_enable   | 0x1    | 1     | Automatic blackcalibration is enabled when 1, bypassed when 0  |    |
|   |     | [9:1]   | blackcal_offset        | 0x00   | 0     | Black Calibration offset used when auto_black_cal_en = '0'.  |    |
|   |     | [10]    | blackcal_offset_dec    | 0x0    | 0     | blackcal_offset is added when 0, subtracted when 1   |    |
|   |     | [11]    | reserved               | 0x0    | 0     | Reserved   |    |
|   |     | [12]    | reserved               | 0x0    | 0     | Reserved   |    |
|   |     | [13]    | reserved               | 0x0    | 0     | Reserved   |    |
|   |     | [14]    | ref_mode               | 0x0    | 0     | Data contained on reference lines:<br>'0': reference pixels<br>'1': black average for the corresponding data channel   |    |
|   |     | [15]    | ref_bcal_enable        | 0x0    | 0     | Enable black calibration on reference lines<br>'0': Disabled<br>'1': Enabled   |    |
| 2 | 130 |         | general_configuration1 | 0x000F | 15    | Data Formatting - Training Pattern   | RW |
|   |     | [0]     | bl_frame_valid_enable  | 0x1    | 1     | Assert frame_valid for black lines when '1', gate frame_valid for black lines when '0'. Parallel output mode only.   |    |
|   |     | [1]     | bl_line_valid_enable   | 0x1    | 1     | Assert line_valid for black lines when '1', gate line_valid for black lines when '0'. Parallel output mode only.   |    |
|   |     | [2]     | ref_frame_valid_enable | 0x1    | 1     | Assert frame_valid for ref lines when '1', gate frame_valid for black lines when '0'. Parallel output mode only.   |    |
|   |     | [3]     | ref_line_valid_enable  | 0x1    | 1     | Assert line_valid for ref lines when '1', gate line_valid for black lines when '0'. Parallel output mode only.   |    |
|   |     | [4]     | frame_valid_mode       | 0x0    | 0     | Behaviour of frame_valid strobe between overhead lines when [0] and/or [1] is deasserted:<br>'0': retain frame_valid deasserted between lines<br>'1': assert frame_valid between lines |    |
|   |     | [5]     | invert_bitstream       | 0x0    | 0     | Negative Image<br>'0': Normal<br>'1': Negative   |    |



# PYTHON 480

**Table 25. REGISTER MAP** (continued)

| Address Offset | Address | Bit Field | Register Name       | Default (Hex) | Default | Description  | Type   |
|----------------|---------|-----------|---------------------|---------------|---------|--|--------|
|                |         | [8]       | data_negedge        | 0x0           | 0       | Clock-Data Relation<br>'0': data is clocked out on the rising edge of the related clock<br>'1': data is clocked out on the falling edge of the related clock |        |
|                |         | [9]       | reserved            | 0x0           | 0       | Reserved   |        |
| 8              | 136     |           | blackcal_error0     | 0x0000        | 0       | Black Calibration Status   | Status |
|                |         | [1:0]     | blackcal_error[1:0] | 0x0000        | 0       | Black Calibration Error. This flag is set when not enough black samples are available. Black Calibration shall not be valid.                                 |        |
| 12             | 140     |           | reserved            | 0x0000        | 0       | Reserved   | RW     |
|                |         | [15:0]    | reserved            | 0x0000        | 0       | Reserved   |        |
| 16             | 144     |           | test_configuration  | 0x0010        | 16      | Data Formating Test Configuration  | RW     |
|                |         | [0]       | testpattern_en      | 0x0           | 0       | Insert synthesized testpattern when '1'  |        |
|                |         | [1]       | inc_testpattern     | 0x0           | 0       | Incrementing testpattern when '1', constant testpattern when '0'   |        |
|                |         | [2]       | prbs_en             | 0x0           | 0       | Insert PRBS when '1'   |        |
|                |         | [3]       | frame_testpattern   | 0x0           | 0       | Frame test patterns when '1', unframed testpatterns when '0'   |        |
|                |         | [13:4]    | testpattern         | 0x1           | 1       | Testpattern used when testpatterns_en = '1'  |        |

**AEC [Block Offset: 160]**

|   |     |         |                     |        |       |   |    |
|---|-----|---------|---------------------|--------|-------|---|----|
| 0 | 160 |         | configuration       | 0x0010 | 16    | AEC Configuration   | RW |
|   |     | [0]     | enable              | 0x0    | 0     | AEC Enable  |    |
|   |     | [1]     | restart_filter      | 0x0    | 0     | Restart AEC filter  |    |
|   |     | [2]     | freeze              | 0x0    | 0     | Freeze AEC filter and enforcer gains  |    |
|   |     | [3]     | pixel_valid         | 0x0    | 0     | Use every pixel from channel when 0, every 4th pixel when 1                                   |    |
|   |     | [4]     | amp_pri             | 0x1    | 1     | Column amplifier gets higher priority than AFE PGA in gain distribution if 1. Vice versa if 0 |    |
| 1 | 161 |         | intensity           | 0x60B8 | 24760 | AEC Configuration   | RW |
|   |     | [9:0]   | desired_intensity   | 0xB8   | 184   | Target average intensity  |    |
|   |     | [15:10] | reserved            | 0x018  | 24    | Reserved  |    |
| 2 | 162 |         | red_scale_factor    | 0x0080 | 128   | Red Scale Factor  | RW |
|   |     | [9:0]   | red_scale_factor    | 0x80   | 128   | Red Scale Factor<br>3.7 unsigned  |    |
| 3 | 163 |         | green1_scale_factor | 0x0080 | 128   | Green1 Scale Factor   | RW |
|   |     | [9:0]   | green1_scale_factor | 0x80   | 128   | Green1 Scale Factor<br>3.7 unsigned   |    |
| 4 | 164 |         | green2_scale_factor | 0x0080 | 128   | Green2 Scale Factor   | RW |
|   |     | [9:0]   | green2_scale_factor | 0x80   | 128   | Green2 Scale Factor<br>3.7 unsigned   |    |
| 5 | 165 |         | blue_scale_factor   | 0x0080 | 128   | Blue Scale Factor   | RW |
|   |     | [9:0]   | blue_scale_factor   | 0x80   | 128   | Blue Scale Factor<br>3.7 unsigned   |    |
| 6 | 166 |         | reserved            | 0x03FF | 1023  | Reserved  | RW |
|   |     | [15:0]  | reserved            | 0x03FF | 1023  | Reserved  |    |
| 7 | 167 |         | reserved            | 0x0800 | 2048  | Reserved  | RW |
|   |     | [1:0]   | reserved            | 0x0    | 0     | Reserved  |    |
|   |     | [3:2]   | reserved            | 0x0    | 0     | Reserved  |    |
|   |     | [15:4]  | reserved            | 0x080  | 128   | Reserved  |    |

## PYTHON 480

**Table 25. REGISTER MAP** (continued)

| Address Offset | Address | Bit Field | Register Name       | Default (Hex) | Default | Description                                     | Type   |
|----------------|---------|-----------|---------------------|---------------|---------|---|--------|
| 8              | 168     |           | min_exposure        | 0x0001        | 1       | Minimum Exposure Time                           | RW     |
|                |         | [15:0]    | min_exposure        | 0x0001        | 1       | Minimum Exposure Time                           |        |
| 9              | 169     |           | min_gain            | 0x0800        | 2048    | Minimum Gain                                    | RW     |
|                |         | [1:0]     | min_mux_gain        | 0x0           | 0       | Minimum Column Amplifier Gain                   |        |
|                |         | [3:2]     | min_afe_gain        | 0x0           | 0       | Minimum AFE PGA Gain                            |        |
|                |         | [15:4]    | min_digital_gain    | 0x080         | 128     | Minimum Digital Gain<br>5.7 unsigned            |        |
| 10             | 170     |           | max_exposure        | 0x03FF        | 1023    | Maximum Exposure Time                           | RW     |
|                |         | [15:0]    | max_exposure        | 0x03FF        | 1023    | Maximum Exposure Time                           |        |
| 11             | 171     |           | max_gain            | 0x1001        | 4097    | Maximum Gain                                    | RW     |
|                |         | [1:0]     | max_mux_gain        | 0x1           | 1       | Maximum Column Amplifier Gain                   |        |
|                |         | [3:2]     | max_afe_gain        | 0x0           | 0       | Maximum AFE PGA Gain                            |        |
|                |         | [15:4]    | max_digital_gain    | 0x100         | 256     | Maximum Digital Gain<br>5.7 unsigned            |        |
| 12             | 172     |           | reserved            | 0x0083        | 131     | Reserved  | RW     |
|                |         | [7:0]     | reserved            | 0x083         | 131     | Reserved  |        |
|                |         | [13:8]    | reserved            | 0x00          | 0       | Reserved  |        |
|                |         | [15:14]   | reserved            | 0x0           | 0       | Reserved  |        |
| 13             | 173     |           | reserved            | 0x2824        | 10276   | Reserved  | RW     |
|                |         | [7:0]     | reserved            | 0x024         | 36      | Reserved  |        |
|                |         | [15:8]    | reserved            | 0x028         | 40      | Reserved  |        |
| 14             | 174     |           | reserved            | 0x2A96        | 10902   | Reserved  | RW     |
|                |         | [3:0]     | reserved            | 0x6           | 6       | Reserved  |        |
|                |         | [7:4]     | reserved            | 0x9           | 9       | Reserved  |        |
|                |         | [11:8]    | reserved            | 0xA           | 10      | Reserved  |        |
|                |         | [15:12]   | reserved            | 0x2           | 2       | Reserved  |        |
| 15             | 175     |           | reserved            | 0x0080        | 128     | Reserved  | RW     |
|                |         | [9:0]     | reserved            | 0x080         | 128     | Reserved  |        |
| 16             | 176     |           | reserved            | 0x00F1        | 241     | Reserved  | RW     |
|                |         | [9:0]     | reserved            | 0xF1          | 241     | Reserved  |        |
| 17             | 177     |           | reserved            | 0x0100        | 256     | Reserved  | RW     |
|                |         | [9:0]     | reserved            | 0x100         | 256     | Reserved  |        |
| 18             | 178     |           | reserved            | 0x0080        | 128     | Reserved  | RW     |
|                |         | [9:0]     | reserved            | 0x080         | 128     | Reserved  |        |
| 19             | 179     |           | reserved            | 0x00AA        | 170     | Reserved  | RW     |
|                |         | [9:0]     | reserved            | 0x0AA         | 170     | Reserved  |        |
| 20             | 180     |           | reserved            | 0x0100        | 256     | Reserved  | RW     |
|                |         | [9:0]     | reserved            | 0x100         | 256     | Reserved  |        |
| 21             | 181     |           | reserved            | 0x0155        | 341     | Reserved  | RW     |
|                |         | [9:0]     | reserved            | 0x155         | 341     | Reserved  |        |
| 24             | 184     |           | total_pixels0       | 0x0000        | 0       | AEC Status                                      | Status |
|                |         | [15:0]    | total_pixels[15:0]  | 0x0000        | 0       | Total number of pixels sampled for Average, LSB |        |
| 25             | 185     |           | total_pixels1       | 0x0000        | 0       | AEC Status                                      | Status |
|                |         | [7:0]     | total_pixels[23:16] | 0x0           | 0       | Total number of pixels sampled for Average, MSB |        |

Table 25. REGISTER MAP (continued)

| Address Offset | Address | Bit Field | Register Name   | Default (Hex) | Default | Description                             | Type   |
|----------------|---------|-----------|-----------------|---------------|---------|---|--------|
| 26             | 186     |           | average_status  | 0x0000        | 0       | ASE Status                              | Status |
|                |         | [9:0]     | average         | 0x000         | 0       | AEC Average Status                      |        |
|                |         | [12]      | avg_locked      | 0x0           | 0       | AEC Average Lock Status                 |        |
| 27             | 187     |           | exposure_status | 0x0000        | 0       | ASE Status                              | Status |
|                |         | [15:0]    | exposure        | 0x0000        | 0       | AEC Exposure Status                     |        |
| 28             | 188     |           | gain_status     | 0x0000        | 0       | ASE Status                              | Status |
|                |         | [1:0]     | mux_gain        | 0x0           | 0       | AEC MUX Gain Status                     |        |
|                |         | [3:2]     | afe_gain        | 0x0           | 0       | AEC AFE Gain Status                     |        |
|                |         | [15:4]    | digital_gain    | 0x000         | 0       | AEC Digital Gain Status<br>5.7 unsigned |        |
| 29             | 189     |           | reserved        | 0x0000        | 0       | Reserved                                | Status |
|                |         | [12:0]    | reserved        | 0x000         | 0       | Reserved                                |        |
|                |         | [13]      | reserved        | 0x0           | 0       | Reserved                                |        |

Sequencer [Block Offset: 192]

|   |     |         |                       |        |     |  |    |
|---|-----|---------|-----------------------|--------|-----|--|----|
| 0 | 192 |         | general_configuration | 0x0002 | 2   | Sequencer General Configuration  | RW |
|   |     | [0]     | enable                | 0x0    | 0   | Enable sequencer<br>'0': Idle,<br>'1': enabled   |    |
|   |     | [1]     | fast_startup          | 0x1    | 1   | Fast startup<br>'0': First frame is full frame (blanked out)<br>'1': Reduced startup time  |    |
|   |     | [2]     | reserved              | 0x0    | 0   | Reserved   |    |
|   |     | [3]     | reserved              | 0x0    | 0   | Reserved   |    |
|   |     | [4]     | triggered_mode        | 0x0    | 0   | Triggered Mode Selection<br>'0': Normal Mode,<br>'1': Triggered Mode   |    |
|   |     | [5]     | slave_mode            | 0x0    | 0   | Master/Slave Selection<br>'0': master,<br>'1': slave   |    |
|   |     | [6]     | reserved              | 0x0    | 0   | Reserved   |    |
|   |     | [7]     | subsampling           | 0x0    | 0   | Subsampling mode selection<br>'0': no subsampling,<br>'1': subsampling   |    |
|   |     | [8]     | reserved              | 0x0    | 0   | Reserved   |    |
|   |     | [10]    | roi_aec_enable        | 0x0    | 0   | Enable windowing for AEC Statistics.<br>'0': Subsample all windows<br>'1': Subsample configured window                           |    |
|   |     | [13:11] | monitor_select        | 0x0    | 0   | Control of the monitor pins  |    |
|   |     | [14]    | reserved              | 0x0    | 0   | Reserved   |    |
|   |     | [15]    | sequence              | 0x0    | 0   | Enable a sequenced readout with different parameters for even and odd frames   |    |
| 2 | 194 |         | integration_control   | 0x00E4 | 228 | Integration Control  | RW |
|   |     | [0]     | reserved              | 0x0    | 0   | Reserved   |    |
|   |     | [1]     | reserved              | 0x0    | 0   | Reserved   |    |
|   |     | [2]     | fr_mode               | 0x1    | 1   | Representation of fr_length.<br>'0': reset length<br>'1': frame length   |    |
|   |     | [3]     | reserved              | 0x0    | 0   | Reserved   |    |
|   |     | [4]     | int_priority          | 0x0    | 0   | Integration Priority<br>'0': Frame readout has priority over integration<br>'1': Integration End has priority over frame readout |    |

# PYTHON 480

**Table 25. REGISTER MAP** (continued)

| Address Offset | Address | Bit Field | Register Name     | Default (Hex) | Default | Description  | Type |
|----------------|---------|-----------|-------------------|---------------|---------|--|------|
|                |         | [5]       | halt_mode         | 0x1           | 1       | The current frame will be completed when the sequencer is disabled and halt_mode = '1'. When '0', the sensor stops immediately when disabled, without finishing the current frame. |      |
|                |         | [6]       | fss_enable        | 0x1           | 1       | Generation of Frame Sequence Start Sync code (FSS)<br>'0': No generation of FSS<br>'1': Generation of FSS  |      |
|                |         | [7]       | fse_enable        | 0x1           | 1       | Generation of Frame Sequence End Sync code (FSE)<br>'0': No generation of FSE<br>'1': Generation of FSE  |      |
|                |         | [8]       | reverse_y         | 0x0           | 0       | Reverse readout<br>'0': bottom to top readout<br>'1': top to bottom readout  |      |
|                |         | [9]       | reverse_x         | 0x0           | 0       | Reverse readout (X-direction)<br>'0': left to right<br>'1': right to left  |      |
|                |         | [11:10]   | subsampling_mode  | 0x0           | 0       | Subsampling mode<br>"00": Subsampling in x and y (VITA compatible)<br>"01": Subsampling in x, not y<br>"10": Subsampling in y, not x<br>"11": Subsampling in x and y               |      |
|                |         | [13:12]   | reserved          | 0x0           | 0       | Reserved   |      |
|                |         | [14]      | reserved          | 0x0           | 0       | Reserved   |      |
|                |         | [15]      | reserved          | 0x0           | 0       | Reserved   |      |
| 3              | 195     |           | roi_active0_0     | 0x0001        | 1       | Active ROI Selection   | RW   |
|                |         | [3:0]     | roi_active0       | 0x01          | 1       | Active ROI Selection<br>[0] Roi0 Active<br>[1] Roi1 Active<br>...<br>[3] Roi3 Active   |      |
| 5              | 197     |           | black_lines       | 0x0104        | 260     | Black Line Configuration   | RW   |
|                |         | [7:0]     | black_lines       | 0x04          | 4       | Number of black lines. Minimum is 1. Range 1-255   |      |
|                |         | [12:8]    | gate_first_line   | 0x1           | 1       | Blank out first lines<br>0: no blank<br>1-31: blank 1-31 lines   |      |
| 6              | 198     |           | init_reset_length | 0x0040        | 64      | Initial Reset Length   | RW   |
|                |         | [15:0]    | init_reset_length | 0x0040        | 64      | Initial Reset Length in Fast Startup Mode (reg_sec_fast_startup = 0x1)   |      |
| 7              | 199     |           | mult_timer0       | 0x0001        | 1       | Exposure/Frame Rate Configuration  | RW   |
|                |         | [15:0]    | mult_timer0       | 0x0001        | 1       | Mult Timer (Global shutter only)<br>Defines granularity (unit = 1/PLL clock) of exposure and reset_length  |      |
| 8              | 200     |           | fr_length0        | 0x0000        | 0       | Exposure/Frame Rate Configuration  | RW   |
|                |         | [15:0]    | fr_length0        | 0x0000        | 0       | Frame/Reset length (Global shutter only)<br>Reset length when fr_mode = '0',<br>Frame Length when fr_mode = '1'<br>Granularity defined by mult_timer                               |      |
| 9              | 201     |           | exposure0         | 0x0000        | 0       | Exposure/Frame Rate Configuration  | RW   |
|                |         | [15:0]    | exposure0         | 0x0000        | 0       | Exposure Time<br>Granularity defined by mult_timer   |      |
| 10             | 202     |           | reserved          | 0x0000        | 0       | Reserved   | RW   |
|                |         | [15:0]    | reserved          | 0x0000        | 0       | Reserved   |      |
| 11             | 203     |           | reserved          | 0x0000        | 0       | Reserved   | RW   |
|                |         | [15:0]    | reserved          | 0x0000        | 0       | Reserved   |      |

## PYTHON 480

**Table 25. REGISTER MAP** (continued)

| Address Offset | Address | Bit Field | Register Name               | Default (Hex) | Default | Description  | Type |
|----------------|---------|-----------|-----------------------------|---------------|---------|--|------|
| 12             | 204     |           | gain_configuration0         | 0x01E1        | 481     | Gain Configuration   | RW   |
|                |         | [4:0]     | mux_gainsw0                 | 0x01          | 1       | Column Gain Setting  |      |
|                |         | [12:5]    | afe_gain0                   | 0xF           | 15      | AFE Programmable Gain Setting  |      |
|                |         | [13]      | gain_lat_comp               | 0x0           | 0       | Postpone gain update by 1 frame when '1' to compensate for exposure time updates latency. Gain is applied at start of next frame if '0'  |      |
| 13             | 205     |           | digital_gain_configuration0 | 0x0080        | 128     | Gain Configuration   | RW   |
|                |         | [11:0]    | db_gain0                    | 0x080         | 128     | Digital Gain   |      |
| 14             | 206     |           | sync_configuration          | 0x037A        | 890     | Synchronization Configuration  | RW   |
|                |         | [1]       | sync_black_lines            | 0x1           | 1       | Update of black_lines will not be sync'ed at start of frame when '0'   |      |
|                |         | [3]       | sync_exposure               | 0x1           | 1       | Update of exposure will not be sync'ed at start of frame when '0'  |      |
|                |         | [4]       | sync_gain                   | 0x1           | 1       | Update of gain settings (gain_sw, afe_gain) will not be sync'ed at start of frame when '0'   |      |
|                |         | [5]       | sync_roi                    | 0x1           | 1       | Update of roi updates (active_roi) will not be sync'ed at start of frame when '0'  |      |
|                |         | [6]       | sync_ref_lines              | 0x1           | 1       | Update of ref_lines will not be sync'ed at start of frame when '0'   |      |
|                |         | [8]       | blank_roi_switch            | 0x1           | 1       | Blank first frame after ROI switching  |      |
|                |         | [9]       | blank_subsampling_ss        | 0x1           | 1       | Blank first frame after subsampling mode<br>'0': No blanking<br>'1': Blanking  |      |
|                |         | [10]      | exposure_sync_mode          | 0x0           | 0       | When '0', exposure configurations are sync'ed at the start of FOT. When '1', exposure configurations sync is disabled (continuously syncing). This mode is only relevant for Triggered Global - master mode, where the exposure configurations are sync'ed at the start of exposure rather than the start of FOT. For all other modes it should be set to '0'. Note: Sync is still postponed if sync_exposure='0'. |      |
| 15             | 207     |           | ref_lines                   | 0x0000        | 0       | Reference Line Configuration   | RW   |
|                |         | [7:0]     | ref_lines                   | 0x00          | 0       | Number of Reference Lines<br>0-255   |      |
| 16             | 208     |           | reserved                    | 0xC900        | 51456   | Reserved   | RW   |
|                |         | [7:0]     | reserved                    | 0x00          | 0       | Reserved   |      |
|                |         | [15:8]    | reserved                    | 0xC9          | 201     | Reserved   |      |
| 17             | 209     |           | reserved                    | 0x0004        | 4       | Reserved   | RW   |
|                |         | [0]       | reserved                    | 0x0           | 0       | Reserved   |      |
|                |         | [2]       | reserved                    | 0x1           | 1       | Reserved   |      |
|                |         | [15:8]    | xsm_delay                   | 0x00          | 0       | Delay between ROT end and X-readout  |      |
| 19             | 211     |           | reserved                    | 0x0049        | 73      | Reserved   | RW   |
|                |         | [0]       | reserved                    | 0x1           | 1       | Reserved   |      |
|                |         | [1]       | reserved                    | 0x0           | 0       | Reserved   |      |
|                |         | [2]       | reserved                    | 0x0           | 0       | Reserved   |      |
|                |         | [3]       | reserved                    | 0x1           | 1       | Reserved   |      |
|                |         | [6:4]     | reserved                    | 0x4           | 4       | Reserved   |      |
|                |         | [15:8]    | reserved                    | 0x0           | 0       | Reserved   |      |
| 20             | 212     |           | reserved                    | 0x0000        | 0       | Reserved   | RW   |
|                |         | [9:0]     | reserved                    | 0x0000        | 0       | Reserved   |      |

## PYTHON 480

**Table 25. REGISTER MAP** (continued)

| Address Offset | Address | Bit Field | Register Name | Default (Hex) | Default | Description | Type |
|----------------|---------|-----------|---------------|---------------|---------|-------------|------|
|                |         | [15]      | reserved      | 0x00          | 0       | Reserved    |      |
| 21             | 213     |           | reserved      | 0x025F        | 607     | Reserved    | RW   |
|                |         | [9:0]     | reserved      | 0x025F        | 607     | Reserved    |      |
| 22             | 214     |           | reserved      | 0x0100        | 256     | Reserved    | RW   |
|                |         | [7:0]     | reserved      | 0x00          | 0       | Reserved    |      |
| 23             | 215     |           | reserved      | 0x191F        | 6431    | Reserved    | RW   |
|                |         | [0]       | reserved      | 0x1           | 1       | Reserved    |      |
|                |         | [1]       | reserved      | 0x1           | 1       | Reserved    |      |
|                |         | [2]       | reserved      | 0x1           | 1       | Reserved    |      |
|                |         | [3]       | reserved      | 0x1           | 1       | Reserved    |      |
|                |         | [4]       | reserved      | 0x1           | 1       | Reserved    |      |
|                |         | [5]       | reserved      | 0x0           | 0       | Reserved    |      |
|                |         | [6]       | reserved      | 0x0           | 0       | Reserved    |      |
|                |         | [8]       | reserved      | 0x1           | 1       | Reserved    |      |
|                |         | [9]       | reserved      | 0x0           | 0       | Reserved    |      |
|                |         | [10]      | reserved      | 0x0           | 0       | Reserved    |      |
|                |         | [11]      | reserved      | 0x1           | 1       | Reserved    |      |
|                |         | [12]      | reserved      | 0x1           | 1       | Reserved    |      |
|                |         | [13]      | reserved      | 0x0           | 0       | Reserved    |      |
|                |         | [14]      | reserved      | 0x0           | 0       | Reserved    |      |
| 24             | 216     |           | reserved      | 0x0000        | 0       | Reserved    | RW   |
|                |         | [6:0]     | reserved      | 0x00          | 0       | Reserved    |      |
|                |         |           |               |               |         |             |      |
| 25             | 217     |           | reserved      | 0x4848        | 18504   | Reserved    | RW   |
|                |         | [6:0]     | reserved      | 0x48          | 72      | Reserved    |      |
|                |         | [14:8]    | reserved      | 0x48          | 72      | Reserved    |      |
| 26             | 218     |           | reserved      | 0x4848        | 18504   | Reserved    | RW   |
|                |         | [6:0]     | reserved      | 0x48          | 72      | Reserved    |      |
|                |         | [14:8]    | reserved      | 0x48          | 72      | Reserved    |      |
| 27             | 219     |           | reserved      | 0x005C        | 92      | Reserved    | RW   |
|                |         | [6:0]     | reserved      | 0x05C         | 92      | Reserved    |      |
|                |         | [14:8]    | reserved      | 0x00          | 0       | Reserved    |      |
| 28             | 220     |           | reserved      | 0x3624        | 13860   | Reserved    | RW   |
|                |         | [6:0]     | reserved      | 0x24          | 36      | Reserved    |      |
|                |         | [14:8]    | reserved      | 0x36          | 54      | Reserved    |      |
| 29             | 221     |           | reserved      | 0x0036        | 54      | Reserved    | RW   |
|                |         | [6:0]     | reserved      | 0x36          | 54      | Reserved    |      |
|                |         | [14:8]    | reserved      | 0x0           | 0       | Reserved    |      |
| 30             |         |           | reserved      | 0x0           |         | Reserved    | RW   |
|                |         | [14:8]    | reserved      | 0x0           | 0       | Reserved    |      |
| 32             | 224     |           | reserved      | 0x3E07        | 15879   | Reserved    | RW   |
|                |         | [3:0]     | reserved      | 0x7           | 7       | Reserved    |      |
|                |         | [7:4]     | reserved      | 0x00          | 0       | Reserved    |      |
|                |         | [8]       | reserved      | 0x0           | 0       | Reserved    |      |

# PYTHON 480

**Table 25. REGISTER MAP** (continued)

| Address Offset | Address | Bit Field | Register Name | Default (Hex) | Default | Description  | Type |
|----------------|---------|-----------|---------------|---------------|---------|--|------|
|                |         | [9]       | reserved      | 0x1           | 1       | Reserved   |      |
|                |         | [10]      | reserved      | 0x1           | 1       | Reserved   |      |
|                |         | [11]      | reserved      | 0x1           | 1       | Reserved   |      |
|                |         | [12]      | reserved      | 0x1           | 1       | Reserved   |      |
|                |         | [13]      | reserved      | 0x1           | 1       | Reserved   |      |
| 33             | 225     |           | reserved      | 0x5EF1        | 24305   | Reserved   | RW   |
|                |         | [4:0]     | reserved      | 0x11          | 17      | Reserved   |      |
|                |         | [9:5]     | reserved      | 0x17          | 23      | Reserved   |      |
|                |         | [14:10]   | reserved      | 0x17          | 23      | Reserved   |      |
|                |         | [15]      | reserved      | 0x0           | 0       | Reserved   |      |
| 34             | 226     |           | reserved      | 0x6000        | 24576   | Reserved   | RW   |
|                |         | [4:0]     | reserved      | 0x00          | 0       | Reserved   |      |
|                |         | [9:5]     | reserved      | 0x00          | 0       | Reserved   |      |
|                |         | [14:10]   | reserved      | 0x18          | 24      | Reserved   |      |
|                |         | [15]      | reserved      | 0x0           | 0       | Reserved   |      |
| 35             | 227     |           | reserved      | 0x0000        | 0       | Reserved   | RW   |
|                |         | [0]       | reserved      | 0x0           | 0       | Reserved   |      |
|                |         | [1]       | reserved      | 0x0           | 0       | Reserved   |      |
|                |         | [2]       | reserved      | 0x0           | 0       | Reserved   |      |
|                |         | [3]       | reserved      | 0x0           | 0       | Reserved   |      |
|                |         | [4]       | reserved      | 0x0           | 0       | Reserved   |      |
| 36             | 228     |           | roi_active0_1 | 0x0001        | 1       | Active ROI Selection   | RW   |
|                |         | [3:0]     | roi_active1   | 0x01          | 1       | Active ROI Selection<br>[0] ROI0 Active<br>[1] ROI1 Active<br>[2] ROI2 Active<br>[3] ROI3 Active |      |
| 38             | 230     |           | reserved      | 0x0001        | 1       | Reserved   | RW   |
|                |         | [15:0]    | reserved      | 0x0001        | 1       | Reserved   |      |
| 39             | 231     |           | reserved      | 0x0000        | 0       | Reserved   | RW   |
|                |         | [15:0]    | reserved      | 0x0000        | 0       | Reserved   |      |
| 40             | 232     |           | reserved      | 0x0000        | 0       | Reserved   | RW   |
|                |         | [15:0]    | reserved      | 0x0000        | 0       | Reserved   |      |
| 41             | 233     |           | reserved      | 0x0000        | 0       | Reserved   | RW   |
|                |         | [15:0]    | reserved      | 0x0000        | 0       | Reserved   |      |
| 42             | 234     |           | reserved      | 0x0000        | 0       | Reserved   | RW   |
|                |         | [15:0]    | reserved      | 0x0000        | 0       | Reserved   |      |
| 43             | 235     |           | reserved      | 0x01E3        | 483     | Reserved   | RW   |
|                |         | [4:0]     | reserved      | 0x03          | 3       | Reserved   |      |
|                |         | [12:5]    | reserved      | 0xF           | 15      | Reserved   |      |
| 44             | 236     |           | reserved      | 0x0080        | 128     | Reserved   | RW   |
|                |         | [11:0]    | reserved      | 0x080         | 128     | Reserved   |      |
| 47             | 239     |           | reserved      | 0x0000        | 0       | Reserved   | RW   |
|                |         | [1:0]     | reserved      | 0x0           | 0       | Reserved   |      |
| 58             | 250     |           | reserved      | 0x1081        | 4225    | Reserved   | RW   |
|                |         | [4:0]     | reserved      | 0x01          | 1       | Reserved   |      |

Table 25. REGISTER MAP (continued)

| Address Offset | Address | Bit Field | Register Name          | Default (Hex) | Default | Description   | Type |
|----------------|---------|-----------|------------------------|---------------|---------|---|------|
|                |         | [9:5]     | reserved               | 0x04          | 4       | Reserved  |      |
|                |         | [14:10]   | reserved               | 0x04          | 4       | Reserved  |      |
| 59             | 251     |           | reserved               | 0x030F        | 783     | Reserved  | RW   |
|                |         | [7:0]     | reserved               | 0xF           | 15      | Reserved  |      |
|                |         | [15:8]    | reserved               | 0x3           | 3       | Reserved  |      |
| 60             | 252     |           | reserved               | 0x0601        | 1537    | Reserved  | RW   |
|                |         | [7:0]     | reserved               | 0x1           | 1       | Reserved  |      |
|                |         | [15:8]    | reserved               | 0x6           | 6       | Reserved  |      |
| 61             | 253     |           | roi_aec_configuration0 | 0xC900        | 51456   | AEC ROI Configuration   | RW   |
|                |         | [7:0]     | x_start                | 0x00          | 0       | AEC ROI X Start Configuration (used for AEC statistics when roi_aec_enable='1') (bits 8..1) |      |
|                |         | [15:8]    | x_end                  | 0x0C9         | 201     | AEC ROI X End Configuration (used for AEC statistics when roi_aec_enable='1') (bits 8..1)   |      |
| 62             | 254     |           | roi_aec_configuration1 | 0x9700        | 0       | AEC ROI Configuration   | RW   |
|                |         | [7:0]     | y_start                | 0x00          | 0       | AEC ROI Y Start Configuration (used for AEC statistics when roi_aec_enable='1') (bits 9..2) |      |
|                |         | [15:8]    | x_end                  | 0x97          | 151     | AEC ROI End Configuration (used for AEC statistics when roi_aec_enable='1') (bits 9..2)     |      |
| 63             | 255     |           | roi_aec_configuration2 | 0x00C4        | 0       | AEC ROI Configuration   | RW   |
|                |         | [0]       | x_start(0)             | 0x0           | 0       | AEC ROI Y End Configuration (used for AEC statistics when roi_aec_enable='1') (bit 0)       |      |
|                |         | [2]       | x_end(0)               | 0x1           | 1       | AEC ROI End Configuration (used for AEC statistics when roi_aec_enable='1') (bit 0)         |      |
|                |         | [5:4]     | y_start(1:0)           | 0x0           | 0       | AEC ROI End Configuration (used for AEC statistics when roi_aec_enable='1') (bits 1..0)     |      |
|                |         | [7:6]     | y_end(1:0)             | 0x3           | 3       | AEC ROI End Configuration (used for AEC statistics when roi_aec_enable='1') (bits 1..0)     |      |

Sequencer ROI [Block Offset: 256]

|   |     |        |                     |        |       |   |    |
|---|-----|--------|---------------------|--------|-------|---|----|
| 0 | 256 |        | roi0_configuration0 | 0xC900 | 51456 | ROI Configuration                         | RW |
|   |     | [7:0]  | x_start             | 0x00   | 0     | ROI 0 – X Start Configuration (bits 8..1) |    |
|   |     | [15:8] | x_end               | 0xC9   | 201   | ROI 0 – X End Configuration (bits 8..1)   |    |
| 1 | 257 |        | roi0_configuration1 | 0x9700 | 38656 | ROI Configuration                         | RW |
|   |     | [7:0]  | y_start             | 0x00   | 0     | ROI 0 – Y Start Configuration (bits 9..2) |    |
|   |     | [15:8] | y_end               | 0x97   | 151   | ROI 0 – Y End Configuration (bits 9..2)   |    |
| 2 | 258 |        | roi1_configuration0 | 0xC900 | 51456 | ROI Configuration                         | RW |
|   |     | [7:0]  | x_start             | 0x00   | 0     | ROI 1 – X Start Configuration (bits 8..1) |    |
|   |     | [15:8] | x_end               | 0xC9   | 201   | ROI 1 – X End Configuration (bits 8..1)   |    |
| 3 | 259 |        | roi1_configuration1 | 0x9700 | 38656 | ROI Configuration                         | RW |
|   |     | [7:0]  | x_start             | 0x00   | 0     | ROI 1 – Y Start Configuration (bits 9..2) |    |
|   |     | [15:8] | x_end               | 0x97   | 151   | ROI 1 – Y End Configuration (bits 9..2)   |    |
| 4 | 260 |        | roi2_configuration0 | 0xC900 | 51456 | ROI Configuration                         | RW |
|   |     | [7:0]  | x_start             | 0x00   | 0     | ROI 2 – X Start Configuration (bits 8..1) |    |
|   |     | [15:8] | x_end               | 0xC9   | 201   | ROI 2 – X End Configuration (bits 8..1)   |    |
| 5 | 261 |        | roi2_configuration1 | 0x9700 | 38656 | ROI Configuration                         | RW |
|   |     | [7:0]  | y_start             | 0x00   | 0     | ROI 2 – Y Start Configuration (bits 9..2) |    |
|   |     | [15:8] | y_end               | 0x97   | 151   | ROI 2 – Y End Configuration (bits 9..2)   |    |



# PYTHON 480

**Table 25. REGISTER MAP** (continued)

| Address Offset | Address | Bit Field | Register Name         | Default (Hex) | Default | Description                               | Type |
|----------------|---------|-----------|-----------------------|---------------|---------|---|------|
| 6              | 262     |           | roi3_configuration0   | 0xC900        | 51456   | ROI Configuration                         | RW   |
|                |         | [7:0]     | x_start               | 0x00          | 0       | ROI 3 – X Start Configuration (bits 8..1) |      |
|                |         | [15:8]    | x_end                 | 0xC9          | 201     | ROI 3 – X End Configuration (bits 8..1)   |      |
| 7              | 263     |           | roi3_configuration1   | 0x9700        | 38656   | ROI Configuration                         | RW   |
|                |         | [7:0]     | y_start               | 0x00          | 0       | ROI 3 – Y Start Configuration (bits 9..2) |      |
|                |         | [15:8]    | y_end                 | 0x97          | 151     | ROI 3 – Y End Configuration (bits 9..2)   |      |
| 8              | 264     |           | roi_configuration_ls0 | 0xC4C4        | 50372   | ROI Configuration                         | RW   |
|                |         | [0]       | x_start0(0)           | 0x0           | 0       | ROI 0 – X Start Configuration (bit 0)     |      |
|                |         | [2]       | x_end0(0)             | 0x1           | 1       | ROI 0 – X End Configuration (bit 0)       |      |
|                |         | [5:4]     | y_start0(1:0)         | 0x0           | 0       | ROI 0 – Y Start Configuration (bits 1..0) |      |
|                |         | [7:6]     | y_end0(1:0)           | 0x3           | 3       | ROI 0 – Y End Configuration (bits 1..0)   |      |
|                |         | [8]       | x_start1(0)           | 0x0           | 0       | ROI 1 – X Start Configuration (bit 0)     |      |
|                |         | [10]      | x_end1(0)             | 0x1           | 1       | ROI 1 – X End Configuration (bit 0)       |      |
|                |         | [13:12]   | y_start1(1:0)         | 0x0           | 0       | ROI 1 – Y Start Configuration (bits 1..0) |      |
|                |         | [15:14]   | y_end1(1:0)           | 0x3           | 3       | ROI 1 – Y End Configuration (bits 1..0)   |      |
| 9              | 265     |           | roi_configuration_ls1 | 0xC4C4        | 50372   | ROI Configuration                         | RW   |
|                |         | [0]       | x_start0(0)           | 0x0           | 0       | ROI 2 – X Start Configuration (bit 0)     |      |
|                |         | [2]       | x_end0(0)             | 0x1           | 1       | ROI 2 – X End Configuration (bit 0)       |      |
|                |         | [5:4]     | y_start0(1:0)         | 0x0           | 0       | ROI 2 – Y Start Configuration (bits 1..0) |      |
|                |         | [7:6]     | y_end0(1:0)           | 0x3           | 3       | ROI 2 – Y End Configuration (bits 1..0)   |      |
|                |         | [8]       | x_start1(0)           | 0x0           | 0       | ROI 3 – X Start Configuration (bit 0)     |      |
|                |         | [10]      | x_end1(0)             | 0x1           | 1       | ROI 3 – X End Configuration (bit 0)       |      |
|                |         | [13:12]   | y_start1(1:0)         | 0x0           | 0       | ROI 3 – Y Start Configuration (bits 1..0) |      |
|                |         | [15:14]   | y_end1(1:0)           | 0x3           | 3       | ROI 3 – Y End Configuration (bits 1..0)   |      |

**Sequencer ROI [Block Offset: 384]**

|    |     |        |          |  |  |          |    |
|----|-----|--------|----------|--|--|----------|----|
| 0  | 384 |        | reserved |  |  | Reserved | RW |
|    |     | [15:0] | reserved |  |  | Reserved |    |
|    | ... |        | ...      |  |  | ...      | RW |
|    |     |        | ...      |  |  | ...      |    |
| 95 | 479 |        | reserved |  |  | Reserved | RW |
|    |     | [15:0] | reserved |  |  | Reserved |    |

# PYTHON 480

## PACKAGE INFORMATION

### Pin List

The LVDS I/Os comply to the TIA/EIA-644-A Standard and the CMOS I/Os have a 1.8 V signal level.

**Table 26. PIN LIST**

| Pin Map | Pin Name      | I/O Type | Direction | Description  |
|---------|---------------|----------|-----------|--|
| A1      | VDD_PIX       | Supply   |           | Pixel Array Supply                                   |
| B1      | VDD_33        | Supply   |           | 3.3 V Supply   |
| C1      | MONITOR0      | CMOS     | Output    | Monitor Output #0                                    |
| D1      | MONITOR1      | CMOS     | Output    | Monitor Output #1                                    |
| E1      | IBIAS_MASTER  | Analog   | I/O       | Master Bias Reference. Connect with 47kOhm to VSS_33 |
| F1      | CP_RESPD      | Analog   | Output    | For Test Only – Do not connect                       |
| G1      | CP_CALIB      | Analog   | Output    | For Test Only – Do not connect                       |
| H1      | MBSINOUT_1    | Analog   | I/O       | For Test Only – Do not connect                       |
| A2      | VDD_18        | Supply   |           | 1.8 V Supply   |
| B2      | VSS_COLPC     | Supply   |           | Pixel Array Ground                                   |
| C2      | SCAN_EN       | CMOS     | Input     | For Test Only – Connect to VSS_18                    |
| D2      | VSS_18        | Supply   |           | 1.8 V Ground   |
| E2      | VSS_33        | Supply   |           | 3.3 V Ground   |
| F2      | MONITOR2      | CMOS     | Output    | Monitor Output #2                                    |
| G2      | VSS_33        | Supply   |           | 3.3 V Ground   |
| H2      | MBSINOUT_1    | Analog   | I/O       | For Test Only – Do not connect                       |
| A3      | TR2           | CMOS     | Input     | Connect to VSS_18                                    |
| B3      | TR1           | CMOS     | Input     | Connect to VSS_18                                    |
| C3      | TRIGGER0      | CMOS     | Input     | Trigger Input #0                                     |
| G3      | VDD_33        | Supply   |           | 3.3 V Supply   |
| H3      | MBSINOUT_2    | Analog   | I/O       | For Test Only – Do not connect                       |
| A4      | SS_N          | CMOS     | Input     | SPI Slave Select (Active Low)                        |
| B4      | SCK           | CMOS     | Input     | SPI Clock  |
| C4      | RESET_N       | CMOS     | Input     | Sensor Reset (Active Low)                            |
| G4      | MISO          | CMOS     | Output    | SPI Master In – Slave Out                            |
| H4      | CP_SEL_SAMPLE | Analog   | Output    | For Test Only – Do not connect                       |
| A5      | FRAME_VALID   | CMOS     | Output    | Frame Valid Output                                   |
| B5      | LINE_VALID    | CMOS     | Output    | Line Valid Output                                    |
| C5      | DOUT9         | CMOS     | Output    | Data Output #9                                       |
| G5      | MOSI          | CMOS     | Input     | SPI Master Out – Slave In                            |
| H5      | TEST_ENABLE   | CMOS     | Input     | For Test Only – Connect to VSS_18                    |
| A6      | VSS_COLPC     | Supply   |           | Pixel Array Ground                                   |
| B6      | VDD_PIX       | Supply   |           | Pixel Array Supply                                   |
| C6      | DOUT8         | CMOS     | Output    | Data Output #8                                       |
| G6      | VSS_18        | Supply   |           | 1.8 V Ground   |
| H6      | VREF_BOTPLATE | Supply   | Input     | 1.8 V Supply for Sample and Hold                     |
| A7      | DOUT7         | CMOS     | Output    | Data Output #7                                       |
| B7      | DOUT6         | CMOS     | Output    | Data Output #6                                       |

## PYTHON 480

**Table 26. PIN LIST** (continued)

| Pin Map | Pin Name       | I/O Type | Direction | Description                         |
|---------|----------------|----------|-----------|-------------------------------------|
| C7      | DOUT5          | CMOS     | Output    | Data Output #5                      |
| G7      | VSS_18         | Supply   |           | 1.8 V Ground                        |
| H7      | VSS_33         | Supply   |           | 3.3 V Ground                        |
| A8      | CLK_OUT        | CMOS     | Output    | Clock Output                        |
| B8      | DOUT4          | CMOS     | Output    | Data Output #4                      |
| C8      | DOUT3          | CMOS     | Output    | Data Output #3                      |
| G8      | VSS_18         | Supply   |           | 1.8 V Ground                        |
| H8      | VSS_33         | Supply   |           | 3.3 V Ground                        |
| A9      | DOUT2          | CMOS     | Output    | Data Output #2                      |
| B9      | DOUT0          | CMOS     | Output    | Data Output #0                      |
| C9      | DOUT1          | CMOS     | Output    | Data Output #1                      |
| G9      | CLK_PLL        | CMOS     | Input     | Reference Clock Input for PLL       |
| H9      | VDD_18         | Supply   |           | 1.8 V Supply                        |
| A10     | VDD_18         | Supply   |           | 1.8 V Supply                        |
| B10     | VDD_PIX        | Supply   |           | Pixel Array Supply                  |
| C10     | CLOCK_OUTN     | LVDS     | Output    | LVDS Clock Output (Negative)        |
| D10     | DOUTN          | LVDS     | Output    | LVDS Data Output (Negative)         |
| E10     | SYNCN          | LVDS     | Output    | LVDS Sync Channel Output (Negative) |
| F10     | LVDS_CLOCK_INN | LVDS     | Input     | LVDS Clock Input (Negative)         |
| G10     | LOCK_DETECT    | CMOS     | Output    | Lock Detect Output                  |
| H10     | VDD_33         | Supply   |           | 3.3 V Supply                        |
| A11     | VSS_COLPC      | Supply   |           | Pixel Array Ground                  |
| B11     | CLOCK_OUTP     | LVDS     | Output    | LVDS Clock Output (Positive)        |
| C11     | DOUTP          | LVDS     | Output    | LVDS Data Output (Positive)         |
| D11     | SYNCP          | LVDS     | Output    | LVDS Sync Channel Output (Positive) |
| E11     | LVDS_CLOCK_INP | LVDS     | Input     | LVDS Clock Input (Positive)         |
| F11     | VDD_33         | Supply   |           | 3.3 V Supply                        |
| G11     | VSS_18         | Supply   |           | 1.8 V Ground                        |
| H11     | VDD_33         | Supply   |           | 3.3 V Supply                        |

# PYTHON 480

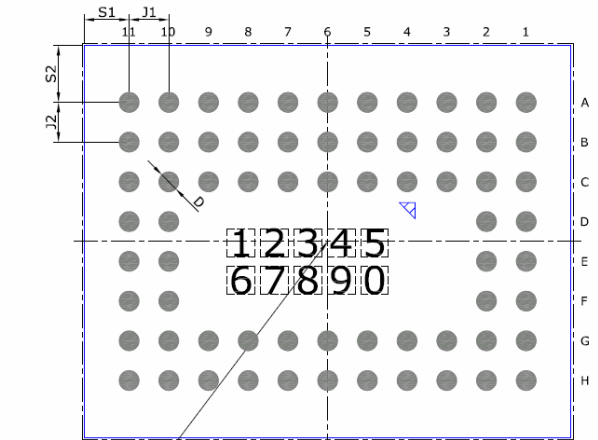
## Mechanical Specifications

| Mechanical Specifications   |   | Symbol | Min   | Typ   | Max   | Units |
|---|---|--------|-------|-------|-------|-------|
| Package Body Dimensions (Top View, Bumps down, with Pin A1 top left corner) | Package Body Dimension X                              | A      | 6105  | 6130  | 6155  | μm    |
|   | Package Body Dimension Y                              | B      | 4905  | 4930  | 4955  | μm    |
|   | Package Height  | C      | 631.2 | 691.2 | 751.2 | μm    |
|   | Ball Height   | C1     | 100   | 130   | 160   | μm    |
|   | Package Body Thickness                                | C2     | 516.2 | 561.2 | 606.2 | μm    |
|   | Distance of Glass Surface to Wafer                    | C3     | 425   | 445   | 465   | μm    |
|   | Ball Diameter   | D      | 220   | 250   | 280   | μm    |
|   | Total Pin Count                                       | N      |       | 67    |       | μm    |
|   | Pin Count X-axis                                      | N1     |       | 11    |       | μm    |
|   | Pin Count Y-axis                                      | N2     |       | 8     |       | μm    |
|   | Pins Pitch X-axis                                     | J1     |       | 500   |       | μm    |
|   | Pins Pitch Y-axis                                     | J2     |       | 500   |       | μm    |
|   | Edge to Pin Center Distance along X                   | S1     | 535   | 565   | 595   | μm    |
|   | Edge to Pin Center Distance along Y                   | S2     | 685   | 715   | 745   | μm    |
|   | Optical center referenced from package center (X-dir) |        |       | 0     |       | μm    |
| Optical center referenced from package center (Y-dir)                       |   |        | -175  |       | μm    |       |
| Glass Lid   | Glass Thickness (Material: AF32ECO)                   |        | 390   | 400   | 410   | μm    |
| Mechanical shock  | JESD22-B104C; Condition G                             |        |       |       | 2000  | g     |
| Vibration   | JESD22-B103B; Condition 1                             |        |       |       | 2000  | Hz    |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

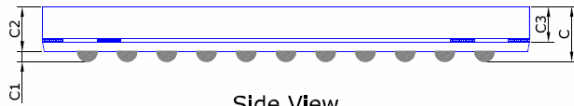


Top View (Bumps Down)



Center of BGA=  
Center of Package

Bottom View (Bumps Up)



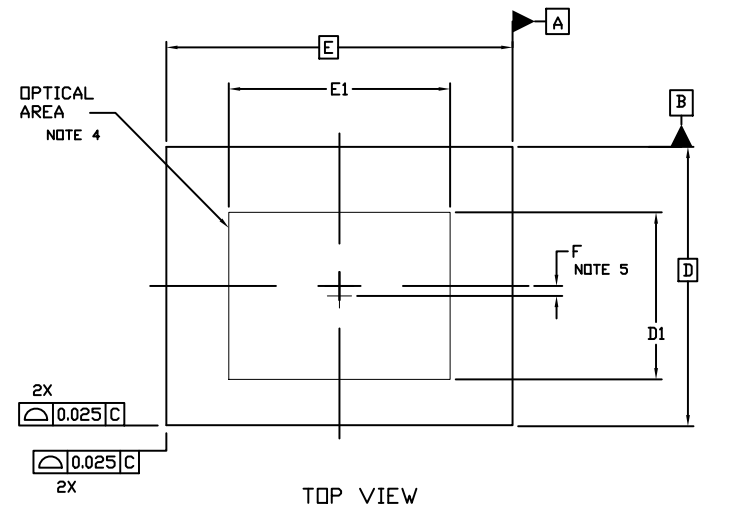
Side View

Bottom View (Bumps Up)  
 Package Size : 6130 × 4930 um  
 Mark code : (Dimension: 350 X 350um)  
 12345: Ecoded Mark ID to describe MPN  
 ( SN480 for NOIP1SN0480A;  
 SE480 for NOIP1SE0480A;  
 SP480 for NOIP1SP0408A;  
 SF480 for NOIP1SF0480A)  
 6: for year ( ex 2016=A, 2017=B)  
 7: Month (1~9, A, B, C)  
 890: serial no for wafer identification.  
 Tracking Code : XxYy Is varled.

Figure 43. Mechanical Diagram

# PYTHON 480

## Package Drawing



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE SOLDER BALLS.
4. MAXIMUM ROTATION OF OPTICAL AREA RELATIVE TO PACKAGE EDGES IS 0.1°.
5. DIMENSION F DEFINES THE OPTICAL CENTER.

| DIM | MILLIMETERS |      |
|-----|-------------|------|
|     | MIN.        | MAX. |
| A   | ---         | 0.75 |
| A1  | 0.10        | 0.16 |
| A2  | 0.56 REF    |      |
| b   | 0.22        | 0.28 |
| D   | 4.93 BSC    |      |
| D1  | 2.96 REF    |      |
| E   | 6.13 BSC    |      |
| E1  | 3.92 REF    |      |
| e   | 0.50 BSC    |      |
| F   | 0.175 REF   |      |

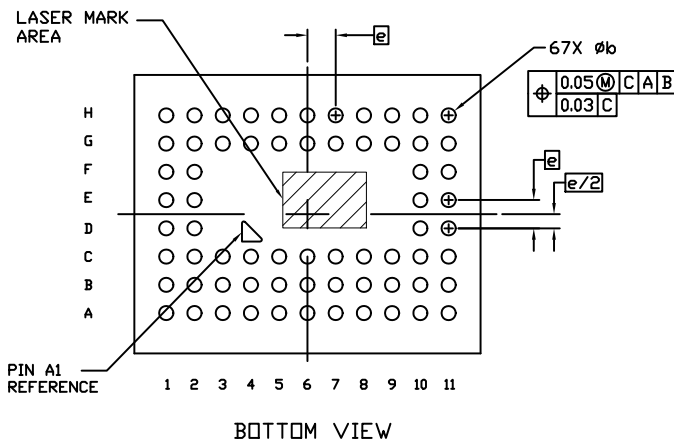
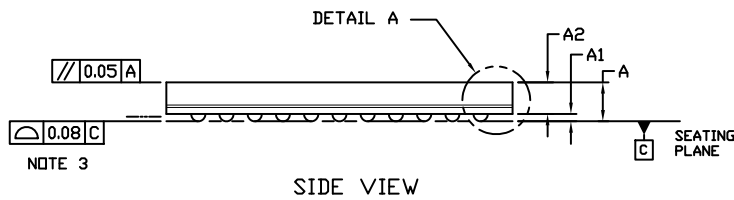


Figure 44. Package Drawing for the ODCSP67 Package



# PYTHON 480



Figure 46. Pin 1 Location



## PYTHON 480

### Glass Lid

The PYTHON 480 image sensors use a glass lid without any coatings. Figure 44 shows the transmission characteristics of the glass lid.

As shown in Figure 42, no infrared attenuating color filter glass is used. Use of an IR cut filter is recommended in the

optical path when color devices are used. (source: <http://www.pgo-online.com>).



Figure 47. Transmission Characteristics of the Glass Lid

### Protective Foil

The sensor is delivered with protective foil that is intended to be removed after assembly. The dimensions of the foil are

as illustrated in Figure 48 with tab aligned left center with Pin A1 to the bottom left.



Figure 48. Dimensions of the Protective Foil

# PYTHON 480

## SPECIFICATIONS AND USEFUL REFERENCES

The following references are available to customers under NDA at the ON Semiconductor Image Sensor Portal: <https://www.onsemi.com/PowerSolutions/myon/erCispFolder.do>

- Product Acceptance Criteria
- Product Qualification Report
- PYTHON Developer's Guide AND9362/D

### Useful References

For information on ESD and cover glass care and cleanliness, please download the *Image Sensor Handling and Best Practices* Application Note (AN52561/D) from [www.onsemi.com](http://www.onsemi.com).


For quality and reliability information, please download the *Quality & Reliability Handbook* (HBD851/D) from [www.onsemi.com](http://www.onsemi.com).

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For information on acronyms and a glossary of terms used, please download *Image Sensor Terminology* (TND6116/D) from [www.onsemi.com](http://www.onsemi.com).

### Return Material Authorization (RMA)

Refer to the ON Semiconductor RMA policy procedure at [http://www.onsemi.com/site/pdf/CAT\\_Returns\\_FailureAnalysis.pdf](http://www.onsemi.com/site/pdf/CAT_Returns_FailureAnalysis.pdf)

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