ISL6622

VR11.1 Compatible Synchronous Rectified Buck MOSFET Drivers

FN6470
Rev 2.00
October 30, 2008

The ISL6622 is a high frequency MOSFET driver designed to drive upper and lower power N-Channel MOSFETs in a synchronous rectified buck converter topology. The advanced PWM protocol of ISL6622 is specifically designed to work with Intersil VR11.1 controllers and combined with N-Channel MOSFETs, form a complete core-voltage regulator solution for advanced microprocessors. When ISL6622 detects a $\overline{PSI}$ protocol sent by an Intersil VR11.1 controller, it activates Diode Emulation (DE) and Gate Voltage Optimization Technology (GVOT) operation; otherwise, it operates in normal Continuous Conduction Mode (CCM) PWM mode.

In the 8 Ld SOIC package, the ISL6622 drives the upper and lower gates to VCC during normal PWM mode, while the lower gate drops down to a fixed 5.75V (typically) during $\overline{PSI}$ mode. The 10 Ld DFN part offers more flexibility: the upper gate can be driven from 5V to 12V via the UVCC pin, while the lower gate has a resistor-selectable drive voltage of 5.75V, 6.75V, and 7.75V (typically) during $\overline{PSI}$ mode. This provides the flexibility necessary to optimize applications involving trade-offs between gate charge and conduction losses.

To further enhance light load efficiency, the ISL6622 enables diode emulation operation during $\overline{PSI}$ mode. This allows Discontinuous Conduction Mode (DCM) by detecting when the inductor current reaches zero and subsequently turning off the low side MOSFET to prevent it from sinking current.

An advanced adaptive shoot-through protection is integrated to prevent both the upper and lower MOSFETs from conducting simultaneously and to minimize dead time. The ISL6622 has a 20kΩ integrated high-side gate-to-source resistor to prevent self turn-on due to high input bus dV/dt. This driver also has an overvoltage protection feature operational while VCC is below the POR threshold: the PHASE node is connected to the gate of the low side MOSFET (LGATE) via a 10kΩ resistor, limiting the output voltage of the converter close to the gate threshold of the low side MOSFET, dependent on the current being shunted, which provides some protection to the load should the upper MOSFET(s) become shorted.

Features

- Dual MOSFET Drives for Synchronous Rectified Bridge
- Advanced Adaptive Zero Shoot-through Protection
- Integrated LDO for Selectable Lower Gate Drive Voltage (5.75V, 6.75V, 7.75V) to Optimize Light Load Efficiency
- 36V Internal Bootstrap Diode
- Advanced PWM Protocol (Patent Pending) to Support $\overline{PSI}$ Mode, Diode Emulation, Three-State Operation
- Diode Emulation for Enhanced Light Load Efficiency
- Bootstrap Capacitor Overcharging Prevention
- Supports High Switching Frequency
  - 3A Sinking Current Capability
  - Fast Rise/Fall Times and Low Propagation Delays
- Integrated High-Side Gate-to-Source Resistor to Prevent from Self Turn-On due to High Input Bus dV/dt
- Pre-POR Overvoltage Protection for Start-up and Shutdown
- Power Rails Undervoltage Protection
- Expandable Bottom Copper Pad for Enhanced Heat Sinking
- Dual Flat No-Lead (DFN) Package
  - Near Chip-Scale Package Footprint; Improves PCB Efficiency and Thinner in Profile
- Pb-Free (RoHS Compliant)

Applications

- High Light Load Efficiency Voltage Regulators
- Core Regulators for Advanced Microprocessors
- High Current DC/DC Converters
- High Frequency and High Efficiency VRM and VRD

Related Literature

- Technical Brief TB363 “Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)”
- Technical Brief TB417 “Designing Stable Compensation Networks for Single Phase Voltage Mode Buck Regulators” for Power Train Design, Layout Guidelines, and Feedback Compensation Design

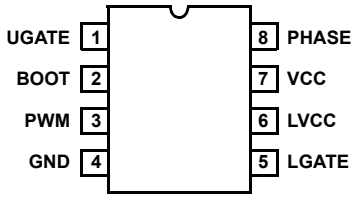
Ordering Information

PART NUMBER (Note)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL6622CBZ*	6622 CBZ	0 to +70	8 Ld SOIC	M8.15
ISL6622CRZ*	622Z	0 to +70	10 Ld 3x3 DFN	L10.3x3
ISL6622IBZ*	6622IBZ	-40 to +85	8 Ld SOIC	M8.15
ISL6622IRZ*	622I	-40 to +85	10 Ld 3x3 DFN	L10.3x3

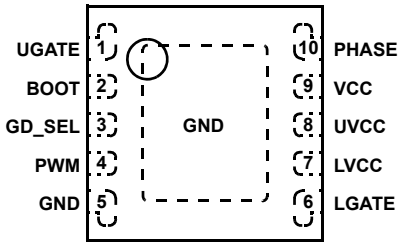
*Add “-T” suffix for tape and reel. Please refer to TB347 for details on reel specifications.
NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020..

Pinouts

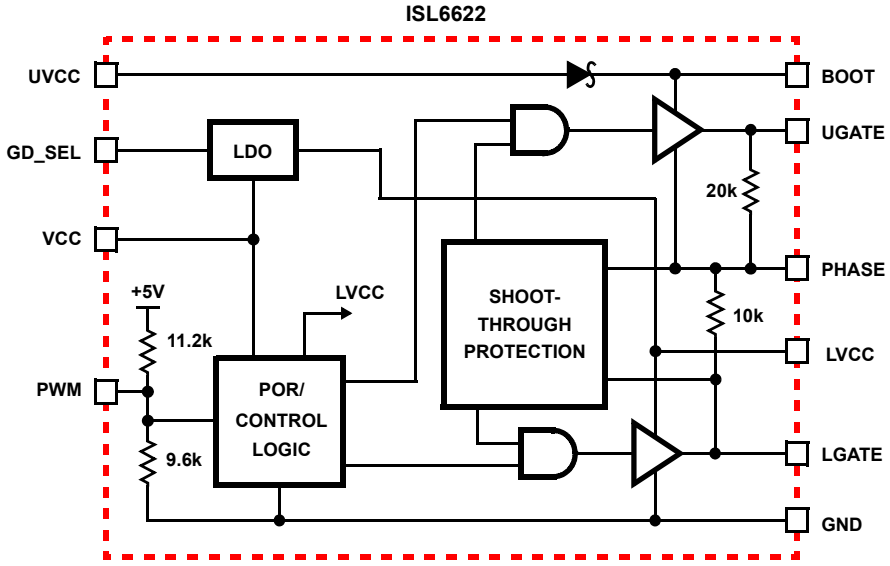
ISL6622
(8 LD SOIC)
TOP VIEW



ISL6622
(10 LD 3x3 DFN)
TOP VIEW

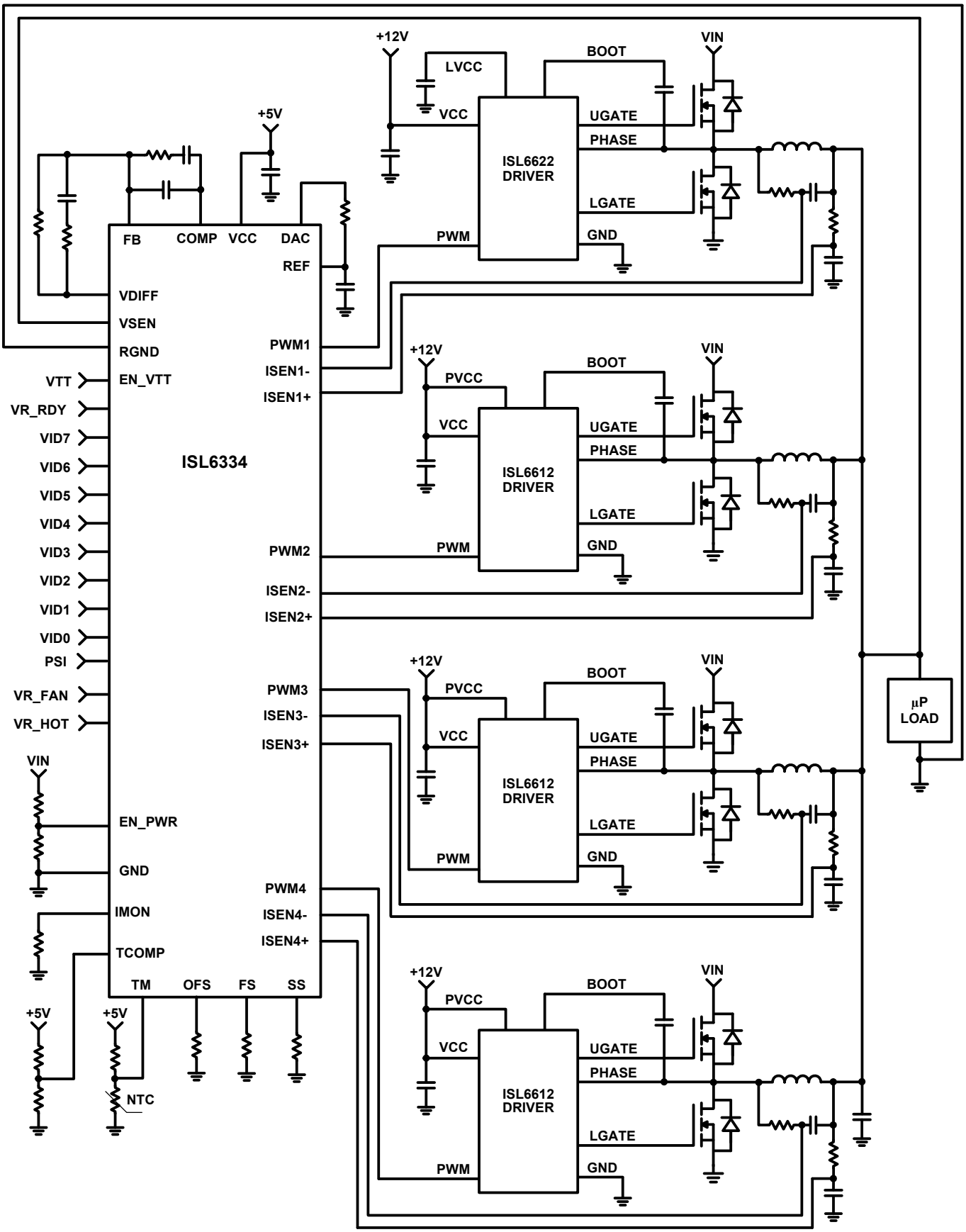


Block Diagrams



UVCC = VCC FOR SOIC
LVCC = 5.75V (TYPICALLY) @ 50mA FOR SOIC

Typical Application Circuit



Absolute Maximum Ratings

Supply Voltage (VCC, UVCC) 15V
BOOT Voltage ($V_{BOOT-GND}$) 36V
Input Voltage (V_{PWM}) . . . . . GND - 0.3V to 7V
UGATE . . . . . V_{PHASE} - 0.3V_{DC} to V_{BOOT} + 0.3V
V_{PHASE} - 3.5V (<100ns Pulse Width, 2µJ) to V_{BOOT} + 0.3V
LGATE . . . . . .GND - 0.3V_{DC} to V_{LVCC} + 0.3V
GND - 5V (<100ns Pulse Width, 2µJ) to V_{LVCC} + 0.3V
PHASE . . . . . GND - 0.3V_{DC} to 15V_{DC}
GND - 8V (<200ns, 10µJ) to 30V (<200ns, $V_{BOOT-GND}$<36V)

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
SOIC Package (Note 1)	100	N/A
DFN Package (Notes 2, 3)	48	7

Maximum Junction Temperature (Plastic Package) . . . . . .+150°C
Maximum Storage Temperature Range . . . . . .-65°C to +150°C
Pb-free Reflow Profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

Ambient Temperature Range
ISL6622IBZ, ISL6622IRZ . . . . . .-40°C to +85°C
ISL6622CBZ, ISL6622CRZ . . . . . 0°C to +70°C
Maximum Operating Junction Temperature . . . . . +125°C
Supply Voltage
VCC . . . . . 6.8V to 13.2V
UVCC . . . . . .4.75V to 13.2V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
2. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
3. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.
4. Limits should be considered typical and are not production tested.

Electrical Specifications

Recommended Operating Conditions. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VCC SUPPLY CURRENT (Note 4)						
No Load Switching Supply Current	I_{VCC}	ISL6622CBZ and ISL6622IBZ, f_{PWM} = 300kHz, V_{VCC} = 12V	-	8.2	-	mA
	I_{VCC}	ISL6622CRZ and ISL6622IRZ, f_{PWM} = 300kHz, V_{VCC} = 12V	-	6.2	-	mA
	I_{UVCC}		-	2.0	-	mA
Standby Supply Current	I_{VCC}	ISL6622CBZ and ISL6622IBZ, PWM Transition from 0V to 2.5V	-	5.7	-	mA
	I_{VCC}	ISL6622CRZ and ISL6622IRZ, PWM Transition from 0V to 2.5V	-	5	-	mA
	I_{UVCC}		-	0.7	-	mA
POWER-ON RESET						
VCC Rising Threshold			6.25	6.45	6.70	V
VCC Falling Threshold			4.8	5.0	5.25	V
LVCC Rising Threshold (Note 4)			-	4.4	-	V
LVCC Falling Threshold (Note 4)			-	3.4	-	V
PWM INPUT (See “TIMING DIAGRAM” on page 6)						
Input Current (Note 4)	I_{PWM}	V_{PWM} = 5V	-	500	-	µA
		V_{PWM} = 0V	-	-430	-	µA
PWM Rising Threshold (Note 4)		VCC = 12V	-	3.4	-	V
PWM Falling Threshold (Note 4)		VCC = 12V	-	1.6	-	V
Three-State Lower Gate Falling Threshold (Note 4)		VCC = 12V	-	1.6	-	V
Three-State Lower Gate Rising Threshold (Note 4)		VCC = 12V	-	1.1	-	V
Three-State Upper Gate Rising Threshold (Note 4)		VCC = 12V	-	3.2	-	V

Electrical Specifications Recommended Operating Conditions. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Three-State Upper Gate Falling Threshold (Note 4)		VCC = 12V	-	2.8	-	V
UGATE Rise Time (Note 4)	t_{RU}	V_{VCC} = 12V, 3nF Load, 10% to 90%	-	26	-	ns
LGATE Rise Time (Note 4)	t_{RL}	V_{VCC} = 12V, 3nF Load, 10% to 90%	-	18	-	ns
UGATE Fall Time (Note 4)	t_{FU}	V_{VCC} = 12V, 3nF Load, 90% to 10%	-	18	-	ns
LGATE Fall Time (Note 4)	t_{FL}	V_{VCC} = 12V, 3nF Load, 90% to 10%	-	12	-	ns
UGATE Turn-On Propagation Delay (Note 4)	t_{PDHU}	V_{VCC} = 12V, 3nF Load, Adaptive	-	20	-	ns
LGATE Turn-On Propagation Delay (Note 4)	t_{PDHL}	V_{VCC} = 12V, 3nF Load, Adaptive	-	10	-	ns
UGATE Turn-Off Propagation Delay (Note 4)	t_{PDLU}	V_{VCC} = 12V, 3nF Load	-	10	-	ns
LGATE Turn-Off Propagation Delay (Note 4)	t_{PDLL}	V_{VCC} = 12V, 3nF Load	-	10	-	ns
Diode Braking Holdoff Time (Note 4)	$t_{UG_OFF_DB}$	V_{VCC} = 12V	-	60	-	ns
Minimum LGATE ON-Time At Diode Emulation	$t_{LG_ON_DM}$	V_{VCC} = 12V	230	330	450	ns
OUTPUT (Note 4)						
Upper Drive Source Current	I_{U_SOURCE}	V_{VCC} = 12V, 3nF Load	-	1.25	-	A
Upper Drive Source Impedance	R_{U_SOURCE}	20mA Source Current	-	2.0	-	Ω
Upper Drive Sink Current	I_{U_SINK}	V_{VCC} = 12V, 3nF Load	-	2	-	A
Upper Drive Sink Impedance	R_{U_SINK}	20mA Sink Current	-	1.35	-	Ω
Lower Drive Source Current	I_{L_SOURCE}	V_{VCC} = 12V, 3nF Load	-	2	-	A
Lower Drive Source Impedance	R_{L_SOURCE}	20mA Source Current	-	1.35	-	Ω
Lower Drive Sink Current	I_{L_SINK}	V_{VCC} = 12V, 3nF Load	-	3	-	A
Lower Drive Sink Impedance	R_{L_SINK}	20mA Sink Current	-	0.90	-	Ω

Functional Pin Description

PACKAGE PIN #		PIN SYMBOL	FUNCTION
SOIC	DFN		
1	1	UGATE	Upper gate drive output. Connect to gate of high-side power N-Channel MOSFET.
2	2	BOOT	Floating bootstrap supply pin for the upper gate drive. Connect the bootstrap capacitor between this pin and the PHASE pin. The bootstrap capacitor provides the charge to turn on the upper MOSFET. See “Internal Bootstrap Device” on page 8 for guidance in choosing the capacitor value.
-	3	GD_SEL	This pin sets the LG drive voltage in PSI mode.
3	4	PWM	The PWM signal is the control input for the driver. The PWM signal can enter three distinct states during operation, see the three-state PWM Input section on page 6 for further details. Connect this pin to the PWM output of the controller.
4	5	GND	Bias and reference ground. All signals are referenced to this node. It is also the power ground return of the driver.
5	6	LGATE	Lower gate drive output. Connect to gate of the low-side power N-Channel MOSFET.
6	7	LVCC	This pin provides power for the LGATE drive. Place a high quality low ESR ceramic capacitor from this pin to GND.
-	8	UVCC	This pin provides power to the upper gate drive. Its operating range is +5V to 12V. Place a high quality low ESR ceramic capacitor from this pin to GND.
7	9	VCC	Connect this pin to 12V bias supply. This pin supplies power to the upper gate in the SOIC and to the LDO for the lower gate drive. Place a high quality low ESR ceramic capacitor from this pin to GND.
8	10	PHASE	Connect this pin to the SOURCE of the upper MOSFET and the DRAIN of the lower MOSFET. This pin provides a return path for the upper gate drive.
-	11	PAD	Connect this pad to the power ground plane (GND) via thermally enhanced connection.

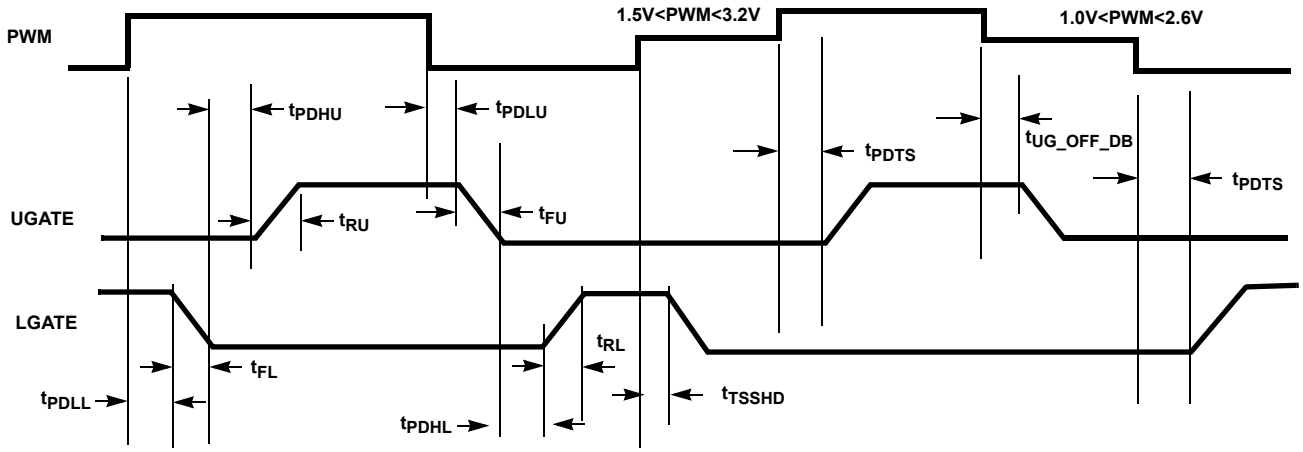


FIGURE 1. TIMING DIAGRAM

Description

Operation and Adaptive Shoot-through Protection

Designed for high speed switching, the ISL6622 MOSFET driver controls both high-side and low-side N-Channel FETs from one externally provided PWM signal.

A rising transition on PWM initiates the turn-off of the lower MOSFET (see Figure 1). After a short propagation delay [t_{PDLL}], the lower gate begins to fall. Typical fall time [t_{FL}] is provided in the “Electrical Specifications” on page 4. Following a 25ns blanking period, adaptive shoot-through circuitry monitors the LGATE voltage and turns on the upper gate following a short delay time [t_{PDHU}] after the LGATE voltage drops below ~1.75V. The upper gate drive then begins to rise [t_{RU}] and the upper MOSFET turns on.

A falling transition on PWM indicates the turn-off of the upper MOSFET and the turn-on of the lower MOSFET. A short propagation delay [t_{PDLU}] is encountered before the upper gate begins to fall [t_{FU}]. The adaptive shoot-through circuitry monitors the UGATE-PHASE voltage and turns on the lower MOSFET a short delay time [t_{PDHL}] after the upper MOSFET’s PHASE voltage drops below +0.8V or 40ns after the upper MOSFET’s gate voltage [UGATE-PHASE] drops below ~1.75V. The lower gate then rises [t_{RL}], turning on the lower MOSFET. These methods prevent both the lower and upper MOSFETs from conducting simultaneously (shoot-through), while adapting the dead time to the gate charge characteristics of the MOSFETs being used.

This driver is optimized for voltage regulators with large step down ratio. The lower MOSFET is usually sized larger compared to the upper MOSFET because the lower MOSFET conducts for a longer time during a switching period. The lower gate driver is therefore sized much larger to meet this application requirement. The 0.8Ω ON-resistance and 3A sink current capability enable the lower gate driver to absorb the current injected into the lower gate through the drain-to-gate capacitor of the lower MOSFET and help prevent shoot-through caused by the self turn-on of the lower MOSFET due to high dV/dt of the switching node.

Advanced PWM Protocol (Patent Pending)

The advanced PWM protocol of ISL6622 is specifically designed to work with Intersil VR11.1 controllers. When ISL6622 detects a $\overline{\text{PSI}}$ protocol sent by an Intersil VR11.1 controller, it turns on diode emulation and GVOT (described in next sections) operation; otherwise, it remains in normal CCM PWM mode.

Another unique feature of ISL6622 and other Intersil drivers is the addition of a three-state shutdown window to the PWM input. If the PWM signal enters and remains within the shutdown window for a set holdoff time, the driver outputs are disabled and both MOSFET gates are pulled and held low. The shutdown state is removed when the PWM signal moves outside the shutdown window. Otherwise, the PWM rising and falling thresholds outlined in the “Electrical Specifications” on page 4 determine when the lower and upper gates are enabled. This feature helps prevent a negative transient on the output voltage when the output is shut down, eliminating the Schottky diode that is used in some systems for protecting the load from reversed output voltage events.

Note that the LGATE will not turn off until the diode emulation minimum ON-time of 350ns is expired for a PWM low to tri-level (2.5V) transition.

Diode Emulation

Diode emulation allows for higher converter efficiency under light-load situations. With diode emulation active, the ISL6622 detects the zero current crossing of the output inductor and turns off LGATE. This prevents the low side MOSFET from sinking current and ensures that discontinuous conduction mode (DCM) is achieved. The LGATE has a minimum ON-time of 350ns in DCM mode.

Gate Voltage Optimization Technology (GVOT)

The ISL6622 provides the user flexibility in choosing the gate drive voltage for efficiency optimization. During light load operation, the switching losses dominate system performance. Dropping down to a lower drive voltage with GVOT during light

load operation can reduce the switching losses and maximize system efficiency.

Figure 2 shows that the gate drive voltage optimization is accomplished via an internal low drop out regulator (LDO) that regulates the lower gate drive voltage. LVCC is driven to a lower voltage depending on the state of the internal $\overline{PSI}$ signal and the GD_SEL pin impedance. The input and output of this internal regulator is the VCC and LVCC pins, respectively. Both VCC and LVCC should be decoupled with a high quality low ESR ceramic capacitor.

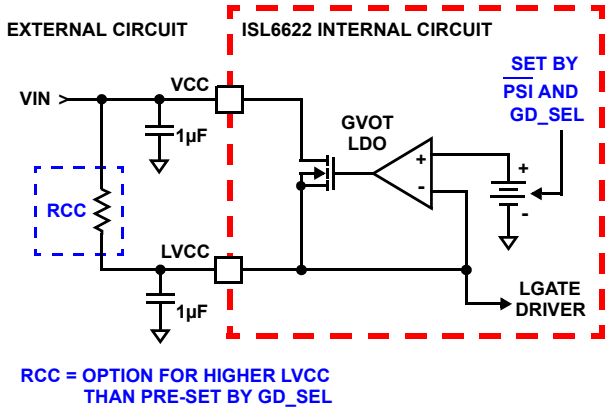


FIGURE 2. GATE VOLTAGE OPTIMIZATION (GVOT) DETAIL

In the 8 Ld SOIC package, the ISL6622 drives the upper and lower gates close to VCC during normal PWM mode, while the lower gate drops down to a fixed 5.75V during $\overline{PSI}$ mode. The 10 Ld DFN part offers more flexibility: the upper gate can be driven from 5V to 12V via the UVCC pin, while the lower gate has a resistor-selectable drive voltage of 5.75V, 6.75V, and 7.75V during $\overline{PSI}$ mode. This provides the flexibility necessary to optimize applications involving trade-offs between gate charge and conduction losses. Table 1 shows the LDO output (LVCC) level set by the PWM input and GD_SEL pin impedance.

TABLE 1. LDO OPERATION AND OPTIONS

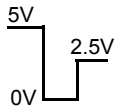
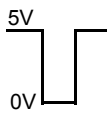
PWM INPUT	GD_SEL PIN	LVCC @ 50mA DC LOAD
	Floating	5.75V (Typical; Fixed in SOIC Package)
	4.5kΩ to GND	6.75V (Typical)
	GND	7.75V (Typical)
	DON'T CARE	11.20V (Typical)

Figure 3 illustrates the internal LDO's variation with the average load current plotted over a range of temperatures spanning from -40°C to +120°C. Should finer tweaking of this LVCC voltage be necessary, a resistor (R_{CC}) can be used to shunt the LDO, as shown in Figure 2. The resistor delivers part of the LGATE drive current, leaving less current going through the internal LDO, elevating the LDO's output voltage. Further reduction in RCC's value can raise the LVCC voltage further, as desired.

Figure 4 also details the typical LDO performance when the pass element is fully enhanced, as it is the case when the driver operates in CCM.

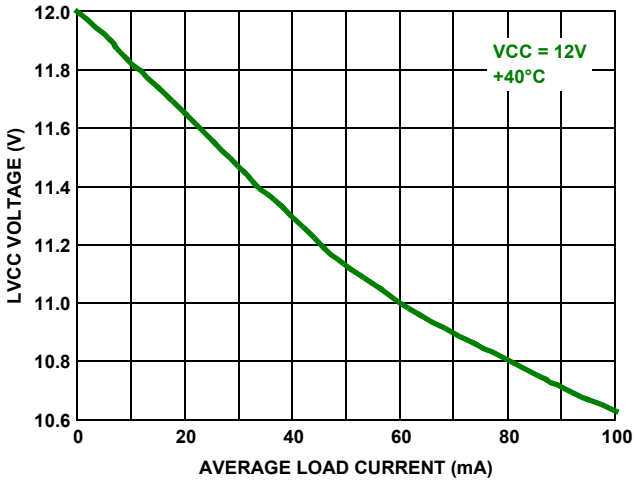


FIGURE 3. TYPICAL LVCC VARIATION WITH LOAD (CCM)

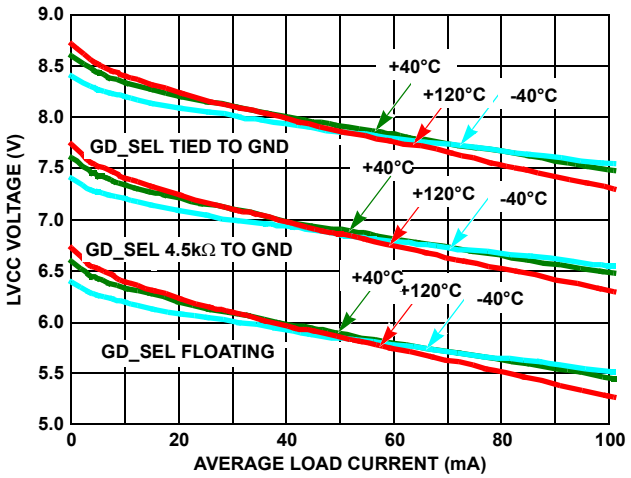


FIGURE 4. TYPICAL LVCC VARIATION WITH LOAD (DEM)

Power-On Reset (POR) Function

During initial start-up, the VCC voltage rise is monitored. Once the rising VCC voltage exceeds rising POR threshold, operation of the driver is enabled and the PWM input signal takes control of the gate drives. If VCC drops below the POR falling threshold, operation of the driver is disabled.

Pre-POR Overvoltage Protection

While VCC is below its POR level, the upper gate is held low and LGATE is connected to the PHASE pin via an internal 10kΩ (typically) resistor. By connecting the PHASE node to the gate of the low side MOSFET, the driver offers some passive protection to the load if the upper MOSFET(s) is or becomes shorted. If the PHASE node goes higher than the

gate threshold of the lower MOSFET, it results in the progressive turn-on of the device and the effective clamping of the PHASE node's rise. The actual PHASE node clamping level depends on the lower MOSFET's electrical characteristics, as well as the characteristics of the input supply and the path connecting it to the respective PHASE node.

Internal Bootstrap Device

The ISL6622 features an internal bootstrap Schottky diode. Simply adding an external capacitor across the BOOT and PHASE pins completes the bootstrap circuit. The bootstrap function is also designed to prevent the bootstrap capacitor from overcharging due to the large negative swing at the trailing-edge of the PHASE node. This reduces the voltage stress on the BOOT to PHASE pins.

The bootstrap capacitor must have a maximum voltage rating well above the maximum voltage intended for UVCC. Its minimum capacitance value can be estimated from Equation 1:

$$C_{BOOT_CAP} \geq \frac{Q_{UGATE}}{\Delta V_{BOOT_CAP}} \qquad \text{(EQ. 1)}$$

$$Q_{UGATE} = \frac{Q_{G1} \bullet UVCC}{V_{GS1}} \bullet N_{Q1}$$

where Q_{G1} is the amount of gate charge per upper MOSFET at V_{GS1} gate-source voltage and N_{Q1} is the number of control MOSFETs. The ΔV_{BOOT_CAP} term is defined as the allowable droop in the rail of the upper gate drive. Select results are exemplified in Figure 5.

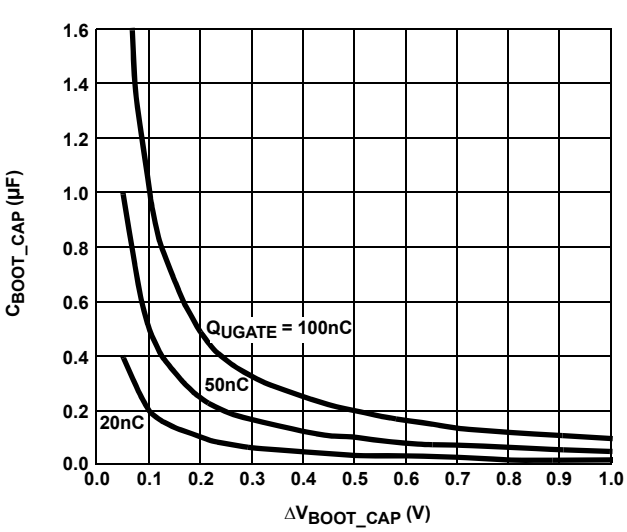


FIGURE 5. BOOTSTRAP CAPACITANCE vs BOOT RIPPLE VOLTAGE

Power Dissipation

Package power dissipation is mainly a function of the switching frequency (F_{SW}), the output drive impedance, the layout resistance, and the selected MOSFET's internal gate resistance and total gate charge (Q_G). Calculating the power dissipation in the driver for a desired application is critical to ensure safe operation. Exceeding the maximum allowable power dissipation level may push the IC beyond the maximum recommended operating junction temperature. The DFN package is more suitable for high frequency applications. See "Layout Considerations" on page 9 for thermal impedance improvement suggestions. The total gate drive power losses due to the gate charge of MOSFETs and the driver's internal circuitry and their corresponding average driver current can be estimated using Equations 2 and 3, respectively:

$$P_{Qg_TOT} = P_{Qg_Q1} + P_{Qg_Q2} + I_Q \bullet VCC \qquad \text{(EQ. 2)}$$

$$P_{Qg_Q1} = \frac{Q_{G1} \bullet UVCC^2}{V_{GS1}} \bullet F_{SW} \bullet N_{Q1}$$

$$P_{Qg_Q2} = \frac{Q_{G2} \bullet LVCC^2}{V_{GS2}} \bullet F_{SW} \bullet N_{Q2}$$

$$I_{DR} = \left(\frac{Q_{G1} \bullet UVCC \bullet N_{Q1}}{V_{GS1}} + \frac{Q_{G2} \bullet LVCC \bullet N_{Q2}}{V_{GS2}}\right) \bullet F_{SW} + I_Q \qquad \text{(EQ. 3)}$$

where the gate charge (Q_{G1} and Q_{G2}) is defined at a particular gate to source voltage (V_{GS1} and V_{GS2}) in the corresponding MOSFET datasheet; I_Q is the driver's total quiescent current with no load at both drive outputs; N_{Q1} and N_{Q2} are number of upper and lower MOSFETs, respectively; UVCC and LVCC are the drive voltages for both upper and lower FETs, respectively. The I_Q*VCC product is the quiescent power of the driver without a load.

The total gate drive power losses are dissipated among the resistive components along the transition path, as outlined in Equation 4. The drive resistance dissipates a portion of the total gate drive power losses, the rest will be dissipated by the external gate resistors (R_{G1} and R_{G2}) and the internal gate resistors (R_{GI1} and R_{GI2}) of MOSFETs. Figures 6 and 7 show the typical upper and lower gate drives turn-on current paths.

$$P_{DR} = P_{DR_UP} + P_{DR_LOW} + I_Q \bullet VCC \qquad \text{(EQ. 4)}$$

$$P_{DR_UP} = \left(\frac{R_{HI1}}{R_{HI1} + R_{EXT1}} + \frac{R_{LO1}}{R_{LO1} + R_{EXT1}}\right) \bullet \frac{P_{Qg_Q1}}{2}$$

$$P_{DR_LOW} = \left(\frac{R_{HI2}}{R_{HI2} + R_{EXT2}} + \frac{R_{LO2}}{R_{LO2} + R_{EXT2}}\right) \bullet \frac{P_{Qg_Q2}}{2}$$

$$R_{EXT1} = R_{G1} + \frac{R_{GI1}}{N_{Q1}} \qquad R_{EXT2} = R_{G2} + \frac{R_{GI2}}{N_{Q2}}$$

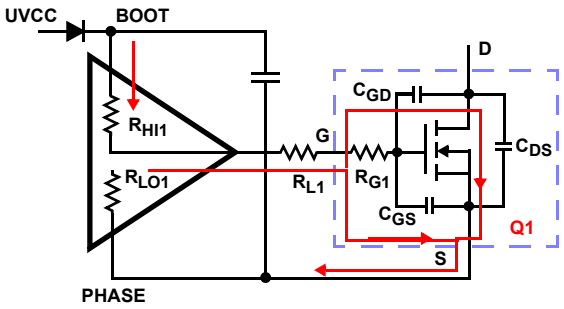


FIGURE 6. TYPICAL UPPER-GATE DRIVE TURN-ON PATH

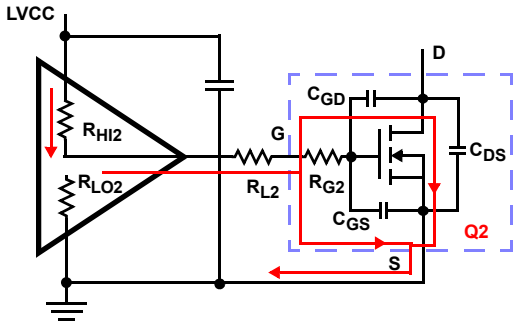


FIGURE 7. TYPICAL LOWER-GATE DRIVE TURN-ON PATH

Application Information

Layout Considerations

During switching of the devices, the parasitic inductances of the PCB and the power devices' packaging (both upper and lower MOSFETs) leads to ringing, possibly in excess of the absolute maximum rating of the devices. Careful layout can help minimize such unwanted stress. The following advice is meant to lead to an optimized layout:

- Keep decoupling loops (LVCC-GND and BOOT-PHASE) as short as possible.
- Minimize trace inductance, especially low-impedance lines: all power traces (UGATE, PHASE, LGATE, GND, LVCC) should be short and wide, as much as possible.
- Minimize the inductance of the PHASE node: ideally, the source of the upper and the drain of the lower MOSFET should be as close as thermally allowable.
- Minimize the input current loop: connect the source of the lower MOSFET to ground as close to the transistor pin as feasible; input capacitors (especially ceramic decoupling) should be placed as close to the drain of upper and source of lower MOSFETs as possible.

In addition, for improved heat dissipation, place copper underneath the IC whether it has an exposed pad or not. The copper area can be extended beyond the bottom area of the IC and/or connected to buried power ground plane(s) with thermal vias. This combination of vias for vertical heat escape, extended surface copper islands, and buried planes combine to allow the IC and the power switches to achieve their full thermal potential.

Upper MOSFET Self Turn-On Effect at Start-up

Should the driver have insufficient bias voltage applied, its outputs are floating. If the input bus is energized at a high dV/dt rate while the driver outputs are floating, due to self-coupling via the internal C_{GD} of the MOSFET, the gate of the upper MOSFET could momentarily rise up to a level greater than the threshold voltage of the device, potentially turning on the upper switch. Therefore, if such a situation could conceivably be encountered, it is a common practice to place a resistor (R_{UGPH}) across the gate and source of the upper MOSFET to suppress the Miller coupling effect. The value of the resistor depends mainly on the input voltage's rate of rise, the C_{GD}/C_{GS} ratio, as well as the gate-source threshold of the upper MOSFET. A higher dV/dt, a lower C_{DS}/C_{GS} ratio, and a lower gate-source threshold upper FET will require a smaller resistor to diminish the effect of the internal capacitive coupling. For most applications, the integrated 20kΩ resistor is sufficient, not affecting normal performance and efficiency.

$$V_{GS_MILLER} = \frac{dV}{dt} \cdot R \cdot C_{rss}\left(1 - e^{\frac{-V_{DS}}{\frac{dV}{dt} \cdot R \cdot C_{iss}}}\right) \qquad \text{(EQ. 5)}$$

$$R = R_{UGPH} + R_{GI} \qquad C_{rss} = C_{GD} \qquad C_{iss} = C_{GD} + C_{GS}$$

The coupling effect can be roughly estimated with Equation 5, which assumes a fixed linear input ramp and neglects the clamping effect of the body diode of the upper drive and the bootstrap capacitor. Other parasitic components such as lead inductances and PCB capacitances are also not taken into account. Figure 8 provides a visual reference for this phenomenon and its potential solution.

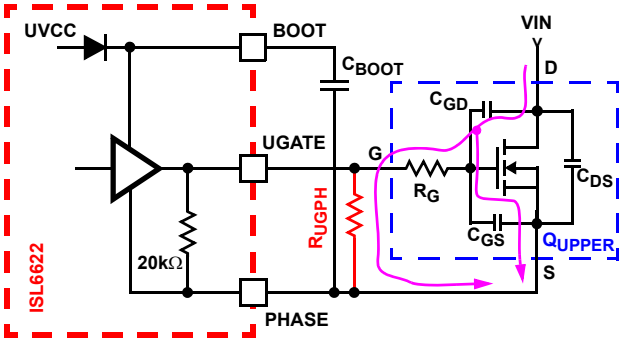


FIGURE 8. GATE TO SOURCE RESISTOR TO REDUCE UPPER MOSFET MILLER COUPLING

Gate Drive Voltage Options

Intersil provides various gate drive voltage options in the ISL6622 product family, as shown in Table 2.

The ISL6622 can drop the low-side MOSFET's gate drive voltage when operating in DEM, while the high-side FET's gate drive voltage of the DFN package can be connected to VCC or LVCC.

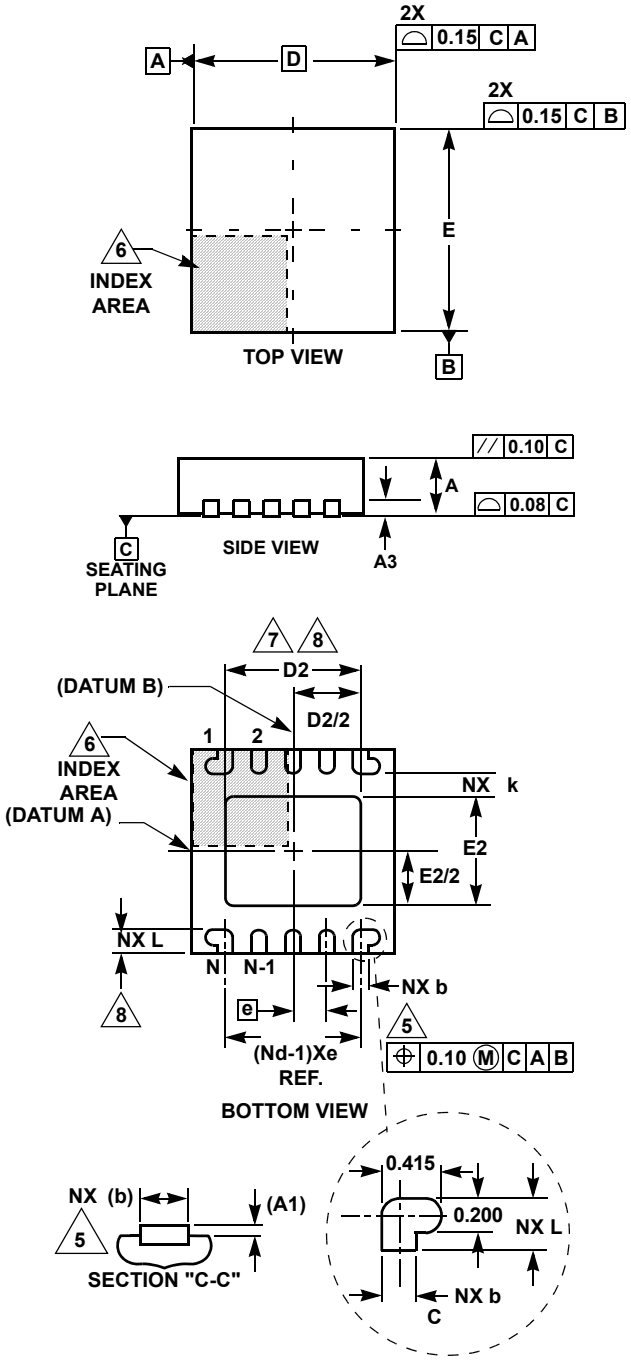
The ISL6622A allows the low-side MOSFET(s) to operate from an externally-provided rail as low as 5V, eliminating the LDO losses, while the high-side MOSFET's gate drive voltage of the DFN package can be connected to VCC or LVCC.

The ISL6622B sets the low-side MOSFET's gate drive voltage at a fixed, programmable LDO level, while the high-side FETs' gate drive voltage of the DFN package can be connected to VCC or LVCC.

TABLE 2. ISL6622 FAMILY BIAS OPTIONS

POWER RAILS		LVCC		UVCC	VCC
		$\overline{PSI}$ = LOW	$\overline{PSI}$ = HIGH		
ISL6622	SOIC	5.75V	11.2V	VCC	Operating Voltage Ranges from 6.8V to 13.2V
	DFN	Programmable	11.2V	Own Rail	
ISL6622A	SOIC	Own Rail		VCC	
	DFN	Own Rail		Own Rail	
ISL6622B	SOIC	5.75V		VCC	
	DFN	Programmable		Own Rail	

Dual Flat No-Lead Plastic Package (DFN)



L10.3x3

10 LEAD DUAL FLAT NO-LEAD PLASTIC PACKAGE

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A3		0.20 REF		-
b	0.18	0.23	0.28	5,8
D		3.00 BSC		-
D2	1.95	2.00	2.05	7,8
E		3.00 BSC		-
E2	1.55	1.60	1.65	7,8
e		0.50 BSC		-
k	0.25	-	-	-
L	0.30	0.35	0.40	8
N		10		2
Nd		5		3

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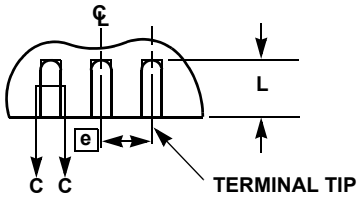
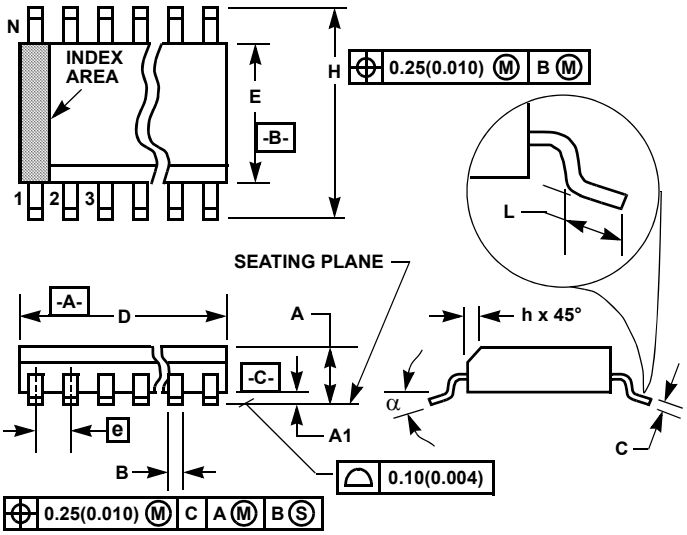
NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd refers to the number of terminals on D.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.



FOR ODD TERMINAL/SIDE

Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M8.15 (JEDEC MS-012-AA ISSUE C)
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.1890	0.1968	4.80	5.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
α	0°	8°	0°	8°	-

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