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# LC749402PT

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CMOS IC

## Silicon gate LCD Picture Quality Improvement IC

### Overview

LC749402PT is a picture quality improvement IC that processes the output signals to the LCD panel for high picture quality display. This IC performs various picture quality adjustments to provide the ideal correction for the display panel.

It can support up to WVGA/SVGA panels. \*

### Features

(1) Digital input/output

- Digital YCbCr/YPbPr 24bit (4:4:4) or 16bit (4:2:2) or 8bit (ITU-R BT.656) signal input
- Digital RGB 24bit signal input
- Digital RGB 18bit/24bit signal output
- Digital YCbCr 16bit (4:2:2)/24bit (4:4:4) signal output

(2) Image quality correction

- Y image quality correction: luminance adjustment, contour correction, CDEX (Color Depth Expander), dynamic- $\gamma$ , black/white stretch
- C image quality correction: color exciter, flesh tone correction, hue, color gain
- RGB image quality correction: brightness, contrast, white balance, black balance,  $\gamma$  correction

(3) Panel interface

- Built-in panel driver timing controller
- Panel protection timing signal generation
- Backlight control PWM (video adaptive low power consumption processing)

\*: The LC749402PT video input should satisfy the following conditions:

40MHz or less operating frequency, 896 dots or less horizontal size, 768 lines or less vertical size.

## LSI Specifications

- Supply voltage Core: 1.2V  
I/O: 1.8V/2.85V/3.3V
- Maximum operating frequency: 40MHz
- Package: TQFP100

## Principal Applications

- LCD display equipment

## CDEX (Color Depth Expander)



Original



CDEX

## Specifications

**Absolute Maximum Ratings** at Ta = 25°C, DVSS = 0V, AVSS\_OSC = 0V

| Parameter                     | Symbol                | Conditions | Ratings             | Unit |
|-------------------------------|-----------------------|------------|---------------------|------|
| Maximum supply voltage (I/O)  | DVDD_IO               |            | -0.3 to +3.96       | V    |
| Maximum supply voltage (core) | DVDD_CORE<br>AVDD_OSC |            | -0.3 to +1.8        | V    |
| Digital input voltage         | VI                    |            | -0.3 to DVDD_IO+0.3 | V    |
| Digital output voltage        | VO                    |            | -0.3 to DVDD_IO+0.3 | V    |
| Operating temperature         | Topr                  |            | -40 to +85          | °C   |
| Storage temperature           | Tstg                  |            | -55 to +125         | °C   |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

**Allowable Operating Ranges** at Ta = -40 to +85°C, DVSS = 0V, AVSS\_OSC = 0V

| Parameter             | Symbol                | Conditions | Ratings |      |         | unit |
|-----------------------|-----------------------|------------|---------|------|---------|------|
|                       |                       |            | min     | typ  | max     |      |
| Supply voltage (I/O)  | DVDD_IO               |            | 2.6     | 2.85 | 3.6     | V    |
|                       |                       |            | 1.7     | 1.8  | 1.9     | V    |
| Supply voltage (core) | DVDD_CORE<br>AVDD_OSC |            | 1.1     | 1.2  | 1.3     | V    |
| Input voltage range   | VIN                   |            | 0       |      | DVDD_IO | V    |

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**DC Characteristics** at  $T_a = -40$  to  $+85^\circ\text{C}$ ,  $DV_{SS} = 0\text{V}$ ,  $AV_{SS\_OSC} = 0\text{V}$ ,

$DV_{DD\_IO} = 1.7\text{V}$  to  $1.9\text{V}$  or  $2.6\text{V}$  to  $3.6\text{V}$ ,  $DV_{DD\_CORE} = 1.1\text{V}$  to  $1.3\text{V}$

| Parameter                 | Symbol     | Conditions   | Ratings              |     |                  | unit          |
|---------------------------|------------|--|----------------------|-----|------------------|---------------|
|                           |            |  | min                  | typ | max              |               |
| Input high-level voltage  | $V_{IH}$   | CMOS level inputs  | $0.7DV_{DD\_IO}$     |     |                  | V             |
|                           |            | CMOS level schmitt inputs  | $0.7DV_{DD\_IO}$     |     |                  | V             |
| Input low-level voltage   | $V_{IL}$   | CMOS level inputs  |                      |     | $0.3DV_{DD\_IO}$ | V             |
|                           |            | CMOS level schmitt inputs  |                      |     | $0.3DV_{DD\_IO}$ | V             |
| Input high-level current  | $I_{IH}$   | $V_I = DV_{DD\_IO}$  |                      |     | 10               | $\mu\text{A}$ |
|                           |            | $V_I = DV_{DD\_IO}$ , with pull-down resistance  |                      |     | 100              | $\mu\text{A}$ |
| Input low-level current   | $I_{IL}$   | $V_I = DV_{SS}$  | -10                  |     |                  | $\mu\text{A}$ |
| Output high-level voltage | $V_{OH}$   | CMOS voltage: 2.6V to 3.6V<br>Pin D: $I_{OH} = -2\text{mA}$<br>Pin F: $I_{OH} = -2\text{mA}$ (when set to 2mA)<br>$I_{OH} = -4\text{mA}$ (when set to 4mA)<br>Pin G: $I_{OH} = -4\text{mA}$ (when set to 4mA)<br>$I_{OH} = -8\text{mA}$ (when set to 8mA)<br>Pin H: $I_{OH} = -4\text{mA}$ | $DV_{DD\_IO} - 0.4$  |     |                  | V             |
|                           |            | CMOS voltage: 1.7V to 1.9V<br>Pin D: $I_{OH} = -1\text{mA}$<br>Pin F: $I_{OH} = -1\text{mA}$ (when set to 2mA)<br>$I_{OH} = -2\text{mA}$ (when set to 4mA)<br>Pin G: $I_{OH} = -2\text{mA}$ (when set to 4mA)<br>$I_{OH} = -4\text{mA}$ (when set to 8mA)<br>Pin H: $I_{OH} = -2\text{mA}$ | $DV_{DD\_IO} - 0.45$ |     |                  | V             |
| Output low-level voltage  | $V_{OL}$   | CMOS   |                      |     | 0.4              | V             |
| Output leak current       | $I_{OZ}$   | At output of high-impedance  | -10                  |     | 10               | $\mu\text{A}$ |
| Pull-down resistor        | $R_{DN}$   | Typical conditions:<br>$T_a = 25^\circ\text{C}$<br>$DV_{DD\_IO} = 2.85\text{V}$<br>$DV_{DD\_CORE} = 1.2\text{V}$   |                      | 98  |                  | k $\Omega$    |
| Dynamic supply current    | $I_{DDOP}$ | Typical conditions:<br>$T_a = 25^\circ\text{C}$<br>$DV_{DD\_IO} = 2.85\text{V}$<br>$DV_{DD\_CORE} = 1.2\text{V}$<br>tck=10MHz 10 steps   |                      | 18  |                  | mA            |
|                           |            | Typical conditions:<br>$T_a = 25^\circ\text{C}$<br>$DV_{DD\_IO} = 2.85\text{V}$<br>$DV_{DD\_CORE} = 1.2\text{V}$<br>tck=40MHz 10 steps   |                      | 57  |                  | mA            |
| Static supply current *1  | $I_{DDST}$ | Typical conditions:<br>$T_a = 25^\circ\text{C}$<br>$DV_{DD\_IO} = 2.85\text{V}$<br>$DV_{DD\_CORE} = 1.2\text{V}$<br>Outputs open<br>$V_I = DV_{SS}$ or $DV_{DD\_IO}$   |                      | 20  |                  | $\mu\text{A}$ |

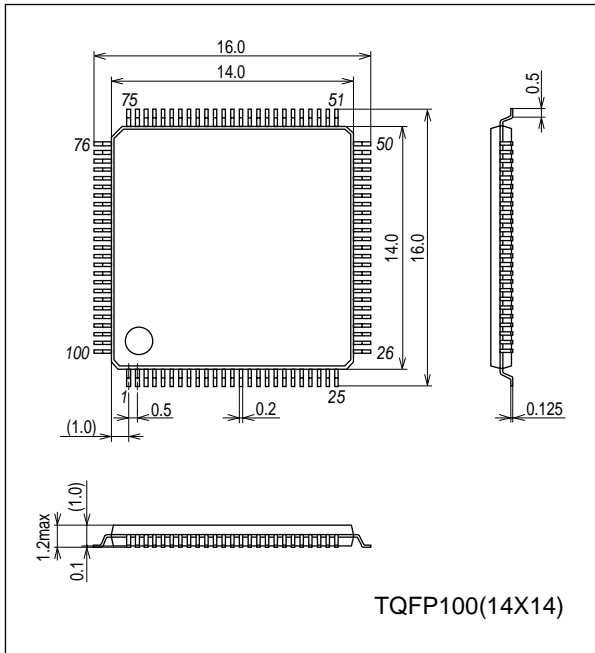
\*1: There is a input terminal which builds in pull down resistance. Please note that there is no guarantee about static consumption current depending on circuit composition.

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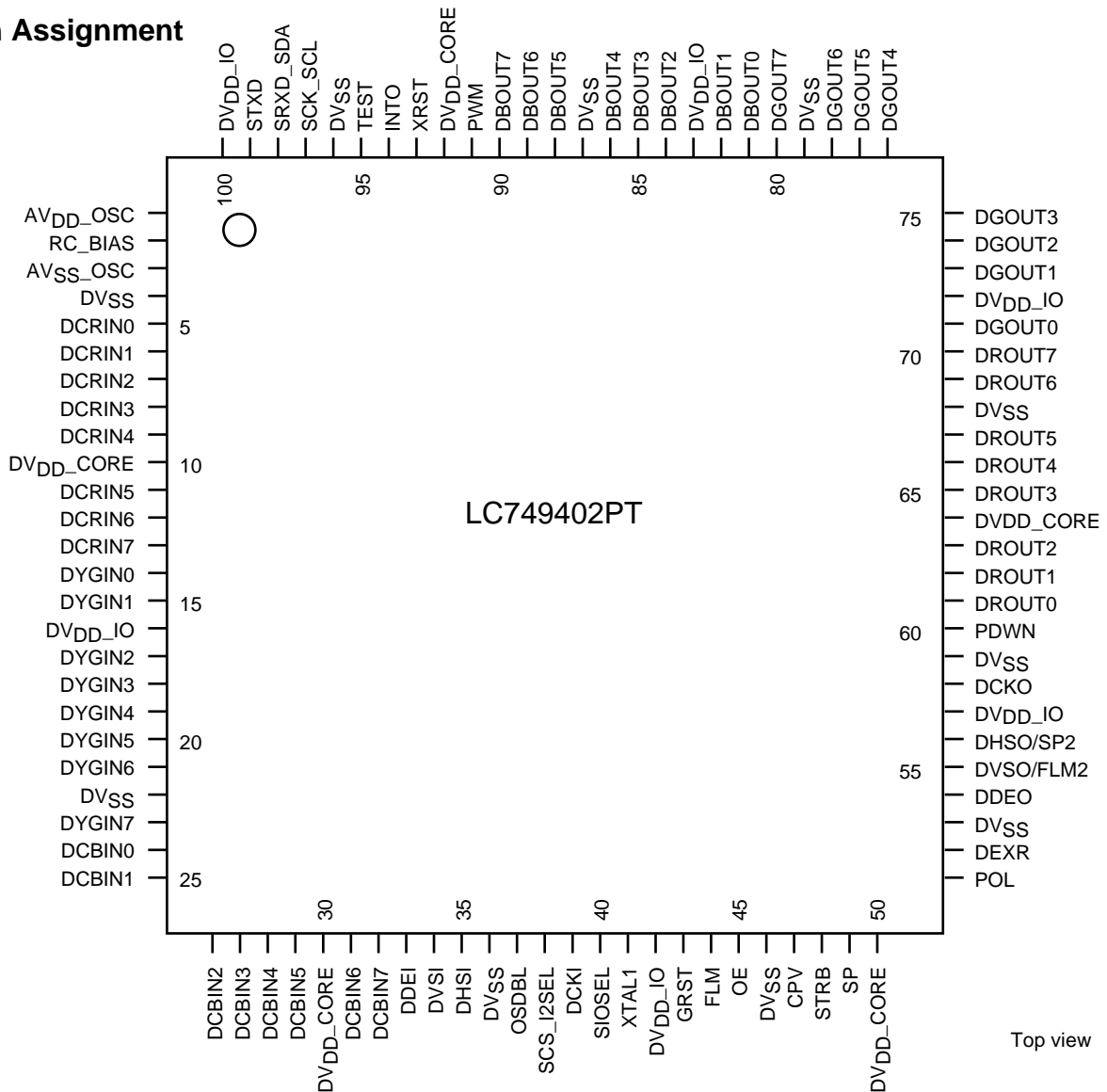
## Package Dimensions

unit:mm (typ)

3274



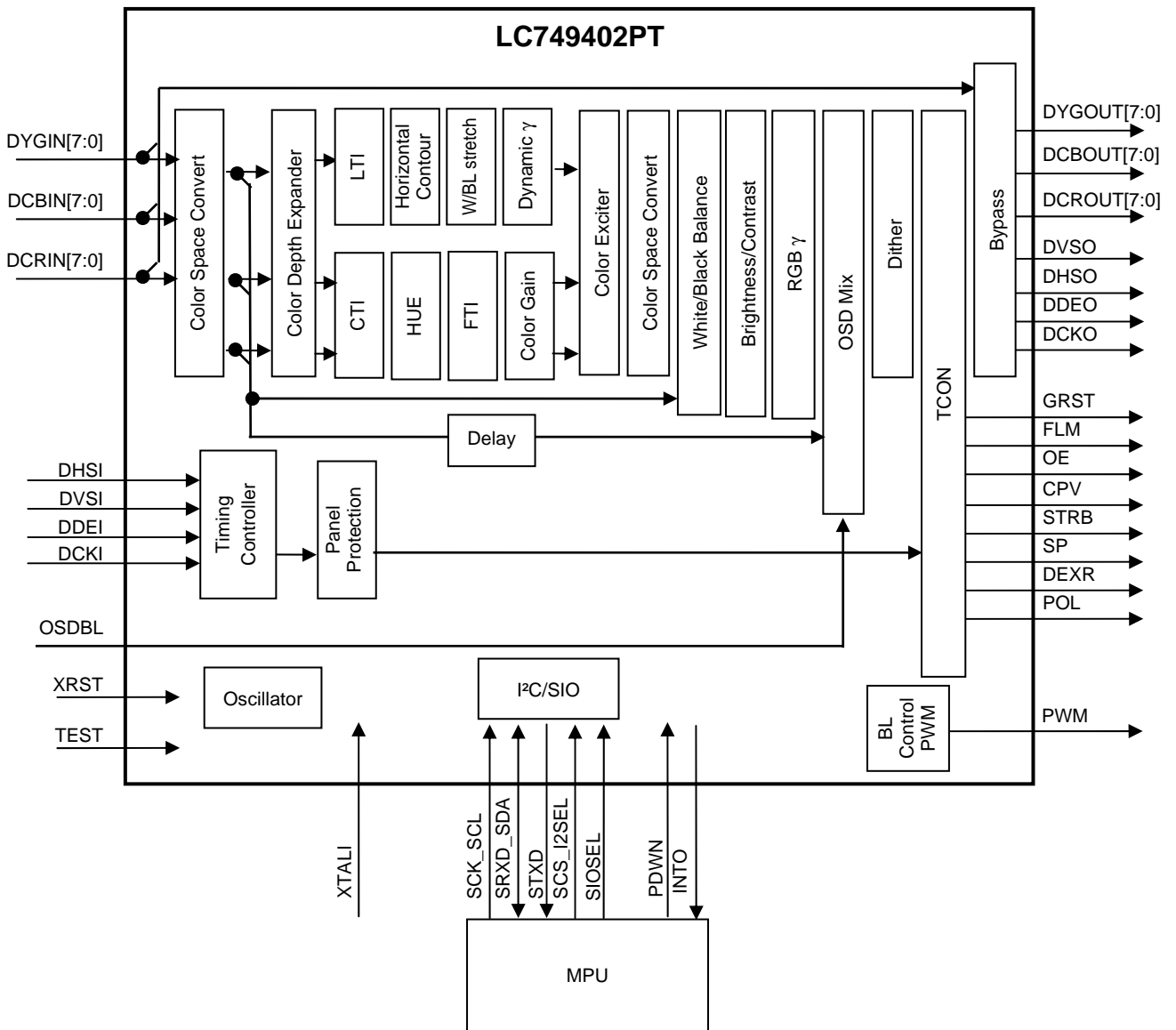
## Pin Assignment



Top view

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## Block Diagram



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## Pin Functions

| Pin No. | Pin symbol             | In/output format |        | Connecting destination |         | Remarks   |
|---------|------------------------|------------------|--------|------------------------|---------|---|
|         |                        | I/O              | Format |                        |         |   |
| 1       | AV <sub>DD</sub> _OSC  | P                | -      | Core Voltage           | Analog  |   |
| 2       | RC_BIAS                | I                | J      | Resistor               | Analog  | Bias resistor connection<br>(Connect to ground through 20kΩ resistor)         |
| 3       | AV <sub>SS</sub> _OSC  | P                | -      | GND                    | Analog  |   |
| 4       | DV <sub>SS</sub>       | P                | -      | GND                    | Digital |   |
| 5       | DCRIN0                 | I                | C      | CMOS                   | Digital | R/Cr video input. (LSB Connect to GND when not used.)                         |
| 6       | DCRIN1                 | I                | C      | CMOS                   | Digital | R/Cr video input. (Connect to GND when not used.)                             |
| 7       | DCRIN2                 | I                | C      | CMOS                   | Digital | R/Cr video input (Connect to GND when not used.)                              |
| 8       | DCRIN3                 | I                | C      | CMOS                   | Digital | R/Cr video input (Connect to GND when not used.)                              |
| 9       | DCRIN4                 | I                | C      | CMOS                   | Digital | R/Cr video input (Connect to GND when not used.)                              |
| 10      | DV <sub>DD</sub> _CORE | P                | -      | Core Voltage           | Digital |   |
| 11      | DCRIN5                 | I                | C      | CMOS                   | Digital | R/Cr video input (Connect to GND when not used.)                              |
| 12      | DCRIN6                 | I                | C      | CMOS                   | Digital | R/Cr video input (Connect to GND when not used.)                              |
| 13      | DCRIN7                 | I                | C      | CMOS                   | Digital | R/Cr video input (MSB Connect to GND when not used.)                          |
| 14      | DYGIN0                 | I                | C      | CMOS                   | Digital | G/Y/656 video input (LSB Connect to GND when not used.)                       |
| 15      | DYGIN1                 | I                | C      | CMOS                   | Digital | G/Y/656 video input (Connect to GND when not used.)                           |
| 16      | DV <sub>DD</sub> _IO   | P                | -      | IO voltage             | Digital |   |
| 17      | DYGIN2                 | I                | C      | CMOS                   | Digital | G/Y/656 video input (Connect to GND when not used.)                           |
| 18      | DYGIN3                 | I                | C      | CMOS                   | Digital | G/Y/656 video input (Connect to GND when not used.)                           |
| 19      | DYGIN4                 | I                | C      | CMOS                   | Digital | G/Y/656 video input (Connect to GND when not used.)                           |
| 20      | DYGIN5                 | I                | C      | CMOS                   | Digital | G/Y/656 video input (Connect to GND when not used.)                           |
| 21      | DYGIN6                 | I                | C      | CMOS                   | Digital | G/Y/656 video input (Connect to GND when not used.)                           |
| 22      | DV <sub>SS</sub>       | P                | -      | GND                    | Digital |   |
| 23      | DYGIN7                 | I                | C      | CMOS                   | Digital | G/Y/656 video input (MSB Connect to GND when not used.)                       |
| 24      | DCBIN0                 | I                | C      | CMOS                   | Digital | B/Cb/C video (LSB Connect to GND when not used.)                              |
| 25      | DCBIN1                 | I                | C      | CMOS                   | Digital | B/Cb/C video input (Connect to GND when not used.)                            |
| 26      | DCBIN2                 | I                | C      | CMOS                   | Digital | B/Cb/C video input (Connect to GND when not used.)                            |
| 27      | DCBIN3                 | I                | C      | CMOS                   | Digital | B/Cb/C video input (Connect to GND when not used.)                            |
| 28      | DCBIN4                 | I                | C      | CMOS                   | Digital | B/Cb/C video input (Connect to GND when not used.)                            |
| 29      | DCBIN5                 | I                | C      | CMOS                   | Digital | B/Cb/C video input (Connect to GND when not used.)                            |
| 30      | DV <sub>DD</sub> _CORE | P                | -      | Core Voltage           | Digital |   |
| 31      | DCBIN6                 | I                | C      | CMOS                   | Digital | B/Cb/C video input (Connect to GND when not used.)                            |
| 32      | DCBIN7                 | I                | C      | CMOS                   | Digital | B/Cb/C video input (MSB Connect to GND when not used.)                        |
| 33      | DDEI                   | I                | C      | CMOS                   | Digital | Data enable signal. (Connect to GND when not used.)                           |
| 34      | DVSI                   | I                | C      | CMOS                   | Digital | Vertical sync signal  |
| 35      | DHSI                   | I                | C      | CMOS                   | Digital | Horizontal sync signal.   |
| 36      | DV <sub>SS</sub>       | P                | -      | GND                    | Digital |   |
| 37      | OSDBL                  | I                | C      | CMOS                   | Digital | Data enable signal for external OSD.<br>(Connect to GND when not used.)       |
| 38      | SCS_I2SEL              | I                | A      | CMOS                   | Digital | SIO chip enable / I <sup>2</sup> C slave select                               |
| 39      | DCKI                   | I                | C      | CMOS                   | Digital | Video clock.  |
| 40      | SIOSEL                 | I                | C      | CMOS                   | Digital | "L": I <sup>2</sup> C slave, "H": 4 wire SIO                                  |
| 41      | XTAL1                  | I                | C      | CMOS                   | Digital | External clock input for panel protection.<br>(Connect to GND when not used.) |
| 42      | DV <sub>DD</sub> _IO   | P                | -      | IO voltage             | Digital |   |
| 43      | GRST                   | O                | F      | CMOS                   | Digital | Gate driver reset signal.   |
| 44      | FLM                    | O                | F      | CMOS                   | Digital | Start pulse signal for gate driver  |
| 45      | OE                     | O                | F      | CMOS                   | Digital | Output enable signal for gate driver.   |
| 46      | DV <sub>SS</sub>       | P                | -      | GND                    | Digital |   |
| 47      | CPV                    | O                | F      | CMOS                   | Digital | Gate driver clock signal.   |
| 48      | STRB                   | O                | F      | CMOS                   | Digital | Data strobe signal for source driver.   |
| 49      | SP                     | O                | F      | CMOS                   | Digital | Start pulse signal for source driver.   |

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Continued from preceding page.

| Pin No. | Pin symbol             | In/output format |        | Connecting destination |         | Remarks   |
|---------|------------------------|------------------|--------|------------------------|---------|---|
|         |                        | I/O              | Format |                        |         |   |
| 50      | DV <sub>DD</sub> _CORE | P                | -      | Core Voltage           | Digital |   |
| 51      | POL                    | O                | F      | CMOS                   | Digital | Voltage polarity selection signal for the source driver.              |
| 52      | DEXR                   | O                | F      | CMOS                   | Digital | Reversed video signal output for DTR. Low output when the DTR is OFF. |
| 53      | DV <sub>SS</sub>       | P                | -      | GND                    | Digital |   |
| 54      | DDEO                   | O                | F      | CMOS                   | Digital | Data enable signal  |
| 55      | DVSO / FLM2            | O                | F      | CMOS                   | Digital | Vertical sync signal / Start pulse signal for gate driver             |
| 56      | DHSO / SP2             | O                | F      | CMOS                   | Digital | Horizontal sync signal / Start pulse signal for source driver         |
| 57      | DV <sub>DD</sub> _IO   | P                | -      | IO voltage             | Digital |   |
| 58      | DCKO                   | O                | G      | CMOS                   | Digital | Video clock output  |
| 59      | DV <sub>SS</sub>       | P                | -      | GND                    | Digital |   |
| 60      | PDWN                   | I                | A      | CMOS                   | Digital | "H" power down control (Connect to GND when not used.)                |
| 61      | DROUT0                 | O                | F      | CMOS                   | Digital | R/Cr video output (LSB when 8-bit output is selected)                 |
| 62      | DROUT1                 | O                | F      | CMOS                   | Digital | R/Cr video output   |
| 63      | DROUT2                 | O                | F      | CMOS                   | Digital | R/Cr video output (LSB when 6-bit output is selected)                 |
| 64      | DV <sub>DD</sub> _CORE | P                | -      | Core Voltage           | Digital |   |
| 65      | DROUT3                 | O                | F      | CMOS                   | Digital | R/Cr video output   |
| 66      | DROUT4                 | O                | F      | CMOS                   | Digital | R/Cr video output   |
| 67      | DROUT5                 | O                | F      | CMOS                   | Digital | R/Cr video output   |
| 68      | DV <sub>SS</sub>       | P                | -      | GND                    | Digital |   |
| 69      | DROUT6                 | O                | F      | CMOS                   | Digital | R/Cr video output   |
| 70      | DROUT7                 | O                | F      | CMOS                   | Digital | R/Cr video output (MSB)   |
| 71      | DGOUT0                 | O                | F      | CMOS                   | Digital | G/Y video output (LSB when 8-bit output is selected)                  |
| 72      | DV <sub>DD</sub> _IO   | P                | -      | IO voltage             | Digital |   |
| 73      | DGOUT1                 | O                | F      | CMOS                   | Digital | G/Y video output  |
| 74      | DGOUT2                 | O                | F      | CMOS                   | Digital | G/Y video output (LSB when 6-bit output is selected)                  |
| 75      | DGOUT3                 | O                | F      | CMOS                   | Digital | G/Y video output  |
| 76      | DGOUT4                 | O                | F      | CMOS                   | Digital | G/Y video output  |
| 77      | DGOUT5                 | O                | F      | CMOS                   | Digital | G/Y video output  |
| 78      | DGOUT6                 | O                | F      | CMOS                   | Digital | G/Y video output  |
| 79      | DV <sub>SS</sub>       | P                | -      | GND                    | Digital |   |
| 80      | DGOUT7                 | O                | F      | CMOS                   | Digital | G/Y video output (MSB)  |
| 81      | DBOUT0                 | O                | F      | CMOS                   | Digital | B/Cb/C video output (LSB when 8-bit output is selected)               |
| 82      | DBOUT1                 | O                | F      | CMOS                   | Digital | B/Cb/C video output   |
| 83      | DV <sub>DD</sub> _IO   | P                | -      | IO voltage             | Digital |   |
| 84      | DBOUT2                 | O                | F      | CMOS                   | Digital | B/Cb/C video output (LSB when 6-bit output is selected)               |
| 85      | DBOUT3                 | O                | F      | CMOS                   | Digital | B/Cb/C video output   |
| 86      | DBOUT4                 | O                | F      | CMOS                   | Digital | B/Cb/C video output   |
| 87      | DV <sub>SS</sub>       | P                | -      | GND                    | Digital |   |
| 88      | DBOUT5                 | O                | F      | CMOS                   | Digital | B/Cb/C video output   |
| 89      | DBOUT6                 | O                | F      | CMOS                   | Digital | B/Cb/C video output   |
| 90      | DBOUT7                 | O                | F      | CMOS                   | Digital | B/Cb/C video output (MSB)   |
| 91      | PWM                    | O                | D      | CMOS                   | Digital | Pulse width modulation waveform output                                |
| 92      | DV <sub>DD</sub> _CORE | P                | -      | Core Voltage           | Digital |   |
| 93      | XRST                   | I                | A      | CMOS                   | Digital | System reset ("L" reset)  |
| 94      | INTO                   | O                | D      | CMOS                   | Digital | Interrupt   |
| 95      | TEST                   | I                | B      | CMOS                   | Digital | Test setting (Connect to GND normally)                                |
| 96      | DV <sub>SS</sub>       | P                | -      | GND                    | Digital |   |
| 97      | SCK_SCL                | I                | C      | CMOS                   | Digital | Bus clock (shared with SIO/I <sup>2</sup> C)                          |
| 98      | SRXD_SDA               | I/O              | H      | CMOS                   | Digital | SIO data input / I <sup>2</sup> C data input/output                   |
| 99      | STXD                   | O                | D      | CMOS                   | Digital | SIO data  |
| 100     | DV <sub>DD</sub> _IO   | P                | -      | IO voltage             | Digital |   |

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## Pin Type

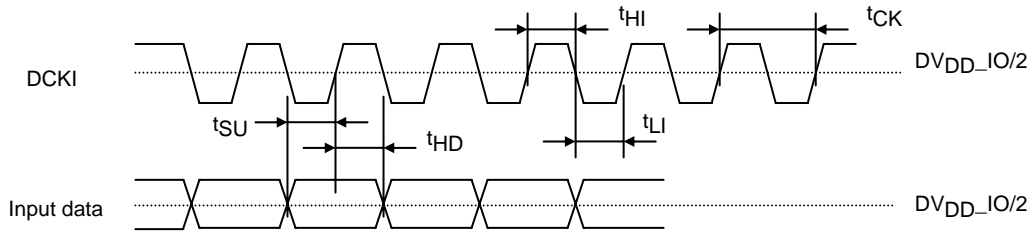
| In/Output form | Function  | Equivalent circuit | Application Terminal   |
|----------------|---|--------------------|--|
| A              | Schmitt trigger<br>CMOS input                     |                    | XRST, PDWN, SCS_I2SEL  |
| B              | CMOS input with built-in<br>pull-down resistor    |                    | TEST   |
| C              | CMOS input  |                    | SCK_SCL, SIOSEL,<br>DVSI, DHSI, DDEI, OSDBL,<br>DYGIN7, DYGIN6, DYGIN5, DYGIN4,<br>DYGIN3, DYGIN2, DYGIN1, DYGIN0,<br>DCBIN7, DCBIN6, DCBIN5, DCBIN4,<br>DCBIN3, DCBIN2, DCBIN1, DCBIN0,<br>DCRIN7, DCRIN6, DCRIN5, DCRIN4,<br>DCRIN3, DCRIN2, DCRIN1, DCRIN0                            |
| D              | 2mA 3-STATE drive<br>CMOS output                  |                    | STXD, PWM, INTO  |
| F              | 2mA/4mA switching<br>3-STATE drive<br>CMOS output |                    | DBOUT7, DBOUT6, DBOUT5, DBOUT4,<br>DBOUT3, DBOUT2, DBOUT1, DBOUT0,<br>DROUT7, DROUT6, DROUT5, DROUT4,<br>DROUT3, DROUT2, DROUT1, DROUT0<br>DGOUT7, DGOUT6, DGOUT5, DGOUT4,<br>DGOUT3, DGOUT2, DGOUT1, DGOUT0,<br>DHSO/SP2, DVSO/FLM2, DDEO<br>FLM, DEXR, POL, GRST, CPV,<br>SP, OE, STRB |
| G              | 4mA/8mA switching<br>3-STATE drive<br>CMOS output |                    | DCKO   |
| H              | 4mA 3-STATE drive<br>CMOS input/output            |                    | SRXD_SDA   |
| J              | Analog input/output                               |                    | RC_BIAS  |



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## I/O Timing

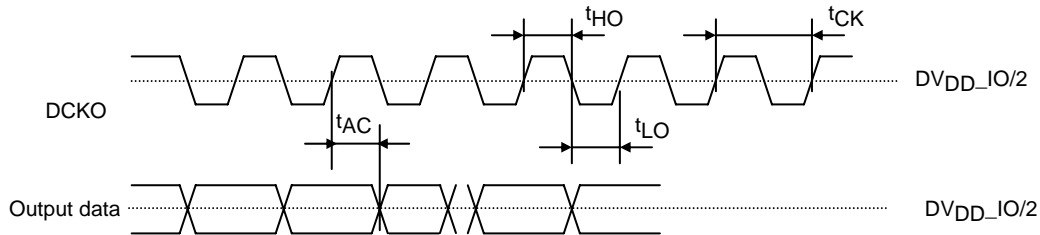
### (1) Input data timing



| Pin name  | Parameter                                      | Symbol | min | typ | max | unit |
|---|--|--------|-----|-----|-----|------|
| DCKI  | Clock cycle                                    | tCK    | 25  |     |     | ns   |
|   | Duty   |        |     | 50  |     | %    |
| DCRIN*, DYGIN*,<br>DCBIN*, DVSI,<br>DHSI, DDEI, OSDBL | Input data setup time<br>(DVDD_IO=2.6 to 3.6V) | tSU    | 3   |     |     | ns   |
|   | Input data setup time<br>(DVDD_IO=1.7 to 1.9V) | tSU    | 3   |     |     | ns   |
|   | Input data hold time<br>(DVDD_IO=2.6 to 3.6V)  | tHD    | 2   |     |     | ns   |
|   | Input data hold time<br>(DVDD_IO=1.7 to 1.9V)  | tHD    | 2   |     |     | ns   |

\*: The recommended duty cycle of input clock is 50%

### (2) Output data timing



| Pin name  | Parameter   | Symbol | min | typ | max | unit |
|---|---|--------|-----|-----|-----|------|
| DCKO  | Clock cycle   | tCK    | 25  |     |     | ns   |
|   | Duty  |        |     | 50  |     | %    |
| DROUT*, DGOUT*, DBOUT*,<br>DVSO, DHSO, DDEO, DEXR, POL,<br>SP, STRB, CPV, OE, FLM, GRST | Output data delay time<br>(DVDD_IO=2.6 to 3.6V)<br>Pin F: when set to 4mA<br>Pin G: when set to 8mA | tAC    | -3  |     | 3   | ns   |
|   | Output data delay time<br>(DVDD_IO=2.6 to 3.6V)<br>Pin F: when set to 2mA<br>Pin G: when set to 4mA | tAC    | -3  |     | 6   | ns   |
|   | Output data delay time<br>(DVDD_IO=1.7 to 1.9V)<br>Pin F: when set to 4mA<br>Pin G: when set to 8mA | tAC    | -5  |     | 4   | ns   |
|   | Output data delay time<br>(DVDD_IO=1.7 to 1.9V)<br>Pin F: when set to 2mA<br>Pin G: when set to 4mA | tAC    | -6  |     | 9   | ns   |

\* When DCKO is set to the forward rotation output. Output load capacity: 5pF

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### Офис по работе с юридическими лицами:

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: [info@moschip.ru](mailto:info@moschip.ru)

Skype отдела продаж:

moschip.ru

moschip.ru\_4

moschip.ru\_6

moschip.ru\_9