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September 2014

FDMC86160

N-Channel Shielded Gate PowerTrench[®] MOSFET 100 V, 43 A, 14 m Ω

Features

- Shielded Gate MOSFET Technology
- Max $r_{DS(on)}$ = 14 m Ω at V_{GS} = 10 V, I_D = 9 A
- Max $r_{DS(on)} = 23 \text{ m}\Omega$ at $V_{GS} = 6 \text{ V}$, $I_D = 7 \text{ A}$
- High performance technology for extremely low r_{DS(on)}
- Termination is Lead-free and RoHS Compliant

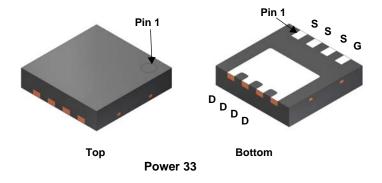


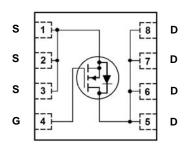
General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process that incorporates Shielded Gate technology. This process has been optimized for the on-state resistance. This device is well suited for applications where ulta low $R_{DS\ (on)}$ is required in small spaces such as High performance VRM, POL and orring functions.

Applications

- Bridge Topologies
- Synchronous Rectifier





MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted

Symbol		Paramet	ter		Ratings	Units
V_{DS}	Drain to Source Voltage				100	V
V_{GS}	Gate to Source V	/oltage			±20	V
	Drain Current	-Continuous	T _C = 25 °C		43	
I _D	-Continuous		T _A = 25 °C	(Note 1a)	9	Α
		-Pulsed		(Note 4)	50	
E _{AS}	Single Pulse Ava	lanche Energy		(Note 3)	181	mJ
D	Power Dissipatio	n	T _C = 25 °C		54	w
P_{D}	Power Dissipatio	n	T _A = 25 °C	(Note 1a)	2.3	VV
T_J , T_{STG}	Operating and St	orage Junction Temperat	ure Range		-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	(Note 1)	2.3	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	53	C/VV

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC86160	FDMC86160	Power33	13 "	12 mm	3000 units

Electrical Characteristics T_J = 25 °C unless otherwise noted

Symbol	Parameter	Parameter Test Conditions		Тур	Max	Units
Off Chara	cteristics					
BV _{DSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$	100			V
$\frac{\Delta BV_{DSS}}{\Delta T_{J}}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μ A, referenced to 25 °C		73		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 80 V, V _{GS} = 0 V			1	μА
I _{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$			±100	nA

On Characteristics

V _{GS(th)}	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu A$	2	2.9	4	V
$\Delta V_{GS(th)} \over \Delta T_J$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μ A, referenced to 25 °C		-9		mV/°C
		V _{GS} = 10 V, I _D = 9 A		11.2	14	
r _{DS(on)}	Static Drain to Source On Resistance	$V_{GS} = 6 \text{ V}, I_D = 7 \text{ A}$		16	23	$m\Omega$
, ,		V _{GS} = 10 V, I _D = 9 A, T _J = 125 °C		21	26	
9 _{FS}	Forward Transconductance	V _{DD} = 10 V, I _D = 9 A		43		S

Dynamic Characteristics

C _{iss}	Input Capacitance	V 50 V V 0 V		968	1290	pF
C _{oss}	Output Capacitance	$V_{DS} = 50 \text{ V}, V_{GS} = 0 \text{ V},$ f = 1 MHz		241	320	pF
C _{rss}	Reverse Transfer Capacitance	1 - 1 101112		11	20	pF
R_{α}	Gate Resistance		0.1	0.6	2.5	Ω

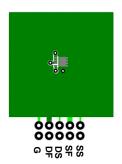
Switching Characteristics

t _{d(on)}	Turn-On Delay Time				9.7	19	ns
t _r	Rise Time	$V_{DD} = 50 \text{ V}, I_{D} = 9$			3.6	10	ns
t _{d(off)}	Turn-Off Delay Time	$V_{GS} = 10 \text{ V}, R_{GEN}$	= 6 Ω		16	30	ns
t _f	Fall Time				3.4	10	ns
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0 \text{ V to } 10 \text{ V}$			15	22	nC
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0 \text{ V to 6 V}$	$V_{DD} = 50 \text{ V},$		9.8	15	nC
Q_{gs}	Total Gate Charge		I _D = 9 A		4.4		nC
Q_{gd}	Gate to Drain "Miller" Charge				3.5		nC

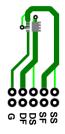
Drain-Source Diode Characteristics

V _{SD} Source	Source to Drain Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_{S} = 9 \text{ A}$	(Note 2)	0.79	1.3	V
	Source to Drain Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_{S} = 1.9 \text{ A}$	(Note 2)	0.72	1.2	V
t _{rr}	Reverse Recovery Time	I _F = 9 A, di/dt = 100 A/μs		47	75	ns
Q _{rr}	Reverse Recovery Charge			45	73	nC

^{1.} R_{0JA} is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. R_{0JC} is guaranteed by design while R_{0CA} is determined by the user's board design.



a. 53 °C/W when mounted on a 1 in² pad of 2 oz copper



b. 125 °C/W when mounted on a minimum pad of 2 oz copper

^{2.} Pulse Test: Pulse Width < 300 $\mu\text{s},$ Duty cycle < 2.0%.

^{3.} E_{AS} of 181 mJ is based on starting $T_{J} = 25$ °C, L = 3 mH, $I_{AS} = 11$ A, $V_{DD} = 100$ V, $V_{GS} = 10$ V. 100% test at L = 0.1 mH, $I_{AS} = 35$ A.

^{4.} Pulse Id refers to Figure.11 Forward Bias Safe Operation Area.

Typical Characteristics $T_J = 25$ °C unless otherwise noted

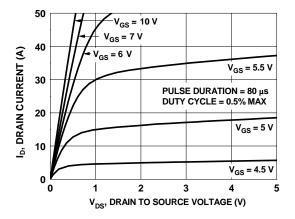


Figure 1. On-Region Characteristics

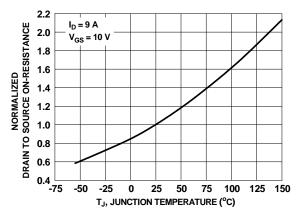


Figure 3. Normalized On-Resistance vs Junction Temperature

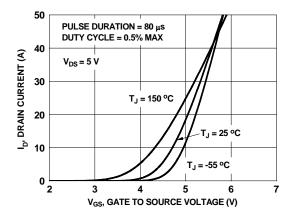


Figure 5. Transfer Characteristics

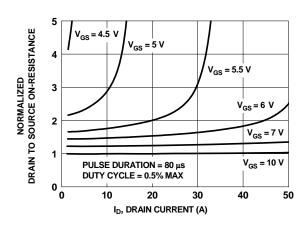


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

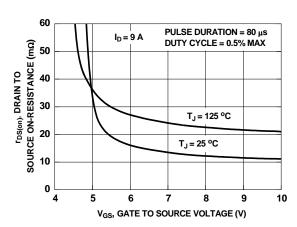


Figure 4. On-Resistance vs Gate to Source Voltage

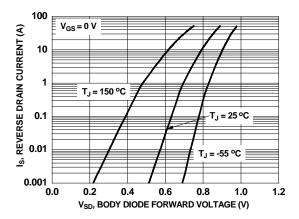


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics $T_J = 25$ °C unless otherwise noted

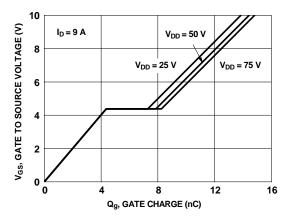


Figure 7. Gate Charge Characteristics

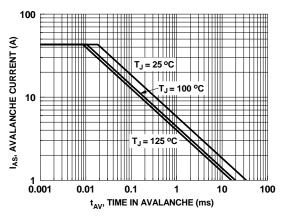


Figure 9. Unclamped Inductive Switching Capability

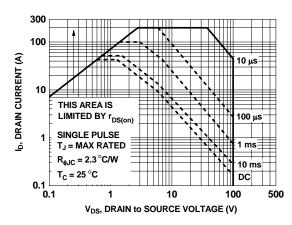


Figure 11. Forward Bias Safe Operating Area

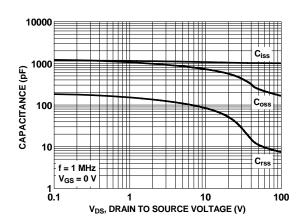


Figure 8. Capacitance vs Drain to Source Voltage

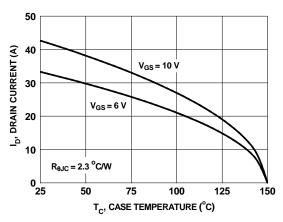


Figure 10. Maximum Continuous Drain Current vs Case Temperature

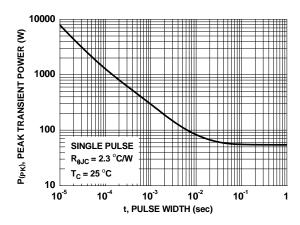


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics T_J = 25 °C unless otherwise noted

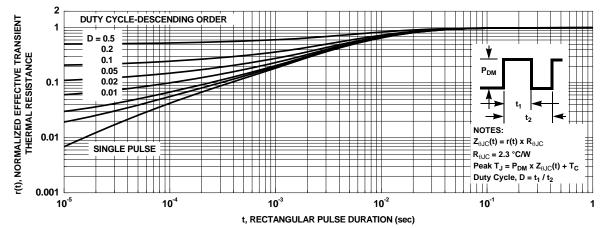


Figure 13. Junction-to-Case Transient Thermal Response Curve

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