

74HCU04-Q100

Hex unbuffered inverter

Rev. 2 — 22 October 2015

Product data sheet

1. General description

The 74HCU04-Q100 is a hex unbuffered inverter. Inputs include clamp diodes that enable the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

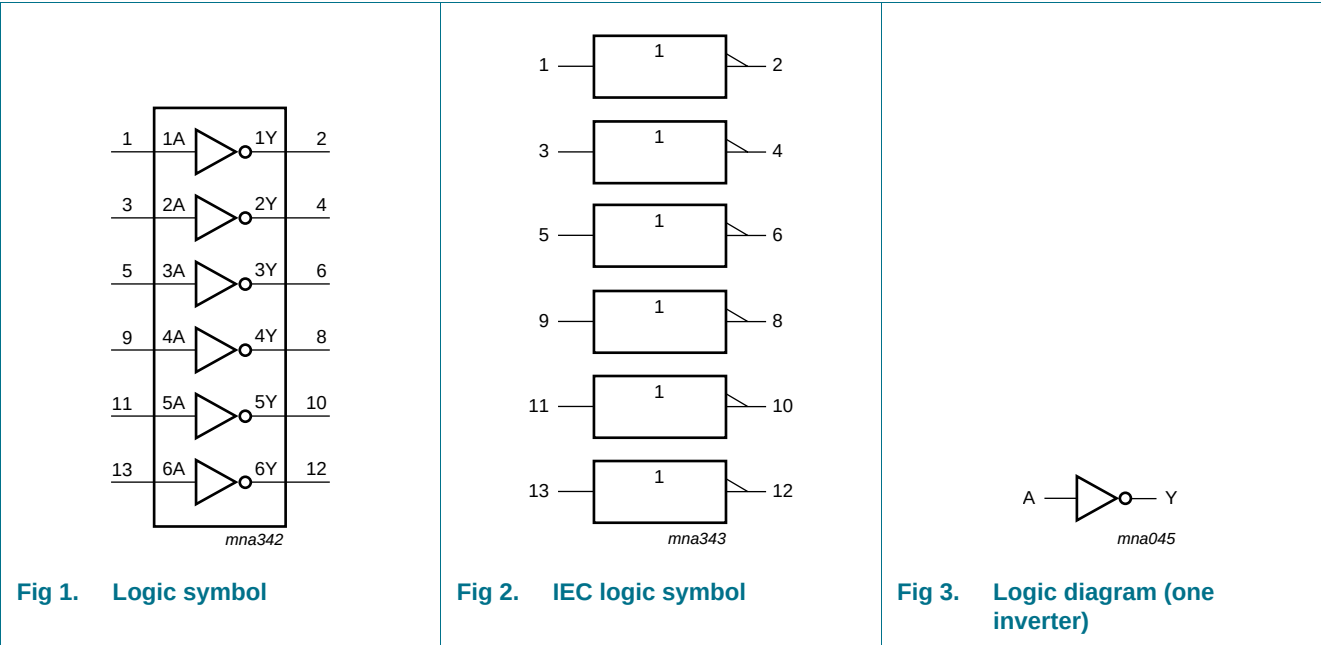
- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
 - ◆ Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ and from $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$
- Complies with JEDEC standard JESD7A
- Balanced propagation delays
- ESD protection:
 - ◆ MIL-STD-883, method 3015 exceeds 2000 V
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V ($C = 200\text{ pF}$, $R = 0\text{ }\Omega$)
- Multiple package options

3. Ordering information

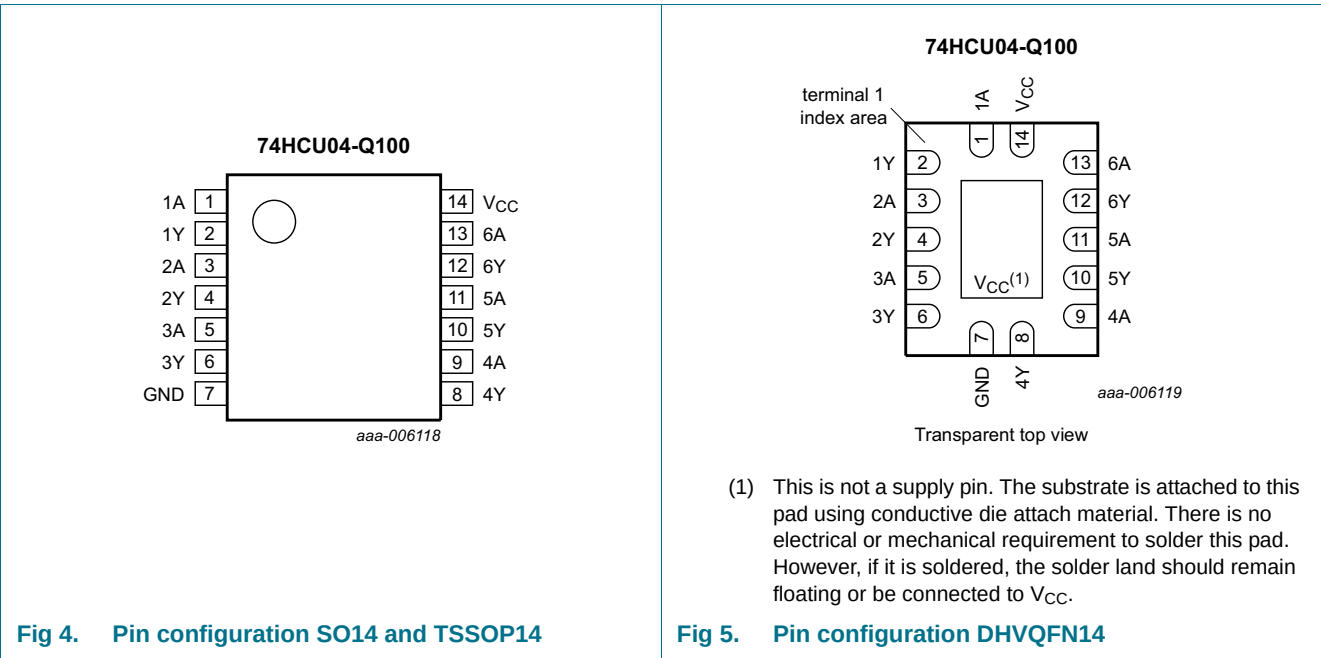
Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HCU04D-Q100	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74HCU04PW-Q100	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74HCU04BQ-Q100	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body $2.5 \times 3 \times 0.85\text{ mm}$	SOT762-1

4. Functional diagram



5. Pinning information



5.1 Pin description

Table 2. Pin description

Symbol	Pin	Description
1A	1	data input
1Y	2	data output
2A	3	data input
2Y	4	data output
3A	5	data input
3Y	6	data output
GND	7	ground (0 V)
4Y	8	data output
4A	9	data input
5Y	10	data output
5A	11	data input
6Y	12	data output
6A	13	data input
V _{CC}	14	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level

Input	Output
nA	nY
L	H
H	L

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{CC}	supply voltage			−0.5	+7.0	V
I _{IK}	input clamping current	V _I < −0.5 V or V _I > V _{CC} + 0.5 V	[1]	-	±20	mA
I _{OK}	output clamping current	V _O < −0.5 V or V _O > V _{CC} + 0.5 V	[1]	-	±50	mA
I _O	output current	−0.5 V < V _O < V _{CC} + 0.5 V		-	±25	mA
I _{CC}	supply current			-	50	mA
I _{GND}	ground current			−50	-	mA
T _{stg}	storage temperature			−65	+150	°C
P _{tot}	total power dissipation		[2]			
	SO14, TSSOP14 and DHVQFN14 packages			-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

- [2] For SO14 package: P_{tot} derates linearly with 8 mW/K above 70 °C.
 For TSSOP14 packages: P_{tot} derates linearly with 5.5 mW/K above 60 °C.
 For DHVQFN14 packages: P_{tot} derates linearly with 4.5 mW/K above 60 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		2.0	5.0	6.0	V
V_{I}	input voltage		0	-	V_{CC}	V
V_{O}	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	°C

9. Static characteristics

Table 6. Static characteristics

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	$V_{\text{CC}} = 2.0 \text{ V}$	1.7	1.4	-	1.7	-	1.7	-	V
		$V_{\text{CC}} = 4.5 \text{ V}$	3.6	2.6	-	3.6	-	3.6	-	V
		$V_{\text{CC}} = 5.5 \text{ V}$	4.8	3.4	-	4.8	-	4.8	-	V
V_{IL}	LOW-level input voltage	$V_{\text{CC}} = 2.0 \text{ V}$	-	0.6	0.3	-	0.3	-	0.3	V
		$V_{\text{CC}} = 4.5 \text{ V}$	-	1.9	0.9	-	0.9	-	0.9	V
		$V_{\text{CC}} = 5.5 \text{ V}$	-	2.6	1.2	-	1.2	-	1.2	V
V_{OH}	HIGH-level output voltage	$V_{\text{I}} = V_{\text{IH}}$ or V_{IL}								
		$I_{\text{O}} = -20 \text{ }\mu\text{A}$; $V_{\text{CC}} = 2.0 \text{ V}$	1.8	2.0	-	1.8	-	1.8	-	V
		$I_{\text{O}} = -20 \text{ }\mu\text{A}$; $V_{\text{CC}} = 4.5 \text{ V}$	4.0	4.5	-	4.0	-	4.0	-	V
		$I_{\text{O}} = -4.0 \text{ mA}$; $V_{\text{CC}} = 4.5 \text{ V}$	3.98	4.32	-	3.84	-	3.7	-	V
		$I_{\text{O}} = -20 \text{ }\mu\text{A}$; $V_{\text{CC}} = 6.0 \text{ V}$	5.5	6.0	-	5.5	-	5.5	-	V
V_{OL}	LOW-level output voltage	$V_{\text{I}} = V_{\text{IH}}$ or V_{IL}								
		$I_{\text{O}} = 20 \text{ }\mu\text{A}$; $V_{\text{CC}} = 2.0 \text{ V}$	-	0	0.2	-	0.2	-	0.2	V
		$I_{\text{O}} = 20 \text{ }\mu\text{A}$; $V_{\text{CC}} = 4.5 \text{ V}$	-	0	0.5	-	0.5	-	0.5	V
		$I_{\text{O}} = 4.0 \text{ mA}$; $V_{\text{CC}} = 4.5 \text{ V}$	-	0.15	0.26	-	0.33	-	0.4	V
		$I_{\text{O}} = 20 \text{ }\mu\text{A}$; $V_{\text{CC}} = 6.0 \text{ V}$	-	0	0.5	-	0.5	-	0.5	V
I_{I}	input leakage current	$V_{\text{I}} = V_{\text{CC}}$ or GND; $V_{\text{CC}} = 6.0 \text{ V}$	-	-	± 0.1	-	± 1.0	-	± 1.0	μA
I_{CC}	supply current	$V_{\text{I}} = V_{\text{CC}}$ or GND; $I_{\text{O}} = 0 \text{ A}$; $V_{\text{CC}} = 6.0 \text{ V}$	-	-	2	-	20	-	20	μA
C_{I}	input capacitance		-	3.5	-	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); For test circuit see [Figure 7](#).

Symbol	Parameter	Conditions		25 °C		–40 °C to +85 °C	–40 °C to +125 °C	Unit
				Typ	Max	Max	Max	
t _{pd}	propagation delay	nA to nY; see Figure 6	[1]					
		V _{CC} = 2.0 V; C _L = 50 pF		19	70	90	105	ns
		V _{CC} = 4.5 V; C _L = 50 pF		7	14	18	21	ns
		V _{CC} = 5.0 V; C _L = 15 pF		5	-	-	-	ns
		V _{CC} = 6.0 V; C _L = 50 pF		6	12	15	18	ns
t _t	transition time	see Figure 6	[2]					
		V _{CC} = 2.0 V; C _L = 50 pF		19	75	95	110	ns
		V _{CC} = 4.5 V; C _L = 50 pF		7	15	19	22	ns
		V _{CC} = 6.0 V; C _L = 50 pF		6	13	16	19	ns
C _{PD}	power dissipation capacitance	per inverter; V _I = GND to V _{CC}	[3]	10	-			pF

[1] t_{pd} is the same as t_{PHL} , t_{PLH} .

[2] t_t is the same as t_{THL} , t_{TLH} .

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

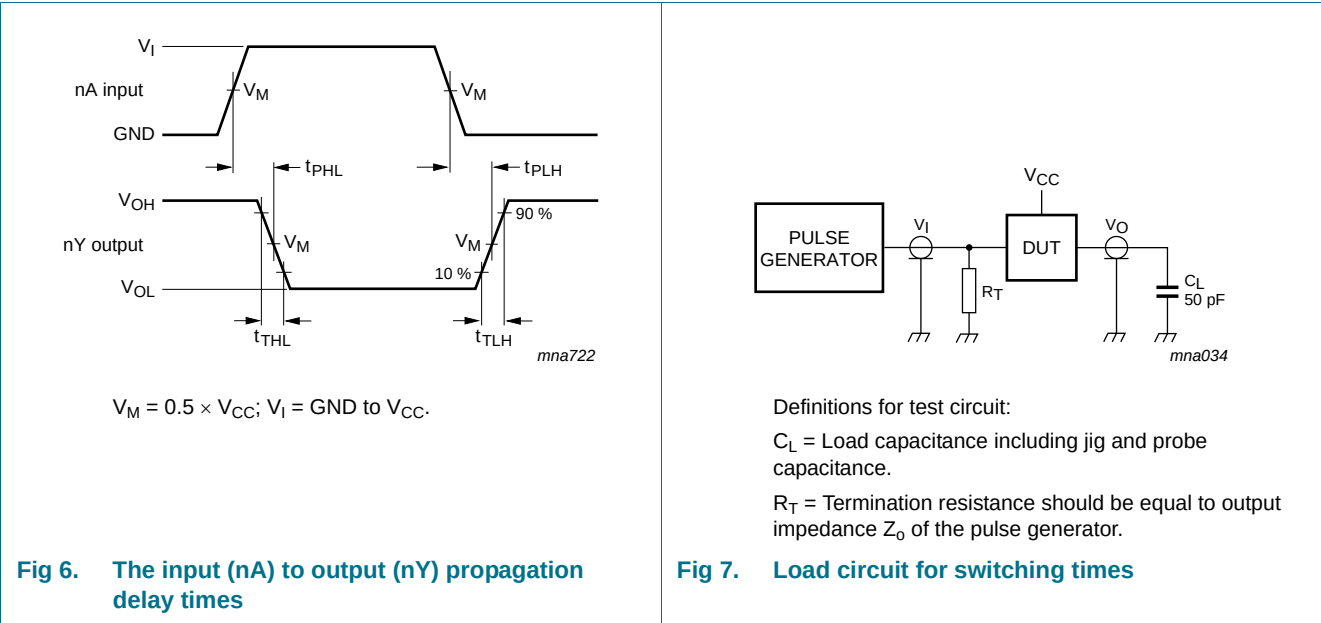
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

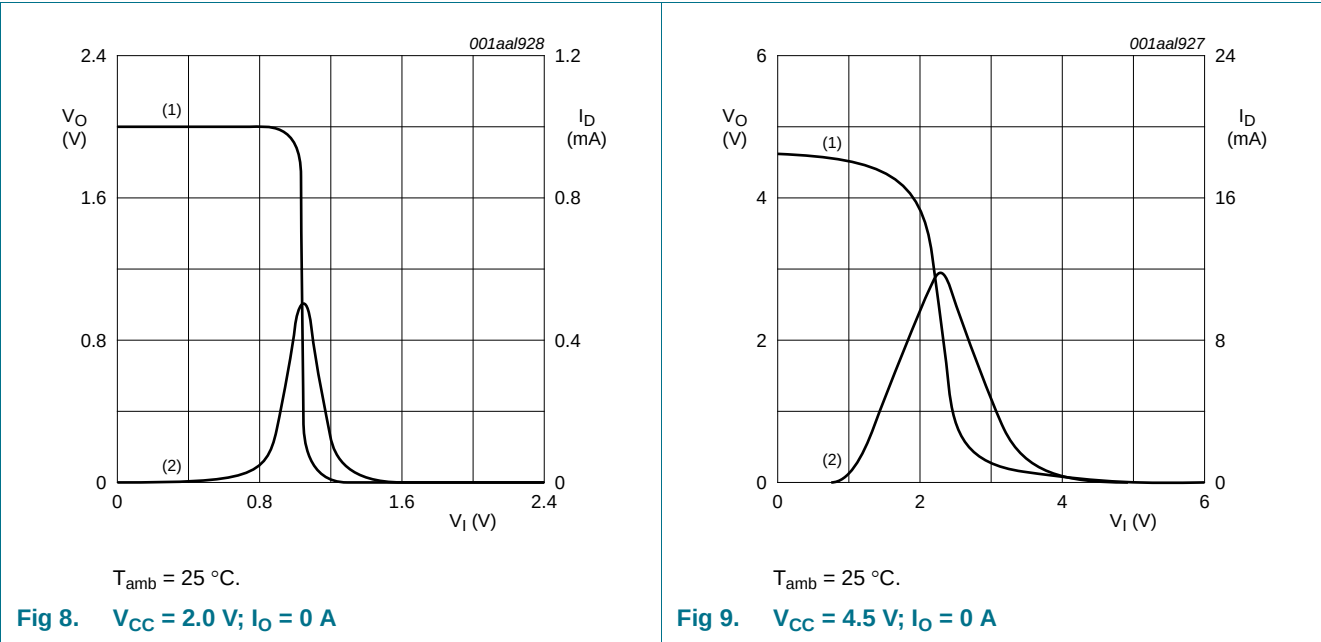
N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

11. Waveforms



12. Typical transfer characteristics



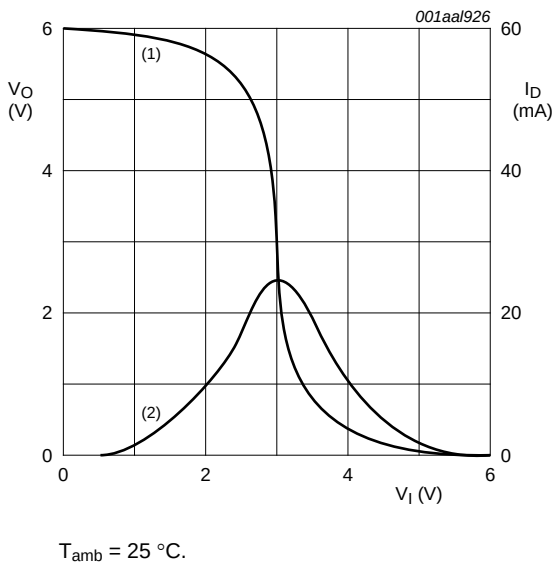
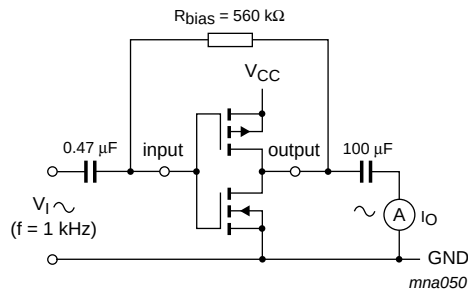


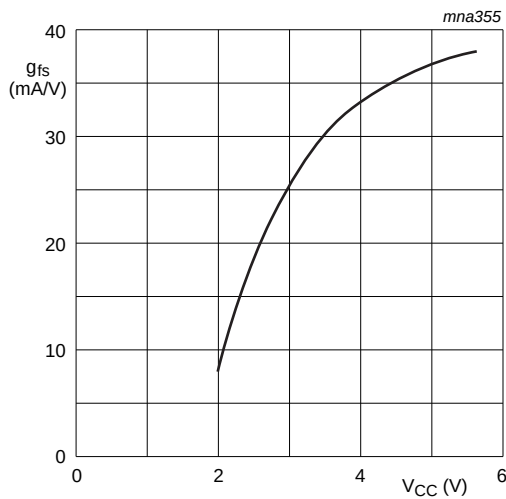
Fig 10. $V_{CC} = 6.0\text{ V}; I_O = 0\text{ A}$



$$g_{fs} = \frac{\Delta I_O}{\Delta V_I}$$

$f_i = 1\text{ kHz}$ at V_O is constant

Fig 11. Test set-up for measuring forward transconductance



$T_{amb} = 25\text{ °C}.$

Fig 12. Typical forward transconductance as a function of the supply voltage

13. Application information

Some applications are:

- Linear amplifier (see [Figure 13](#))
- Crystal oscillator design (see [Figure 14](#))
- Astable multivibrator (see [Figure 15](#))

Remark: All values given are typical unless otherwise specified.

Maximum $V_{O(p-p)} = V_{CC} - 2.0\text{ V}$ centered at $0.5 \times V_{CC}$.

$$G_v = - \frac{G_{ol}}{1 + \frac{R1}{R2}(1 + G_{ol})}$$

G_{ol} = open loop gain
 G_v = voltage gain
 $R1 \geq 3\text{ k}\Omega$, $R2 \leq 1\text{ M}\Omega$
 $Z_L > 10\text{ k}\Omega$; $G_{ol} = 20$ (typical)
 $V_{CC} = 6.0\text{ V}$
Typical unity gain bandwidth product is 5 MHz.

Fig 13. Used as a linear amplifier

$C1 = 47\text{ pF}$ (typical)
 $C2 = 33\text{ pF}$ (typical)
 $R1 = 1\text{ M}\Omega$ to $10\text{ M}\Omega$ (typical)
 $R2$ optimum value depends on the frequency and required stability against changes in V_{CC} or average minimum I_{CC} . I_{CC} is typically 5 mA at $V_{CC} = 5\text{ V}$ and $f_i = 10\text{ MHz}$.

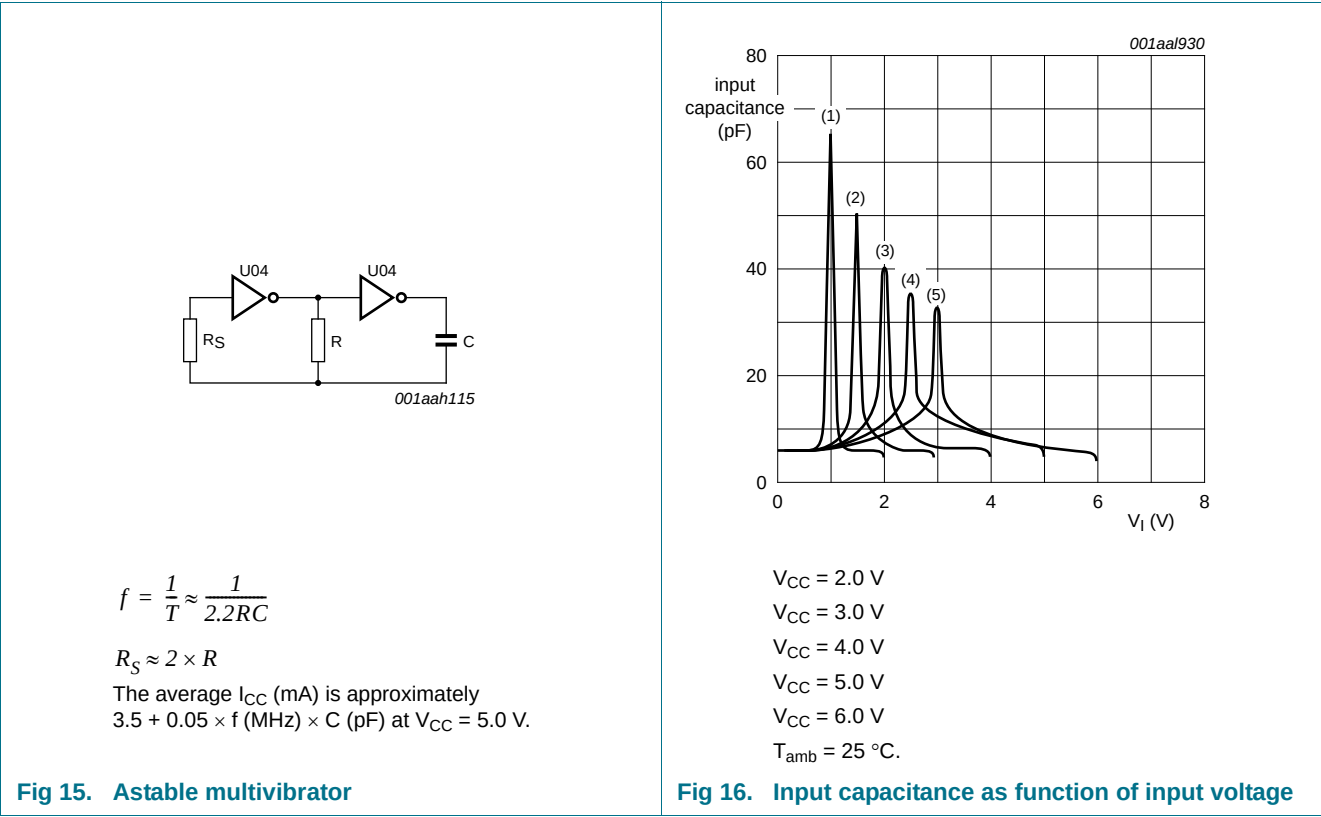
Fig 14. Crystal oscillator configuration

Table 8. External components for resonator (f < 1 MHz)
All values given are typical and must be used as an initial set-up.

Frequency	R1	R2	C1	C2
10 kHz to 15.9 kHz	22 MΩ	220 kΩ	56 pF	20 pF
16 kHz to 24.9 kHz	22 MΩ	220 kΩ	56 pF	10 pF
25 kHz to 54.9 kHz	22 MΩ	100 kΩ	56 pF	10 pF
55 kHz to 129.9 kHz	22 MΩ	100 kΩ	47 pF	5 pF
130 kHz to 199.9 kHz	22 MΩ	47 kΩ	47 pF	5 pF
200 kHz to 349.9 kHz	10 MΩ	47 kΩ	47 pF	5 pF
350 kHz to 600 kHz	10 MΩ	47 kΩ	47 pF	5 pF

Table 9. Optimum value for R2

Frequency	R2	Optimum for
3 kHz	2.0 kΩ	minimum required I _{CC}
	8.0 kΩ	minimum influence due to change in V _{CC}
6 kHz	1.0 kΩ	minimum required I _{CC}
	4.7 kΩ	minimum influence by V _{CC}
10 kHz	0.5 kΩ	minimum required I _{CC}
	2.0 kΩ	minimum influence by V _{CC}
14 kHz	0.5 kΩ	minimum required I _{CC}
	1.0 kΩ	minimum influence by V _{CC}
>14 kHz	-	replace R2 by C3 with a typical value of 35 pF



14. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

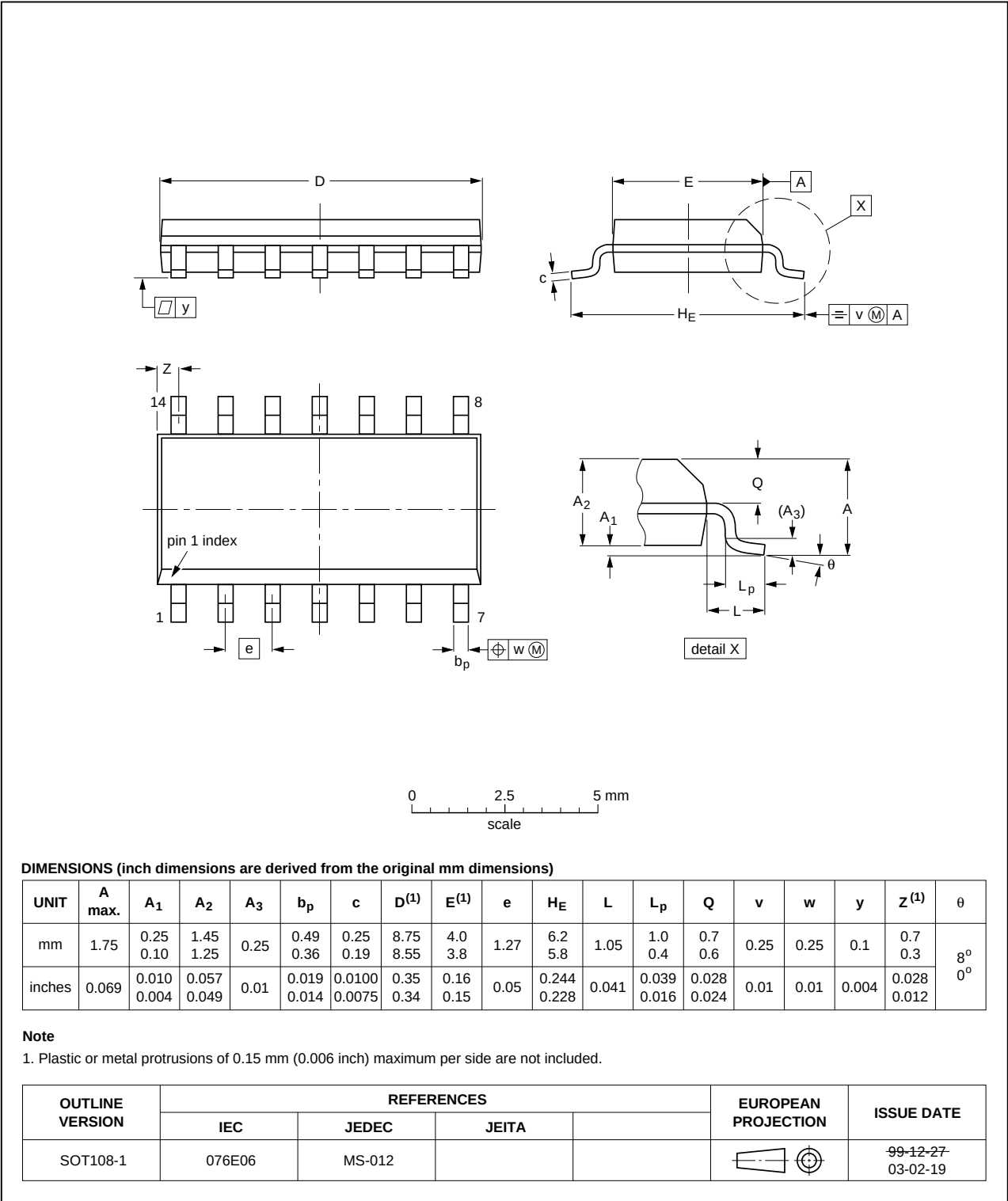


Fig 17. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

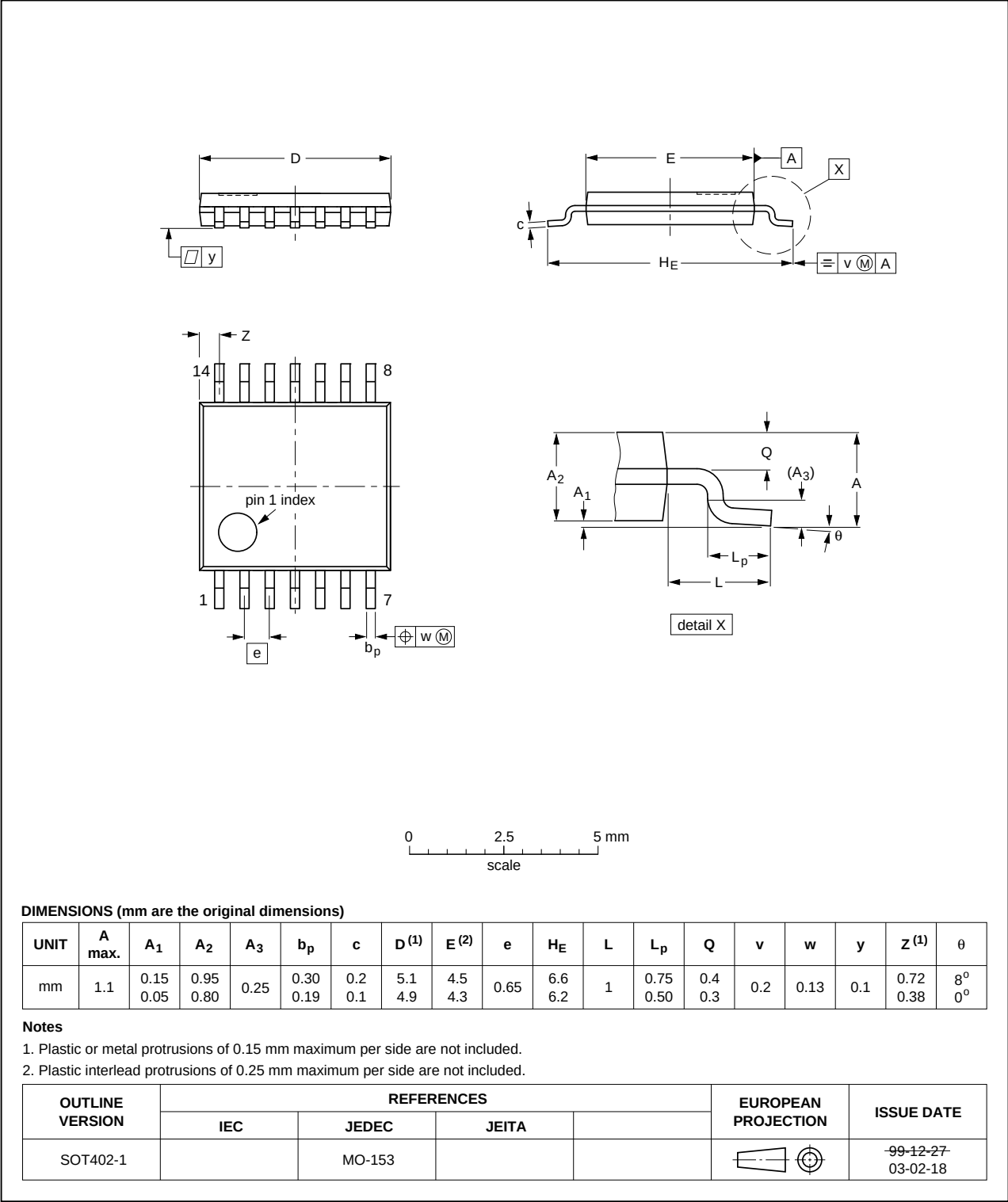
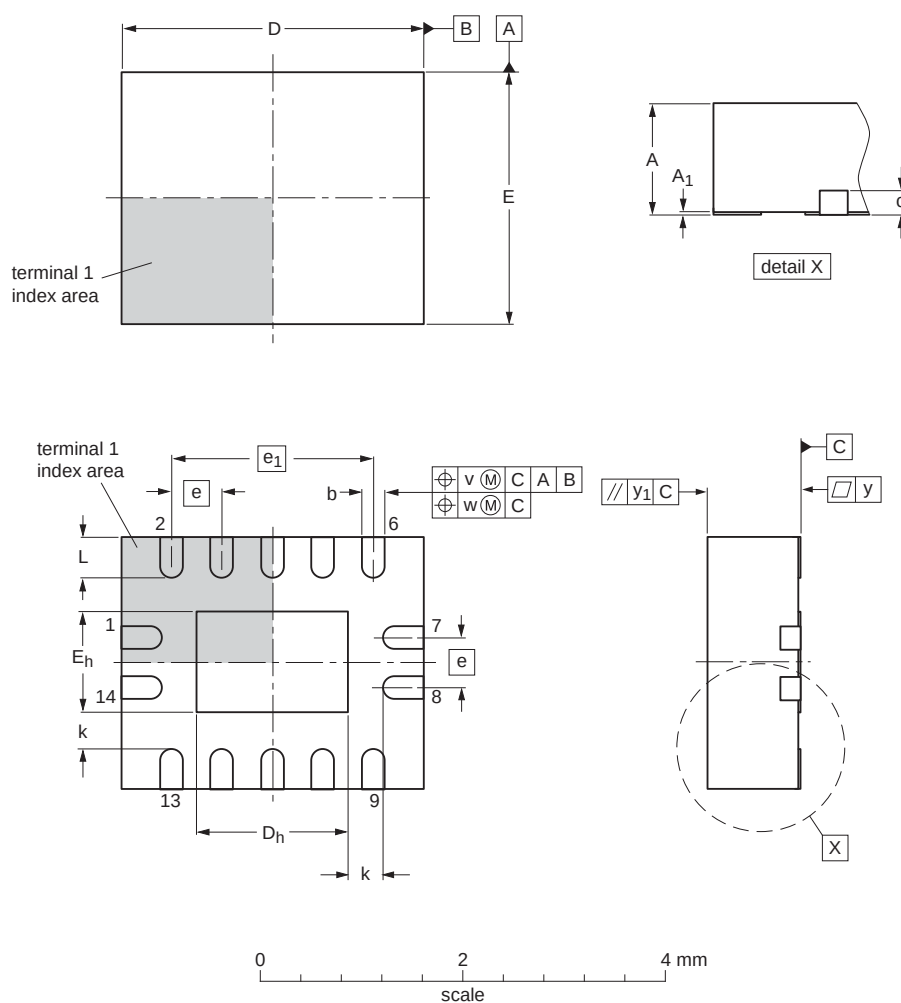


Fig 18. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1



Dimensions (mm are the original dimensions)

Unit		A ⁽¹⁾	A ₁	b	c	D ⁽¹⁾	D _h	E ⁽¹⁾	E _h	e	e ₁	k	L	v	w	y	y ₁
mm	max	1	0.05	0.30	0.2	3.1	1.65	2.6	1.15	0.5	2		0.5	0.1	0.05	0.05	0.1
	nom		0.02	0.25		3.0	1.50	2.5	1.00				0.4				
	min		0.00	0.18		2.9	1.35	2.4	0.85				0.3				

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot762-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT762-1		MO-241				15-04-10 15-05-05

Fig 19. Package outline SOT762-1 (DHVQFN14)

15. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
LSTTL	Low-power Schottky Transistor-Transistor Logic
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
MIL	Military
TTL	Transistor-Transistor Logic

16. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HCU04_Q100 v.2	20151022	Product data sheet	-	74HCU04_Q100 v.1
Modifications:	• Conditions V_{IL} and V_{IH} corrected (errata).			
74HCU04_Q100 v.1	20130131	Product data sheet	-	-

17. Legal information

17.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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