

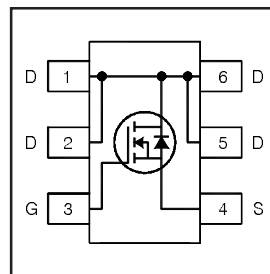
Applications

- High frequency DC-DC converters

V_{DSS}	R_{DS(on)} max	I_D
200V	2.2Ω	0.6A

Benefits

- Low Gate to Drain Charge to Reduce Switching Losses
- Fully Characterized Capacitance Including Effective C_{OSS} to Simplify Design, (See App. Note AN1001)
- Fully Characterized Avalanche Voltage and Current
- Lead-Free
- Halogen-Free



Absolute Maximum Ratings

	Parameter	Max.	Units
I _D @ T _A = 25°C	Continuous Drain Current, V _{GS} @ 10V	0.6	A
I _D @ T _A = 70°C	Continuous Drain Current, V _{GS} @ 10V	0.48	
I _{DM}	Pulsed Drain Current ①	4.8	
P _D @ T _A = 25°C	Power Dissipation	2.0	W
	Linear Derating Factor	0.016	W/°C
V _{GS}	Gate-to-Source Voltage	± 30	V
dv/dt	Peak Diode Recovery dv/dt ②	9.6	V/ns
T _J	Operating Junction and	-55 to + 150	°C
T _{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
R _{θJA}	Junction-to-Ambient ④	—	62.5	°C/W

Notes ① through ⑥ are on page 8
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Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	200	—	—	V	V _{GS} = 0V, I _D = 250μA
ΔV _{(BR)DSS/ΔT_J}	Breakdown Voltage Temp. Coefficient	—	0.26	—	V/°C	Reference to 25°C, I _D = 1mA ③
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	—	2.2	Ω	V _{GS} = 10V, I _D = 0.36A ③
V _{GS(th)}	Gate Threshold Voltage	3.0	—	5.5	V	V _{DS} = V _{GS} , I _D = 250μA
I _{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	V _{DS} = 200V, V _{GS} = 0V
		—	—	250		V _{DS} = 160V, V _{GS} = 0V, T _J = 150°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V _{GS} = 30V
	Gate-to-Source Reverse Leakage	—	—	-100		V _{GS} = -30V

Dynamic @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
g _{fs}	Forward Transconductance	0.44	—	—	S	V _{DS} = 50V, I _D = 0.36A
Q _g	Total Gate Charge	—	3.9	—	nC	I _D = 0.36A V _{DS} = 160V V _{GS} = 10V
Q _{gs}	Gate-to-Source Charge	—	0.8	—		
Q _{gd}	Gate-to-Drain ("Miller") Charge	—	2.2	—		
t _{d(on)}	Turn-On Delay Time	—	6.5	—	ns	V _{DD} = 100V I _D = 0.36A R _G = 53Ω V _{GS} = 10V ③
t _r	Rise Time	—	8.0	—		
t _{d(off)}	Turn-Off Delay Time	—	8.8	—		
t _f	Fall Time	—	19	—		
C _{iss}	Input Capacitance	—	88	—	pF	V _{GS} = 0V V _{DS} = 25V f = 1.0MHz
C _{oss}	Output Capacitance	—	18	—		
C _{rss}	Reverse Transfer Capacitance	—	6.3	—		
C _{oss}	Output Capacitance	—	102	—		
C _{oss}	Output Capacitance	—	8.4	—		
C _{oss eff.}	Effective Output Capacitance	—	26	—		

Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E _{AS}	Single Pulse Avalanche Energy②	—	9.9	mJ
I _{AR}	Avalanche Current①	—	0.6	A

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	1.8	A	MOSFET symbol showing the integral reverse p-n junction diode.
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	4.8		
V _{SD}	Diode Forward Voltage	—	—	1.3	V	T _J = 25°C, I _S = 0.36A, V _{GS} = 0V ③
t _{rr}	Reverse Recovery Time	—	45	—	ns	T _J = 25°C, I _F = 0.36A
Q _{rr}	Reverse Recovery Charge	—	54	—	nC	di/dt = 100A/μs ③

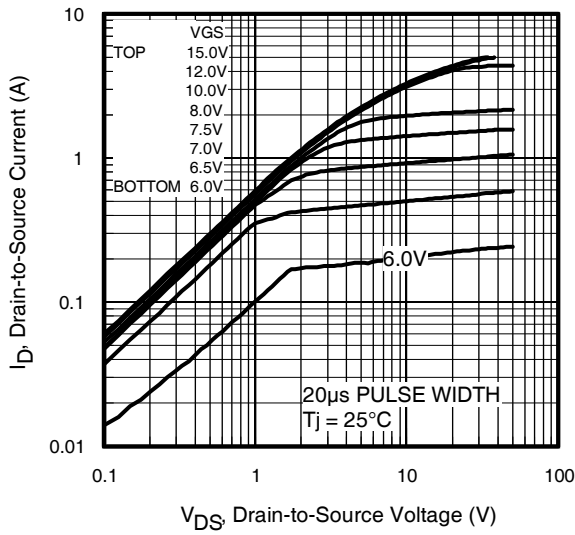


Fig 1. Typical Output Characteristics

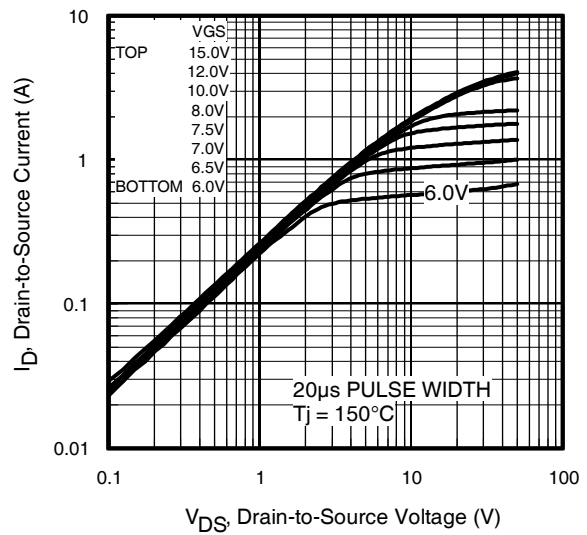


Fig 2. Typical Output Characteristics

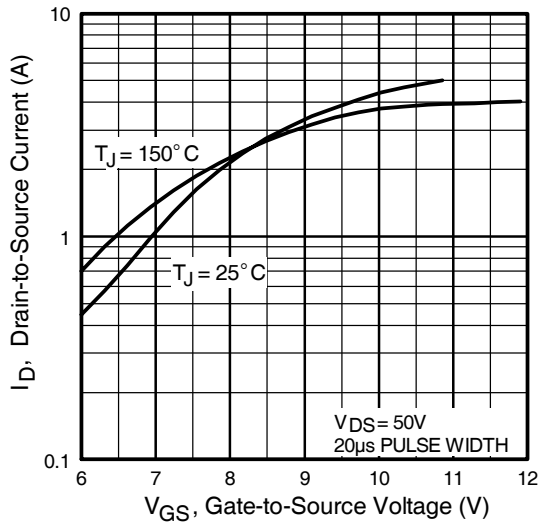


Fig 3. Typical Transfer Characteristics

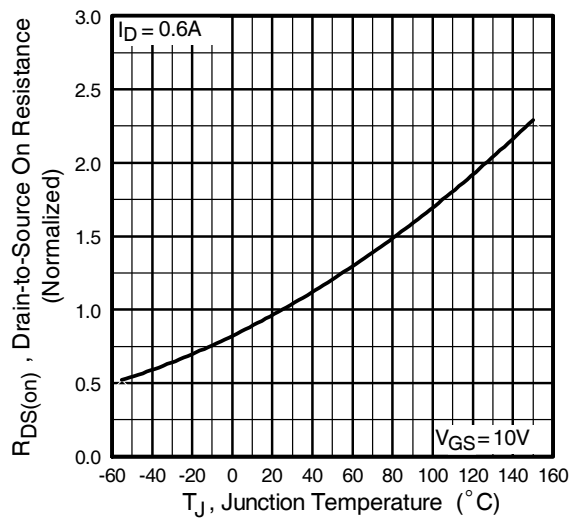


Fig 4. Normalized On-Resistance Vs. Temperature

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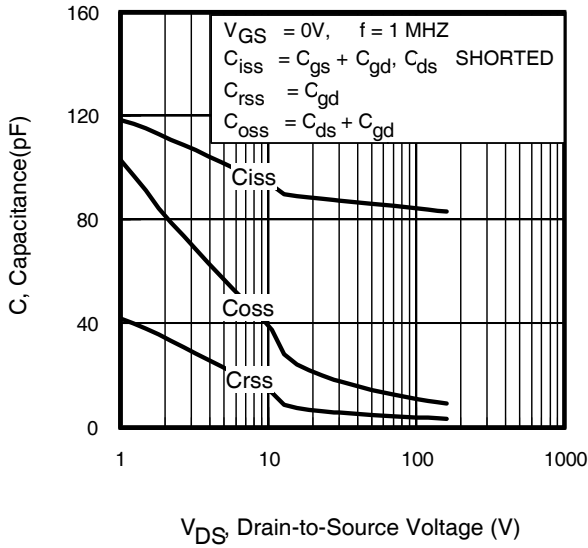


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

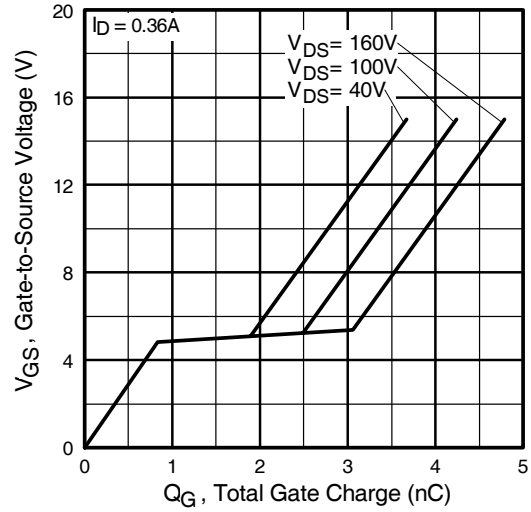


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

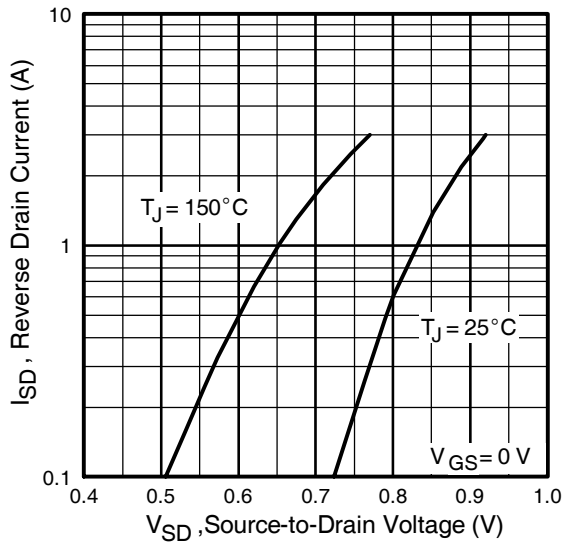


Fig 7. Typical Source-Drain Diode Forward Voltage

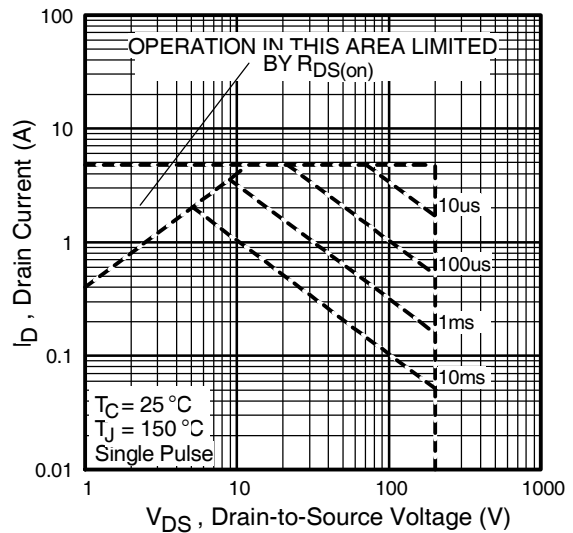


Fig 8. Maximum Safe Operating Area

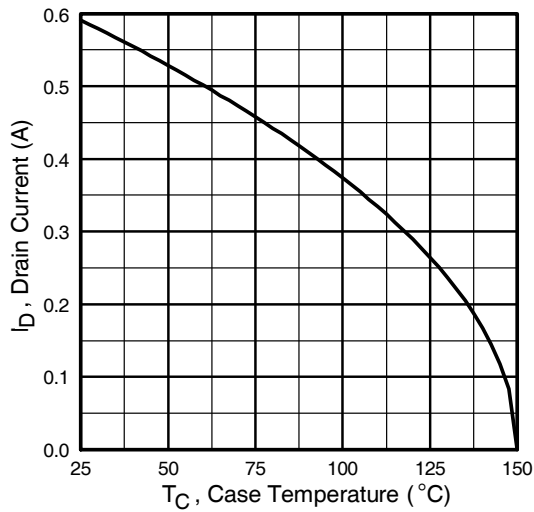


Fig 9. Maximum Drain Current Vs. Case Temperature

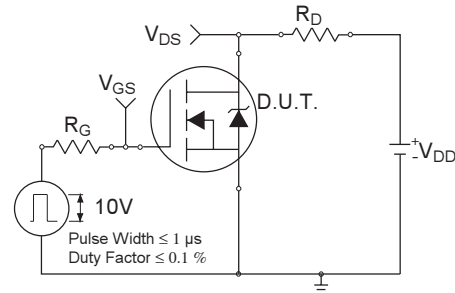


Fig 10a. Switching Time Test Circuit

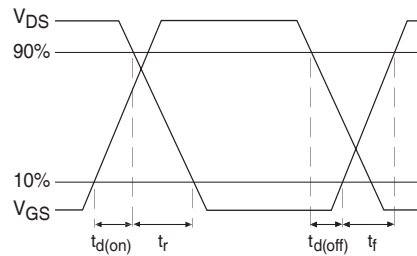


Fig 10b. Switching Time Waveforms

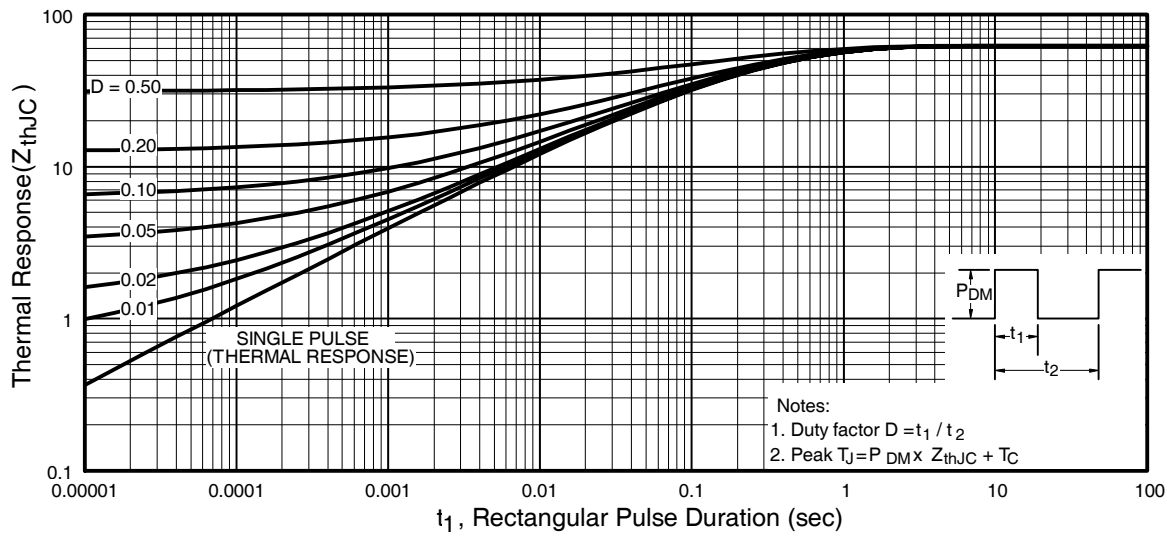


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

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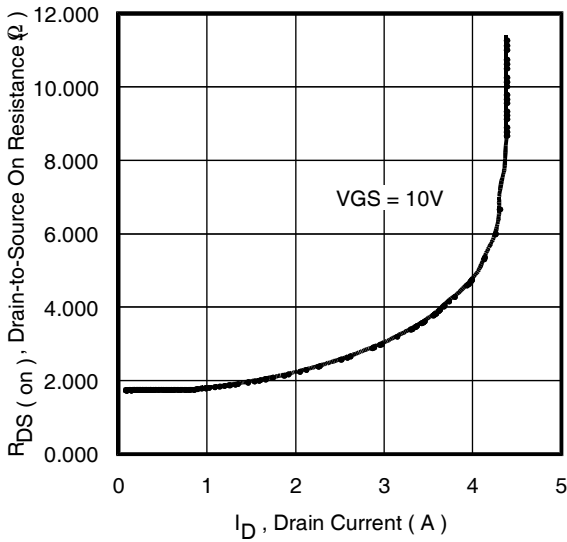


Fig 12. On-Resistance Vs. Drain Current

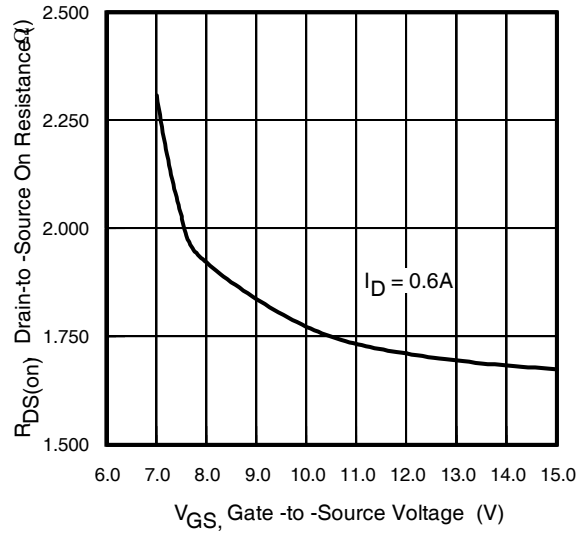


Fig 13. On-Resistance Vs. Gate Voltage

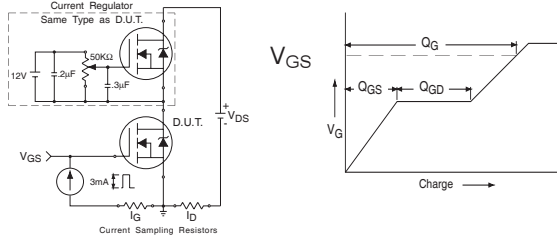


Fig 14a&b. Basic Gate Charge Test Circuit and Waveform

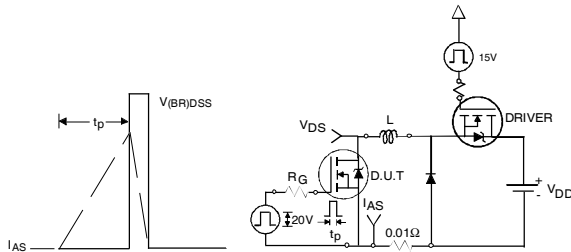


Fig 15a&b. Unclamped Inductive Test circuit and Waveforms

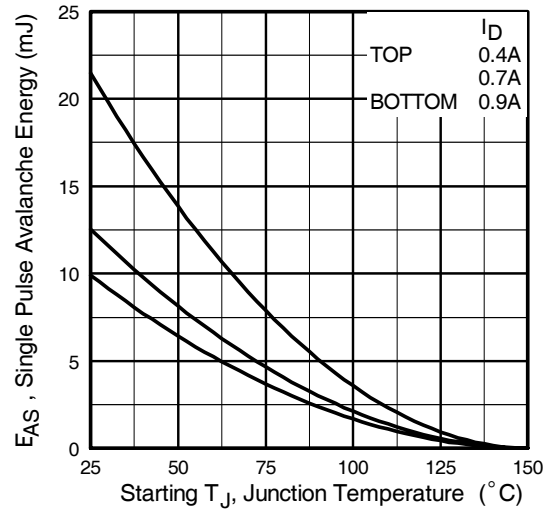
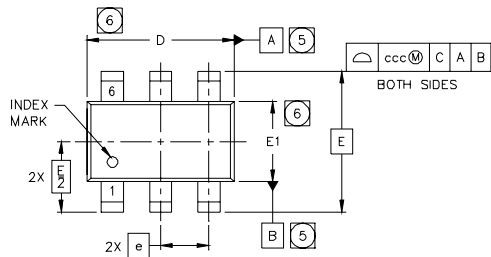
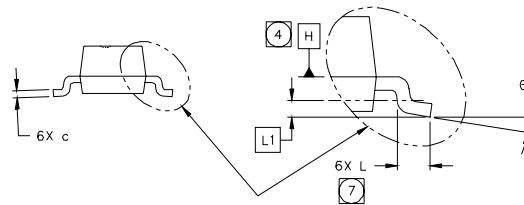
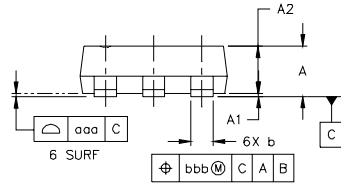


Fig 15c. Maximum Avalanche Energy Vs. Drain Current

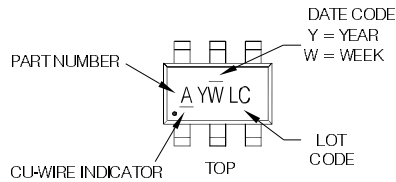
TSOP-6 Package Outline



SYMBOL	MO-193AA DIMENSIONS					
	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.10	---	---	.0433
A1	0.01	---	0.10	.0004	---	.0039
A2	0.80	0.90	1.00	.0315	.0354	.0393
b	0.25	---	0.50	.0099	---	.0196
c	0.10	---	0.26	.004	---	.010
D	2.90	3.00	3.10	.115	.118	.122
E	2.75 BSC			.108 BSC		
E1	1.30	1.50	1.70	.052	.059	.066
e	1.00 BSC			.039 BSC		
L	0.20	0.40	0.60	.0079	.0157	.0236
L1	0.30 BSC			.0118 BSC		
θ	0°	---	8°	0°	---	8°
aaa	0.10			.004		
bbb	0.15			.006		
ccc	0.25			.010		



TSOP-6 Part Marking Information



PART NUMBER CODE REFERENCE:

- A = SI3443DV K = IRF5810
- B = IRF5800 L = IRF5804
- C = IRF5850 M = IRF5803
- D = IRF5851 N = IRF5802
- E = IRF5852
- F = IRF5801
- I = IRF5805
- J = IRF5806

Notes:

- A line above the work week (as shown here) indicates Lead-Free
- A line below the part number (as shown here) indicates Cu-wire

W = (1-26) IF PRECEDED BY LAST DIGIT OF CALENDAR YEAR

YEAR	Y	WORK WEEK	W
2001	1	01	A
2002	2	02	B
2003	3	03	C
2004	4	04	D
2005	5		
2006	6		
2007	7		
2008	8		
2009	9		
2010	0	24	X
		25	Y
		26	Z

W = (27-52) IF PRECEDED BY A LETTER

YEAR	Y	WORK WEEK	W
2001	A	27	A
2002	B	28	B
2003	C	29	C
2004	D	30	D
2005	E		
2006	F		
2007	G		
2008	H		
2009	J		
2010	K	50	X
		51	Y
		52	Z

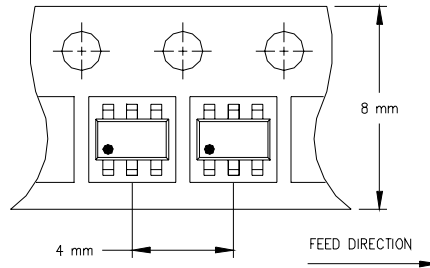
Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

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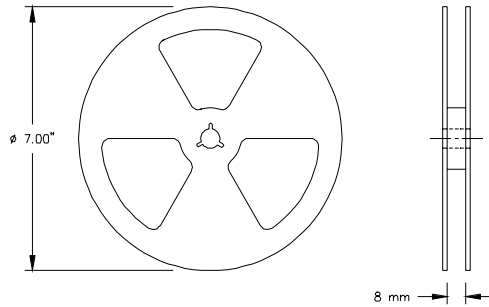
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TSOP-6 Tape & Reel Information



NOTES:

1. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES:

1. OUTLINE CONFORMS TO EIA-481 & EIA-541.

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting $T_J = 25^\circ\text{C}$, $L = 27\text{mH}$
 $R_G = 25\Omega$, $I_{AS} = 0.36\text{A}$.
- ③ Pulse width $\leq 400\mu\text{s}$; duty cycle $\leq 2\%$.
- ④ When mounted on 1 inch square copper board, $t < 10\text{sec}$.
- ⑤ C_{OSS} eff. is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑥ $I_{SD} \leq 0.36\text{A}$, $di/dt \leq 93\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 150^\circ\text{C}$.

Data and specifications subject to change without notice.
This product has been designed and qualified for the Consumer market.
Qualification Standards can be found on IR's Web site.

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