KAF-6303

3072 (H) x 2048 (V) Full Frame CCD Image Sensor

ON Semiconductor®

www.onsemi.com

Description

The KAF−6303 Image Sensor is a high performance CCD (charge-coupled device) with 3072 (H) × 2048 (V) photo active pixels designed for a wide range of image sensing applications.

The sensor incorporates true two-phase CCD technology, simplifying the support circuits required to drive the sensor as well as reducing dark current without compromising charge capacity. The sensor also utilizes the TRUESENSE Transparent Gate Electrode to improve sensitivity compared to the use of a standard front side illuminated polysilicon electrode.

Table 1. GENERAL SPECIFICATIONS

Parameter	Typical Value
Architecture	Full Frame CCD
Total Number of Pixels	3088 (H) × 2056 (V)
Number of Active Pixels	3072 (H) × 2048 (V) = approx. 6.3 Mp
Pixel Size	9 μm (H) × 9 μm (V)
Active Image Size	27.65 mm (H) × 18.48 mm (V) 33.4 mm (Diagonal) APS−H Optical Format
Chip Size	29.0 mm (H) × 19.1 mm (V)
Saturation Signal	100,000 e^-
Output Sensitivity	10 μV/e^-
Quantum Efficiency (450, 550, 650 mm)	40%, 52%, 65%
Readout Noise (10 MHz)	15 e^- rms
Dark Current (Accumulation Mode)	< 10 pA/cm^2
Dark Current Doubling Rate	6°C
Dynamic Range (Saturation Signal/Dark Noise)	76 dB
Maximum Date Rate	10 MHz
Package	CERDIP Package (Sidebrazed)
Cover Glass	Clear or AR Coated, 2 Sides

NOTE: Parameters above are specified at T = 25°C unless otherwise noted.

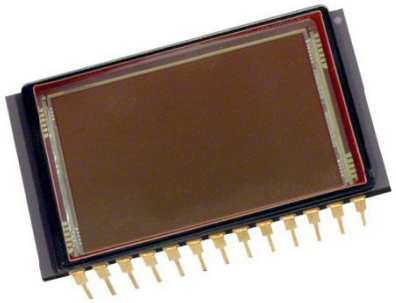


Figure 1. KAF−6303 Full Frame CCD Image Sensor

Features

- True Two Phase Full Frame Architecture
- TRUESENSE Transparent Gate Electrode for High Sensitivity
- 100% Fill Factor
- Low Dark Current

Applications

- Medical Imaging
- Scientific Imaging

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

ORDERING INFORMATION

Table 2. ORDERING INFORMATION − KAF−6303 IMAGE SENSOR

Part Number	Description	Marking Code
KAF−6303−AAA−CD−B2	Monochrome, No Microlens, CERDIP Package (Sidebrazed), Clear Cover Glass with AR Coating (Both Sides), Grade 2	KAF−6303−AAA Serial Number
KAF−6303−AAA−CD−AE	Monochrome, No Microlens, CERDIP Package (Sidebrazed), Clear Cover Glass with AR Coating (Both Sides), Engineering Sample	
KAF−6303−AAA−CP−B2	Monochrome, No Microlens, CERDIP Package (Sidebrazed), Taped Clear Cover Glass (No Coatings), Grade 2	
KAF−6303−AAA−CP−AE	Monochrome, No Microlens, CERDIP Package (Sidebrazed), Taped Clear Cover Glass (No Coatings), Engineering Sample	

Table 3. ORDERING INFORMATION − EVALUATION SUPPORT

Part Number	Description
KAF−6303−12−5−A−EVK	Evaluation Board (Complete Kit)

See the ON Semiconductor *Device Nomenclature* document (TND310/D) for a full description of the naming convention used for image sensors. For reference documentation, including information on evaluation kits, please visit our web site at www.onsemi.com.

DEVICE DESCRIPTION

Architecture

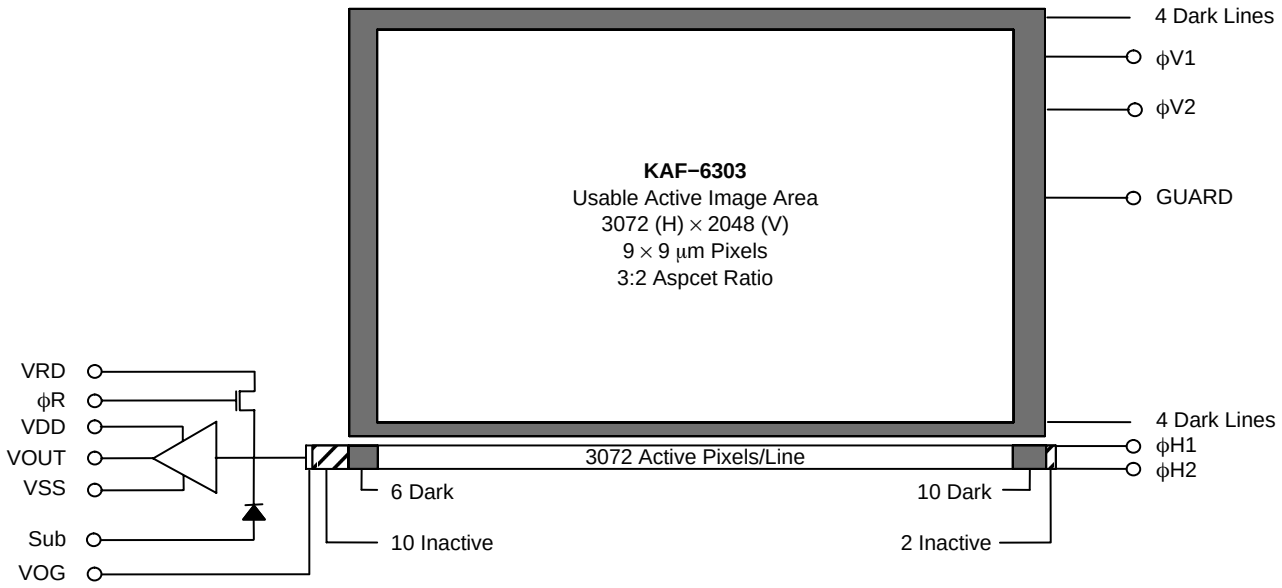


Figure 2. Block Diagram

The sensor consists of 3,088 parallel (vertical) CCD shift registers each 2,056 elements long. These registers act as both the photosensitive elements and as the transport circuits that allow the image to be sequentially read out of the sensor. The elements of these registers are arranged into a 3,072 × 2,048 photosensitive array surrounded by a light shielded dark reference of 16 columns and 8 rows. The parallel (vertical) CCD registers transfer the image one line at a time into a single 3,100 element (horizontal) CCD shift register. The horizontal register transfers the charge to a single output amplifier. The output amplifier is a two-stage source follower that converts the photo-generated charge to a voltage for each pixel.

Dark Reference Pixels

Surrounding the peripheral of the device is a border of light shielded pixels. This includes 6 leading and 10 trailing pixels on every line excluding dummy pixels. There are also 4 full dark lines at the start of every frame and 4 full dark lines at the end of each frame. Under normal circumstances, these pixels do not respond to light. However, dark reference pixels in close proximity to an active pixel, or the outer bounds of the chip (including the first two lines out), can scavenge signal depending on light intensity and wavelength and therefore will not represent the true dark signal.

Dummy Pixels

Within the horizontal shift register are 10 leading and 2 trailing additional shift phases that are not associated with a column of pixels from the vertical register. These pixels contain only horizontal shift register dark current signal and do not respond to light. A few leading dummy pixels may scavenge false signal depending on operating conditions.

Image Acquisition

An electronic representation of an image is formed when incident photons falling on the sensor plane create electron-hole pairs within the sensor. These photon-induced electrons are collected locally by the formation of potential wells at each photogate or pixel site. The number of electrons collected is linearly dependent on light level and exposure time and non-linearly dependent on wavelength. When the pixel's capacity is reached, excess electrons will leak into the adjacent pixels within the same column. This is termed blooming. During the integration period, the ϕV1 and ϕV2 register clocks are held at a constant (low) level. See Figure 8.

Charge Transport

Referring again to Figure 8, the integrated charge from each photogate is transported to the output using a two-step process. Each line (row) of charge is first transported from the vertical CCD's to the horizontal CCD register using the ϕV1 and ϕV2 register clocks. The horizontal CCD is presented a new line on the falling edge of ϕV2 while ϕH1 is held high. The horizontal CCD's then transport each line, pixel by pixel, to the output structure by alternately clocking the ϕH1 and ϕH2 pins in a complementary fashion. On each falling edge of ϕH2, a new charge packet is transferred onto a floating diffusion and sensed by the output amplifier.

Horizontal Register

Output Structure

Charge presented to the floating diffusion (FD) is converted into a voltage and current amplified in order to drive off-chip loads. The resulting voltage change seen at the output is linearly related to the amount of charge placed on FD. Once the signal has been sampled by the system electronics, the reset gate (ϕR) is clocked to remove the signal and FD is reset to the potential applied by VRD. More signal at the floating diffusion reduces the voltage seen at the output pin. In order to activate the output structure, an off-chip load must be added to the VOUT pin of the device. See Figure 3.

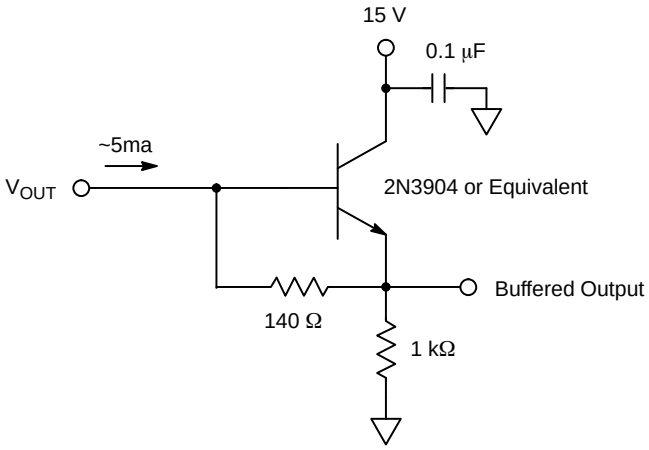


Figure 3. Typical Output Structure Load Diagram

Physical Description

Pin Description and Device Orientation

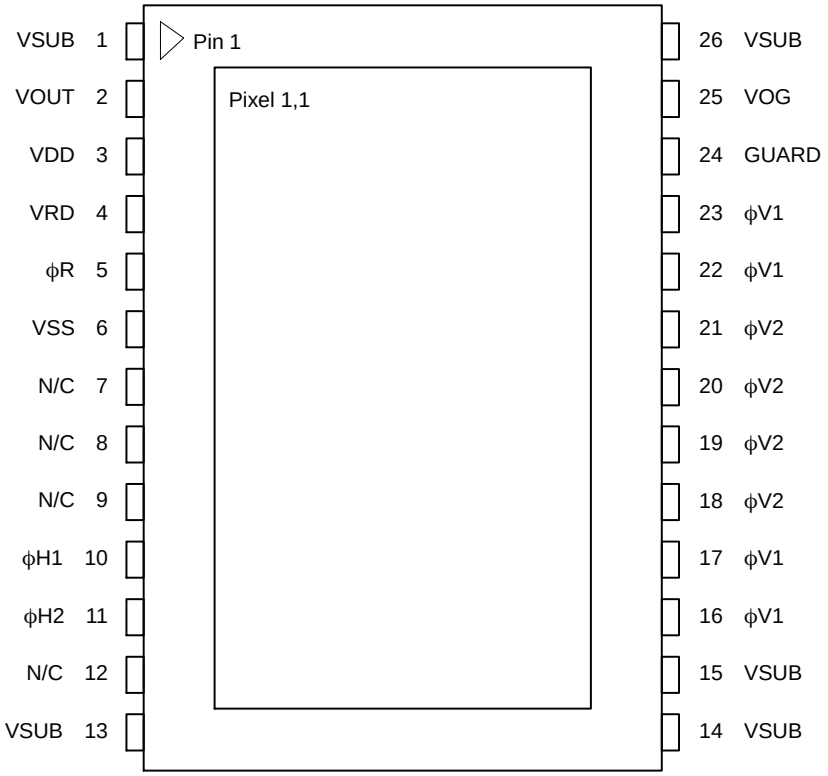


Figure 4. Pinout Diagram

NOTE: The KAF−1603 is mechanically the same and electrically identical to the KAF−0402 sensor. It is also mechanically the same as the KAF−0261 and KAF−3200 sensors. There are some electrical differences since the KAF−0261 has two outputs and two additional clock inputs. The KAF−3200 requires that pin 11 be a “No connect” and be electrically floating. Refer to their specifications for details.

Table 4. PIN DESCRIPTION

Pin	Name	Description
1	VSUB	Substrate (Ground)
2	VOUT	Video Output
3	VDD	Amplifier Supply
4	VRD	Reset Drain
5	ϕR	Reset Clock
6	VSS	Amplifier Supply Return
7	N/C	No Connection (Open Pin)
8	N/C	No Connection (Open Pin)
9	N/C	No Connection (Open Pin)
10	ϕH1	Horizontal CCD Clock − Phase 1
11	ϕH2	Horizontal CCD Clock − Phase 2
12	N/C	No Connection (Open Pin)
13	VSUB	Substrate (Ground)

Pin	Name	Description
14	VSUB	Substrate (Ground)
15	VSUB	Substrate (Ground)
16	ϕV1	Vertical CCD Clock − Phase 1
17	ϕV1	Vertical CCD Clock − Phase 1
18	ϕV2	Vertical CCD Clock − Phase 2
19	ϕV2	Vertical CCD Clock − Phase 2
20	ϕV2	Vertical CCD Clock − Phase 2
21	ϕV2	Vertical CCD Clock − Phase 2
22	ϕV1	Vertical CCD Clock − Phase 1
23	ϕV1	Vertical CCD Clock − Phase 1
24	GUARD	Guard Ring
25	VOG	Output Gate
26	VSUB	Substrate (Ground)

IMAGING PERFORMANCE

Table 5. SPECIFICATIONS

(All values measured at 25°C, and nominal operating conditions. These parameters exclude defective pixels.)

Description	Symbol	Min.	Nom.	Max.	Unit	Notes	Verification Plan
Saturation Signal Vertical CCD Capacity Horizontal CCD Capacity Output Node Capacity	N_{SAT}	 85,000 170,000 190,000	 100,000 200,000 220,000	 120,000 240,000 240,000	e^-/Pixel	1	Design[11]
Quantum Efficiency Red Green Blue	 R_R R_G R_B	 52 42 30	 65 52 40	 75 62 48	%QE		Design[11]
Photoresponse Non-Linearity	PRNL	−	1.0	2.0	%	2	Design[11]
Photoresponse Non-Uniformity	PRNU	−	1.0	3.0	%	3	Die[10]
Dark Signal	J_{DARK}	− −	15 3.5	50 10	e^-/Pix/Sec pA/cm^2	4	Die[10]
Dark Signal Doubling Temperature		5.0	6.3	7.5	°C		Design[11]
Dark Signal Non-Uniformity	DSNU	−	10	50	e^-/Pix/Sec	5	Die[10]
Dynamic Range	DR	70	76	−	dB	6	Design[11]
Charge Transfer Efficiency	CTE	0.99997	0.99999	−			Die[10]
Output Amplifier DC Offset	V_{ODC}	9.5	10.5	11.5	V	7	Die[10]
Output Amplifier Bandwidth	f_{-3dB}	−	45	−	MHz	8	Design[11]
Output Amplifier Sensitivity	V_{OUT}/N_{e^-}	9	10	11	μV/e^-		Design[11]
Output Amplifier Output Impedance	Z_{OUT}	175	200	2,520	Ω		Design[11]
Noise Floor	n_{e^-}	−	15	20	e^-	9	Die[10]

1. For pixel binning applications, electron capacity up to 330,000 can be achieved with modified CCD inputs. Each sensor may have to be optimized individually for these applications. Some performance parameters may be compromised to achieve the largest signals.
2. Worst-case deviation from straight line fit, between 1% and 90% of V_{SAT}.
3. One Sigma deviation of a 128 × 128 sample when CCD illuminated uniformly.
4. Average of all pixels with no illumination at 25°C.
5. Average dark signal of any of 12 × 8 blocks within the sensor (each block is 128 × 128 pixels).
6. 20Log (N_{SAT} / n_e-) at nominal operating frequency and 25°C.
7. Video level offset with respect to ground.
8. Last output amplifier stage only. Assumes 10 pF off-chip load.
9. Output noise at 25°C, nominal operating frequency, and t_{INT} = 0.
10. A parameter that is measured on every sensor during production testing.
11. A parameter that is quantified during the design verification activity.

TYPICAL PERFORMANCE CURVES

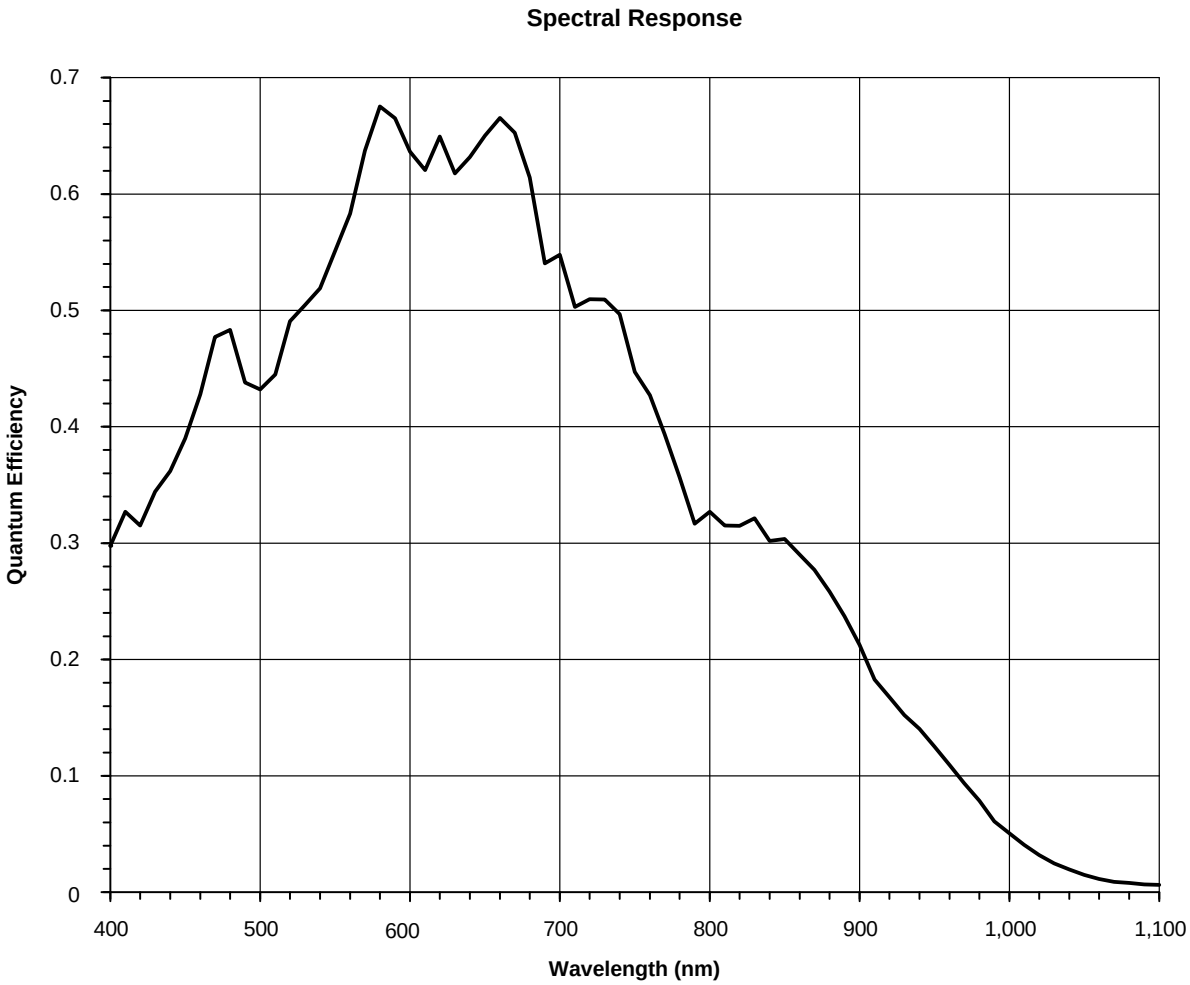


Figure 5. Typical Spectral Response

DEFECT DEFINITIONS

Table 6. SPECIFICATIONS (All tests performed at T = 25°C)

Classification	Point Defect		Cluster Defect		Column Defect	
	Total	Zone A	Total	Zone A	Total	Zone A
C2	≤ 90	≤ 45	≤ 36	≤ 18	0	0

Point Defects

Dark: A pixel which deviates by more than 6% from neighboring pixels when illuminated to 70% of saturation.

Bright: A pixel with a dark current greater than 10,000 e^-/pixel/sec at 25°C.

Cluster Defect

A grouping of not more than 5 adjacent point defects.

Column Defect

A grouping of > 5 contiguous point defects along a single column.

A column containing a pixel with dark current > 30,000 e^-/pix/sec at 25°C (Bright column).

A column that does not meet the CTE specification for all exposures less than the specified Max sat. signal level and greater than 2 ke^-.

A column that loses > 250 e^- under 2 ke^- illumination.

Neighboring Pixels

The surrounding 128 × 128 pixels or ±64 columns/rows.

Defect Separation

Column and cluster defects are separated by no less than two (2) pixels in any direction (excluding single pixel defects).

Defect Region Exclusion

Defect region excludes the outer two (2) rows and columns at each side/end of the sensor.

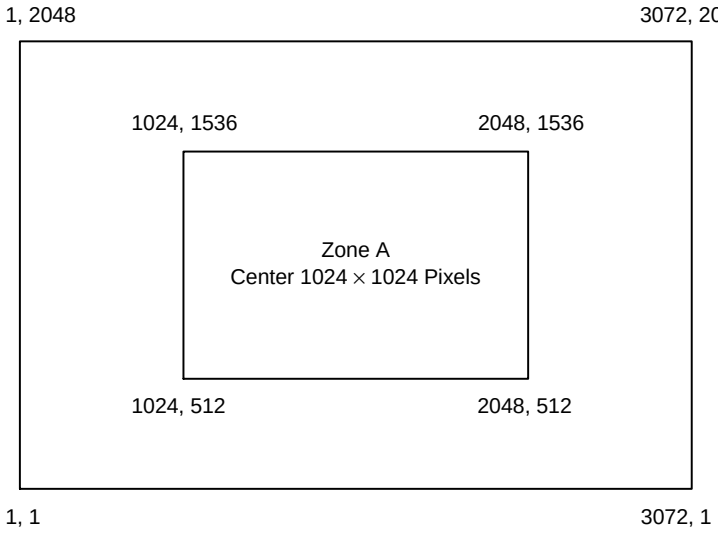


Figure 6. Active Pixel Region

OPERATION

Table 7. ABSOLUTE MAXIMUM RATINGS

Description	Symbol	Minimum	Maximum	Unit	Notes
Diode Pin Voltages	V_{DIODE}	0	20	V	1, 2
Gate Pin Voltages − Type 1	V_{GATE1}	−16	16	V	1, 3
Gate Pin Voltages − Type 2	V_{GATE2}	0	16	V	1, 4
Inter-Gate Voltages	V_{g-g}	−	16	V	5
Output Bias Current	I_{OUT}	−	−10	mA	6
Output Load Capacitance	C_{LOAD}	−	15	pF	6
Storage Temperature	T_{ST}	0	70	°C	
Humidity	RH	5	90	%	7

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Referenced to pin VSUB.
2. Includes pins: VRD, VDD, VSS, VOUT, GUARD.
3. Includes pins: ϕV1, ϕV2, ϕH1, ϕH2.
4. Includes pins: ϕR, VOG.
5. Voltage difference between overlapping gates. Includes: ϕV1 to ϕV2, ϕH1 to ϕH2, ϕV2 to ϕH1, ϕH2 to VOG.
6. Avoid shorting output pins to ground or any low impedance source during operation.
7. T = 25°C. Excessive humidity will degrade MTTF.

Table 8. DC BIAS OPERATING CONDITIONS

Description	Symbol	Minimum	Nominal	Maximum	Unit	Maximum DC Current (mA)	Notes
Reset Drain	V_{RD}	10.5	11.0	11.5	V	0.01	
Output Amplifier Return	V_{SS}	1.5	2.0	2.5	V	0.45	
Output Amplifier Supply	V_{DD}	14.5	15	15.5	V	I_{OUT}	
Substrate	V_{SUB}	0	0	0	V	0.01	
Output Gate	V_{OG}	3.75	4.0	5.0	V	0.01	
Guard Ring	V_{LG}	8.0	10.0	12.0	V	0.01	
Video Output Current	I_{OUT}	−	−5	−10	mA	−	1

1. An output load sink must be applied to VOUT to activate output amplifier − see Figure 3.

AC Operating Conditions

Table 9. CLOCK LEVELS

Description	Symbol	Level	Min.	Nom.	Max.	Unit	Effective Capacitance
Vertical CCD Clock − Phase 1	ϕV1	Low	−10.5	−10	−9.5	V	82 nF (All ϕV1 Pins)
Vertical CCD Clock − Phase 1	ϕV1	High	0.5	1.0	1.5	V	82 nF (All ϕV1 Pins)
Vertical CCD Clock − Phase 2	ϕV2	Low	−10.5	−10.0	−9.5	V	820 nF (All ϕV2 Pins)
Vertical CCD Clock − Phase 2	ϕV2	High	0.5	1.0	1.5	V	820 nF (All ϕV2 Pins)
Horizontal CCD Clock − Phase 1	ϕH1	Low	−6.0	−3.0	−3.0	V	400 pF
Horizontal CCD Clock − Phase 1	ϕH1	High	4.0	7.0	7.0	V	400 pF
Horizontal CCD Clock − Phase 2	ϕH2	Low	−6.0	−3.0	−3.0	V	400 pF
Horizontal CCD Clock − Phase 2	ϕH2	High	4.0	7.0	7.0	V	400 pF
Reset Clock	ϕR	Low	−4.0	−3.0	−2.0	V	10 pF
Reset Clock	ϕR	High	3.5	4.0	5.0	V	10 pF

1. All pins draw less than 10 μA DC current.
2. Capacitance values relative to V_{SUB}.

TIMING

Table 10. REQUIREMENTS AND CHARACTERISTICS

Description	Symbol	Minimum	Nominal	Maximum	Unit	Notes
ϕH1, ϕH2 Clock Frequency	f_H	−	4	15	MHz	1, 2, 3
ϕV1, ϕV2 Clock Frequency	f_V	−	25	50	kHz	1, 2, 3
Pixel Period (1 Count)	t_e	67	250	−	ns	
ϕH1, ϕH2 Set-up Time	$t_{\phi HS}$	0.5	1	−	μs	
ϕV1, ϕV2 Clock Pulse Width	$t_{\phi V}$	10	20	−	μs	2
Reset Clock Pulse Width	$t_{\phi R}$	10	20	−	ns	4
Readout Time	$t_{READOUT}$	531	1,719	−	ms	5
Integration Time	t_{INT}	−	−	−		6
Line Time	t_{LINE}	258.2	836	−	μs	7

1. 50% duty cycle values.
2. CTE may degrade above the nominal frequency.
3. Rise and fall times (10/90% levels) should be limited to 5−10% of clock period. Cross-over of register clocks should be between 40−60% of amplitude.
4. ϕR should be clocked continuously.
5. $t_{READOUT} = (2056 \cdot t_{LINE})$.
6. Integration time (t_{INT}) is user specified. Longer integration times will degrade noise performance.
7. $t_{LINE} = (3 \cdot t_{\phi V}) + t_{\phi HS} + 3100 + t_e$.

Frame Timing

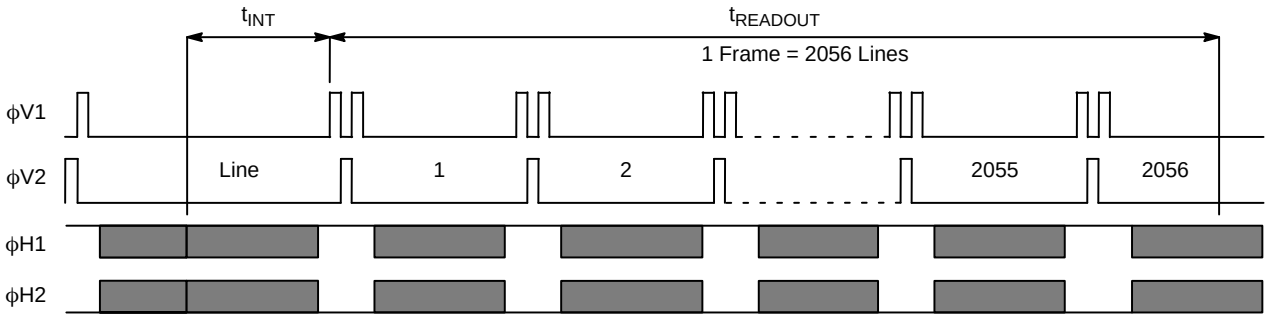
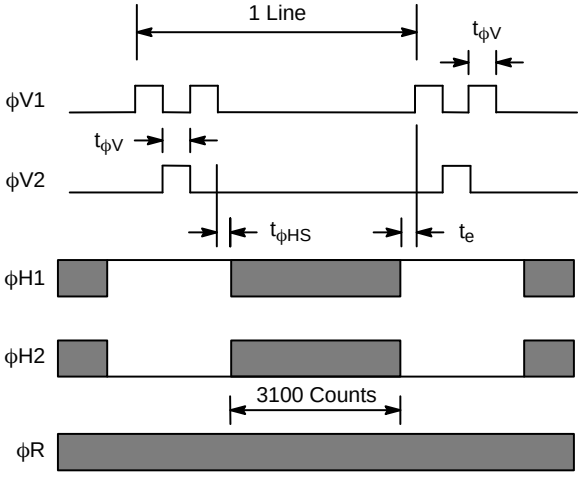


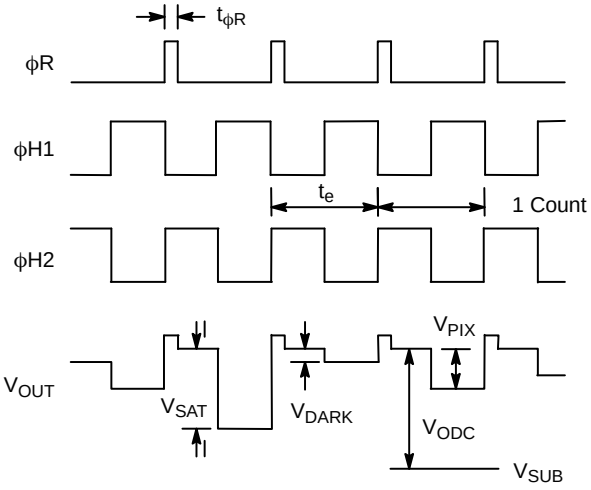
Figure 7. Frame Timing

Line Timing (Each Output)

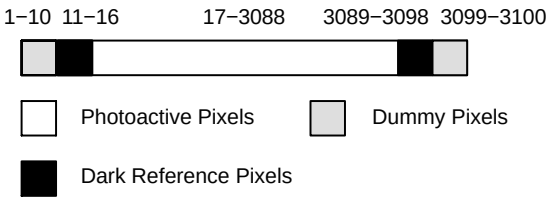
Line Timing Detail



Pixel Timing Detail



Line Content



V_{SAT}	Saturated pixel video output signal
V_{DARK}	Video output signal in no-light situation, not zero due to J_{DARK}
V_{PIX}	Pixel video output signal level, more electrons = more negative*
V_{ODC}	Video level offset with respect to V_{SUB}
V_{SUB}	Analog ground

* See Image Acquisition section (Page 3).

Figure 8. Timing Diagrams

STORAGE AND HANDLING

Table 11. STORAGE CONDITIONS

Description	Symbol	Minimum	Maximum	Unit	Notes
Storage Temperature	T_{ST}	0	70	°C	1
Operating Temperature	T_{OP}	−60	60	°C	

1. Storage toward the maximum temperature will accelerate color filter degradation.

For information on ESD and cover glass care and cleanliness, please download the *Image Sensor Handling and Best Practices* Application Note (AN52561/D) from www.onsemi.com.

For information on soldering recommendations, please download the Soldering and Mounting Techniques Reference Manual (SOLDERRM/D) from www.onsemi.com.

For quality and reliability information, please download the *Quality & Reliability* Handbook (HBD851/D) from www.onsemi.com.

For information on device numbering and ordering codes, please download the *Device Nomenclature* technical note (TND310/D) from www.onsemi.com.

For information on Standard terms and Conditions of Sale, please download Terms and Conditions from www.onsemi.com.

MECHANICAL INFORMATION

Completed Assembly

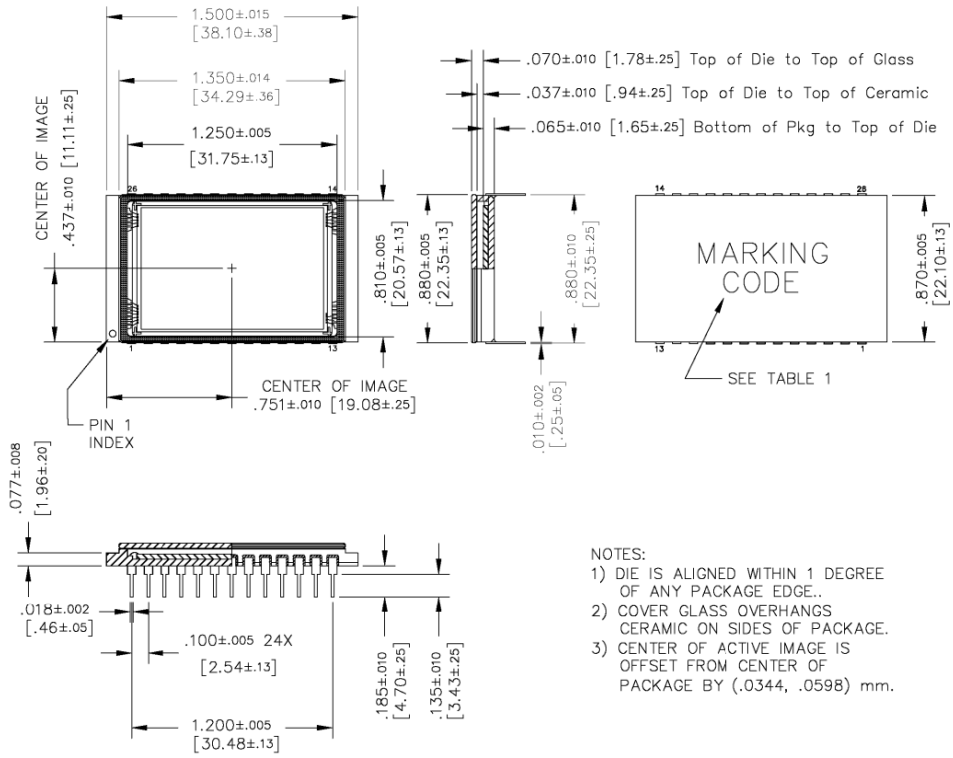


Figure 9. Completed Assembly (1 of 2)

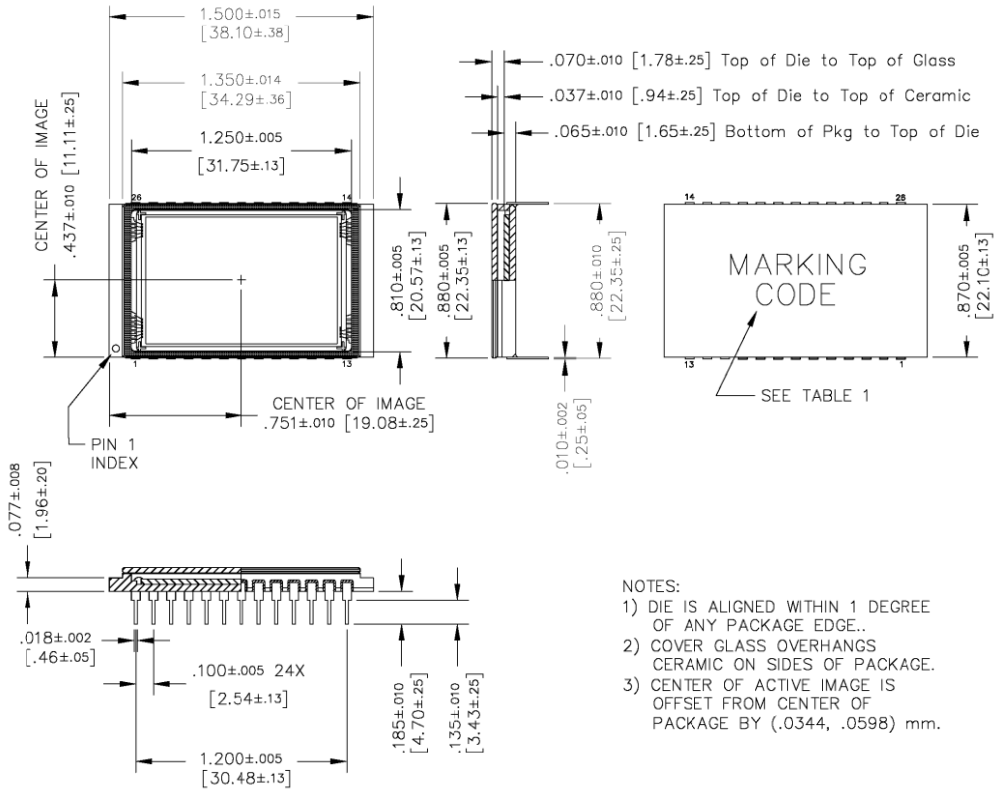


Figure 10. Completed Assembly (2 of 2)

PUBLICATION ORDERING INFORMATION

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Для оперативного оформления запроса Вам необходимо перейти по данной ссылке:

http://moschip.ru/get-element

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