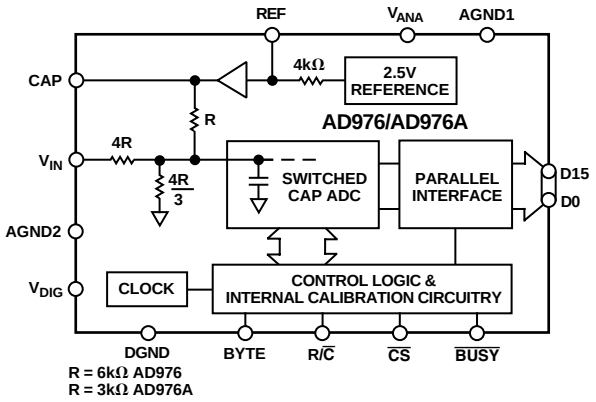
16-Bit, 100 kSPS/200 kSPS BiCMOS A/D Converters

AD976/AD976A

FEATURES
Fast 16-Bit ADC
200 kSPS Throughput – AD976A
100 kSPS Throughput – AD976
Single 5 V Supply Operation
Input Range: ±10 V
100 mW Max Power Dissipation
Choice of External or Internal 2.5 V Reference
High Speed Parallel Interface
On-Chip Clock
28-Lead Skinny DIP, SSOP or SOIC Packages

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD976/AD976A is a high speed, low power 16-bit A/D converter that operates from a single 5 V supply. The part contains a successive approximation, switched capacitor ADC, an internal 2.5 V reference and a high speed parallel interface. The ADC is factory calibrated to minimize all linearity errors. The analog full-scale input is the standard industrial range of ±10 V.

The AD976/AD976A is comprehensively tested for ac parameters such as SNR and THD, as well as the more traditional parameters of offset, gain and linearity.

The AD976/AD976A is fabricated on Analog Devices' proprietary BiCMOS process, which has high performance bipolar devices along with CMOS transistors.

The AD976/AD976A is available in skinny 28-lead DIP, SSOP and SOIC packages.

PRODUCT HIGHLIGHTS

1. Fast Throughput.
   The AD976/AD976A is a high speed (100 kSPS/200 kSPS throughput rates respectively), 16-bit ADC based on a switched capacitor architecture.
2. Single-Supply Operation.
   The AD976/AD976A operates from a single 5 V supply and dissipates only 100 mW max.
3. Comprehensive DC and AC Specifications.
   The AD976/AD976A is factory calibrated and fully tested for SNR and THD as well as the traditional specifications of offset, gain and linearity.
4. Complete A/D Solution.
   The AD976/AD976A offers a highly integrated solution containing an accurate ADC, reference and on-chip clock.

REV. C

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AD976A–SPECIFICATIONS

(–40°C to +85°C, F_S = 200 kHz, Ref = Internal Reference, V_{DIG} = V_{ANA} = +5 V unless otherwise noted)

Parameter	AD976AA Min	AD976AA Typ	AD976AA Max	AD976AB Min	AD976AB Typ	AD976AB Max	AD976AC Min	AD976AC Typ	AD976AC Max	Units
RESOLUTION	16			16			16			Bits
ANALOG INPUT										
Voltage Range		±10			±10			±10		V
Impedance		13			13			13		kΩ
Capacitance		22			22			22		pF
THROUGHPUT SPEED										
Complete Cycle			5			5			5	µs
Throughput Rate	200			200			200			kHz
DC ACCURACY										
Integral Linearity Error			±3			±2		±3		LSB[1]
Differential Linearity Error	–2		+3	–1		+1.75		±2		LSB
No Missing Codes	15			16				15		Bit
Transition Noise[2]		1.0			1.0			1.0		LSB
Full-Scale Error[3, 4]			±0.5			±0.25			±0.5	%
Full-Scale Error Drift		±7			±7			±7		ppm/°C
Full-Scale Error, Ext. REF = 2.5 V			±0.5			±0.25			±0.5	%
Full-Scale Error Drift, Ext. REF = 2.5 V		±2			±2			±2		ppm/°C
Bipolar Zero Error[4]			±10			±10			±15	mV
Bipolar Zero Error Drift		±2			±2			±2		ppm/°C
Power Supply Sensitivity										
V_{ANA} = V_{DIG} = V_D = 5 V ± 5%			±8			±8			±8	LSB
AC ACCURACY										
Spurious Free Dynamic Range[5]	90			96			90			dB[6]
Total Harmonic Distortion[5]			–90			–96			–90	dB
Signal to (Noise + Distortion)[5]	83			85			83			dB
–60 dB Input		27			28			27		dB
Signal to Noise[5]	83			85			83			dB
Full-Power Bandwidth[7]		1			1			1		MHz
Input Bandwidth		2.7			2.7			2.7		MHz
SAMPLING DYNAMICS										
Aperture Delay		40			40			40		ns
Transient Response										
Full-Scale Step			1			1			1	µs
Overvoltage Recovery[8]		150			150			150		ns
REFERENCE										
Internal Reference Voltage	2.48	2.5	2.52	2.48	2.5	2.52	2.48	2.5	2.52	V
Internal Reference Source Current		1			1			1		µA
External Reference Voltage Range for Specified Linearity	2.3	2.5	2.7	2.3	2.5	2.7	2.3	2.5	2.7	V
External Reference Current Drain Ext. REF = 2.5 V			100			100			100	µA
DIGITAL INPUTS										
Logic Levels										
V_{IL}	–0.3		+0.8	–0.3		+0.8	–0.3		+0.8	V
V_{IH}	+2.0		V_{DIG} + 0.3	+2.0		V_{DIG} + 0.3	+2.0		V_{DIG} + 0.3	V
I_{IL}			±10			±10			±10	µA
I_{IH}			±10			±10			±10	µA

NOTES

[1]LSB means least significant bit. With a ±10 V input, one LSB is 305 µV.

[2]Typical rms noise at worst case transitions and temperatures.

[3]Measured with fixed resistors as shown in Figure 5 (AD976) and Figure 6 (AD976A). Adjustable to zero as shown in Figure 7.

[4]Full-scale error is expressed as the % difference between the actual full-scale code transition voltage and the ideal full-scale transition voltage and includes the effect of offset error. The full-scale error is the worst case of either the –full-scale or +full-scale code transition voltage errors.

[5]f_{IN} = 20 kHz (AD976) and f_{IN} = 45 kHz (AD976A), 0.5 dB down, unless otherwise noted.

[6]All specifications in dB are referred to a full scale ±10 V input.

[7]Full-power bandwidth is defined as full-scale input frequency at which signal-to-(noise + distortion) degrades to 60 dB or 10 bits of accuracy.

[8]Recovers to specified performance after a 2 × F_S input overvoltage.

Specifications subject to change without notice.

AD976—SPECIFICATIONS (–40°C to +85°C, F_S = 100 kHz, Ref = Internal Reference, V_{DIG} = V_{ANA} = +5 V unless otherwise noted)

Parameter	AD976A Min	AD976A Typ	AD976A Max	AD976B Min	AD976B Typ	AD976B Max	AD976C Min	AD976C Typ	AD976C Max	Units
RESOLUTION	16			16			16			Bits
ANALOG INPUT										
Voltage Range		±10			±10			±10		V
Impedance		23			23			23		kΩ
Capacitance		22			22			22		pF
THROUGHPUT SPEED										
Complete Cycle			10			10			10	µs
Throughput Rate	100			100			100			kHz
DC ACCURACY										
Integral Linearity Error			±3			±2		±3		LSB[1]
Differential Linearity Error	–2		+3	–1		+1.75		±2		LSB
No Missing Codes	15			16				15		Bit
Transition Noise[2]		1.0			1.0			1.0		LSB
Full-Scale Error[3, 4]			±0.5			±0.25			±0.5	%
Full-Scale Error Drift		±7			±7			±7		ppm/°C
Full-Scale Error, Ext. REF = 2.5 V			±0.5			±0.25			±0.5	%
Full-Scale Error Drift, Ext. REF = 2.5 V		±2			±2			±2		ppm/°C
Bipolar Zero Error[4]			±10			±10			±15	mV
Bipolar Zero Error Drift		±2			±2			±2		ppm/°C
Power Supply Sensitivity										
V_{ANA} = V_{DIG} = V_D = 5 V ± 5%			±8			±8			±8	LSB
AC ACCURACY										
Spurious Free Dynamic Range[5]	90			96			90			dB[6]
Total Harmonic Distortion[5]			–90			–96			–90	dB
Signal to (Noise + Distortion)[5]	83			85			83			dB
–60 dB Input		27			28			27		dB
Signal to Noise[5]	83			85			83			dB
Full-Power Bandwidth[7]		700			700			700		kHz
Input Bandwidth		1.5			1.5			1.5		MHz
SAMPLING DYNAMICS										
Aperture Delay		40			40			40		ns
Transient Response										
Full-Scale Step			2			2			2	µs
Overvoltage Recovery[8]		150			150			150		ns
REFERENCE										
Internal Reference Voltage	2.48	2.5	2.52	2.48	2.5	2.52	2.48	2.5	2.52	V
Internal Reference Source Current		1			1			1		µA
External Reference Voltage Range for Specified Linearity	2.3	2.5	2.7	2.3	2.5	2.7	2.3	2.5	2.7	V
External Reference Current Drain										
Ext. REF = 2.5 V			100			100			100	µA
DIGITAL INPUTS										
Logic Levels										
V_{IL}	–0.3		+0.8	–0.3		+0.8	–0.3		+0.8	V
V_{IH}	+2.0		V_{DIG} + 0.3	+2.0		V_{DIG} + 0.3	+2.0		V_{DIG} + 0.3	V
I_{IL}			±10			±10			±10	µA
I_{IH}			±10			±10			±10	µA

NOTES
[1]LSB means least significant bit. With a ±10 V input, one LSB is 305 µV.
[2]Typical rms noise at worst case transitions and temperatures.
[3]Measured with fixed resistors as shown in Figure 5 (AD976) and Figure 6 (AD976A). Adjustable to zero as shown in Figure 7.
[4]Full-scale error is expressed as the % difference between the actual full-scale code transition voltage and the ideal full-scale transition voltage and includes the effect of offset error. The full-scale error is the worst case of either the –full-scale or +full-scale code transition voltage errors.
[5]f_{IN} = 20 kHz (AD976) and f_{IN} = 45 kHz (AD976A), 0.5 dB down, unless otherwise noted.
[6]All specifications in dB are referred to a full scale ±10 V input.
[7]Full-power bandwidth is defined as full-scale input frequency at which signal-to-(noise + distortion) degrades to 60 dB or 10 bits of accuracy.
[8]Recovers to specified performance after a 2 × F_S input overvoltage.

Specifications subject to change without notice.

Parameter	Conditions	All Grades Min	Typ	Max	Units
DIGITAL OUTPUTS					
Data Format			Parallel 16 Bits		
Data Coding			Binary Twos Complement		
V_{OL}	I_{SINK} = 1.6 mA			+0.4	V
V_{OH}	I_{SOURCE} = 500 µA	+4			V
Leakage Current	High-Z State, V_{OUT} = 0 V to V_{DIG}			±5	µA
Output Capacitance	High-Z State			15	pF
DIGITAL TIMING					
Bus Access Time				83	ns
Bus Relinquish Time				83	ns
POWER SUPPLIES					
Specified Performance					
V_{DIG}		4.75	5	5.25	V
V_{ANA}		4.75	5	5.25	V
I_{DIG}			3.0		mA
I_{ANA}			11		mA
Power Dissipation				100	mW
TEMPERATURE RANGE					
Specified Performance		–40		+85	°C

Specifications subject to change without notice.

TIMING SPECIFICATIONS (AD976A: F_S = 200 kHz; AD976: F_S = 100 kHz; –40°C to +85°C, V_{DIG} = V_{ANA} = +5 V unless otherwise noted)

	Symbol	Min	Typ	Max	Units
Convert Pulsewidth	t_1	50			ns
Data Valid Delay after R/$\overline{C}$ Low (AD976A/AD976)	t_2			4.0/8.0	µs
$\overline{BUSY}$ Delay from R/$\overline{C}$ Low	t_3			83	ns
$\overline{BUSY}$ Low (AD976A/AD976)	t_4			4.0/8.0	µs
$\overline{BUSY}$ Delay after End of Conversion (AD976A/AD976)	t_5		180/360		ns
Aperture Delay	t_6		40		ns
Conversion Time (AD976A/AD976)	t_7		3.8/7.6	4.0/8.0	µs
Acquisition Time	t_8	1.0/2.0			µs
Bus Relinquish Time	t_9	10	35	83	ns
$\overline{BUSY}$ Delay after Data Valid (AD976A/AD976)	t_{10}	50	180/360		ns
Previous Data Valid after R/$\overline{C}$ Low (AD976A/AD976)	t_{11}		3.7/7.4		µs
Throughput Time (AD976A/AD976)	$t_7 + t_8$			5/10	µs
R/$\overline{C}$ to $\overline{CS}$ Setup Time	t_{12}	10			ns
Time Between Conversions (AD976A/AD976)	t_{13}	5/10			µs
Bus Access and Byte Delay	t_{14}	10		83	ns

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Analog Inputs
- V_{IN} . . . . . ±25 V
- CAP . . . . . $+V_{ANA}$ + 0.3 V to AGND2 – 0.3 V
- REF . . . . . Indefinite Short to AGND2

Ground Voltage Differences
- DGND, AGND1, AGND2 . . . . . ±0.3 V

Supply Voltages
- V_{ANA} . . . . . 7 V
- V_{DIG} to V_{ANA} . . . . . ±7 V
- V_{DIG} . . . . . 7 V

Digital Inputs . . . . . –0.3 V to V_{DIG} + 0.3 V

Internal Power Dissipation[2]
- PDIP (N), SOIC (R), SSOP (RS) . . . . . 700 mW

Junction Temperature . . . . . +150°C

Storage Temperature Range (N, R, RS) . . . –65°C to +150°C

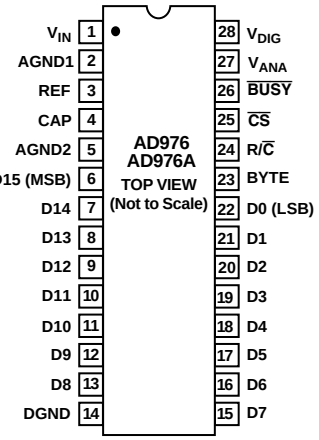
Lead Temperature Range
- (Soldering 10 sec) . . . . . +300°C

NOTES

[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Specification is for device in free air:
28-Lead PDIP: θ_{JA} = 74°C/W; θ_{JC} = 24°C/W,
28-Lead SOIC: θ_{JA} = 72°C/W; θ_{JC} = 23°C/W,
28-Lead SSOP: θ_{JA} = 109°C/W; θ_{JC} = 39°C/W.

PIN CONFIGURATION
DIP, SOIC and SSOP Packages



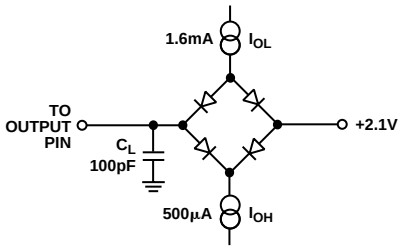


Figure 1. Load Circuit for Digital Interface Timing

ORDERING GUIDE

Model	Temperature Range	Max INL	Min S/(N+D)	Throughput Rate	Package Descriptions	Package Options
AD976AN	–40°C to +85°C	±3.0 LSB	83 dB	100 kSPS	28-Lead, 300 mil Plastic DIP	N-28B
AD976BN	–40°C to +85°C	±2.0 LSB	85 dB	100 kSPS	28-Lead, 300 mil Plastic DIP	N-28B
AD976CN	–40°C to +85°C		83 dB	100 kSPS	28-Lead, 300 mil Plastic DIP	N-28B
AD976AAN	–40°C to +85°C	±3.0 LSB	83 dB	200 kSPS	28-Lead, 300 mil Plastic DIP	N-28B
AD976ABN	–40°C to +85°C	±2.0 LSB	85 dB	200 kSPS	28-Lead, 300 mil Plastic DIP	N-28B
AD976ACN	–40°C to +85°C		83 dB	200 kSPS	28-Lead, 300 mil Plastic DIP	N-28B
AD976AR	–40°C to +85°C	±3.0 LSB	83 dB	100 kSPS	28-Lead Small Outline Package	R-28
AD976BR	–40°C to +85°C	±2.0 LSB	85 dB	100 kSPS	28-Lead Small Outline Package	R-28
AD976CR	–40°C to +85°C		83 dB	100 kSPS	28-Lead Small Outline Package	R-28
AD976AAR	–40°C to +85°C	±3.0 LSB	83 dB	200 kSPS	28-Lead Small Outline Package	R-28
AD976ABR	–40°C to +85°C	±2.0 LSB	85 dB	200 kSPS	28-Lead Small Outline Package	R-28
AD976ACR	–40°C to +85°C		83 dB	200 kSPS	28-Lead Small Outline Package	R-28
AD976ARS	–40°C to +85°C	±3.0 LSB	83 dB	100 kSPS	28-Lead Shrink Small Outline Package	RS-28
AD976BRS	–40°C to +85°C	±2.0 LSB	85 dB	100 kSPS	28-Lead Shrink Small Outline Package	RS-28
AD976CRS	–40°C to +85°C		83 dB	100 kSPS	28-Lead Shrink Small Outline Package	RS-28
AD976AARS	–40°C to +85°C	±3.0 LSB	83 dB	200 kSPS	28-Lead Shrink Small Outline Package	RS-28
AD976ABRS	–40°C to +85°C	±2.0 LSB	85 dB	200 kSPS	28-Lead Shrink Small Outline Package	RS-28
AD976ACRS	–40°C to +85°C		83 dB	200 kSPS	28-Lead Shrink Small Outline Package	RS-28

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD976/AD976A features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Description
1	V_{IN}	Analog Input. Connect a 200 Ω resistor between V_{IN} and the analog signal source. The full-scale input range is ±10 V.
2	AGND1	Analog Ground. Used as the ground reference point for the REF pin.
3	REF	Reference Input/Output. The internal +2.5 V reference is available at this pin. Alternatively, an external reference can be used to override the internal reference. In either case, connect a 2.2 µF tantalum capacitor between REF and AGND1.
4	CAP	Reference Buffer Output. Connect a 2.2 µF tantalum capacitor between CAP and AGND2.
5	AGND2	Analog Ground.
6	D15 (MSB)	Data Bit 15. Most significant bit of conversion result. High impedance state when $\overline{CS}$ is HIGH or when R/$\overline{C}$ is LOW.
7–13	D14–D8	Data Bits 14–8. High impedance state when $\overline{CS}$ is HIGH or when R/$\overline{C}$ is LOW.
14	DGND	Digital Ground.
15–21	D7–D1	Data Bits 7–1. High impedance state when $\overline{CS}$ is HIGH or when R/$\overline{C}$ is LOW.
22	D0 (LSB)	Data Bit 0. Least significant bit of conversion result. High impedance state when $\overline{CS}$ is HIGH or when R/$\overline{C}$ is LOW.
23	BYTE	Byte Select. With BYTE LOW, data will be output as indicated above; Pin 6 (D15) is the MSB, Pin 22 (D0) is the LSB. With BYTE HIGH, the top and bottom 8 bits of data will be switched; D15–D8 are output on Pins 15–22 and D7–D0 are output on Pins 6–13.
24	R/$\overline{C}$	Read/Convert Input. With $\overline{CS}$ LOW, a falling edge on R/$\overline{C}$ puts the internal sample/hold into the hold state and starts a conversion; a rising edge enables the output data bits.
25	$\overline{CS}$	Chip Select Input. Internally OR'd with R/$\overline{C}$. With R/$\overline{C}$ LOW, a falling edge on $\overline{CS}$ will initiate a conversion. With R/$\overline{C}$ HIGH, a falling edge on $\overline{CS}$ will enable the output data bits. When $\overline{CS}$ is HIGH, the output data bits will be in the Hi-impedance state.
26	$\overline{BUSY}$	Busy Output. Goes LOW when a conversion is started and remains LOW until the conversion is completed and the data is latched into the output register. With $\overline{CS}$ tied LOW and R/$\overline{C}$ HIGH, output data will be valid when $\overline{BUSY}$ rises. The rising edge of $\overline{BUSY}$ can be used to latch the output data.
27	V_{ANA}	Analog Power Supply. Nominally +5 V.
28	V_{DIG}	Digital Power Supply. Nominally +5 V.

DEFINITION OF SPECIFICATIONS

INTEGRAL NONLINEARITY ERROR (INL)

Linearity error refers to the deviation of each individual code from a line drawn from "negative full scale" to "positive full scale." The point used as negative full scale occurs 1/2 LSB before the first code transition. Positive full scale is defined as a level 1 1/2 LSB beyond the last code transition. The deviation is measured from the middle of each particular code to the true straight line.

DIFFERENTIAL NONLINEARITY ERROR (DNL)

In an ideal ADC, code transitions are 1 LSB apart. Differential nonlinearity is the maximum deviation from this ideal value. It is often specified in terms of resolution for which no missing codes are guaranteed.

± FULL-SCALE ERROR

The last + transition (from 011. . .10 to 011. . .11) should occur for an analog voltage 1 1/2 LSB below the nominal full scale (9.9995422 V for a ±10 V range). The full-scale error is the deviation of the actual level of the last transition from the ideal level.

BIPOLAR ZERO ERROR

Bipolar zero error is the difference between the ideal midscale input voltage (0 V) and the actual voltage producing the midscale output code.

INPUT BANDWIDTH

The input bandwidth is that frequency at which the amplitude of the reconstructed fundamental is reduced by 3 dB for a full-scale input.

FULL-POWER BANDWIDTH

Full-power bandwidth is defined as the full-scale input frequency at which signal to (Noise + Distortion) degrades to 60 dB, as 10 bits of accuracy.

APERTURE DELAY

Aperture delay is a measure of the Sample-and-Hold Amplifier (SHA) performance and is measured from the rising edge of the clock input to when the input signal is held for a conversion.

APERTURE JITTER
Aperture jitter is the variation in aperture delay for successive samples and is manifested as noise on the input to the A/D.

TRANSIENT RESPONSE
The time required for the AD976/AD976A to achieve its rated accuracy after a full-scale step function is applied to its input.

OVERVOLTAGE RECOVERY
The time required for the ADC to recover to full accuracy after an analog input signal 150% of full-scale is reduced to 50% of the full-scale value.

Signal-to-(Noise Plus Distortion Ratio) (S/[N+D])
S/(N+D) is the measured signal-to-noise plus distortion ratio at the output of the ADC. The signal is the rms magnitude of the fundamental. Noise plus distortion is the rms sum of all of the nonfundamental signals and harmonics to half the sampling rate excluding dc. The S/(N+D) is dependent upon the number of quantization levels. The more levels, the lower the quantization noise. The theoretical S/(N+D) for a sine wave input signal can be calculated using the following:

$$S/(N+D) = (6.02N + 1.76)\ dB \quad (1)$$

where N is the number of bits.

Thus, for an ideal 16 bit converter, S/(N+D) = 98 dB.

The output spectrum from the ADC is evaluated by applying a low noise, low distortion sine wave signal to the V_{IN} pin and sampling at a 200 kHz throughput rate. By generating a Fast Fourier Transform (FFT) plot, the S/(N+D) data can then be obtained. Figure 10 shows a typical 2048-point FFT plot with an input signal of 45 kHz and a sampling rate of 200 kHz. The S/(N+D) obtained from this graph is 86.23 dB.

Since the measured S/(N+D) is less than the theoretical value, it is possible to get a measure of performance expressed in effective number of bits (ENOB).

$$ENOB = ((S/(N+D) - 1.76) / 6.02)$$

Thus for an input signal of 45 kHz, the typical ENOB is 14.

TOTAL HARMONIC DISTORTION (THD)
THD is the ratio of the rms sum of the harmonics to the rms value of the fundamental. For the AD976/AD976A, THD is defined as:

$$THD\left(dB\right) = 20 \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where V_1 is the rms amplitude of the fundamental, and V_2, V_3, V_4, V_5 and V_6 are the rms amplitudes of the second through sixth harmonics. The THD is also derived from the FFT plot of the ADC output spectrum shown in Figure 10 and is seen there as –105.33 dB.

Spurious Free Dynamic Range (SPFD)
The spurious free dynamic range is defined as the difference, in dB, between the peak spurious or harmonic component in the ADC output spectrum (up to $F_S/2$ and excluding dc) and the rms value of the fundamental. Normally, the value of this specification will be determined by the largest harmonic in the spectrum. The typical SPFD for the AD976/AD976A is –100 dB and can be seen in Figure 10.

FUNCTIONAL DESCRIPTION
The AD976/AD976A is a high speed, low power, 16-bit sampling, analog-to-digital converter that can operate from a single +5 volt power supply. The AD976/AD976A uses laser trimmed scaling input resistors to provide an industry standard ±10 volt input range. With a 100/200 kSPS throughput rate and a parallel interface, the AD976/AD976A is capable of connecting directly to digital signal processors and microcontrollers.

The AD976/AD976A employs a successive-approximation technique to determine the value of the analog input voltage. Instead of using the traditional laser-trimmed resistor-ladder approach, however, this device uses a capacitor array charge distribution technique. Binary weighted capacitors subdivide the input sample to perform the actual analog-to-digital conversion. The capacitor array eliminates variation in the linearity of the device due to temperature-induced mismatches of resistor values. As a result of having an on-chip capacitor array, there is no need for additional external circuitry to perform the sample/hold function.

Initial errors in capacitor matching are eliminated at the time of manufacturing. Calibration coefficients are calculated that correct for capacitor mismatches and are stored in on-chip thin-film resistors that act as ROM. As a conversion is occurring, the appropriate calibration coefficients are read out of ROM. The accumulated coefficients are then used to adjust and improve conversion accuracy. Any initial offset error is also trimmed out during factory calibration. With the addition of an onboard reference the AD976/AD976A provides a complete 16-bit A/D solution.

CONVERSION CONTROL

The AD976/AD976A is controlled by two signals: R/$\overline{C}$ and $\overline{CS}$, as shown in Figures 2 and 3. To initiate a conversion and place the sample/hold circuit into the hold state, both the R/$\overline{C}$ and $\overline{CS}$ signals must be brought low for no less than 50 ns. Once the conversion process begins, the $\overline{BUSY}$ signal will go Low until the conversion is complete. At the end of a conversion, $\overline{BUSY}$ will return High, and the resulting valid data will be available on the data bus. On the first conversion after the AD976/AD976A is powered up, the DATA output will be indeterminate.

The AD976/AD976A exhibits two modes of conversion. In the mode demonstrated in Figure 2, conversion timing is controlled by a negative-going R/$\overline{C}$ signal, at least 50 ns wide. In this mode the $\overline{CS}$ pin is always tied low, and the only limit placed on how long the R/$\overline{C}$ signal can remain low is the desired sampling rate. Less than 83 ns after the initiation of a conversion, the $\overline{BUSY}$ signal will be brought low and remain low until the conversion is complete and the output shift registers have been updated with the new Binary Twos Complement data.

Figure 3 demonstrates the AD976/AD976A conversion timing, using $\overline{CS}$ to control both the conversion process and the reading of output data. To operate in this mode, the R/$\overline{C}$ signal should be brought low no less than 10 ns before the falling edge of a $\overline{CS}$ pulse (50 ns wide) is applied to the ADC. Once these two pulses are applied, $\overline{BUSY}$ will go low and remain low until a conversion is complete. After a maximum of 4 µs (AD976A only), $\overline{BUSY}$ will again return high, and parallel data will be valid on the ADC outputs. To achieve the maximum 100 kHz/200 kHz throughput rate of the part, the negative going R/$\overline{C}$ and $\overline{CS}$ control signals should be applied every 5 µs (AD976A). It should also be noted that although all R/$\overline{C}$ and $\overline{CS}$ commands will be ignored once a conversion has begun, these inputs can be asserted during a conversion; i.e., a read during conversion can be performed. Voltage transients on these inputs could feed through to the analog circuitry and affect conversion results.

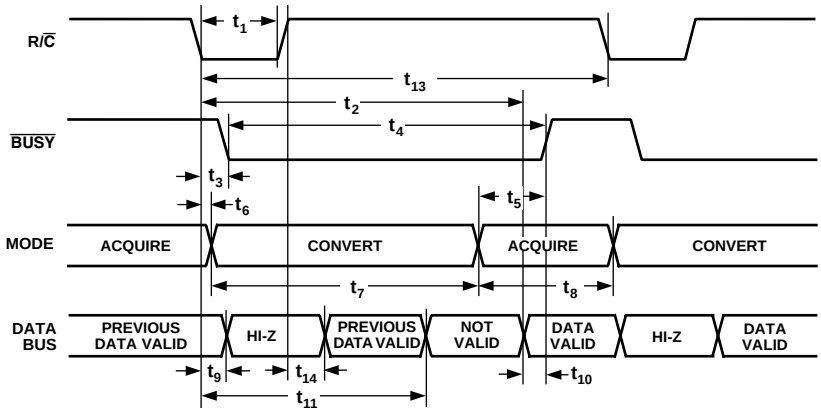


Figure 2. Conversion Timing with Outputs Enabled After Conversion ($\overline{CS}$ Tied Low)

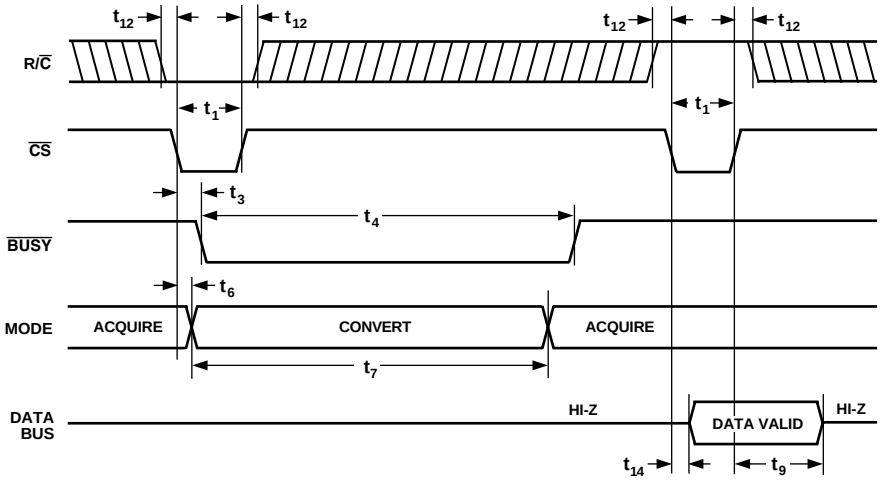


Figure 3. Using $\overline{CS}$ to Control Conversion and Read Timing

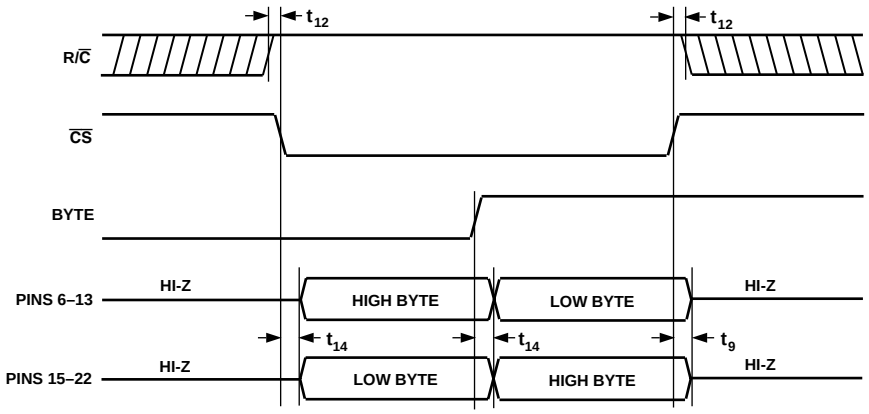


Figure 4. Using $\overline{CS}$ and BYTE to Control Data Bus Read Timing

Regardless of the method for controlling conversions, output data from conversion "n–1" will be valid during the $\overline{BUSY}$ Low time for roughly 3.7 μs (AD976A only), and output data from conversion "n" will be valid at the end of a conversion, 50 ns (t_{10}) before $\overline{BUSY}$ returns High. It is recommended, however, that data is read only after $\overline{BUSY}$ goes high since this timing is much more clearly defined and provides optimal performance. Figure 4 demonstrates the functionality of the BYTE pin and shows how the data will be valid in Binary Twos Complement format only when R/$\overline{C}$ is asserted High and $\overline{CS}$ is Low. The BYTE pin enables the output data on the bus to be read as a full parallel output or as two 8-bit bytes on Pins 6–13 and Pins 15–22.

ANALOG INPUTS

Figure 5 shows the analog input section for the AD976 when operating with an internal reference. The analog input range is nominally a bipolar –10 V to +10 V. Since the AD976/AD976A can be operated with an internal or external reference, the full-scale analog input range can be best represented as ±4 V_{REF}. The nominal input impedance is 23 kΩ/13 kΩ with a 22 pF input capacitance. The analog input section also has a ±25 V overvoltage protection. Since the AD976/AD976A has two analog grounds it is important to ensure that the analog input is referenced to the AGND1 pin, the low current ground. This will minimize any problems associated with a resistive ground drop. It is also important to ensure that the analog input of the AD976/AD976A is driven by a low impedance source. With its primarily resistive analog input circuitry, the ADC can be driven by a wide selection of general purpose amplifiers.

To best match the low distortion requirements of the AD976/AD976A, care should be taken in the selection of the drive circuitry op amp. Figure 6 shows the analog input section for the AD976A when operating with an internal reference only. Figure 9 shows the analog input section for both the AD976 and the AD976A when operating with an external reference.

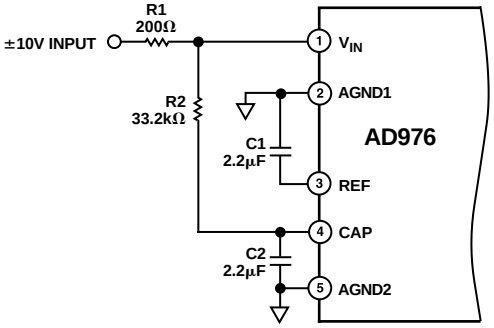


Figure 5. ±10 V Input Connection for the AD976 (Internal Reference)

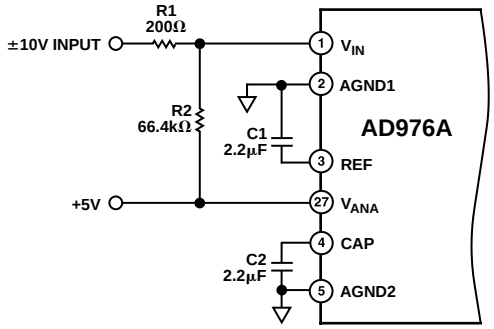


Figure 6. ±10 V Input Connection for the AD976A (Internal Reference) Only

Table I. Offset and Gain Error for AD976

Error Term	With Both External Resistors Included	Without the External 33.2K Resistor	With the External 33.2K Resistor Grounded	Without Either External Resistors Included
Offset Error	–10 mV < Error < 10 mV	–25 mV < Error < –5 mV	–25 mV < Error < –5 mV	–40 mV < Error < –15 mV
+Full Scale Error	–0.50% < Error < 0.50%[1] –0.25% < Error < 0.25%[2]	–0.05% < Error < 0.95%	–0.65% < Error < 0.35%	0.55% < Error < 1.90%
–Full Scale Error	–0.50% < Error < 0.50%[1] –0.25% < Error < 0.25%[2]	0.25% < Error < 1.25%	–0.65% < Error < 0.35%	–2.5% < Error < –1.0%

Table II. Offset and Gain Error for AD976A

Error Term	With Both External Resistors Included	Without the External 33.2K Resistor	With the External 33.2K Resistor Grounded	Without Either External Resistors Included
Offset Error	–10 mV < Error < 10 mV	–25 mV < Error < –5 mV	–25 mV < Error < –5 mV	–55 mV < Error < –25 mV
+Full Scale Error	–0.50% < Error < 0.50%[1] –0.25% < Error < 0.25%[2]	–0.05% < Error < 0.95%	–0.65% < Error < 0.35%	1.0% < Error < 2.50%
–Full Scale Error	–0.50% < Error < 0.50%[1] –0.25% < Error < 0.25%[2]	0.25% < Error < 1.25%	–0.65% < Error < 0.35%	–3.50% < Error < –1.75%

NOTES
[1]For A grade part.
[2]For B grade part.

OFFSET AND GAIN ADJUSTMENT

The AD976/AD976A is factory trimmed to minimize gain, offset and linearity errors. In some applications, where the analog input signal is required to meet the full dynamic range of the ADC, the gain and offset errors need to be externally trimmed to zero. Figure 7 shows the required trim circuitry to correct for these offset and gain errors. Figure 8 shows the bipolar transfer characteristic of the AD976/AD976A.

Where adjustment is required, offset error must be corrected before gain error. To achieve this, trim the offset resistor R3 while the input voltage is 1/2 LSB below ground. By applying a voltage of –152.6 μV at the input and adjusting the potentiometer until the major carry transition is located between 1111 1111 1111 1111 and 0000 0000 0000 0000, the internal offset can be corrected. To adjust the gain error, an analog signal should be input at either the first code transition (ADC negative full-scale) or the last code transition (ADC positive full-scale). Thus, to adjust for full-scale error, an input voltage of 9.999542 V (FS/2–3/2 LSBs) can be applied to the input and R4 should be adjusted until the output code flickers between the last positive code transition 0111 1111 1111 1111 and 0111 1111 1111 1110. Should the first code transition need adjusting, the trim procedure should consist of applying an analog input signal of –9.999847 V (–FS/2 + 1/2 LSB) to the input and adjusting the trim until the output code flickers between 1000 0000 0000 0000 and 1000 0000 0000 0001.

The external 200 Ω and 33.2K resistor shown in the data sheet for the AD976 provide compensation for an internal adjustment of the offset and gain which allows calibration with a single supply. These resistors may not be required in some applications but it should be noted that their removal will result in offset and gain errors in addition to those listed in the electrical specifications of the data sheet. Tables I and II illustrate the worst case range for Bipolar Zero (offset) error and Full-Scale (gain) error for the AD976 and the AD976A. All error terms are with respect to the A/D (i.e., a negative offset in the table would have to be corrected with an externally applied positive voltage).

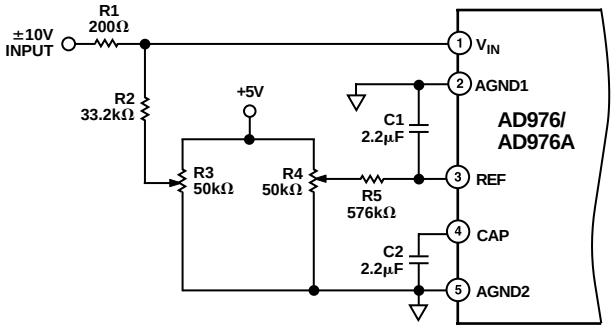


Figure 7. Input Connection with Offset and Gain Adjustment

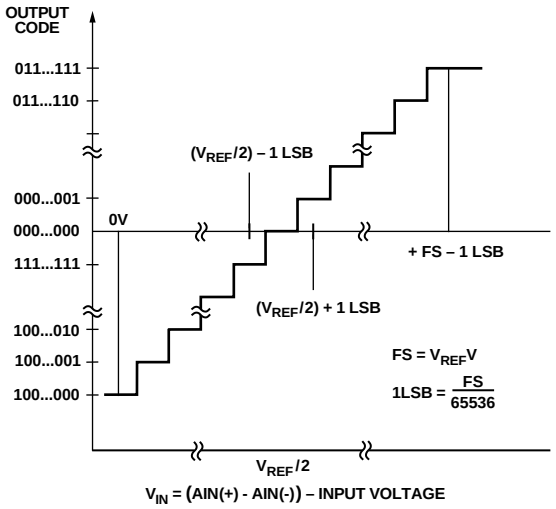


Figure 8. The Bipolar Transfer Characteristic of the AD976/AD976A

VOLTAGE REFERENCE

The AD976/AD976A has an on-chip temperature compensated bandgap voltage reference that is factory trimmed to 2.5 V ± 20 mV. The full-scale range of the ADC is equal to ±4 V_{REF}. Thus, the nominal range will be ±10 V.

The accuracy of the AD976 over the specified temperature range is dominated by the drift performance of the voltage reference. The on-chip voltage reference is laser-trimmed to provide a typical drift of 7 ppm/°C. This typical drift characteristic is shown in Figure 13, which is a plot of the change in reference voltage (in mV) versus the change in temperature—notice the plot is normalized for zero error at +25°C. If improved drift performance is required, an external reference such as the AD780 should be used to provide a drift as low as 3 ppm/°C. In order to simplify the drive requirements of the voltage reference (internal or external), an onboard reference buffer is provided. The output of this buffer is provided at the CAP pin and is available to the user; however, when externally loading the reference buffer, it is important to make sure that proper precautions are taken to minimize any degradation in the ADC's performance. Figure 14 shows the load regulation of the reference buffer. Notice that this figure is also normalized so that there is zero error with no dc load. In the linear region, the output impedance at this point is typically 1 ohm. Because of this 1 ohm output impedance, it is important to minimize any ac or input dependent loads that will lead to increased distortion. Any dc loads will simply act as a gain error. Although the typical characteristic of Figure 14 shows that the AD976 is capable of driving loads greater than 15 mA, it is not recommended that the steady state current exceed 2 mA.

In addition to the on-chip reference, an external 2.5 V reference can be applied. When choosing an external reference for a 16-bit application, however, careful attention should be paid to noise and temperature drift. These critical specifications can have a significant effect on the ADC performance.

Figure 9 shows the AD976/AD976A with the AD780 voltage reference applied to the REF pin. The AD780 is a bandgap reference that exhibits ultralow drift, low initial error, and low output noise. For low power applications, the REF192 provides a low quiescent current, high accuracy and low temperature drift solution.

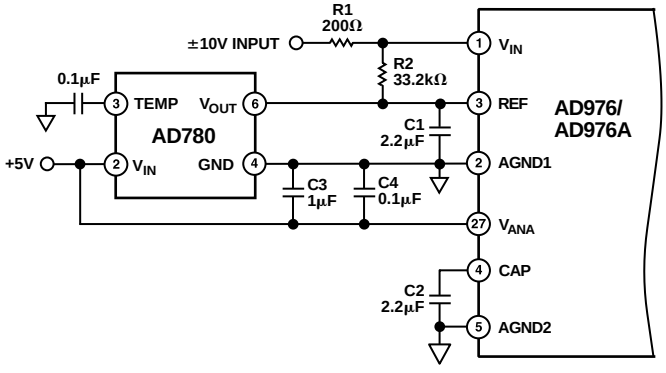


Figure 9. AD780 External Reference Connection to the AD976/AD976A

AC PERFORMANCE

The AD976/AD976A is fully specified and tested for dynamic performance specifications. The ac parameters are required for signal processing applications such as speech recognition and spectrum analysis. These applications require information on the ADC's effect on the spectral content of the input signal. Hence, the parameters for which the AD976/AD976A is specified include: S/(N+D), THD and Spurious Free Dynamic Range. These terms are discussed in greater detail in the following sections.

As a general rule, it is recommended that the results from several conversions be averaged to reduce the effects of noise, thus improving parameters such as S/(N+D) and THD. The ac performance of the AD976/AD976A can be optimized by operating the ADC at its maximum sampling rate of 100 kHz/200 kHz and by digitally filtering the resulting bit stream to the desired signal bandwidth. By distributing noise over a wider frequency range, the noise density in the frequency band of interest can be reduced. For example, if the required input bandwidth is 50 kHz, the AD976A could be oversampled by a factor of 2. This would yield a 3 dB improvement in the effective SNR performance.

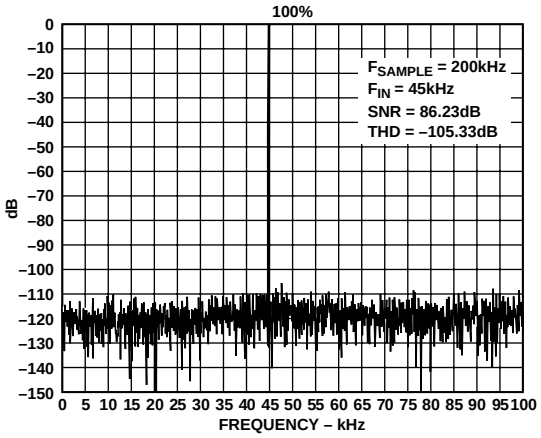


Figure 10. FFT PLOT

DC PERFORMANCE

The factory calibration scheme used for the AD976/AD976A compensates for bit weight errors that may exist in the capacitor array. The mismatch in capacitor values is adjusted (using the calibration coefficients) during a conversion, resulting in excellent dc linearity performance. Figures 11, 12, 15, 16, 17 and 18, respectively, show typical INL, typical DNL, typical positive and negative INL and DNL distribution plots for the AD976/AD976A at +25°C.

A histogram test is a statistical method for deriving an A/D converter's differential nonlinearity. A ramp input is sampled by the ADC and a large number of conversions are taken and stored. Theoretically, the codes would all be the same size and therefore have an equal number of occurrences. A code with an average number of occurrences would have a DNL of "0." A code that is different than the average would have a DNL that was either greater or less than zero LSB. A DNL of –1 LSB indicates that there is a missing code present at the 16-bit level and that the ADC exhibits 15-bit performance.

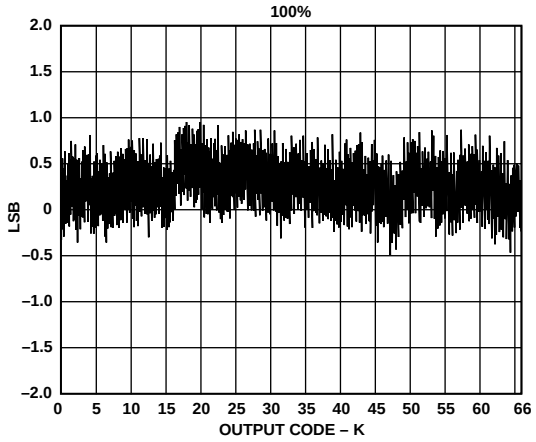


Figure 11. INL Plot

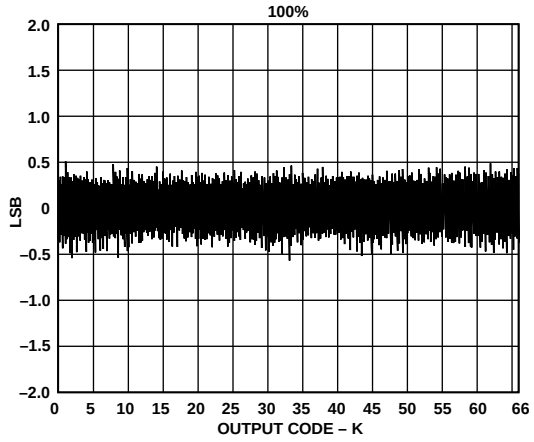


Figure 12. DNL Plot

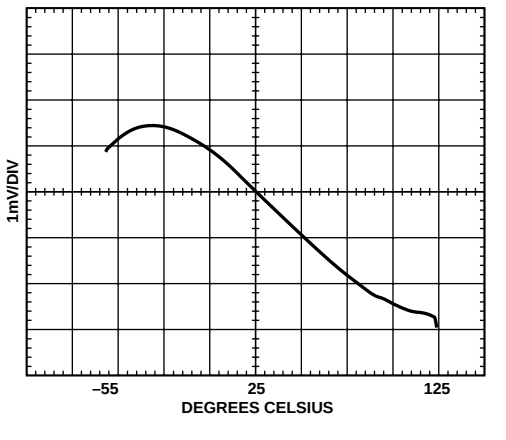


Figure 13. Reference Drift

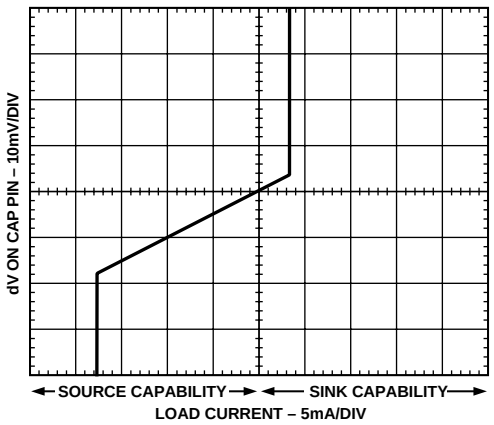


Figure 14. CAP (Pin 4) Load Regulation

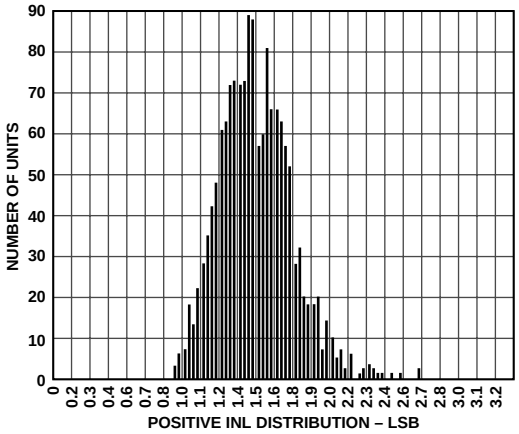


Figure 15. Typical Positive INL Distribution (1516 Units)

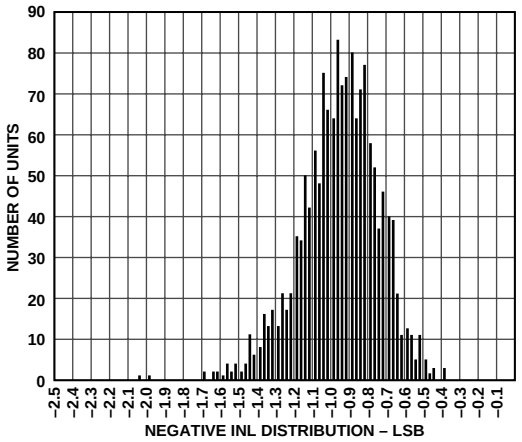


Figure 16. Typical Negative INL Distribution (1516 Units)

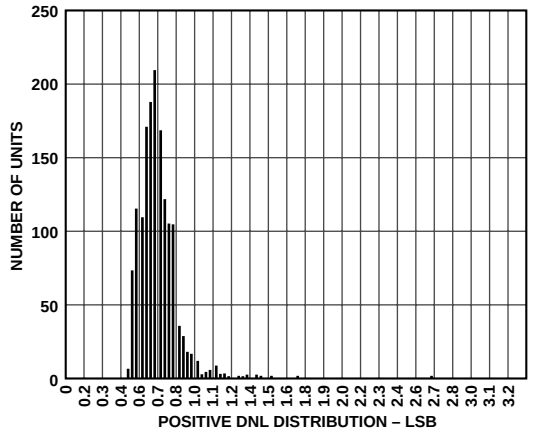


Figure 17. Typical Position DNL Distribution (1516 Units)

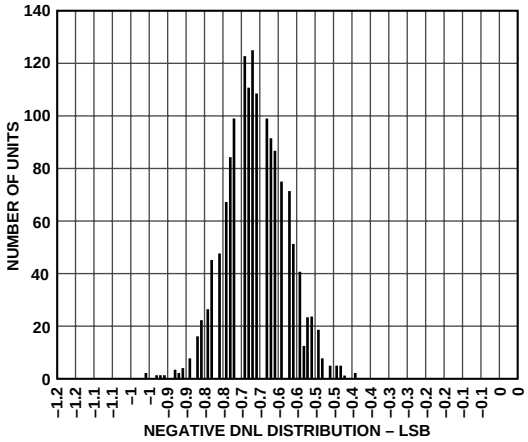


Figure 18. Typical Negative DNL Distribution (1516 Units)

DC CODE UNCERTAINTY

Ideally, a fixed dc input should result in the same output code for repetitive conversions; however, as a consequence of unavoidable circuit noise within the wideband circuits of the ADC, a range of output codes may occur for a given input voltage. Thus, when a dc signal is applied to the AD976/AD976A input, and 10,000 conversions are recorded, the result will be a distribution of codes as shown in Figure 19. This histogram shows a bell-shaped curve consistent with the Gaussian nature of thermal noise. The histogram is approximately seven codes wide. The standard deviation of this Gaussian distribution results in a code transition noise of 1 LSB rms.

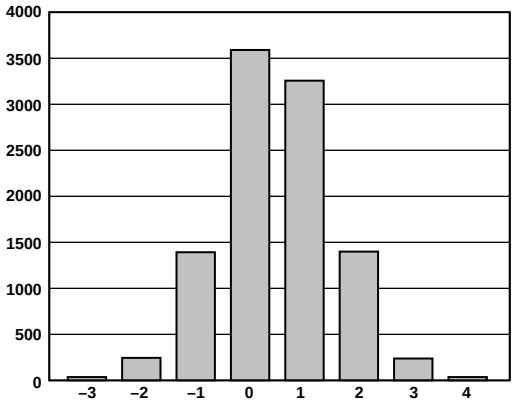


Figure 19. Histogram of 10,000 Conversions of a DC Input

MICROPROCESSOR INTERFACING

The AD976/AD976A is ideally suited for traditional dc measurement applications supporting a microprocessor and ac signal processing applications interfacing to a digital signal processor. The AD976/AD976A is designed to interface with a 16-bit data bus and provides all output data bits in a single read cycle. A variety of external buffers can be used with the AD976/AD976A to prevent bus noise from coupling into the ADC. The following sections illustrate the use of the AD976/AD976A with the MC68000 and 8051 microcontrollers and the TMS320C25 and ADSP-2111 signal processors.

MC68000 Interface

Figure 20 shows a general interface diagram for the MC68000 16-bit microprocessor to the AD976/AD976A. In Figure 20, conversion is initiated by bringing CSA low (i.e., writing to the appropriate address). This allows the processor to maintain control over the complete conversion process.

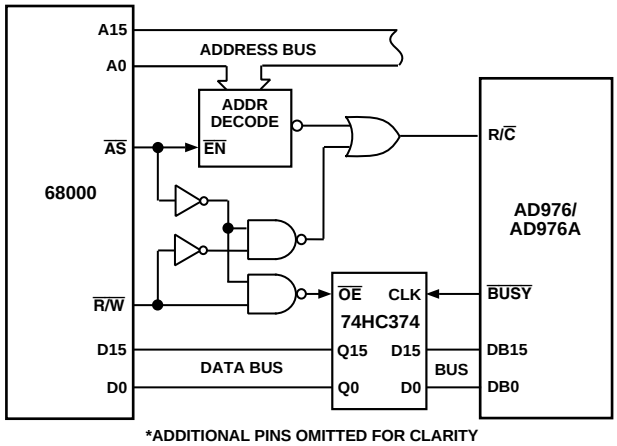


Figure 20. AD976/AD976A to 68000 Interface

8051 Interface

Figure 21 illustrates the use of the AD976/AD976A with an 8051 microcontroller.

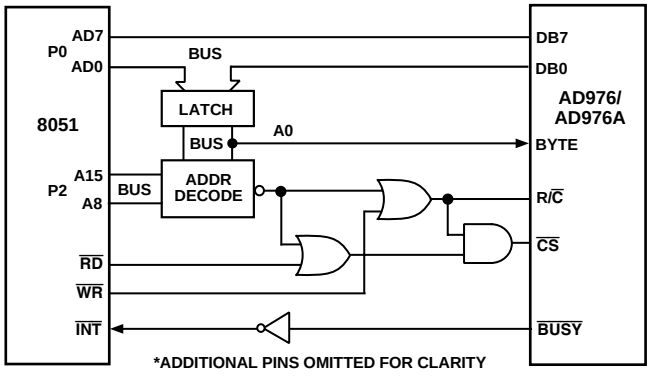


Figure 21. AD976/AD976A to 8051 Interface

TMS320C25 Interface

Figure 22 shows an interface between the AD976/AD976A and the TMS320C25.

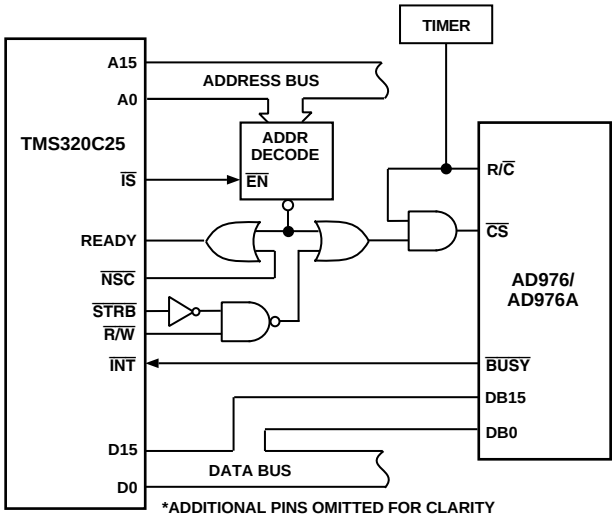


Figure 22. AD976/AD976A to TMS320C25 Interface

ADSP-2111 Interface

Figure 23 shows an interface to the ADSP-2111 signal processor. In this example, $\overline{CS}$ is being used to control conversions and is generated by an external timer. A conversion is initiated each time the timer output goes low as long as you are not reading from the AD976/AD976A and while the Flag Output (FO) pin of the ADSP-2111 is low. When a conversion is complete, the $\overline{BUSY}$ line will return high. With the $\overline{IRQn}$ pin programmed to generate an interrupt on a high-to-low transition, an interrupt will occur at the end of each conversion. The 16-bit result of the conversion can be read from within the interrupt service routine by first forcing FO high, then performing a read operation with the AD976/AD976A.

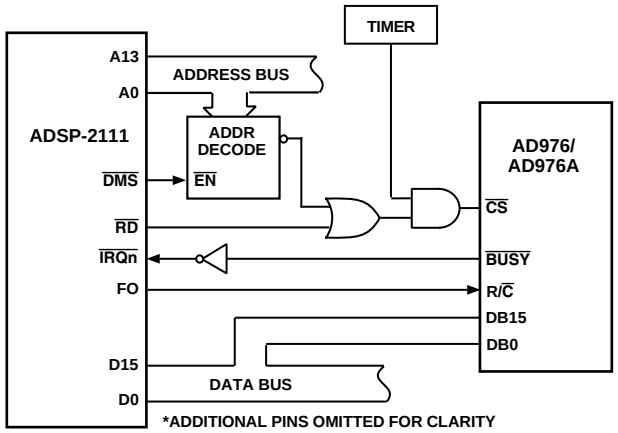


Figure 23. AD976/AD976A to ADSP-2111 Interface

POWER SUPPLIES AND DECOUPLING

The AD976/AD976A has two power supply input pins. V_{ANA} and V_{DIG} provide the supply voltages to the analog and digital portions, respectively. V_{ANA} is the +5 V supply for the on-chip analog circuitry, and V_{DIG} is the +5 V supply for the on-chip digital circuitry. The AD976/AD976A is designed to be independent of power supply sequencing and, thus, free from supply voltage induced latch-up.

With high performance linear circuits, changes in the power supplies can result in undesired circuit performance. Optimally, well regulated power supplies should be chosen with less than 1% ripple. The ac output impedance of a power supply is a complex function of frequency and it will generally increase with frequency. Thus, high frequency switching, such as that encountered with digital circuitry, requires the fast transient currents that most power supplies can not adequately provide. Such a situation results in large voltage spikes on the supplies. To compensate for the finite ac output impedance of most supplies, charge "reserves" should be stored in bypass capacitors. This will effectively lower the supplies impedance presented to the AD976/AD976A V_{ANA} and V_{DIG} pins and reduce the magnitude of these spikes. Decoupling capacitors, typically 0.1 μF, should be placed close to the power supply pins of the AD976/AD976A to minimize any inductance between the capacitors and the V_{ANA} and V_{DIG} pins.

The AD976/AD976A may be operated from a single +5 V supply. When separate supplies are used, however, it is beneficial to have larger capacitors, 10 μF, placed between the logic supply (V_{DIG}) and digital common (DGND) and between the analog supply (V_{ANA}) and the analog common (AGND2). Additionally, 10 μF capacitors should be located in the vicinity of the ADC to further reduce low frequency ripple. In systems where the device will be subjected to harsh environmental noise, additional decoupling may be required.

GROUNDING

The AD976/AD976A has three ground pins; AGND1, AGND2 and DGND. The analog ground pins are the "high quality" ground reference points and should be connected to the system analog common. AGND2 is the ground to which most internal ADC analog signals are referenced. This ground is most susceptible to current induced voltage drops and thus must be connected with the least resistance back to the power supply. AGND1 is the low current analog supply ground and should be the analog common for the external reference, input op amp drive circuitry and the input resistor divider circuit. By applying the inputs referenced to this ground, any ground variations will be offset and have a minimal effect on the resulting analog input to the ADC. The digital ground pin, DGND, is the reference point for all of the digital signals that control the AD976/AD976A.

The AD976/AD976A can be powered with two separate power supplies or with a single analog supply. When the system digital supply is noisy or fast switching digital signals are present, it is recommended to connect the analog supply to both the V_{ANA} and V_{DIG} pins of the AD976/AD976A and the system supply to the remaining digital circuitry. With this configuration, AGND1, AGND2, and DGND should be connected back at the ADC. When there is significant bus activity on the digital output pins, the digital and analog supply pins on the ADC should be separated. This would eliminate any high speed digital noise from coupling back to the analog portion of the AD976/AD976A. In this configuration, the digital ground pin DGND should be connected to the system digital ground and be separate from the AGND pins.

BOARD LAYOUT

Designing with high resolution data converters requires careful attention to board layout. Trace impedance is a significant issue. A 1.22 mA current through a 0.5 Ω trace will develop a voltage drop of 0.6 mV, which is 2 LSBs at the 16-bit level over the 20 volt full-scale range. Ground circuit impedances should be reduced as much as possible since any ground potential differences between the signal source and the ADC appear as an error voltage in series with the input signal. In addition to ground drops, inductive and capacitive coupling needs to be considered. This is especially true when high accuracy analog input signals share the same board with digital signals. Thus, to minimize input noise coupling, the input signal leads to V_{IN} and the signal return leads from AGND should be kept as short as possible. In addition, power supplies should also be decoupled to filter out ac noise.

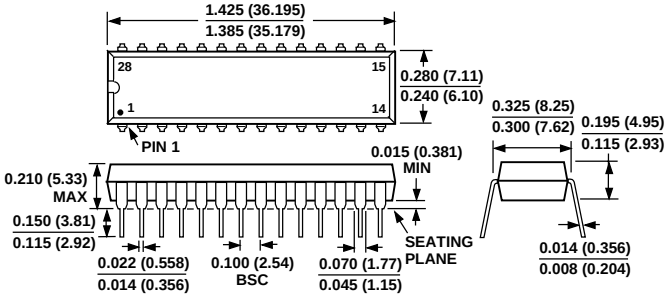
Analog and digital signals should not share a common path. Each signal should have an appropriate analog or digital return routed close to it. Using this approach, signal loops enclose a small area, minimizing the inductive coupling of noise. Wide PC tracks, large gauge wire and ground planes are highly recommended to provide low impedance signal paths. Separate analog and digital ground planes are also recommended with a single interconnection point to minimize ground loops. Analog signals should be routed as far as possible from high speed digital signals and should only cross them, if absolutely necessary, at right angles.

In addition, it is recommended that multilayer PC boards be used with separate power and ground planes. When designing the separate sections, careful attention should be paid to the layout.

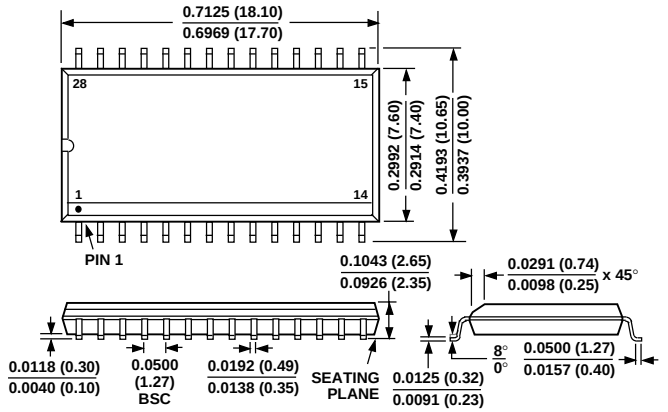
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

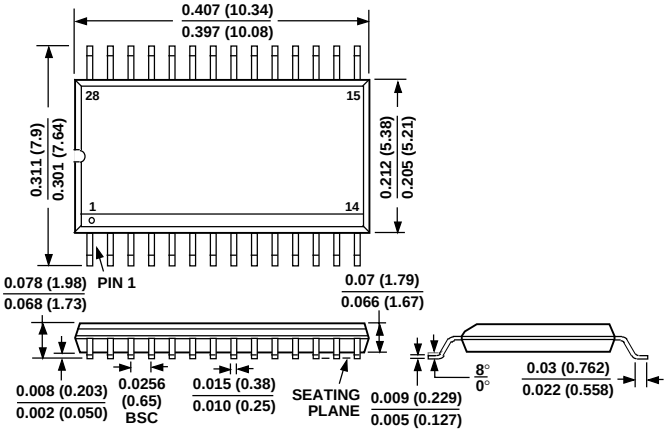
28-Lead 300 mil Plastic DIP (N-28B)



28-Lead SOIC (R-28)



28-Lead SSOP (RS-28)



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