

Low Charge Injection 24-Channel SPST High Voltage Analog Switch

Features

- ▶ 24 Channels of high voltage analog switch
- ▶ 3.3 or 5.0V CMOS input logic level
- ▶ 24 Channel SPST configuration
- ▶ 20MHz data shift clock frequency
- ▶ HVCMOS technology for high performance
- ▶ Very low quiescent power dissipation-10 μ A
- ▶ Low parasitic capacitance
- ▶ DC to 50MHz analog signal frequency
- ▶ -60dB typical OFF-isolation at 5.0MHz
- ▶ CMOS logic circuitry for low power
- ▶ Excellent noise immunity
- ▶ Cascadable serial data register with latches
- ▶ Flexible operating supply voltages

Applications

- ▶ Medical ultrasound imaging
- ▶ Piezoelectric transducer drivers
- ▶ Inkjet printer heads
- ▶ Optical MEMS modules

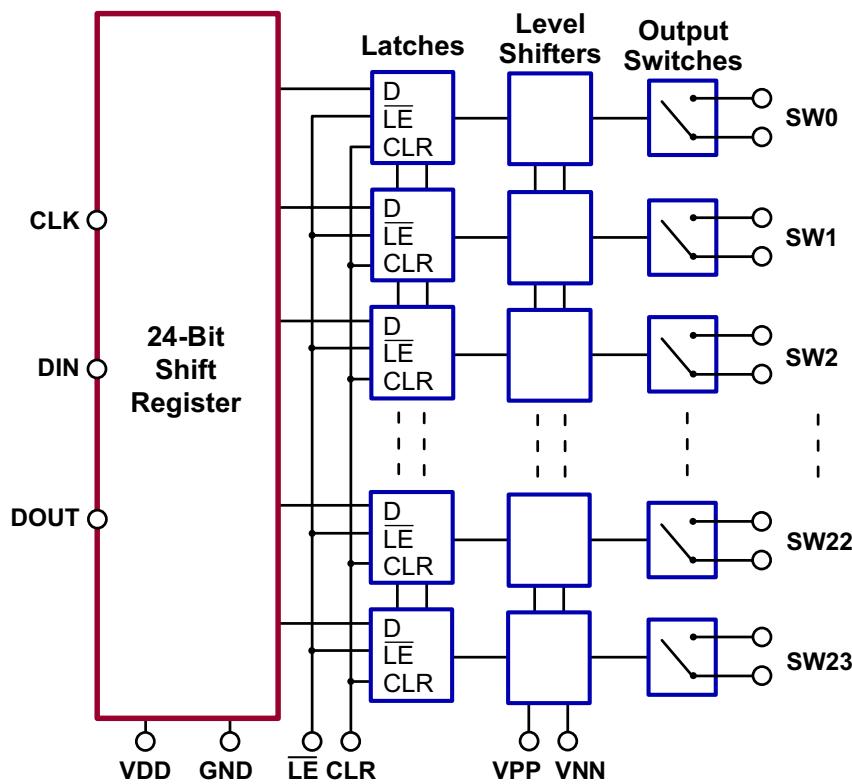
General Description

The Supertex HV2662 is a low charge injection 24-channel high voltage analog switch integrated circuit (IC) intended for use in applications requiring high voltage switching controlled by low voltage control signals, such as medical ultrasound imaging, piezoelectric transducer driver, and printers.

Input data is shifted into a 24bit shift register that can then be retained in a 24bit latch. To reduce any possible clock feed through noise, the latch enable bar should be left high until all bits are clocked in. Data are clocked in during the rising edge of the clock. Using HVCMOS technology, this device combines high voltage bilateral DMOS switches and low power CMOS logic to provide efficient control of high voltage analog signals.

The device is suitable for various combinations of high voltage supplies, e.g., V_{PP}/V_{NN} : +40V/-160V, +100V/-100V, and +160V/-40V.

Block Diagram



Ordering Information

| Part Number | Package | Packing |
|-------------|--------------|----------|
| HV2662LA-G | 64-Pad LFGA | 260/Tray |
| HV2662LB-G | 64-Ball LFGA | 260/Tray |

-G indicates package is RoHS compliant ('Green')



Absolute Maximum Ratings

| Parameter | Value |
|---------------------------------------|--------------------------|
| V_{DD} logic supply | -0.5V to +6.5V |
| $V_{PP} - V_{NN}$ differential supply | 220V |
| V_{PP} positive supply | -0.5V to $V_{NN} + 200V$ |
| V_{NN} negative supply | +0.5V to -200V |
| Logic input voltage | -0.5V to $V_{DD} + 0.3V$ |
| Analog signal range | V_{NN} to V_{PP} |
| Peak analog signal current/channel | 2.0A |
| Storage temperature | -65°C to 150°C |
| Power dissipation | 1.0W |

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Typical Thermal Resistance

| Package | θ_{ja} |
|--------------|---------------|
| 64-Pad LFGA | 36°C/W |
| 64-Ball LFGA | 37°C/W |

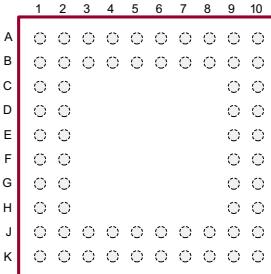
Recommended Operating Conditions

| Sym | Parameter | Value |
|-----------|------------------------------------|----------------------------------|
| V_{DD} | Logic power supply voltage | 3.0V to 5.5V |
| V_{PP} | Positive high voltage supply | +40V to $V_{NN} + 200V$ |
| V_{NN} | Negative high voltage supply | -40V to -160V |
| V_{IH} | High level input voltage | $0.9V_{DD}$ to V_{DD} |
| V_{IL} | Low level input voltage | 0V to $0.1V_{DD}$ |
| V_{SIG} | Analog signal voltage peak-to-peak | $V_{NN} + 10V$ to $V_{PP} - 10V$ |
| T_A | Operating free air temperature | 0°C to 70°C |

Notes:

1. Power up/down sequence is arbitrary except GND must be powered-up first and powered-down last.
2. V_{SIG} must be $V_{NN} \leq V_{SIG} \leq V_{PP}$ or floating during power up/down transition.
3. Rise and fall times of power supplies V_{DD} , V_{PP} and V_{NN} should not be less than 1.0msec.

Pin Configuration



64-Lead LFGA (LA/LB)
(top view)

Product Marking

• HV2662LA
LLLLLLLLL
YYWW
AAA CCC

L = Lot Number
YY = Year Sealed
WW = Week Sealed
A = Assembler ID
C = Country of Origin
— = "Green" Packaging

Package may or may not include the following marks: Si or 64-Pad LFGA (LA)

• HV2662LB
LLLLLLLLL
YYWW
AAA CCC

L = Lot Number
YY = Year Sealed
WW = Week Sealed
A = Assembler ID
C = Country of Origin
— = "Green" Packaging

Package may or may not include the following marks: Si or 64-Ball LFGA (LB)

DC Electrical Characteristics (Over recommended operating conditions unless otherwise specified)

| Sym | Parameter | 0°C | | +25°C | | | +70°C | | Unit | Conditions |
|------------------|--|------|-----|-------|------|-----|-------|-----|---------------|--|
| | | Min | Max | Min | Typ | Max | Min | Max | | |
| R_{ONS} | Small signal switch ON-resistance | - | - | - | 26 | - | - | - | Ω | $I_{SIG} = 5.0\text{mA}$, $V_{PP} = +40\text{V}$, $V_{NN} = -160\text{V}$ |
| | | - | - | - | 22 | - | - | - | | $I_{SIG} = 200\text{mA}$ |
| | | - | - | - | 22 | - | - | - | | $I_{SIG} = 5.0\text{mA}$, $V_{PP} = +100\text{V}$, $V_{NN} = -100\text{V}$ |
| | | - | - | - | 18 | - | - | - | | $I_{SIG} = 200\text{mA}$ |
| | | - | - | - | 20 | - | - | - | | $I_{SIG} = 5.0\text{mA}$, $V_{PP} = +160\text{V}$, $V_{NN} = -40\text{V}$ |
| | | - | - | - | 16 | - | - | - | | $I_{SIG} = 200\text{mA}$ |
| ΔR_{ONS} | Small signal switch ON-resistance matching | - | 20 | - | 5.0 | 20 | - | 20 | % | $I_{SIG} = 5.0\text{mA}$, $V_{PP} = +100\text{V}$, $V_{NN} = -100\text{V}$ |
| R_{ONL} | Large signal switch ON-resistance | - | - | - | 30 | - | - | - | Ω | $V_{SIG} = V_{PP} - 10\text{V}$, $I_{SIG} = 1\text{A}$ |
| I_{SOL} | Switch OFF-leakage per switch | - | 5.0 | - | 1.0 | 10 | - | 15 | μA | $V_{SIG} = V_{PP} - 10\text{V}$, $V_{NN} + 10\text{V}$ |
| V_{OS} | DC offset switch OFF | - | 300 | - | 100 | 300 | - | 300 | mV | No load |
| | DC offset switch ON | - | 500 | - | 100 | 500 | - | 500 | | |
| I_{PPQ} | Quiescent V_{PP} supply current | - | - | - | 10 | 50 | - | - | μA | All switches OFF |
| I_{NNQ} | Quiescent V_{NN} supply current | - | - | - | -10 | -50 | - | - | μA | All switches ON, $I_{sw} = 5.0\text{mA}$ |
| I_{PPQ} | Quiescent V_{PP} supply current | - | - | - | 10 | 50 | - | - | μA | All switches ON, $I_{sw} = 5.0\text{mA}$ |
| I_{NNQ} | Quiescent V_{NN} supply current | - | - | - | -10 | -50 | - | - | μA | All switches ON, $I_{sw} = 5.0\text{mA}$ |
| I_{sw} | Switch output peak current | - | - | - | 2.0 | 1.3 | - | - | A | V_{SIG} duty cycle < 0.1% |
| f_{sw} | Output switching frequency | - | - | - | - | 50 | - | - | kHz | Duty cycle = 50% |
| I_{PP} | Average V_{PP} supply current | - | 4.0 | - | - | 4.5 | - | 5.0 | mA | $V_{PP} = +40\text{V}$, $V_{NN} = -160\text{V}$ |
| | | - | 4.0 | - | - | 4.5 | - | 5.0 | | $V_{PP} = +100\text{V}$, $V_{NN} = -100\text{V}$ |
| | | - | 4.0 | - | - | 4.5 | - | 5.0 | | $V_{PP} = +160\text{V}$, $V_{NN} = -40\text{V}$ |
| I_{NN} | Average V_{NN} supply current | - | 4.0 | - | - | 4.5 | - | 5.0 | mA | $V_{PP} = +40\text{V}$, $V_{NN} = -160\text{V}$ |
| | | - | 4.0 | - | - | 4.5 | - | 5.0 | | $V_{PP} = +100\text{V}$, $V_{NN} = -100\text{V}$ |
| | | - | 4.0 | - | - | 4.5 | - | 5.0 | | $V_{PP} = +160\text{V}$, $V_{NN} = -40\text{V}$ |
| I_{DD} | Average V_{DD} supply current | - | 8.0 | - | - | 8.0 | - | 8.0 | mA | $f_{CLK} = 5.0\text{MHz}$, $V_{DD} = 5.0\text{V}$ |
| I_{DDQ} | Quiescent V_{DD} supply current | - | 10 | - | - | 10 | - | 10 | μA | All logic inputs are static |
| I_{SOR} | Data out source current | 0.45 | - | 0.45 | 0.70 | - | 0.40 | | mA | $V_{OUT} = V_{DD} - 0.7\text{V}$ |
| I_{SINK} | Data out sink current | 0.45 | - | 0.45 | 0.70 | - | 0.40 | | mA | $V_{OUT} = 0.7\text{V}$ |
| C_{IN} | Logic input capacitance | - | 10 | - | - | 10 | - | 10 | pF | --- |

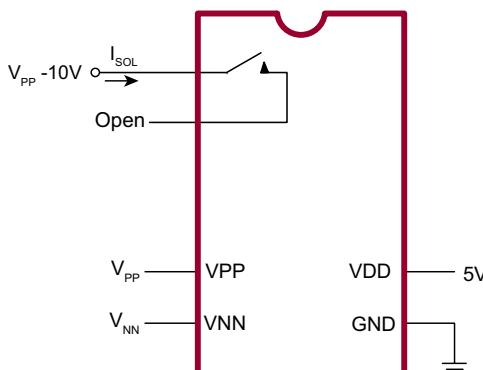
* See Test Circuits on page 5

AC Electrical Characteristics (Over recommended operating conditions unless otherwise specified)

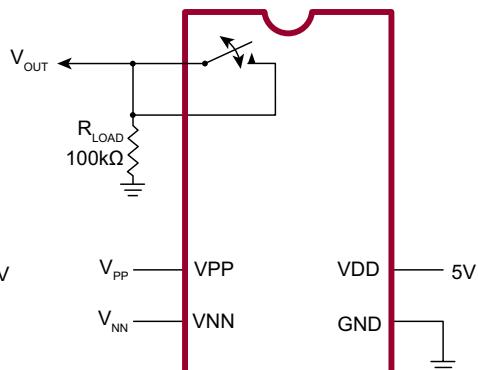
| Sym | Parameter | 0°C | | +25°C | | | +70°C | | Unit | Conditions |
|---------------|--|-----|-----|-------|-----|-----|-------|-----|---------|--|
| | | Min | Max | Min | Typ | Max | Min | Max | | |
| t_{SD} | Set up time before \overline{LE} rises | 25 | - | 25 | - | - | 25 | - | ns | --- |
| t_{WLE} | Time width of \overline{LE} | 56 | - | 56 | - | - | 56 | - | ns | $V_{DD} = 3.0V$ |
| | | 12 | - | 12 | - | - | 12 | - | | $V_{DD} = 5.0V$ |
| t_{DO} | Clock delay time to data out | 9.0 | 40 | 9.0 | - | 40 | 9.0 | 40 | ns | $V_{DD} = 3.0V$ |
| | | 8.0 | 30 | 8.0 | - | 30 | 8.0 | 30 | | $V_{DD} = 5.0V$ |
| t_{WCLR} | Time width of CLR | 55 | - | 55 | - | - | 55 | - | ns | --- |
| t_{SU} | Set up time data to clock | 21 | - | 21 | - | - | 21 | - | ns | $V_{DD} = 3.0V$ |
| | | 7.0 | - | 7.0 | - | - | 7.0 | - | | $V_{DD} = 5.0V$ |
| t_H | Hold time data from clock | 5.0 | - | 5.0 | - | - | 5.0 | - | ns | $V_{DD} = 3.0V$ |
| | | 5.0 | - | 5.0 | - | - | 5.0 | - | | $V_{DD} = 5.0V$ |
| f_{CLK} | Clock frequency | - | 8 | - | - | 8 | - | 8 | MHz | $V_{DD} = 3.0V$ |
| | | - | 20 | - | - | 20 | - | 20 | | $V_{DD} = 5.0V$ |
| t_R, t_F | Clock rise and fall times | - | 50 | - | - | 50 | - | 50 | ns | --- |
| t_{ON} | Turn ON time | - | 5.0 | - | - | 5.0 | - | 5.0 | μs | $V_{SIG} = V_{PP} - 10V, R_{LOAD} = 10k\Omega$ |
| t_{OFF} | Turn OFF time | - | 5.0 | - | - | 5.0 | - | 5.0 | | |
| dv/dt | Maximum V_{SIG} slew rate | - | 20 | - | - | 20 | - | 20 | V/ns | $V_{PP} = +40V, V_{NN} = -160V$ |
| | | - | 20 | - | - | 20 | - | 20 | | $V_{PP} = +100V, V_{NN} = -100V$ |
| | | - | 20 | - | - | 20 | - | 20 | | $V_{PP} = +160V, V_{NN} = -40V$ |
| K_O | OFF isolation | -30 | - | -30 | -33 | - | -30 | - | dB | $f = 5.0MHz, 1.0K\Omega//15pF$ load |
| | | -58 | - | -58 | -60 | - | -58 | - | | $f = 5.0MHz, 50\Omega$ load |
| K_{CR} | Switch crosstalk | -60 | - | -60 | -70 | - | -60 | - | dB | $f = 5.0MHz, 50\Omega$ load |
| I_{ID} | Output switch isolation diode current | - | 300 | - | - | 300 | - | 300 | mA | 300ns pulse width, 2.0% duty cycle |
| $C_{SG(OFF)}$ | OFF capacitance SW to GND | - | 14 | - | 9.0 | 14 | - | 14 | pF | $V_{SIG} = 0V, f = 1.0MHz$ |
| $C_{SG(ON)}$ | ON capacitance SW to GND | - | 17 | - | 12 | 17 | - | 17 | | |
| $+V_{SPK}$ | Output voltage spike (per switch) | - | - | - | - | 150 | - | - | mV | $V_{PP} = +40V, V_{NN} = -160V$ |
| | | - | - | - | - | 150 | - | - | | $R_{LOAD} = 50\Omega$ |
| | | - | - | - | - | 150 | - | - | | $V_{PP} = +100V, V_{NN} = -100V$ |
| | | - | - | - | - | 150 | - | - | | $R_{LOAD} = 50\Omega$ |
| | | - | - | - | - | 150 | - | - | | $V_{PP} = +160V, V_{NN} = -40V$ |
| | | - | - | - | - | 150 | - | - | | $R_{LOAD} = 50\Omega$ |
| QC | Charge injection (per switch) | - | - | - | 820 | - | - | - | pC | $V_{PP} = +40V, V_{NN} = -160V$ |
| | | - | - | - | 600 | - | - | - | | $V_{PP} = +100V, V_{NN} = -100V$ |
| | | - | - | - | 350 | - | - | - | | $V_{PP} = +160V, V_{NN} = -40V$ |

* See Test Circuits on page 5

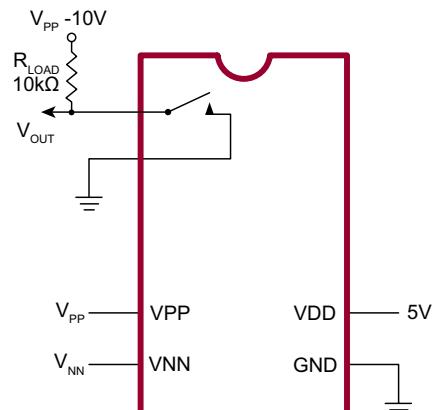
Test Circuits



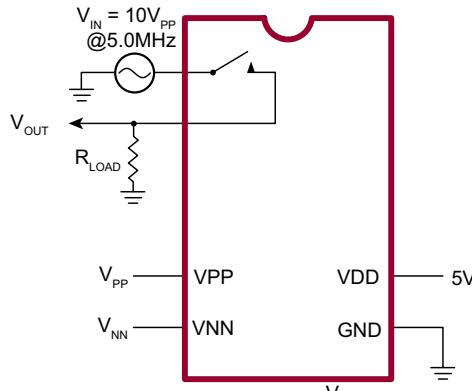
**Switch Off Leakage
per Switch**



**DC Offset Switch
ON/OFF**

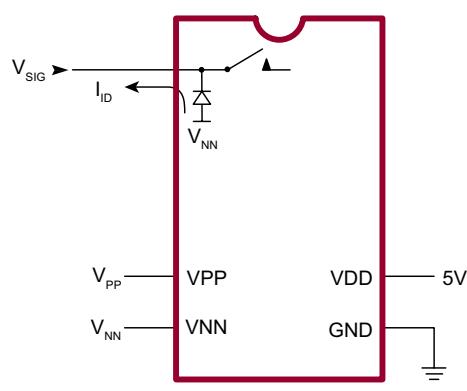


T_{ON}/T_{OFF} Test Circuit

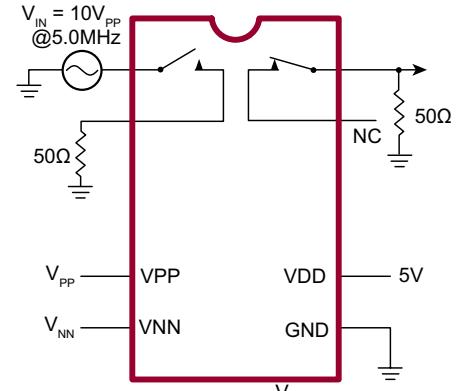


$$K_O = 20 \log \frac{V_{OUT}}{V_{IN}}$$

OFF Isolation

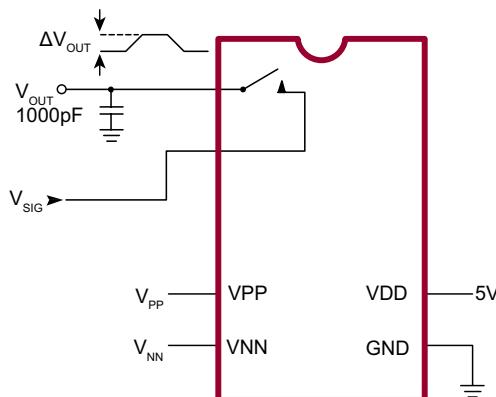


**Output Switch
Isolation Diode Current**



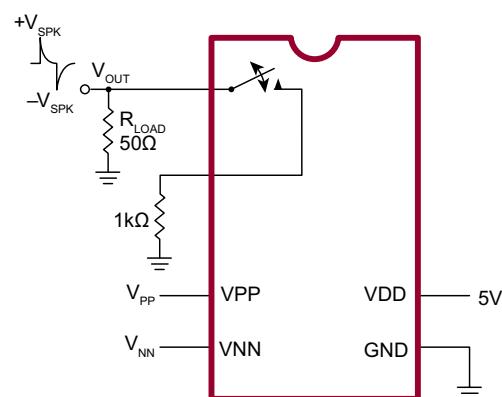
$$K_{CR} = 20 \log \frac{V_{OUT}}{V_{IN}}$$

Switch Crosstalk



$$Q = 1000pF \times \Delta V_{OUT}$$

Charge Injection



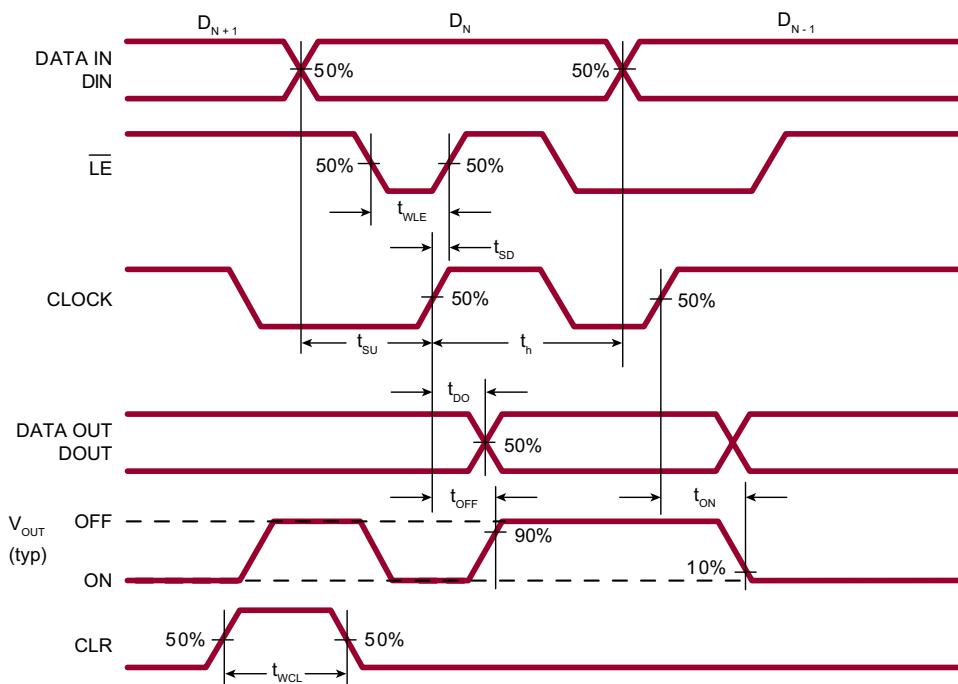
Output Voltage Spike

Truth Table

| D0 | D1 | ... | D15 | D16 | ... | D23 | \bar{LE} | CLR | SW0 | SW1 | ... | SW15 | SW16 | ... | SW23 |
|----|----|-----|-----|-----|-----|-----|------------|-----|-----|-----|-----|------|------|-----|---------------------|
| L | - | | - | - | | - | L | L | OFF | - | | - | - | | - |
| H | - | | - | - | | - | L | L | ON | - | | - | - | | - |
| - | L | | - | - | | - | L | L | - | OFF | | - | - | | - |
| - | H | | - | - | | - | L | L | - | ON | | - | - | | - |
| - | - | | - | - | | - | L | L | - | - | | - | - | | - |
| - | - | | - | - | | - | L | L | - | - | | - | - | | - |
| - | - | | - | - | | - | L | L | - | - | | - | - | | - |
| - | - | | - | - | | - | L | L | - | - | | - | - | | - |
| - | - | | - | - | | - | L | L | - | - | | - | - | | - |
| - | - | | - | - | | - | L | L | - | - | | - | - | | - |
| - | - | | - | - | | - | L | L | - | - | | - | - | | - |
| - | - | | - | - | | - | L | L | - | - | | - | - | | - |
| - | - | | - | - | | - | L | L | - | - | | - | - | | - |
| - | - | | - | - | | - | L | L | - | - | | - | - | | - |
| - | - | | - | - | | - | L | L | - | - | | - | - | | - |
| - | - | | - | - | | - | L | L | - | - | | - | - | | - |
| - | - | | - | - | | - | L | L | - | - | | - | - | | - |
| X | X | X | X | X | X | X | H | L | | | | | | | HOLD PREVIOUS STATE |
| X | X | X | X | X | X | X | X | H | | | | | | | ALL SWITCHES OFF |

Notes:

1. The 24 switches operate independently.
2. Serial data is clocked in on the L to H transition of the CLK.
3. All 24 switches go to a state retaining their latched condition at the rising edge of \bar{LE} . When \bar{LE} is low the shift registers data flow through the latch.
4. DOUT is high when data in the register 23 is high.
5. Shift registers clocking has no effect on the switch states if \bar{LE} is high.
6. The CLR clear input overrides all other inputs.

Logic Timing Waveforms

Pad Description - 64-Pad LFGA (LA)

| Pin | Name |
|-----|-------|
| A1 | SW22B |
| A2 | VNN |
| A3 | SW21B |
| A4 | SW20B |
| A5 | SW19B |
| A6 | SW18B |
| A7 | SW17B |
| A8 | SW16B |
| A9 | SW15B |
| A10 | SW15A |
| B1 | SW23B |
| B2 | SW23A |
| B3 | SW22A |
| B4 | SW21A |
| B5 | SW20A |
| B6 | SW19A |

| Pin | Name |
|-----|-------|
| B7 | SW18A |
| B8 | SW17A |
| B9 | SW16A |
| B10 | SW14B |
| C1 | N/C |
| C2 | VPP |
| C9 | SW14A |
| C10 | SW13B |
| D1 | CLR |
| D2 | NC |
| D9 | VNN |
| D10 | SW13A |
| E1 | LE |
| E2 | CLK |
| E9 | SW12B |
| E10 | SW12A |

| Pin | Name |
|-----|-------|
| F1 | VDD |
| F2 | GND |
| F9 | SW11B |
| F10 | SW11A |
| G1 | DIN |
| G2 | DOUT |
| G9 | SW10B |
| G10 | VNN |
| H1 | NC |
| H2 | VPP |
| H9 | SW10A |
| H10 | SW9B |
| J1 | SW0A |
| J2 | SW0B |
| J3 | SW1B |
| J4 | SW2B |

| Pin | Name |
|-----|------|
| J5 | SW3B |
| J6 | SW4B |
| J7 | SW5B |
| J8 | SW6B |
| J9 | SW7B |
| J10 | SW9A |
| K1 | SW1A |
| K2 | VNN |
| K3 | SW2A |
| K4 | SW3A |
| K5 | SW4A |
| K6 | SW5A |
| K7 | SW6A |
| K8 | SW7A |
| K9 | SW8A |
| K10 | SW8B |

Ball Description - 64-Ball LFGA (LB)

| Pin | Name |
|-----|-------|
| A1 | SW22B |
| A2 | VNN |
| A3 | SW21B |
| A4 | SW20B |
| A5 | SW19B |
| A6 | SW18B |
| A7 | SW17B |
| A8 | SW16B |
| A9 | SW15B |
| A10 | SW15A |
| B1 | SW23B |
| B2 | SW23A |
| B3 | SW22A |
| B4 | SW21A |
| B5 | SW20A |
| B6 | SW19A |

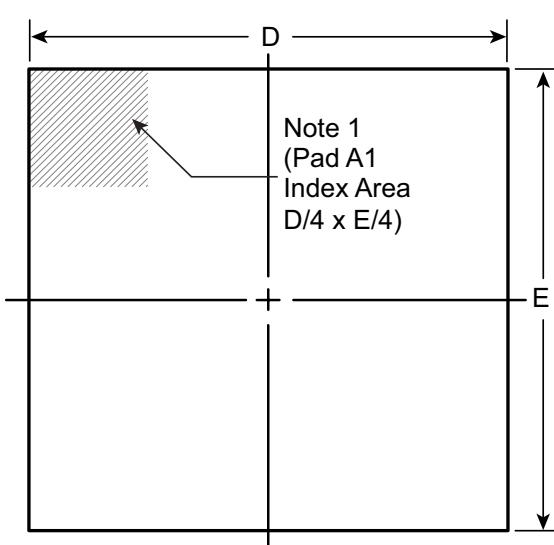
| Pin | Name |
|-----|-------|
| B7 | SW18A |
| B8 | SW17A |
| B9 | SW16A |
| B10 | SW14B |
| C1 | N/C |
| C2 | VPP |
| C9 | SW14A |
| C10 | SW13B |
| D1 | CLR |
| D2 | NC |
| D9 | VNN |
| D10 | SW13A |
| E1 | LE |
| E2 | CLK |
| E9 | SW12B |
| E10 | SW12A |

| Pin | Name |
|-----|-------|
| F1 | VDD |
| F2 | GND |
| F9 | SW11B |
| F10 | SW11A |
| G1 | DIN |
| G2 | DOUT |
| G9 | SW10B |
| G10 | VNN |
| H1 | NC |
| H2 | VPP |
| H9 | SW10A |
| H10 | SW9B |
| J1 | SW0A |
| J2 | SW0B |
| J3 | SW1B |
| J4 | SW2B |

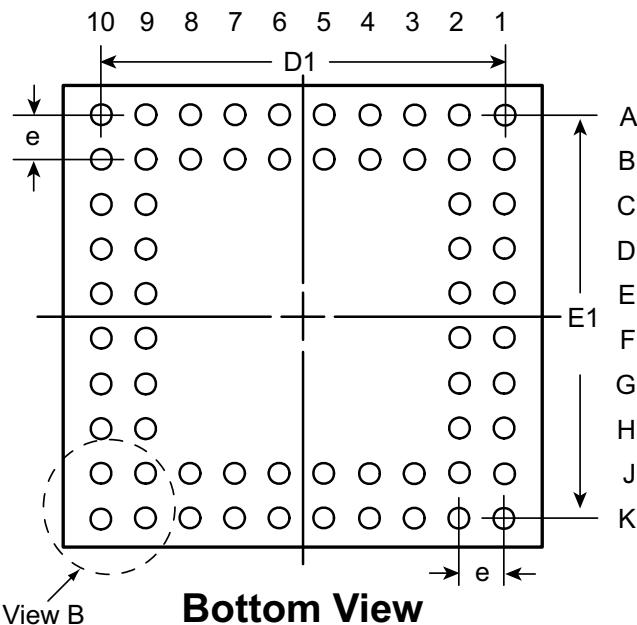
| Pin | Name |
|-----|------|
| J5 | SW3B |
| J6 | SW4B |
| J7 | SW5B |
| J8 | SW6B |
| J9 | SW7B |
| J10 | SW9A |
| K1 | SW1A |
| K2 | VNN |
| K3 | SW2A |
| K4 | SW3A |
| K5 | SW4A |
| K6 | SW5A |
| K7 | SW6A |
| K8 | SW7A |
| K9 | SW8A |
| K10 | SW8B |

64-Pad LFGA Package Outline (LA)

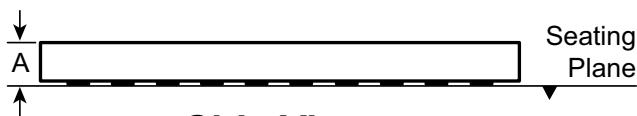
7.00x7.00mm body, 0.85mm height (max), 0.65mm pitch



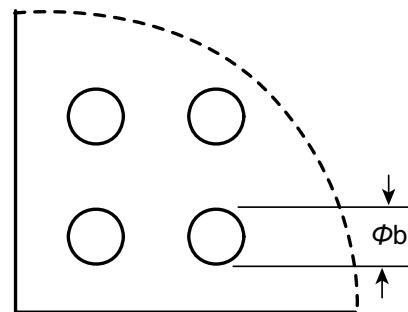
Top View



Bottom View



Side View



View B

Notes:

1. Pad A1 identifier must be located in the index area indicated. Pad A1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.

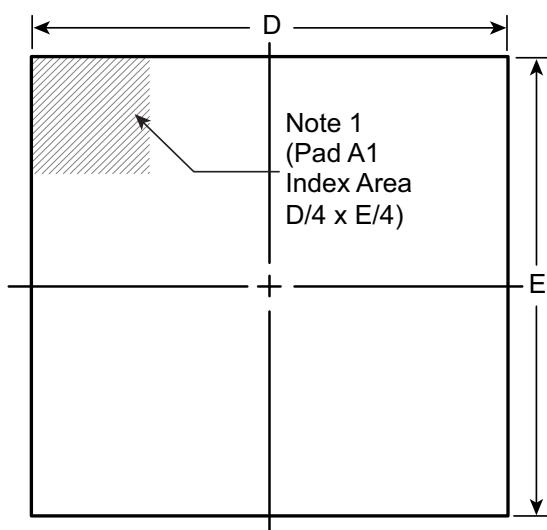
| Symbol | A | b | D | D1 | E | E1 | e |
|-------------------|-----|------|------|-------|-------|------|------|
| Dimension (mm) | MIN | 0.75 | 0.25 | 6.925 | 6.925 | 5.85 | 0.65 |
| | NOM | 0.80 | 0.30 | 7.000 | 7.000 | BSC | BSC |
| | MAX | 0.85 | 0.35 | 7.075 | 7.075 | BSC | BSC |

Drawings not to scale.

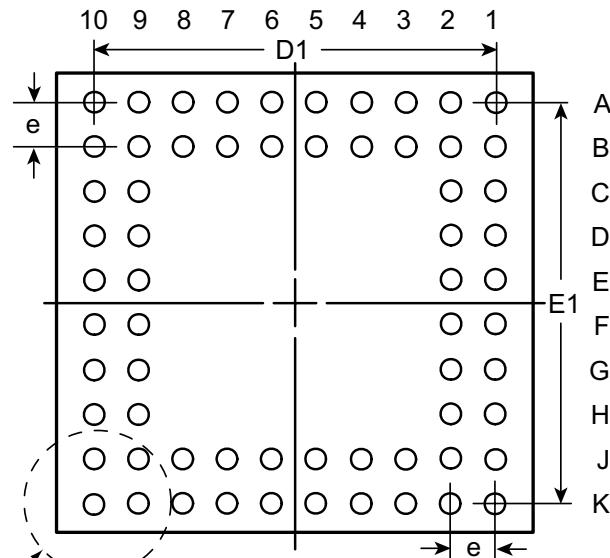
Supertex Doc. #: DSFP-HV2662, Version A021511.

64-Ball LFGA Package Outline (LB)

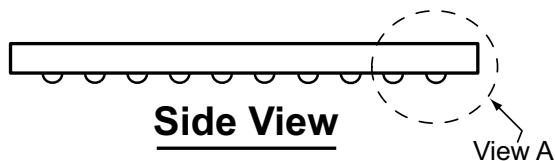
7.00x7.00mm body, 1.00mm height (max), 0.65mm pitch



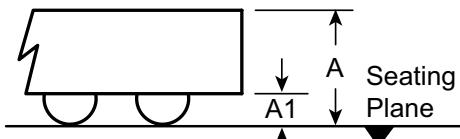
Top View



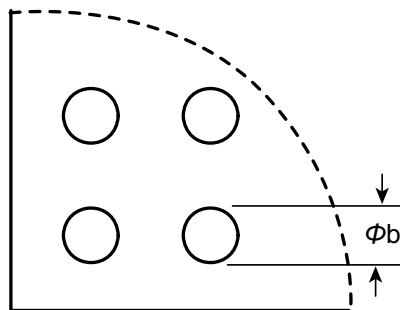
Bottom View



Side View



View A



View B

Notes:

- Ball A1 identifier must be located in the index area indicated. Ball A1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.

| Symbol | A | A1 | b | D | D1 | E | E1 | e |
|----------------|-----|------|------|------|-------|-------|------|------|
| Dimension (mm) | MIN | 0.90 | 0.10 | 0.25 | 6.925 | 6.925 | 5.85 | 0.65 |
| | NOM | 0.95 | 0.15 | 0.30 | 7.000 | | | |
| | MAX | 1.00 | 0.20 | 0.35 | 7.075 | | | |

Drawings not to scale.

Supertex Doc. #: DSPD-64LFGALB, Version A021511.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

Supertex inc. does not recommend the use of its products in life support applications, and will not knowingly sell them for use in such applications unless it receives an adequate "product liability indemnification insurance agreement." **Supertex inc.** does not assume responsibility for use of devices described, and limits its liability to the replacement of the devices determined defective due to workmanship. No responsibility is assumed for possible omissions and inaccuracies. Circuitry and specifications are subject to change without notice. For the latest product specifications refer to the **Supertex inc.** (website: <http://www.supertex.com>)

Данный компонент на территории Российской Федерации**Вы можете приобрести в компании MosChip.**

Для оперативного оформления запроса Вам необходимо перейти по данной ссылке:

<http://moschip.ru/get-element>

Вы можете разместить у нас заказ для любого Вашего проекта, будь то серийное производство или разработка единичного прибора.

В нашем ассортименте представлены ведущие мировые производители активных и пассивных электронных компонентов.

Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибуторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ Р В 0015-002 и ЭС РД 009

Офис по работе с юридическими лицами:

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:

moschip.ru
moschip.ru_4

moschip.ru_6
moschip.ru_9