LC²MOS, High Speed 1-, 4-, and 8-Channel 10-Bit ADCs

AD7776/AD7777/AD7778

FEATURES
AD7776: 1-Channel
AD7777: 4-Channel
AD7778: 8-Channel
Fast 10-Bit ADC: 2.5 μs Worst Case
+5 V Only
Half-Scale Conversion Option
Fast Interface Port
Power-Down Mode

APPLICATIONS
HDD Servos
Instrumentation

GENERAL DESCRIPTION

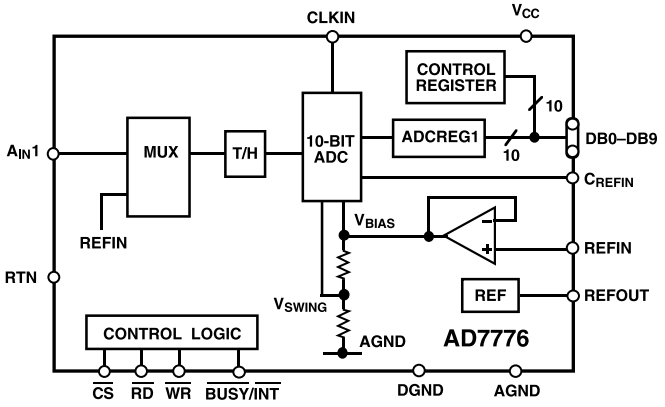
The AD7776/AD7777/AD7778 are a family of high speed, multichannel, 10-bit ADCs primarily intended for use in R/W head positioning servos found in high density hard disk drives. They have unique input signal conditioning features that make them ideal for use in such single supply applications.

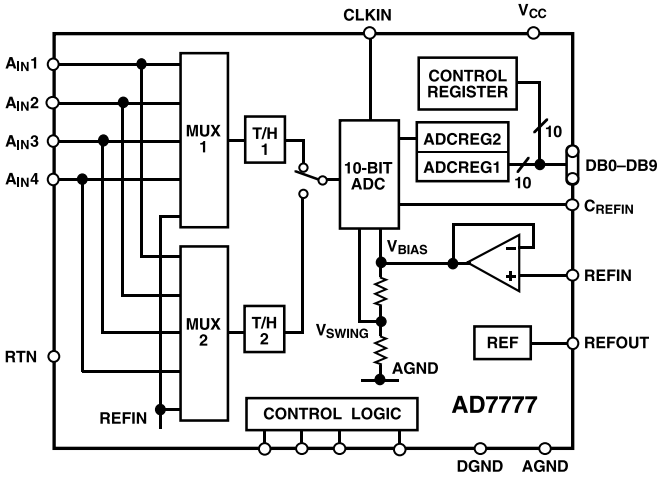
By setting a bit in a control register within both the four-channel version, AD7777, and the eight-channel version, AD7778, the input channels can either be independently sampled or any two channels can be simultaneously sampled. For all versions, the specified input signal range is of the form $V_{BIAS} \pm V_{SWING}$. However, if the RTN pin is biased at, for example, 2 V the analog input signal range becomes 0 V to +2 V for all input channels. This is covered in more detail under the section Changing the Analog Input Voltage Range. The voltage V_{BIAS} is the offset of the ADC's midpoint code from ground and is supplied either by an onboard reference available to the user (REFOUT) or by an external voltage reference applied to REFIN. The full-scale range (FSR) of the ADC is equal to 2 V_{SWING} where V_{SWING} is nominally equal to REFIN/2. Additionally, when placed in the half-scale conversion mode, the value of REFIN is converted. This allows the channel offset(s) to be measured.

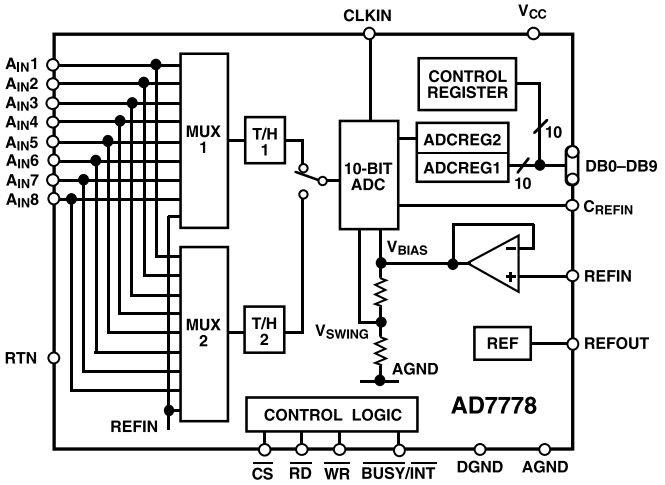
Control register loading and ADC register reading, channel select and conversion start are under the control of the μP. The twos complement coded ADCs are easily interfaced to a standard 16-bit MPU bus via their 10-bit data port and standard microprocessor control lines.

The AD7776/AD7777/AD7778 are fabricated in linear compatible CMOS (LC²MOS), an advanced, mixed technology process that combines precision bipolar circuits with low power CMOS logic. The AD7776 is available in a 24-lead SOIC package; the AD7777 is available in both 28-lead DIP and 28-lead SOIC packages; the AD7778 is available in a 44-lead PQFP package.

FUNCTIONAL BLOCK DIAGRAMS







REV. A

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 www.analog.com
Fax: 617/326-8703

AD7776/AD7777/AD7778–SPECIFICATIONS (V_{CC} = +5 V ± 5%; AGND = DGND = 0 V; CLKIN = 8 MHz; RTN = 0 V; C_{REFIN} = 10 nF; all specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	A Versions[1]	Units	Conditions/Comments
DC ACCURACY			
Resolution[2]	10	Bits	
Relative Accuracy	±1	LSB max	See Terminology
Differential Nonlinearity	±1	LSB max	No Missing Codes; See Terminology
Bias Offset Error	±12	LSB max	See Terminology
Bias Offset Error Match	10	LSB max	Between Channels, AD7777/AD7778 Only; See Terminology
Plus or Minus Full-Scale Error	±12	LSB max	See Terminology
Plus or Minus Full-Scale Error Match	10	LSB max	Between Channels, AD7777/AD7778 Only; See Terminology
ANALOG INPUTS			
Input Voltage Range			
All Inputs	$V_{BIAS} \pm V_{SWING}$	V min/V max	
Input Current	+200	µA max	$V_{IN} = V_{BIAS} \pm V_{SWING}$; Any Channel
REFERENCE INPUT			
REFIN	1.9/2.1	V min/V max	For Specified Performance
REFIN Input Current	+200	µA max	
REFERENCE OUTPUT			
REFOUT	1.9/2.1	V min/V max	Nominal REFOUT = 2.0 V
DC Output Impedance	5	Ω typ	
Reference Load Change	±2	mV max	For Reference Load Current Change of 0 to ±500 µA
	±5	mV max	For Reference Load Current Change of 0 to ±1 mA
			Reference Load Should Not Change During Conversion
Short Circuit Current[3]	20	mA max	See Terminology
LOGIC OUTPUTS			
DB0–DB9, $\overline{BUSY}/\overline{INT}$			
V_{OL}, Output Low Voltage	0.4	V max	I_{SINK} = 1.6 mA
V_{OH}, Output High Voltage	4.0	V min	I_{SOURCE} = 200 µA
Floating State Leakage Current	±10	µA max	
Floating State Capacitance[3]	10	pF max	
ADC Output Coding	Twos Complement		
LOGIC INPUTS			
DB0–DB9, $\overline{CS}$, $\overline{WR}$, $\overline{RD}$, CLKIN			
Input Low Voltage, V_{INL}	0.8	V max	
Input High Voltage, V_{INH}	2.4	V min	
Input Leakage Current	10	µA max	
Input Capacitance[3]	10	pF max	
CONVERSION TIMING			
Acquisition Time	4.5 t_{CLKIN}	ns min	See Terminology
	5.5 t_{CLKIN} + 70	ns max	
Single Conversion	14 t_{CLKIN}	ns max	
Double Conversion	28 t_{CLKIN}	ns max	
t_{CLKIN}	125/500	ns min/ns max	Period of Input Clock CLKIN
t_{CLKIN} High	50	ns min	Minimum High Time for CLKIN
t_{CLKIN} Low	40	ns min	Minimum Low Time for CLKIN
POWER REQUIREMENTS			
V_{CC} Range	4.75/5.25	V min/V max	For Specified Performance
I_{CC}, Normal Mode	15	mA max	$\overline{CS}$ = $\overline{RD}$ = +5 V, CR8 = 0
I_{CC}, Power-Down Mode	1.5	mA max	CR8 = 1. All Linear Circuitry OFF
Power-Up Time to Operational			
Specifications	500	µs max	From Power-Down Mode
DYNAMIC PERFORMANCE			See Terminology
Signal to Noise and Distortion			
S/(N+D) Ratio	–56	dB min	V_{IN} = 99.88 kHz Full-Scale Sine Wave with $f_{SAMPLING}$ = 380.95 kHz
Total Harmonic Distortion (THD)	–60	dB min	V_{IN} = 99.88 kHz Full-Scale Sine Wave with $f_{SAMPLING}$ = 380.95 kHz
Intermodulation Distortion (IMD)	–75	dB typ	fa = 103.2 kHz, fb = 96.5 kHz with $f_{SAMPLING}$ = 380.95 kHz. Both Signals Are Sine Waves at Half-Scale Amplitude
Channel-to-Channel Isolation	–90	dB typ	V_{IN} = 100 kHz Full-Scale Sine Wave with $f_{SAMPLING}$ = 380.95 kHz

NOTES

[1]Temperature range as follows: A = –40°C to +85°C.

[2]1 LSB = $(2 \times V_{SWING})/1024$ = 1.95 mV for V_{SWING} = 1.0 V.

[3]Guaranteed by design, not production tested.

Specifications subject to change without notice.

TIMING SPECIFICATIONS[1, 2] (V_{CC} = +5 V ± 5%; AGND = DGND = 0 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	Label	Limit at T_{MIN} to T_{MAX}	Unit	Test Conditions/Comments
INTERFACE TIMING				
$\overline{CS}$ Falling Edge to $\overline{WR}$ or $\overline{RD}$ Falling Edge	t_1	0	ns min	
$\overline{WR}$ or $\overline{RD}$ Rising Edge to $\overline{CS}$ Rising Edge	t_2	0	ns min	
$\overline{WR}$ Pulsewidth	t_3	53	ns min	
$\overline{CS}$ or $\overline{RD}$ Active to Valid Data[3, 4]	t_4	60	ns max	Timed from Whichever Occurs Last
Bus Relinquish Time after $\overline{RD}$[3, 5]	t_5	10	ns min	
		45	ns max	
Data Valid to $\overline{WR}$ Rising Edge	t_6	55	ns min	
Data Valid after $\overline{WR}$ Rising Edge	t_7	10	ns min	
$\overline{WR}$ Rising Edge to $\overline{BUSY}$ Falling Edge	t_8	1.5 t_{CLKIN}	ns min	CR9 = 0
		2.5 t_{CLKIN} + 70	ns max	
$\overline{WR}$ Rising Edge to $\overline{BUSY}$ Rising Edge or $\overline{INT}$ Falling Edge	t_9	19.5 t_{CLKIN} + 70	ns max	Single Conversion, CR6 = 0
	t_{10}	33.5 t_{CLKIN} + 70	ns max	Double Conversion, CR6 = 1
$\overline{WR}$ or $\overline{RD}$ Falling Edge to $\overline{INT}$ Rising Edge	t_{11}	60	ns max	CR9 = 1

NOTES
[1]See Figures 1 to 3.
[2]All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.
[3]100% production tested. All other times are guaranteed by design, not production tested.
[4]t_4 is measured with the load circuit of Figure 4 and defined as the time required for an output to cross 0.8 V or 2.4 V.
[5]t_5 is derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 4. The measured time is then extrapolated back to remove the effects of charging or discharging the 100 pF capacitor. This means that the time t_5 quoted above is the true bus relinquish time of the device and, as such, is independent of the external bus loading capacitance.

Specifications subject to change without notice.

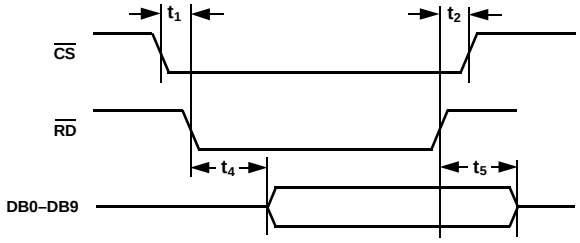


Figure 1. Read Cycle Timing

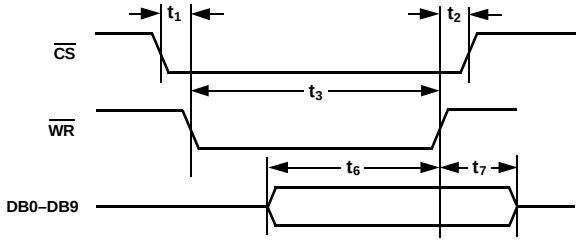


Figure 2. Write Cycle Timing

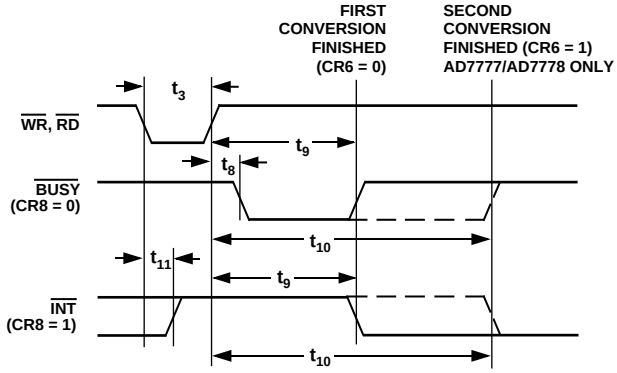


Figure 3. $\overline{BUSY}/\overline{INT}$ Timing

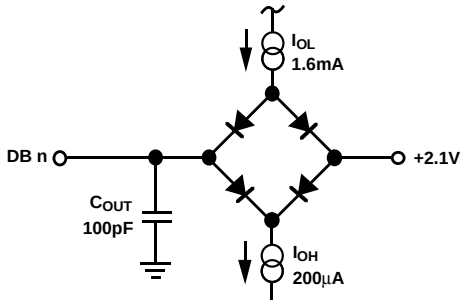


Figure 4. Load Circuit for Bus Timing Characteristics

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{CC} to AGND or DGND . . . . . –0.3 V, +7 V
AGND, RTN to DGND . . . . . –0.3 V, V_{CC} + 0.3 V
$\overline{CS}$, $\overline{RD}$, $\overline{WR}$, CLKIN, DB0–DB9,
$\overline{BUSY}/\overline{INT}$ to DGND . . . . . –0.3 V, V_{CC} + 0.3 V
Analog Input Voltage to AGND . . . . . –0.3 V, V_{CC} + 0.3 V
REFOUT to AGND . . . . . –0.3 V, V_{CC} + 0.3 V
REFIN to AGND . . . . . –0.3 V, V_{CC} + 0.3 V
Operating Temperature Range
All Versions . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Junction Temperature . . . . . +150°C
DIP Package, Power Dissipation . . . . . 875 mW
θ_{JA} Thermal Impedance . . . . . 75°C/W
Lead Temperature, Soldering (10 sec) . . . . . +260°C
SOIC Packages, Power Dissipation . . . . . 875 mW
θ_{JA} Thermal Impedance . . . . . 75°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) . . . . . 215°C
Infrared (15 sec) . . . . . 220°C
PQFP Package, Power Dissipation . . . . . 500 mW
θ_{JA} Thermal Impedance . . . . . 95°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) . . . . . 215°C
Infrared (15 sec) . . . . . 220°C

*Stresses above those listed under absolute maximum ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model	Temperature Range	No. of Channels	Package Option*
AD7776AR	–40°C to +85°C	1	RW-24
AD7777AN	–40°C to +85°C	4	N-28
AD7777AR	–40°C to +85°C	4	RW-28
AD7778AS	–40°C to +85°C	8	S-44

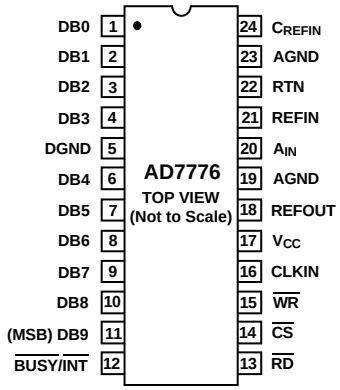
*R = SOIC, N = PDIP, S = PQFP

CAUTION

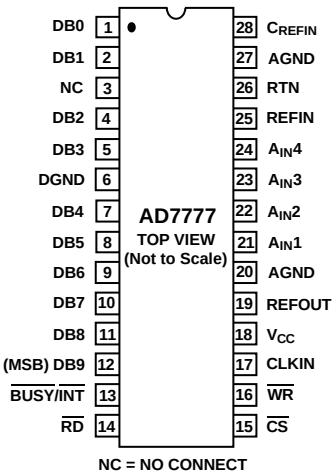
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7776/AD7777/AD7778 feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS

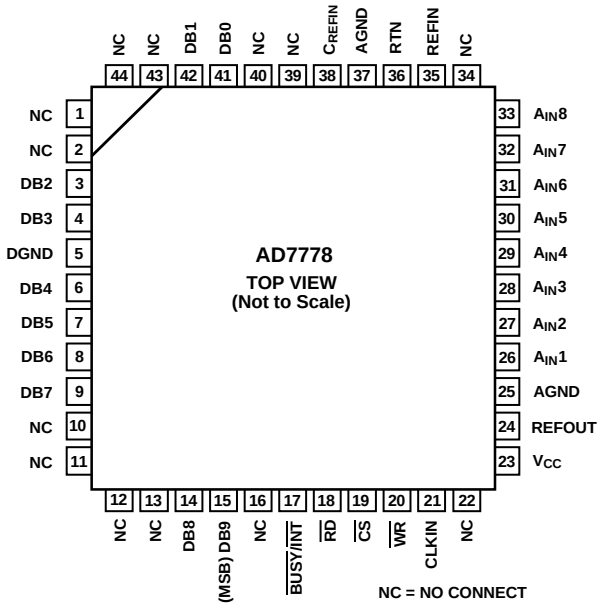
24-Lead SOIC



28-Lead PDIP and SOIC



44-Lead PQFP



PIN FUNCTION DESCRIPTION

Mnemonic	Description
V_{CC}	+5 V Power Supply.
AGND	Analog Ground.
DGND	Digital Ground. Ground reference for digital circuitry.
DB0–DB9	Input/Output Data Bus. This is a bidirectional data port from which ADC output data may be read and to which control register data may be written.
$\overline{BUSY/INT}$	Busy/Interrupt Output. Active low logic output indicating A/D converter status. This logic output has two modes of operation depending on whether location CR9 of the control register has been set low or high: If CR9 is set low, the $\overline{BUSY/INT}$ output behaves as a $\overline{BUSY}$ signal. The $\overline{BUSY}$ signal goes low and stays low for the duration of a single conversion, or if simultaneous sampling has been selected, $\overline{BUSY}$ stays low for the duration of both conversions. If CR9 is set high, $\overline{BUSY/INT}$ output behaves as an INTERRUPT signal. The $\overline{INT}$ signal goes low and remains low after either a single conversion is completed or after a double conversion is completed if simultaneous sampling has been selected. With CR9 high, the falling edge of $\overline{WR}$ or $\overline{RD}$ resets the $\overline{INT}$ line high.
$\overline{CS}$	Chip Select Input. The device is selected when this input is low.
$\overline{WR}$	Write Input (Active Low). It is used in conjunction with $\overline{CS}$ to write data to the control register. Data is latched to the registers on the rising edge of $\overline{WR}$. Following the rising edge of $\overline{WR}$, the analog input is acquired and a conversion is started.
$\overline{RD}$	Read Input (Active Low). It is used in conjunction with $\overline{CS}$ to enable the data outputs from the ADC registers.
$A_{IN}1–8$	Analog Inputs 1–8. The analog input range is $V_{BIAS} \pm V_{SWING}$ where V_{BIAS} and V_{SWING} are defined by the reference voltage applied to REFIN. Input resistance between any of the analog input pins and AGND is 10 kΩ or greater.
REFIN	Voltage Reference Input. The AD7776/AD7777/AD7778 are specified over a voltage reference range of 1.9 V to 2.1 V with a nominal value of 2.0 V. This REFIN voltage provides the V_{BIAS} and V_{SWING} levels for the input channel(s). V_{BIAS} is equal to REFIN and V_{SWING} is nominally equal to REFIN/2. Input resistance between this REFIN pin and AGND is 10 kΩ or greater.
REFOUT	Voltage Reference Output. This pin provides the internal voltage reference, which is nominally 2.0 V. It can provide the bias voltage (V_{BIAS}) for the input channel(s).
C_{REFIN}	Reference Decoupling Capacitor. A 10 nF capacitor must be connected from this pin to AGND to ensure correct operation of the high speed ADC.
RTN	Signal Return Path for the input channel(s). Normally RTN is connected to AGND at the package.

CIRCUIT DESCRIPTION

ADC Transfer Function

For all versions, an input signal of the form $V_{BIAS} \pm V_{SWING}$ is expected. This V_{BIAS} signal level operates as a pseudo ground to which all input signals must be referred. The V_{BIAS} level is determined by the voltage applied to the REFIN pin. This can be driven by an external voltage source or, alternatively, by the onboard 2 V reference, available at REFOUT. The magnitude of the input signal swing is equal to $V_{BIAS}/2$ (or REFIN/2) and is set internally. With a REFIN of 2 V, the analog input signal level varies from 1 V to 3 V, i.e., 2 ± 1 V. Figure 5 shows the transfer function of the ADC and its relationship to V_{BIAS} and V_{SWING}. The half-scale two's complement code of the ADC, 000 Hex (00 0000 0000 Binary), occurs at an input voltage equal to V_{BIAS}. The input full-scale range of the ADC is equal to 2 V_{SWING}, so that the Plus Full-Scale transition (1FE to 1FF) occurs at a voltage equal to $V_{BIAS} + V_{SWING} – 1.5$ LSBs, and the minus full-scale code transition (200 to 201) occurs at a voltage $V_{BIAS} – V_{SWING} + 0.5$ LSBs.

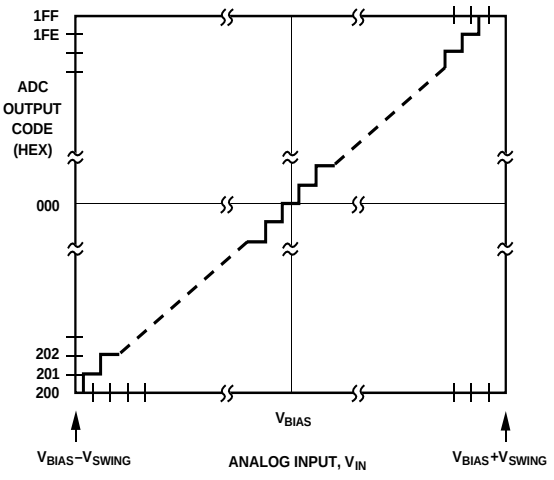


Figure 5. ADC Transfer Function

CONTROL REGISTER

The control register is 10-bit wide and can only be written to. On power-on, all locations in the control register are automatically loaded with 0s. For the single channel AD7776, locations CR0 to CR6 of the control register are "don't cares." For the quad channel AD7777, locations CR2 and CR5 are "don't cares." Individual bit functions are described below.

CR0–CR2: Channel Address Locations. Determines which channel is selected and converted for single-channel operation. For simultaneous sampling operation, CR0–CR2 holds the address of one of the two channels to be sampled.

AD7776

CR2	CR1	CR0	Function
X*	X	X	Select $A_{IN}1$

*X = Don't Care

AD7777

CR2	CR1	CR0	Function
X*	0	0	Select $A_{IN}1$
X	0	1	Select $A_{IN}2$
X	1	0	Select $A_{IN}3$
X	1	1	Select $A_{IN}4$

*X = Don't Care

AD7778

CR2	CR1	CR0	Function
0	0	0	Select $A_{IN}1$
0	0	1	Select $A_{IN}2$
0	1	0	Select $A_{IN}3$
0	1	1	Select $A_{IN}4$
1	0	0	Select $A_{IN}5$
1	0	1	Select $A_{IN}6$
1	1	0	Select $A_{IN}7$
1	1	1	Select $A_{IN}8$

CR3–CR5: Channel Address Locations. Only applicable for simultaneous sampling with the AD7777 or AD7778 when CR3–CR5 holds the address of the second channel to be sampled.

AD7777

CR5	CR4	CR3	Function
X*	0	0	Select $A_{IN}1$
X	0	1	Select $A_{IN}2$
X	1	0	Select $A_{IN}3$
X	1	1	Select $A_{IN}4$

*X = Don't Care

AD7778

CR5	CR4	CR3	Function
0	0	0	Select $A_{IN}1$
0	0	1	Select $A_{IN}2$
0	1	0	Select $A_{IN}3$
0	1	1	Select $A_{IN}4$
1	0	0	Select $A_{IN}5$
1	0	1	Select $A_{IN}6$
1	1	0	Select $A_{IN}7$
1	1	1	Select $A_{IN}8$

CR6: Determines whether operation is on a single channel or simultaneous sampling on two channels. Location CR6 is a "don't care" for the AD7776.

CR6	Function
0	Single channel operation. Channel select address is contained in locations CR0–CR2.
1	Two channels simultaneously sampled and sequentially converted. Channel select addresses contained in locations CR0–CR2 and CR3–CR5.

CR7: Determines whether the device is in the normal operating mode or in the half-scale test mode.

CR7	Function
0	Normal Operating Mode
1	Half-Scale Test Mode

In the half-scale test mode, REFIN is internally connected as an analog input(s). In this mode, locations CR0–CR2 and CR3–CR5 are all "don't cares" since it is REFIN which is converted. For the AD7777 and AD7778, the contents of location CR6 still determine whether a single or a double conversion is carried out on the REFIN level.

CR8: Determines whether the device is in the normal operating mode or in the power-down mode.

CR8	Function
0	Normal Operating Mode
1	Power-Down Mode

In the power-down mode all linear circuitry is turned off and the REFOUT output is weakly (5 kΩ) pulled to AGND. The input impedance of the analog inputs and of the REFIN input remains the same in either normal mode or power-down mode. See under Circuit Description—Power-Down Mode.

CR9: Determines whether $\overline{BUSY}/\overline{INT}$ output flag goes low and remains low during conversion(s) or else goes low and remains low after the conversion(s) is (are) complete.

CR9	$\overline{BUSY}/\overline{INT}$ Functionality
0	Output goes low and remains low during conversion(s).
1	Output goes low and remains low after conversion(s) is (are) complete.

ADC Conversion Start Timing

Figure 6 shows the operating waveforms for the start of a conversion cycle. On the rising edge of $\overline{WR}$, the conversion cycle starts with the acquisition and tracking of the selected ADC channel, $A_{IN}1$–8. The analog input voltage is held 40 ns (typically) after the first rising edge of CLKIN following four complete CLKIN cycles. If t_D in Figure 6 is greater than 12 ns, the falling edge of CLKIN as shown is seen as the first falling clock edge. If t_D is less than 12 ns, the first falling clock edge to be recognized does not occur until one cycle later.

Following the "hold" on the analog input(s), two complete CLKIN cycles are allowed for settling purposes before the MSB decision is made. The actual decision point occurs approximately 40 ns after the rising edge of CLKIN as shown in Figure 6. Two more CLKIN cycles are allowed for the second MSB decision. The succeeding bit decisions are made approximately 40 ns after each rising edge of CLKIN until the conversion is complete. At the end of conversion, if a single conversion has been requested (CR6 = 0), the $\overline{BUSY}/\overline{INT}$ line changes state (as programmed by CR9) and the SAR contents are transferred to the first register ADCREG1. The SAR is then reset in readiness for a new conversion. If simultaneous sampling has been requested (CR6 = 1), no change occurs in the status of the $\overline{BUSY}/\overline{INT}$ output, and the ADC automatically starts the second conversion. At the end of this conversion, the $\overline{BUSY}/\overline{INT}$ line changes state (as programmed by CR9) and the SAR contents are transferred to the second register, ADCREG2.

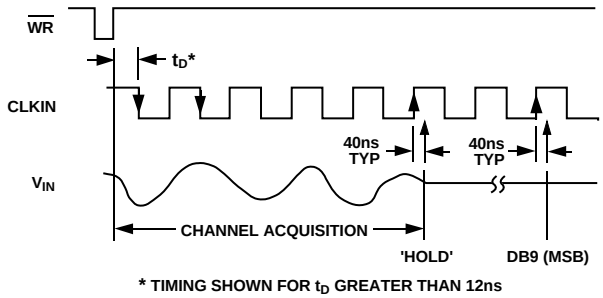


Figure 6. ADC Conversion Start Timing

Track-and-Hold

The track-and-hold (T/H) amplifiers on the analog input(s) of the AD7776/AD7777/AD7778 allow the ADC to accurately convert an input sine wave of 2 V peak-peak amplitude up to a frequency of 189 kHz, the Nyquist frequency of the ADC when operated at its maximum throughput rate of 378 kHz. This maximum rate of conversion includes conversion time and the time between conversions. Because the input bandwidth of the track-and-hold is much greater than 189 kHz, the input signal should be band limited to avoid folding unwanted signals into the band of interest.

Power-Down

The AD7776/AD7777/AD7778 can be placed in a power-down mode simply by writing a logic high to location CR8 of the control register. The following changes are effected immediately upon writing a "1" to location CR8:

- Any conversion in progress is terminated.
- If a conversion is in progress, the leading edge of $\overline{WR}$ immediately drives the $\overline{BUSY}/\overline{INT}$ output high.
- All the linear circuitry is turned off.
- The REFOUT output stops being driven and is weakly (5 kΩ) pulled to analog ground.

Control inputs $\overline{CS}$, $\overline{WR}$, and $\overline{RD}$ retain their purpose while the AD7776/AD7777/AD7778 is in power-down mode. If no conversions are in progress when the AD7776/AD7777/AD7778 is placed into power-down mode, the contents of the ADC registers, ADCREG1 and ADCREG2, are retained during power-down and can be read as normal. On returning to normal operating mode, a new conversion (or conversions, dependent on CR6) is automatically started. Upon completion, the invalid conversion results are loaded into the ADC registers, losing the previous valid results.

To achieve the lowest possible power consumption in the power-down mode, special attention must be paid to the state of the digital and analog inputs and outputs:

- Because each analog input channel sees a resistive divider to AGND, the input resistance of which does not change between normal and power-down modes, driving the analog input signals to 0 V or as close as possible to 0 V minimizes the power dissipated in the input signal conditioning circuitry.
- Similarly, the REFIN input sees a resistive divider to AGND, the input resistance of which does not change between normal and power-down modes. If an external reference is being used, then driving this reference input to 0 V or as close as possible to 0 V minimizes the power dissipated in the input signal conditioning circuitry.
- Since the REFOUT pin is pulled to AGND via, typically, a 5 kΩ resistor, any voltage above 0 V that this output may be pulled to by external circuitry dissipates unnecessary power.
- Digital inputs $\overline{CS}$, $\overline{WR}$, and $\overline{RD}$ should all be held at V_{CC} or as close as possible. CLKIN should be held as close as possible to either 0 V or V_{CC}.
- Since the $\overline{BUSY}/\overline{INT}$ output is actively driven to a logic high, any loading on this pin to 0 V dissipates power.

The AD7776/AD7777/AD7778 comes out of the power-down mode when a Logic "0" is written to location CR8 of the control register. Note that the contents of the other locations in the control register are retained when the device is placed in power-down and are valid when power is restored. However, coming out of power-down provides an opportunity to reload the complete contents of the control register without any extra instructions.

Microprocessor Interfacing Circuits

The AD7776/AD7777/AD7778 family of ADCs is intended to interface to DSP machines such as the ADSP-2101, ADSP-2105, the TMS320 family and microcontrollers such as the 80C196 family.

Figure 7 shows the AD7776/AD7777/AD7778 interfaced to the TMS320C10 at 20.5 MHz and the TMS320C14 at 25 MHz. Figure 8 shows the interface with the TMS320C25 at 40 MHz. Note that one wait state is required with this interface. The ADSP-2101-50 and the ADSP-2105-40 interface is shown in Figure 9. One wait state is required with these machines.

Figure 10 shows the interface with the 80C196KB at 12 MHz and the 80C196KC at 16 MHz. One wait state is required with the 16 MHz machine. The 80C196 is configured to operate with a 16-bit multiplexed address/data bus.

Table I provides a truth table for the AD7776/AD7777/AD7778 and summarizes their microprocessor interfacing features. Note that a read instruction to any of the devices while a conversion is in progress immediately stops that conversion and returns unreliable data over the data bus.

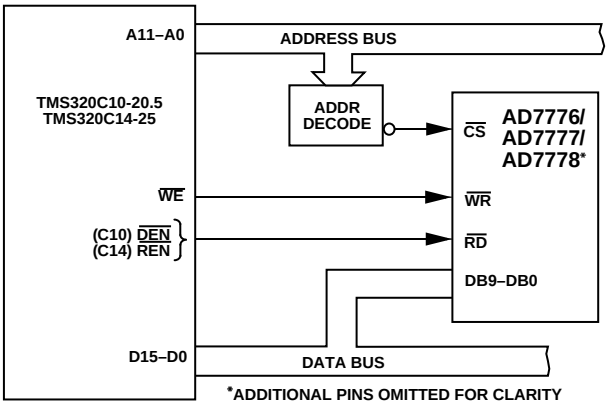


Figure 7. AD7776/AD7777/AD7778 to TMS320C10 and TMS320C14 Interface

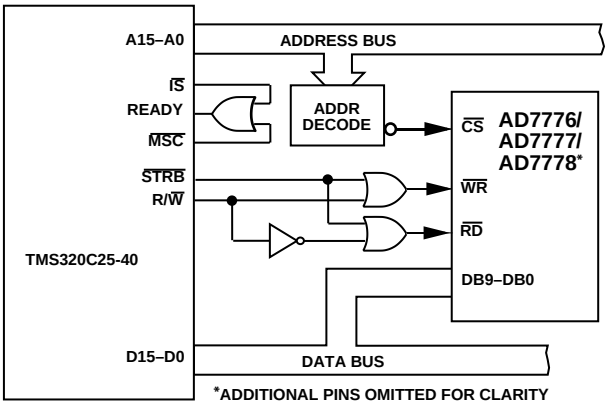


Figure 8. AD7776/AD7777/AD7778 to TMS320C25 Interface

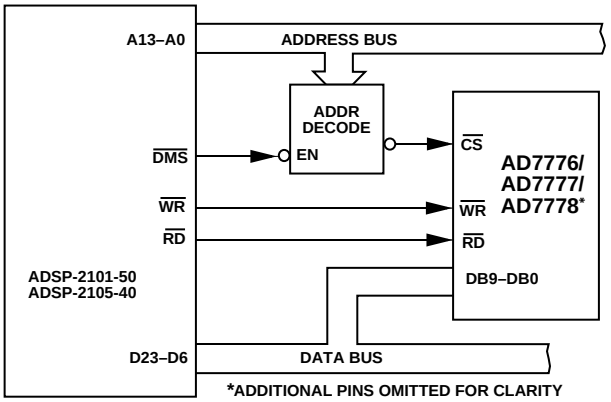


Figure 9. AD7776/AD7777/AD7778 to ADSP-2101 and ADSP-2105 Interface

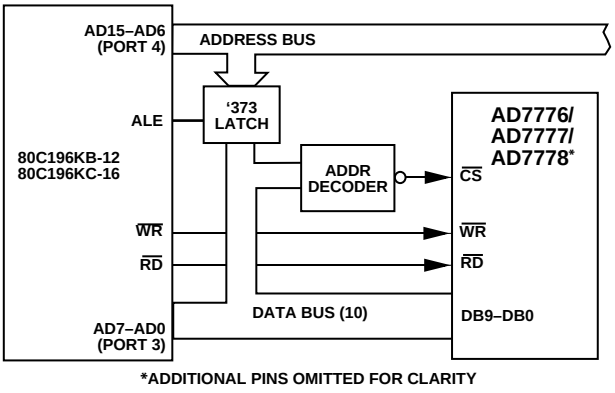


Figure 10. AD7776/AD7777/AD7778 to 80C196 Interface

Table I. AD7776/AD7777/AD7778 Truth Table for Microprocessor Interfacing

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	DB0–DB9	Function/Comments
1	X*	X*	High Z	Data Port High Impedance
0	1	⌐	CR Data	Load control register (CR) data to control register and start a conversion.
0	⌐	1	ADC Data	ADC data placed on data bus. Depending upon location CR6 of the control register, one or two Read instructions are required.
				If CR6 is low, i.e., single-channel conversion selected, a read instruction returns the contents of ADCREG1. Succeeding read instructions continue to return the contents of ADCREG1.
				If CR6 is high, i.e., simultaneous sampling (double conversion) selected, the first read instruction returns the contents of ADCREG1 while the second read instruction returns the contents of ADCREG2. A third read instruction returns ADCREG1 again, the fourth ADCREG2, etc.

*X = Don't Care

DESIGN INFORMATION

Layout Hints

Ensure that the layout for the printed circuit board has the digital and analog grounds separated as much as possible. Take care not to run any digital track alongside an analog signal track. Guard (screen) the analog input(s) with RTN.

Establish a single-point analog ground separate from the logic system ground and as close as possible to the AD7776/AD7777/AD7778. Both the RTN and AGND pins on the AD7776/AD7777/AD7778 and all other signal grounds should be connected to this single point analog ground. In turn, this star ground should be connected to the digital ground at one point only—preferably at the low impedance power supply itself.

Low impedance analog and digital power supply common returns are important for correct operation of the devices, so make the foil width for these tracks as wide as possible.

To ensure a low impedance +5 V power supply at the actual V_{CC} pin, it is necessary to use bypass capacitors from the pin itself to DGND. A 4.7 μF tantalum capacitor in parallel with a 0.1 μF ceramic capacitor is sufficient.

ADC Corruption

Executing a read instruction to the AD7776/AD7777/AD7778 while a conversion is in progress immediately halts the conversion and returns invalid data over the data bus. The $\overline{BUSY}$/ $\overline{INT}$ output pin should be monitored closely and all read instructions to the AD7776/AD7777/AD7778 prevented while this output shows that a conversion is in progress.

Executing a write instruction to the AD7776/AD7777/AD7778 while a conversion is in progress immediately halts the conversion, while the falling edge of $\overline{WR}$ driving the $\overline{BUSY}$/$\overline{INT}$ output high. The analog input(s) is sampled as normal, and a new conversion sequence (dependent upon CR6) is started.

ADC Conversion Time

Although each conversion takes only 14 CLKIN cycles, it can take between 4.5 and 5.5 CLKIN cycles to acquire the analog input(s) after the $\overline{WR}$ input goes high and before any conversions start.

TERMINOLOGY

Relative Accuracy

For the AD7776/AD7777/AD7778, relative accuracy or endpoint nonlinearity is the maximum deviation, in LSBs, of the ADC's actual code transition points from a straight line drawn between the endpoints of the ADC transfer function.

Differential Nonlinearity

Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified maximum differential nonlinearity of ±1 LSB ensures no missed codes.

Bias Offset Error

For an ideal 10-bit ADC, the output code for an input voltage equal to V_{BIAS} should be midscale. The bias offset error is the difference between the actual midpoint voltage for midscale code and V_{BIAS}, expressed in LSBs.

Bias Offset Error Match

This is a measure of how closely the bias offset errors of all channels track each other. The bias offset error match of any channel must be no further away than 10 LSBs from the bias offset error of any other channel, regardless of whether the channels are independently sampled or simultaneously sampled.

Plus and Minus Full-Scale Error

The input channels of the ADC can be considered to have bipolar (positive and negative) input ranges, but are referred to V_{BIAS} (or REFIN) instead of AGND. Positive full-scale error for the ADC is the difference between the actual input voltage required to produce the plus full-scale code transition and the ideal input voltage (V_{BIAS} + V_{SWING} –1.5 LSB), expressed in LSBs. Minus full-scale error is similarly specified for the minus full-scale code transition, relative to the ideal input voltage for this transition (V_{BIAS} – V_{SWING} + 0.5 LSB). Note that the full-scale errors for the ADC input channels are measured after their respective bias offset errors have been adjusted out.

Plus and Minus Full-Scale Error Match

This is a measure of how closely the full-scale errors of all channels track each other. The full-scale error match of any channel must be no further away than 10 LSBs from the respective full-scale error of any other channel, regardless of whether the channels are independently sampled or simultaneously sampled.

Short Circuit Current
This is defined as the maximum current which flows either into or out of the REFOUT pin if this pin is shorted to any potential between 0 V and V_{CC}. This condition can be allowed for up to 10 seconds provided that the power dissipation of the package is not exceeded.

Signal-to-Noise and Distortion Ratio, S/(N+D)
Signal-to-noise and distortion ratio, S/(N+D), is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics, but excluding dc. The value for S/(N+D) is given in decibels.

Total Harmonic Distortion, THD
Total harmonic distortion is the ratio of the rms sum of the first five harmonic components to the rms value of a full-scale input signal and is expressed in decibels. For the AD7776/AD7777/AD7778, total harmonic distortion (THD) is defined as:

$$20 \log \frac{\left(V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2\right)^{1/2}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5, and V_6 are the rms amplitudes of the individual harmonics.

Intermodulation Distortion, IMD
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities creates distortion products, of order (m + n), at sum and difference frequencies of mfa + nfb, where m, n = 0, 1, 2, 3. Intermodulation terms are those for which m or n is not equal to zero. For example, the second order terms include (fa + fb) and (fa – fb) and the third order terms include (2 fa + fb), (2 fa – fb), (fa + 2 fb), and (fa – 2 fb).

Channel-to-Channel Isolation
Channel-to-channel isolation is a measure of the level of cross-talk between channels. It is measured by applying a full-scale 100 kHz sine wave signal to any one of the input channels and monitoring the remaining channels. The figure given is the worst case across all channels.

DIGITAL SIGNAL PROCESSING APPLICATIONS

In digital signal processing (DSP) application areas like voice recognition, echo cancellation, and adaptive filtering, the dynamic characteristics S/(N+D), THD, and IMD of the ADC are critical. The AD7776/AD7777/AD7778 are specified dynamically as well as with standard dc specifications. Because the track/hold amplifier has a wide bandwidth, an antialiasing filter should be placed on the analog inputs to avoid aliasing high frequency noise back into the bands of interest.

The dynamic performance of the ADC is evaluated by applying a sine wave signal of very low distortion to a single analog input which is sampled at 380.95 kHz. A fast Fourier transform (FFT) plot or histogram plot is then generated from which the signal to noise and distortion, harmonic distortion, and dynamic differential nonlinearity data can be obtained. Similarly, for intermodulation distortion, an input signal consisting of two pure sine waves at different frequencies is applied to the AD7776/AD7777/AD7778.

Figure 11 shows a 2048-point FFT plot for a single channel of the AD7778 with an input signal of 99.88 kHz. The SNR is 58.71 dB. It can be seen that most of the harmonics are buried in the noise floor. It should be noted that the harmonics are taken into account when calculating the S/(N+D).

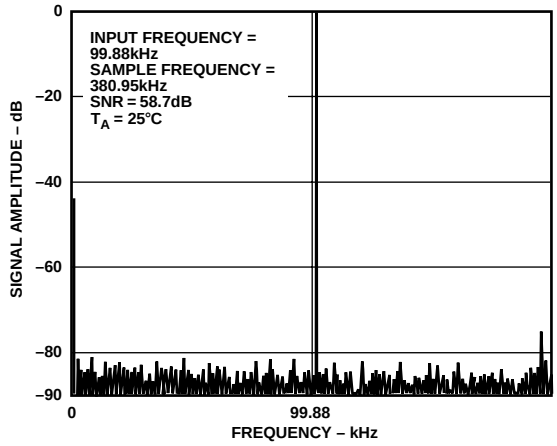


Figure 11. ADC FFT Plot

The relationship between S/(N+D) and resolution (n) is expressed by the following equation:

$$S/(N+D) = (6.02n + 1.76)\,dB$$

This is for an ideal part with no differential or integral linearity errors. These errors cause a degradation in S/(N+D). By working backwards from the above equation, it is possible to get a measure of ADC performance expressed in effective number of bits (n).

$$n(effective) = \frac{S/(N+D)(dB) - 1.76}{6.02}$$

The effective number of bits plotted versus frequency for a single channel of the AD7778 is shown in Figure 12. The effective number of bits is typically 9.5.

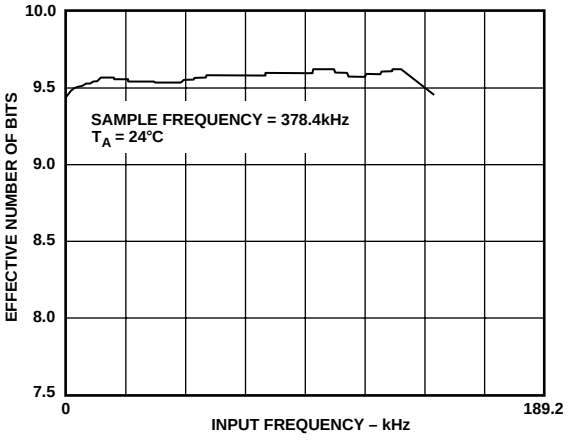


Figure 12. Effective Number of Bits vs. Frequency

Changing the Analog Input Voltage Range

By biasing the RTN pin above AGND, it is possible to change the analog input voltage range from its $V_{BIAS} \pm V_{SWING}$ format to a more traditional 0 V to V_{REF} range. The new input range can be described as

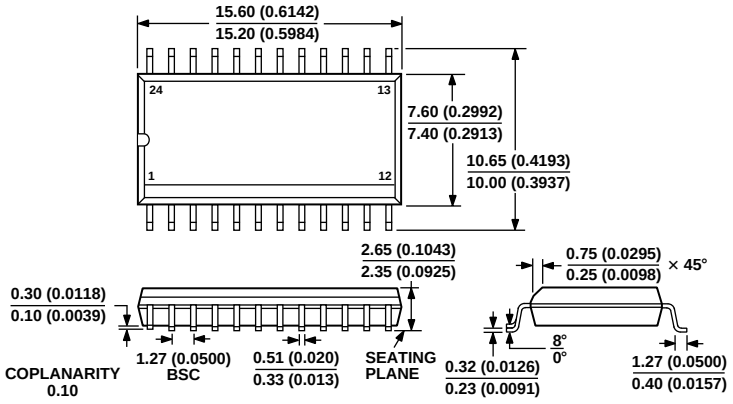
$$V_{OFFSET} \text{ to } (V_{OFFSET} + REFIN)$$

where $0 \text{ V} \le V_{OFFSET} \le 1 \text{ V}$. To produce this range, the RTN pin must be biased to (REFIN – 2 V_{OFFSET}). For instance, if RTN is tied to REFOUT, then the analog input range becomes 0 V to 2 V. The fixed 2 V analog input voltage span of the ADC can range from 1 V to 3 V (RTN = 0 V) to 0 V to 2 V (RTN = 2 V), i.e., with proper biasing, an input signal range from 0.3 V to 2.3 V can be covered. Both the relative accuracy and differential nonlinearity performance remain essentially unchanged in this mode, while the SNR and THD performance are typically 2 dB to 3 dB worse than standard.

OUTLINE DIMENSIONS

24-Lead Standard Small Outline Package [SOIC]
Wide Body
(RW-24)

Dimensions shown in millimeters and (inches)



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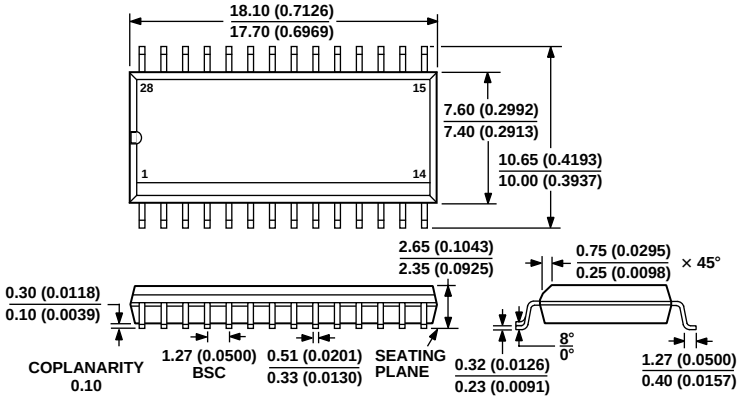
28-Lead Standard Small Outline Package [SOIC]
Wide Body
(RW-28)

Dimensions shown in millimeters and (inches)



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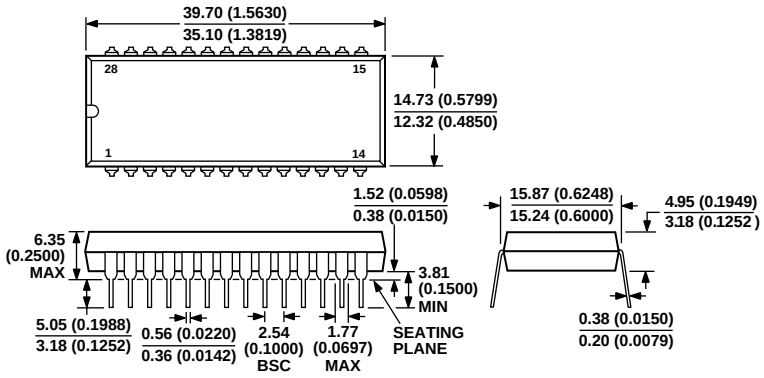
OUTLINE DIMENSIONS

28-Lead Plastic Dual-in-Line Package [PDIP]
(N-28)

Dimensions shown in millimeters and (inches)



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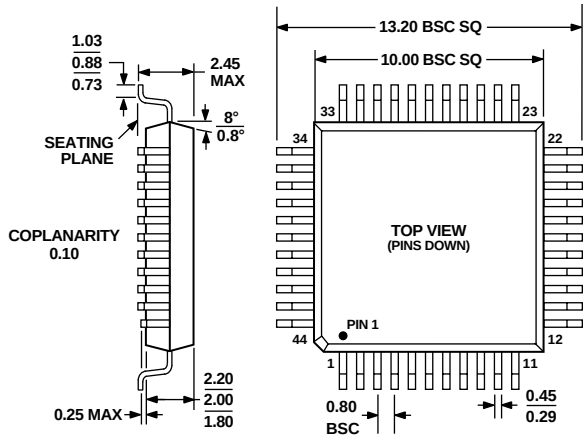
44-Lead Plastic Quad Flatpack [PQFP]
(S-44)

Dimensions shown in millimeters



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C01196–0–10/02(A)

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Revision History

Location	Page
10/02—Data Sheet changed from REV. 0 to REV. A.	
Changes to SPECIFICATIONS	2
Changes to ORDERING GUIDE	4
Changes to Total Harmonic Distortion, THD section	10
Changes to OUTLINE DIMENSIONS	12

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Офис по работе с юридическими лицами:

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:
moschip.ru
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