Click here for production status of specific part numbers.

MAX40025A/MAX40025C/ MAX40026

280ps High-Speed Comparator, Ultra-Low Dispersion with LVDS Outputs

General Description

The MAX40025 and MAX40026 are single-supply, high-speed comparators with a typical propagation delay of 280ps. The overdrive dispersion is extremely low (typical 25ps), making these comparators ideal for time-of-flight distance measurement applications.

The input common mode range of 1.5V to V_{DD} + 0.1V is compatible with the output swings of several widely used high-speed trans-impedance amplifiers, such as the MAX40658.

The output stage is LVDS (Low-Voltage Differential Signaling), which helps to minimize power dissipation and interfaces directly with many FPGAs and CPUs. Complementary outputs help in suppression of common-mode noise on each output line.

The MAX40025 is offered in a space-saving, tiny, 1.218mm x 0.818mm, 6-bump wafer-level package (WLP), while the MAX40026 is available in a 2mm x 2mm 8-pin TDFN side-wettable package and meets AEC-Q100 automotive qualification requirements. The MAX40025/ MAX40026 operate over -40°C to +125°C temperature range and run from a single supply voltage of 2.7V to 3.6V.

Applications

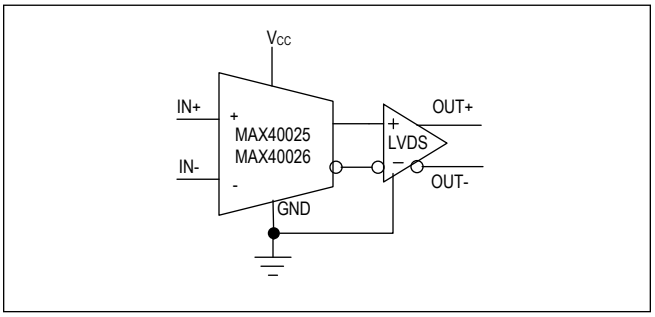
- Distance Sensing in LIDAR, RADAR, and SONAR
- Time-of-Flight Sensors
- High-Speed Differential Line Receivers
- High-Speed Triggering in Oscilloscopes
- Communications
- Oscillators
- Threshold Detectors
- High-Speed Level-Shifting
- Test and Measurement
- Automotive Applications

Benefits and Features

- Fast Propagation Delay: 280ps, Typ
- Low Overdrive Dispersion: 25ps (V_{OD} = 10mV to 1V)
- Supply Voltage 2.7V to 3.6V
- 39.4mW at 2.7V Supply
- Power-Efficient LVDS Outputs
- -40°C to +125°C Temperature Range
- Automotive AEC-Q100 Qualified (TDFN-8 Version)
- Internal 1.5mV Hysteresis: MAX40026
- Internal 2.5mV Hysteresis: MAX40025A

***Ordering Information* appears at end of data sheet.**

Functional Diagram



19-100439; Rev 5; 9/19

maxim integrated™

Absolute Maximum Ratings

V_{CC} to GND ..... -0.3V to +3.6V
Either IN+ or IN- to GND ..... -0.3V to V_{CC} + 0.3V
Either OUT+ or OUT- to GND ..... -0.3V to V_{DD} + 0.3V
OUT+ to OUT- ..... -0.5V to +0.5V
Current Into Any Pin (Continuous) 10mA
Continuous Power Dissipation (Multilayer Board) (WLP) (T_A = +70°C, derate 10.51mW/°C above +70°C) 816mW
Continuous Power Dissipation (Multilayer Board) (TDFN) (T_A = +70°C, derate 9.8mW/°C above +70°C.) 784mW
Operating Temperature Range ..... -40°C to +125°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -40°C to +150°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

WLP

Package Code	W60D1+1
Outline Number	21-100296
Land Pattern Number	Refer to *Application Note 1891*
Thermal Resistance, Four-Layer Board:	
Junction-to-Ambient (θ_{JA})	95.15°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	N/A

8-TDFN

Package Code	T822Y+3
Outline Number	21-100185
Land Pattern Number	90-100070
Thermal Resistance, Single-Layer Board:	
Junction-to-Ambient (θ_{JA})	130°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	8°C/W
Thermal Resistance, Four-Layer Board:	
Junction-to-Ambient (θ_{JA})	102°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	8°C/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(V_{CC} = 3.3V, V_{CM} = 2.5V, R_{LOAD} = 100Ω, connected from OUT+ to OUT-, T_A = -40ºC to +125ºC (Note 1))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage (Note 2)	V_{CC}	Guaranteed by PSRR specification	2.7		3.6	V
Supply Current	I_{CC}			17	23	mA

Electrical Characteristics (continued)

(V_{CC} = 3.3V, V_{CM} = 2.5V, R_{LOAD} = 100Ω, connected from OUT+ to OUT-, T_A = -40ºC to +125ºC (Note 1))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power-Up Time	t_{ON}	Measured using supply current >75% of final value		20		µs
Power Supply Rejection Ratio (Note 2)	PSRR	2.7V ≤ V_{CC} ≤ 3.6V	50	80		dB
Input Common Mode Range (Note 2)	V_{CM}	Guaranteed by CMRR specification	1.5		V_{CC} + 0.1	V
Input Offset Voltage (Note 2)	V_{OS}	Over the Input common mode range		0.5	5	mV
Common Mode Rejection Ratio (Note 2)	CMRR	Over the Input common mode range	52	80		dB
Input Hysteresis	V_{HYS}	MAX40025A		2.5		mV
		MAX40026		1.5		
Input Bias Current	I_B	Over the Input common mode range. Inputs shorted together.		1.3	10	µA
Input Offset Current	I_{OS}	V_{IN+} = V_{IN-}		0.1	4	µA
Input Capacitance	C_{IN}	Either input, over entire Input common mode range		2		pF
Output Differential Voltage	$V_{OUTDIFF}$	$\lvert V_{OUT+} - V_{OUT-} \rvert$	247	350	454	mV
Output Differential Voltage Match		$\lvert V_{OUT+} - V_{OUT-} \rvert$	-50		+50	mV
Output Common-Mode Voltage	V_{CMOUT}	Either output polarity	1.125	1.23	1.375	V
Output Common-Mode Voltage Match		Either output polarity	-50		+50	mV
Output Common-Mode Transient		Either output transition polarity		18		mVp-p
Output Short-Circuit Current	I_{SC}	Either output shorted to ground, either polarity			24	mA
		Outputs shorted together, either polarity	-12		+12	
Propagation Delay	t_{PD}	20mV overdrive		270		ps
		100mV overdrive		280		
		200mV overdrive		280		
Jitter	t_{JITTER}	Measured using square wave with Rise and Fall Time = 150ps, 100mV overdrive		2		ps
Overdrive Dispersion	$t_{OD-disp}$	10mV to 1V		25		ps
		20mV to 100mV		10		
Rise Time	t_R	From 25% to 75% output swing		150		ps
Fall Time	t_F	From 75% to 25% output swing		165		ps

Electrical Characteristics (continued)

(V_{CC} = 3.3V, V_{CM} = 2.5V, R_{LOAD} = 100Ω, connected from OUT+ to OUT-, T_A = -40ºC to +125ºC (Note 1))

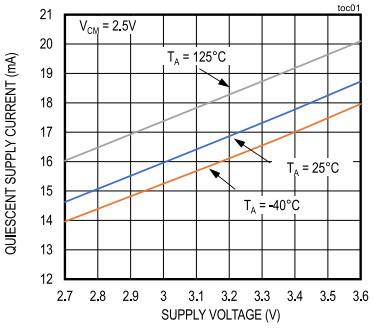
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Skew		Measured using square wave with Rise and Fall Time = 150ps, 100mV overdrive	Propagation Delay difference between OUT+ and OUT-		10		ps
Maximum Toggle Rate	T_R	V_{OUT} = 550mV, V_{OD} = 100mV	MAX40025		4		Gbps
			MAX40026		3		
Minimum Pulse Width		both MAX40025/ MAX40026			330		ps

Note 1: Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.

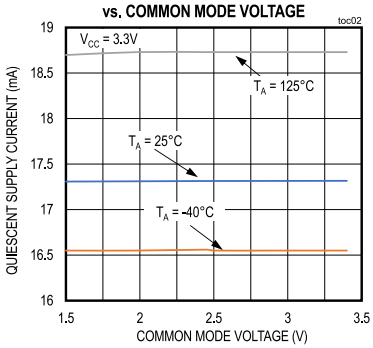
Note 2: Specifications are guaranteed by design and characterization and not production tested.

Typical Operating Characteristics

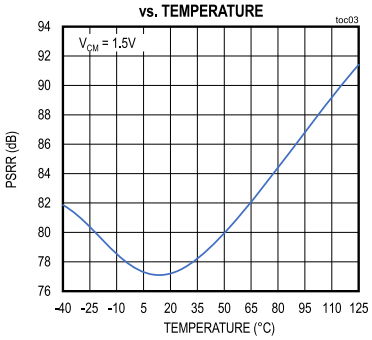
SUPPLY CURRENT vs. SUPPLY VOLTAGE



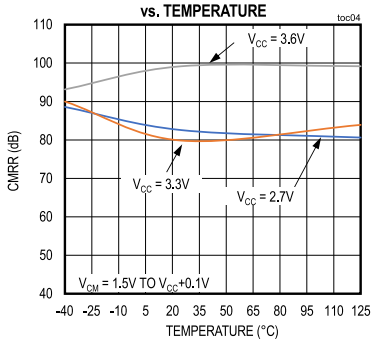
SUPPLY CURRENT vs. COMMON MODE VOLTAGE



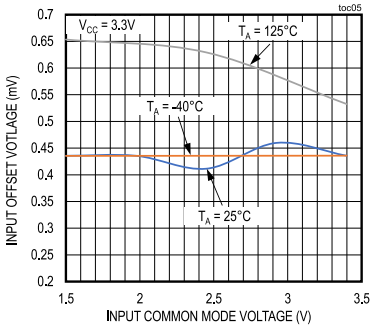
DC POWER SUPPLY REJECTION RATIO vs. TEMPERATURE



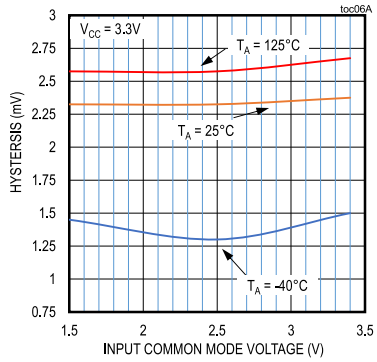
DC COMMON MODE REJECTION RATIO vs. TEMPERATURE



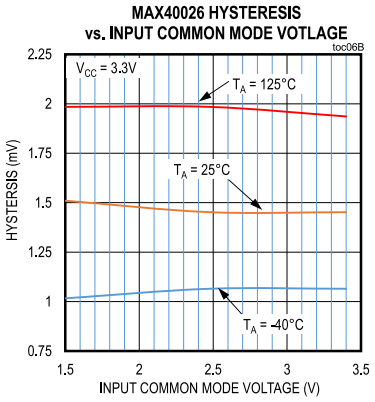
INPUT OFFSET VOLTAGE vs. INPUT COMMON MODE VOLTAGE



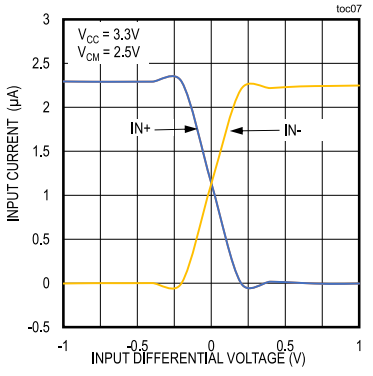
MAX40025A HYSTERESIS vs. INPUT COMMON MODE VOTLAGE



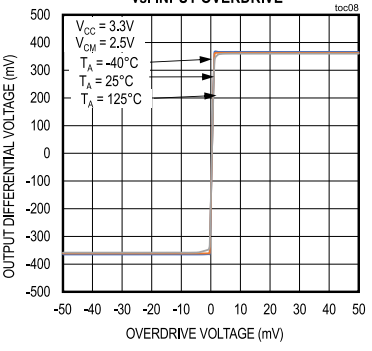
MAX40026 HYSTERESIS vs. INPUT COMMON MODE VOTLAGE



INPUT CURRENT vs. INPUT DIFFERENTIAL VOLTAGE

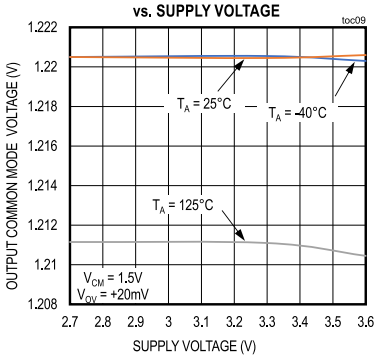


OUTPUT DIFFERENTIAL VOLTAGE vs. INPUT OVERDRIVE

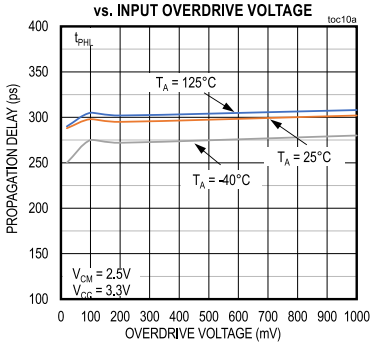


Typical Operating Characteristics (continued)

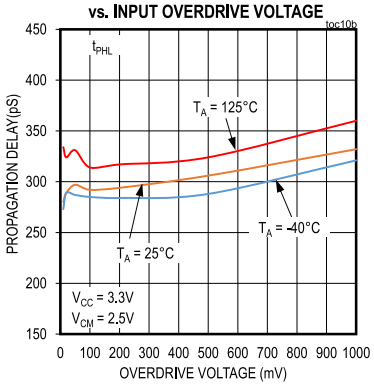
OUTPUT COMMON MODE VOLTAGE
vs. SUPPLY VOLTAGE



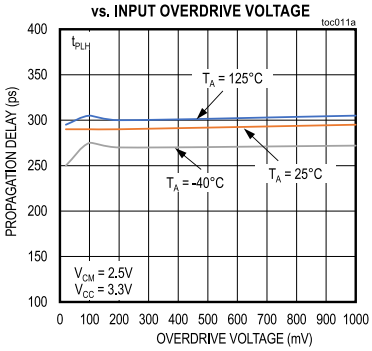
MAX40025 PROPAGATION DELAY
vs. INPUT OVERDRIVE VOLTAGE



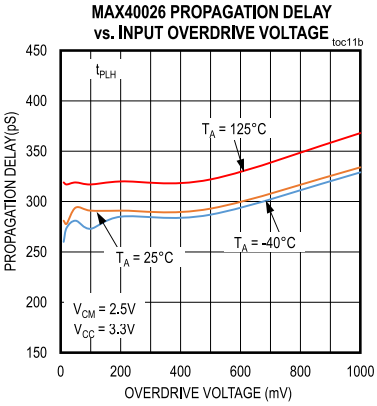
MAX40026 PROPAGATION DELAY
vs. INPUT OVERDRIVE VOLTAGE



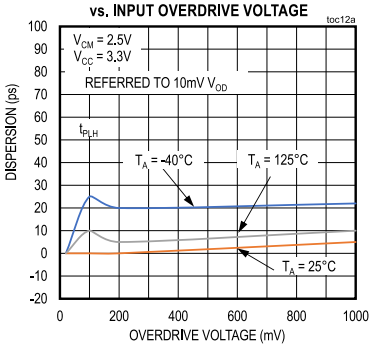
MAX40025 PROPAGATION DELAY
vs. INPUT OVERDRIVE VOLTAGE



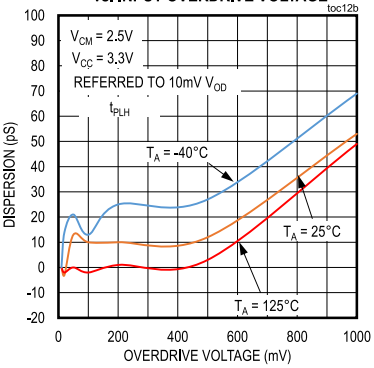
MAX40026 PROPAGATION DELAY
vs. INPUT OVERDRIVE VOLTAGE



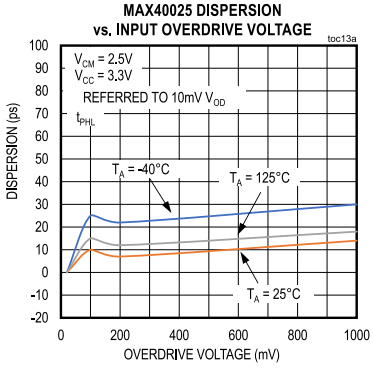
MAX40025 DISPERSION
vs. INPUT OVERDRIVE VOLTAGE



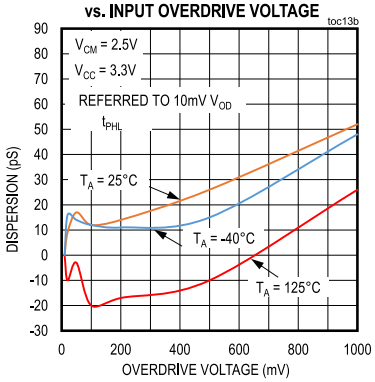
MAX40026 DISPERSION
vs. INPUT OVERDRIVE VOLTAGE



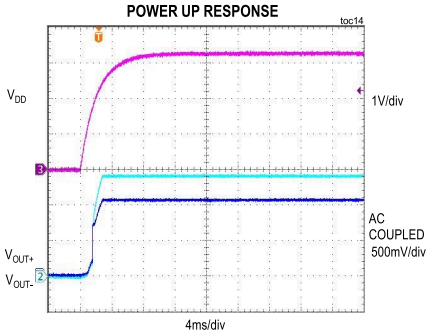
MAX40025 DISPERSION
vs. INPUT OVERDRIVE VOLTAGE



MAX40026 DISPERSION
vs. INPUT OVERDRIVE VOLTAGE

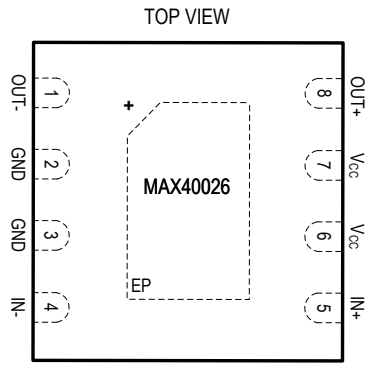


Typical Operating Characteristics (continued)



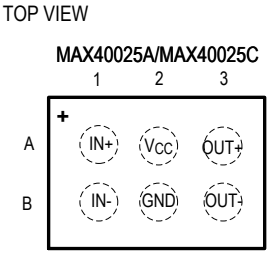
Pin Configurations

8 TDFN



2mm x 2mm

WLP



Pin Description

PIN		NAME	FUNCTION
MAX40026	MAX40025A/ MAX40025C		
1	B3	OUT-	Inverting LVDS Output. Connect a 100Ω termination resistor between OUT- and OUT+. OUT- is at logic-low if V_{IN+} is at higher voltage compared to V_{IN-}.
2, 3	B2	GND	Ground. Signal and power return (for TDFN-8: connect pins 2 and 3 together externally).
4	B1	IN-	Inverting Input
5	A1	IN+	Non-Inverting Input
6,7	A2	V_{CC}	Positive Supply. For TDFN-8, connect pins 6 and 7 together externally.
8	A3	OUT+	Non-Inverting LVDS Output. Connect a 100Ω termination resistor between OUT+ and OUT-. OUT+ is at logic-high if V_{IN+} is at higher voltage compared to V_{IN-}.
EP	—	Exposed Paddle	Exposed Pad (TDFN-8 Only). This pad must be connected to ground.

Detailed Description

The MAX40025 and MAX40026 are single-supply, high-speed comparators with a typical propagation delay of 280ps. The overdrive dispersion is extremely low (25ps, typ.), making these comparators ideal for time-of-flight distance measurement applications.

The input common-mode range of 1.5V to V_{DD} + 0.1V is compatible with the outputs of several widely used high-speed transimpedance amplifiers, such as the MAX40658. The output stage is LVDS (Low-Voltage Differential Signaling), which helps to minimize power dissipation and interfaces directly with many modern FPGAs and CPUs.

The MAX40025 and MAX40026 operate from a +2.7V to +3.6V power supply voltage while typically consuming only 17mA quiescent current at 3.3V. The MAX40025 and MAX40026 are available in space-saving 6-WLP and 8-TDFN packages, respectively.

LVDS Outputs

Each LVDS output has a switched 3.25 mA current source. The outputs are differentially terminated with an external 100Ω resistor, which produces a ±350 mV differential output. The power delivered to the 100Ω load resistor is only 1.1mW while enabling transmission data rates up to a few hundreds of Megabits per second. The output common-mode voltage is maintained at 1.23 V on both outputs, and is independent of power supply voltage. The fully differential LVDS outputs provide high-speed digital signalling with reduced EMI compared to single-ended outputs.

System Timing Definitions

Table 1. Timing Definitions

SYMBOL	SPECIFICATION	DESCRIPTION
V_{OD}	Overdrive Voltage	Differential voltage applied across inputs during test
t_{PDH}	Propagation Delay High on OUT+	Propagation delay measured from the time the differential input signal changes polarity (± input V_{OS}) to the 50% point in the output low-to-high transition on OUT+
t_{PDL}	Propagation Delay Low on OUT-	Propagation delay measured from the time the differential input signal changes polarity (± input V_{OS}) to the 50% point in the output high-to-low transition on OUT-
Δt_{PDHO}	Propagation Delay Skew on High	Difference in propagation delay on output transition from low to high on OUT+ to propagation delay from high to low on OUT-
Δt_{PDLO}	Propagation Delay Skew on Low	Difference in propagation delay on output transition from high to low on OUT+ to propagation delay from low to high on OUT-
t_R	Output Rise Time	Time taken by either OUT+ or OUT- to rise from 25% of final output voltage to 75% of final output voltage
t_F	Output Fall Time	Time taken by either OUT+ or OUT- to fall from 75% of final output voltage to 25% of final output voltage
$t_{PD\overline{L}}$	Propagation Delay Low on OUT-	Propagation delay measured from the time the differential input signal changes polarity (± input V_{OS}) to the 50% point in the output high-to-low transition on OUT-
$t_{PD\overline{H}}$	Propagation Delay High on OUT-	Propagation delay measured from the time the differential input signal changes polarity (± input V_{OS}) to the 50% point in the output low-to-high transition on OUT-
t_{PDHD}	Differential Propagation Delay High	Propagation delay measured from the time the differential input signal changes polarity (± input V_{OS}) to the 50% point in the output differential signal across OUT+ to OUT- while switching low to high

Table 1. Timing Definitions (continued)

t_{PDLD}	Differential Propagation Delay Low	Propagation delay measured from the time the differential input signal changes polarity (± input V_{OS}) to the 50% point in the output differential signal across OUT+ to OUT- while switching high to low
V_{OH}	Output Voltage High	Comparator output high state voltage level
V_{OL}	Output Voltage Low	Comparator output low state voltage level

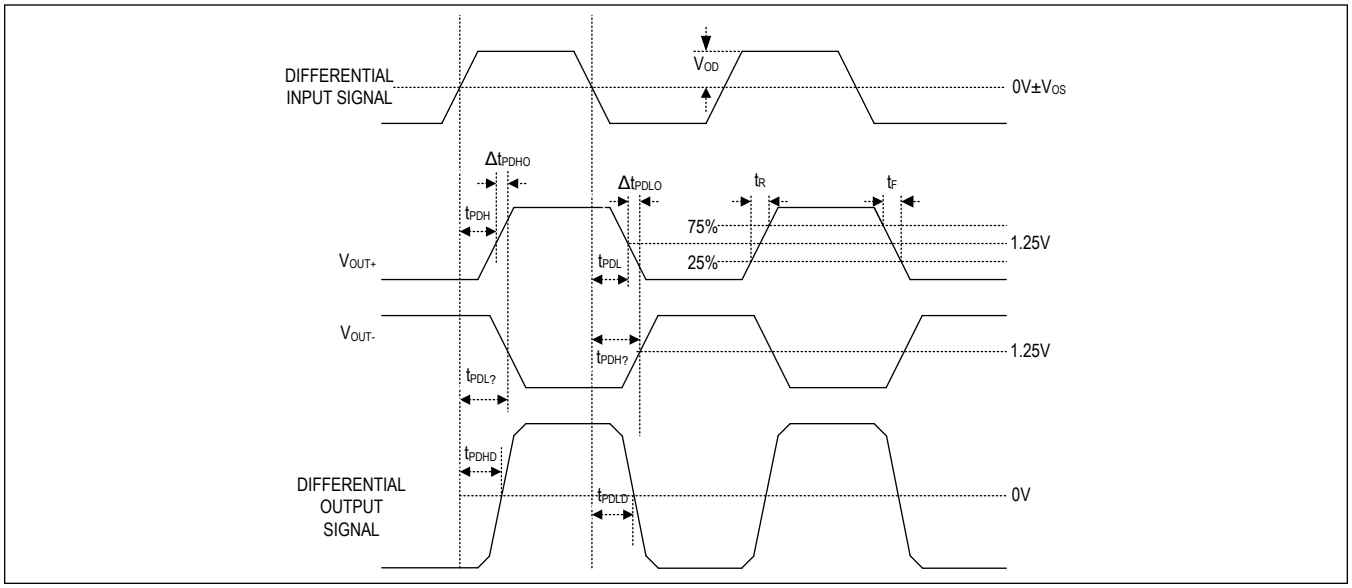


Figure 1. System Timing Diagram

Propagation Delay

The propagation delay is defined as the delay between the differential comparator input voltage changing polarity and the output(s) reaching the mid-point of the high-to-low or low-to-high transition. The low-to-high propagation delay is t_{PDH} on OUT+ and t_{PDH} on OUT-, whereas the high-to-low propagation delay is t_{PDL} on OUT+ and t_{PDL} on OUT-. These high-to-low and low-to-high timing parameters will differ slightly due to mismatches between the two complementary outputs. As a result, this difference in propagation delay is considered to be a skew for a given combination of low-to-high transitions on OUT+ and high-to-low transitions on OUT-.

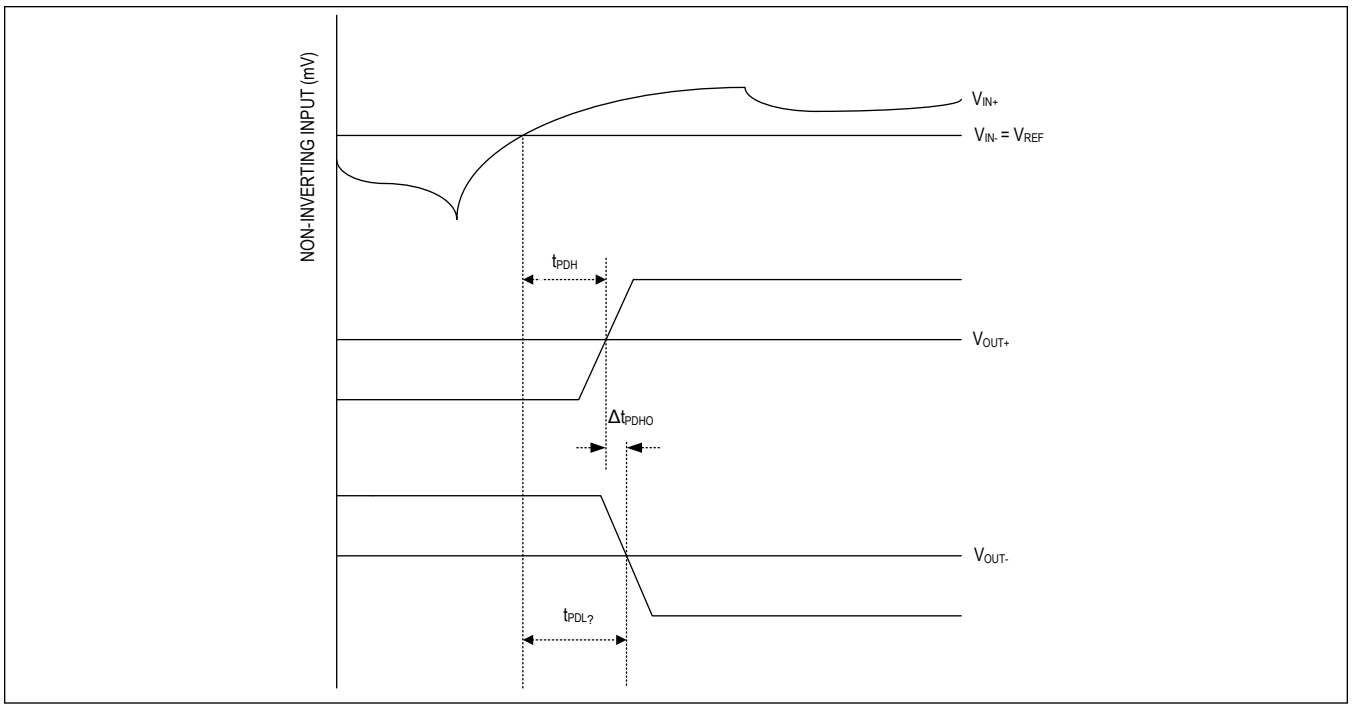


Figure 2. Propagation Delay

Propagation Delay Dispersion

Dispersion, or variation of the propagation delay under different conditions, is affected by the amount of overdrive voltage applied to the comparator inputs. As can be seen in the Typical Operating Characteristics, the dispersion is typically under 25ps for 10mV to 1V, a wide range of input overdrive values.

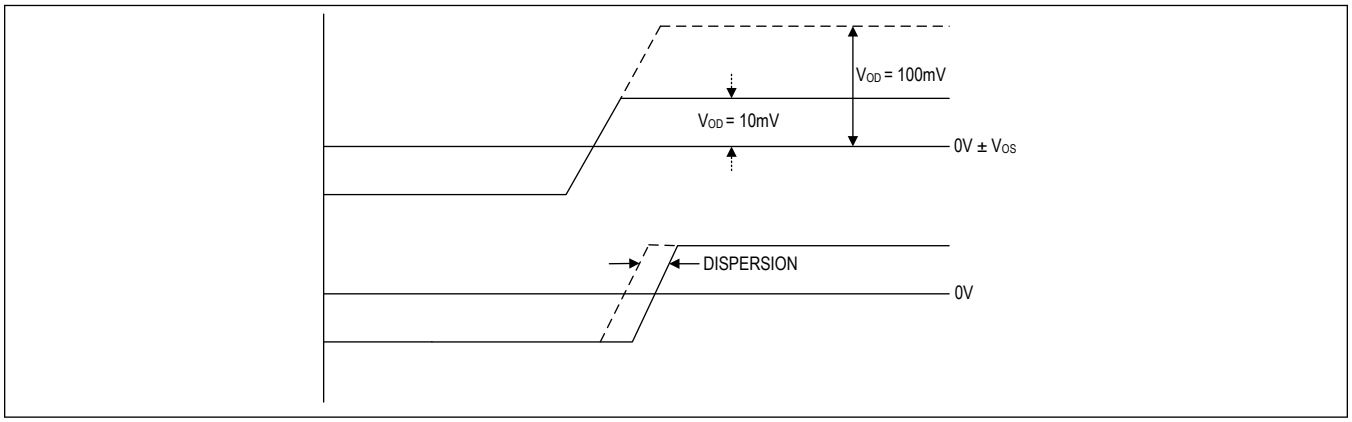


Figure 3. Amplitude Overdrive Dispersion

Dispersion is also affected by the input slew rate. As the slew rate of the input signal changes, the propagation delay also changes. The dispersion is typically under 15ps from 0.4V/µs to 1V/µs input slew rates.

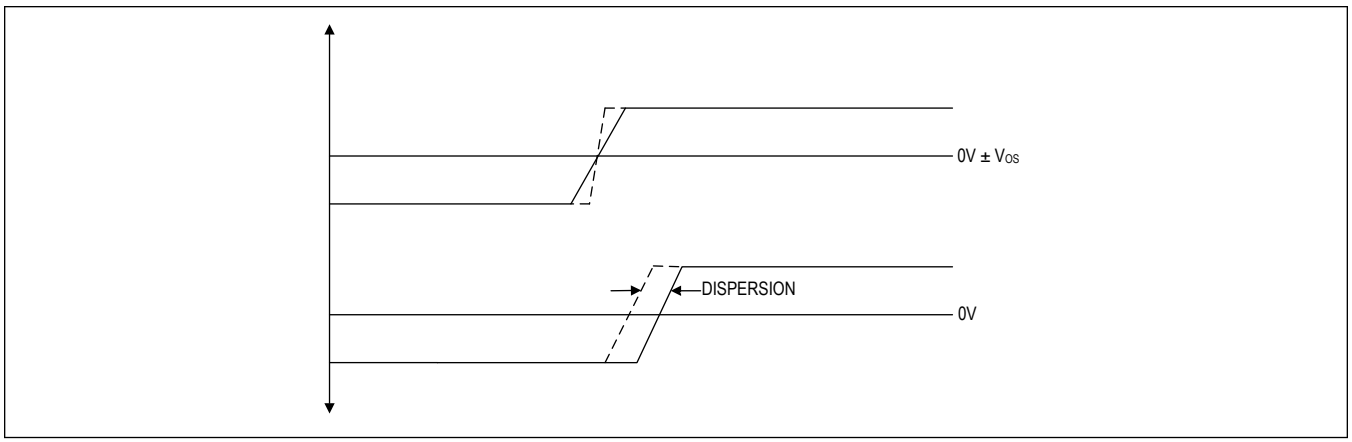


Figure 4. Slew Rate Dispersion

Hysteresis

Adding a small amount hysteresis to a comparator in a noisy environment is useful when input signals are slow-moving and have small noise levels superimposed on them. However, hysteresis must be used carefully when signals are small because it can cause valid signals to be ignored. Figure 5 shows the input signal and output response for a comparator with hysteresis applied.

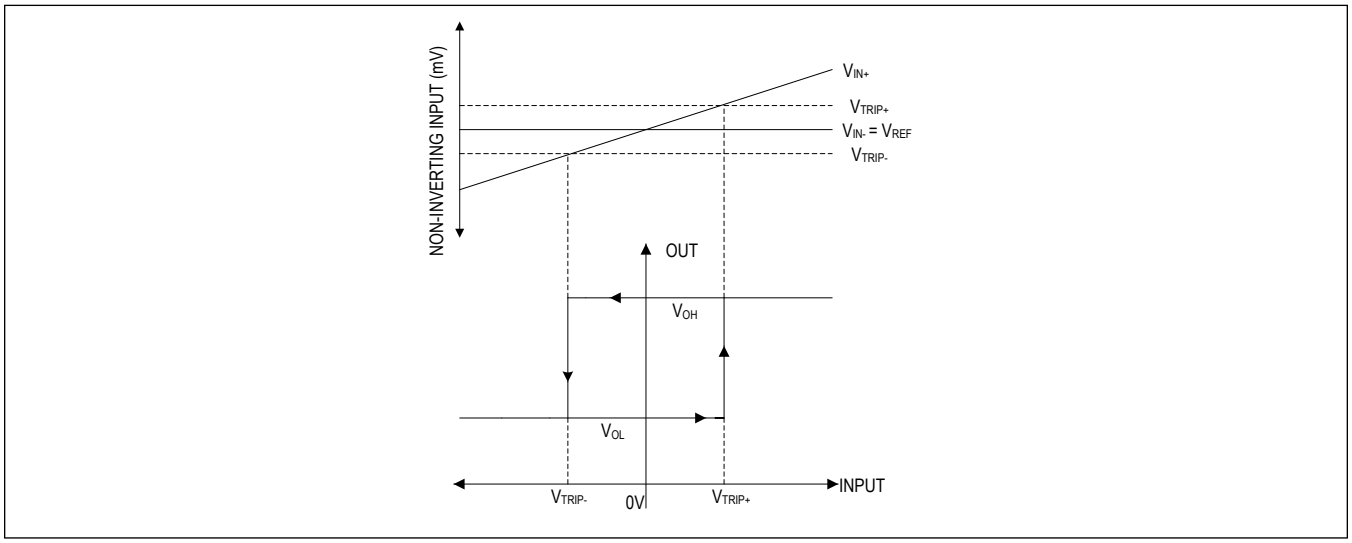


Figure 5. Hysteresis Transfer Function

The MAX40025C is optimized for detecting very small, fast-changing signals and therefore has no internal hysteresis. The MAX40025A has fixed internal 2.5mV hysteresis and the MAX40026 has fixed internal 1.5mV hysteresis, which improves their usefulness for detecting larger differential input signals in the presence of noise. This helps to avoid the external components and potential stability degradation associated with external positive feedback paths.

Input Stage Circuitry

The MAX40025/MAX40026 include internal protection circuitry that prevents damage to the precision input stage from large differential input voltages. This protection circuitry consists of two groups of two front-to-back diodes between IN+ and IN-, as well as two 50Ω resistors (Figure 6). The diodes limit the differential voltage applied to the comparator's internal circuitry to no more than $2V_F$, where V_F is the diode's forward-voltage drop (about 0.7V at +25°C).

For a large differential input voltage (exceeding $2V_F$), this protection circuitry increases the input bias current at IN+ (source) and IN- (sink).

$$\text{INPUT CURRENT} = \frac{\left(V_{IN+} - V_{IN-}\right) - 2 \times V_F}{2 \times 50}$$

Input currents with large differential input voltages should not be confused with input bias currents (I_B). As long as the differential input voltage is less than $2V_F$, this input current is less than $2I_B$.

The input circuitry allows the MAX40025/MAX40026's input common-mode range to extend 100mV beyond the positive power-supply rail. The output remains in the correct logic state if one or both inputs are within the common-mode range. Taking either input outside the common-mode range causes the input to saturate and the propagation delay to increase.

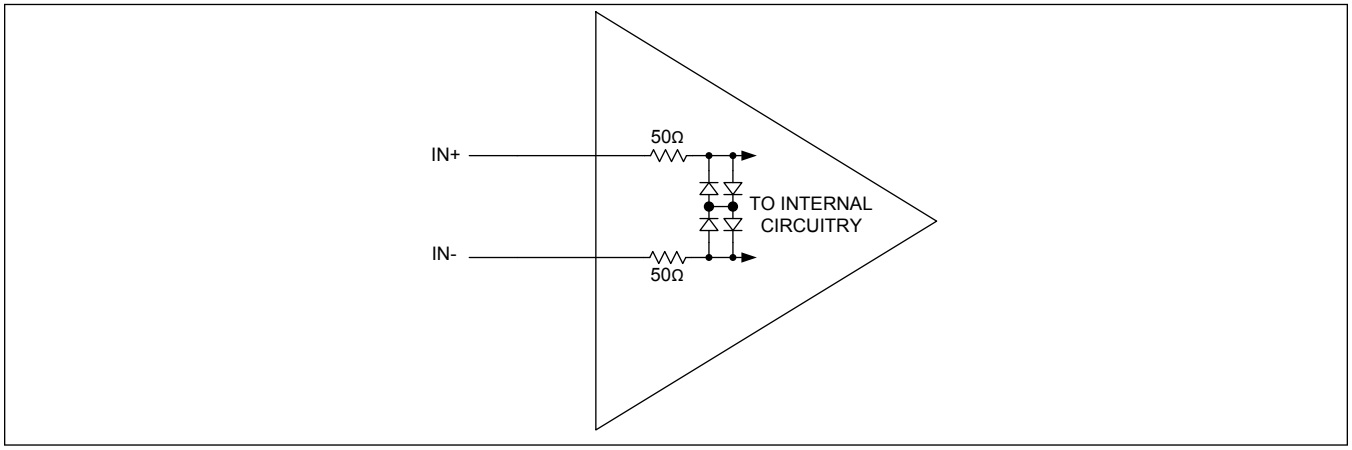


Figure 6. Input Stage Circuitry

Applications Information

Critical Layout Guidelines

Some critical Layout guidelines are listed below.

- Use a PC board with a low-impedance ground plane.
- Mount one or more 10nF ceramic capacitors between GND and V_{CC}, as close to the pins as possible. Multiple bypass capacitors help to reduce the effect of trace impedance and capacitor ESR.
- Choose bypass capacitors for minimum inductance and ESR.
- Use a 100Ω termination resistor for the LVDS output, connected directly between OUT+ and OUT-, if practical. If the destination LVDS inputs can't be located adjacent to the outputs, use a 100Ω microstrip between the output pins and the termination resistor, which should be close to the LVDS inputs of the FPGA or other destination component. This will avoid the creation of stub beyond the termination resistor, which will cause reflections. The added length of the differential trace has less degrading affects than added stub length.
- Ensure that there is no parasitic coupling between the inputs and the outputs. Such coupling serves as feedback, and can result in oscillation.
- Minimize any parasitic layout inductance.
- It is recommended to use higher performance substrate materials (for example, Rogers).
- A differential micro-strip is the recommended layout for MAX40025/MAX40026 with terminations done close to the inputs and outputs of the MAX40025 or MAX40026. Care must be taken to avoid unwanted stubs by removing ground below the traces that are not part of the 50Ω termination line leading into input pins. The parasitic capacitance created between traces and ground slow down and even distort the signals by creating reflections on the path.
- Below is an example from the MAX40025EVKIT#, where ground has been etched/removed underneath a stub as shown in the layer below top layer.

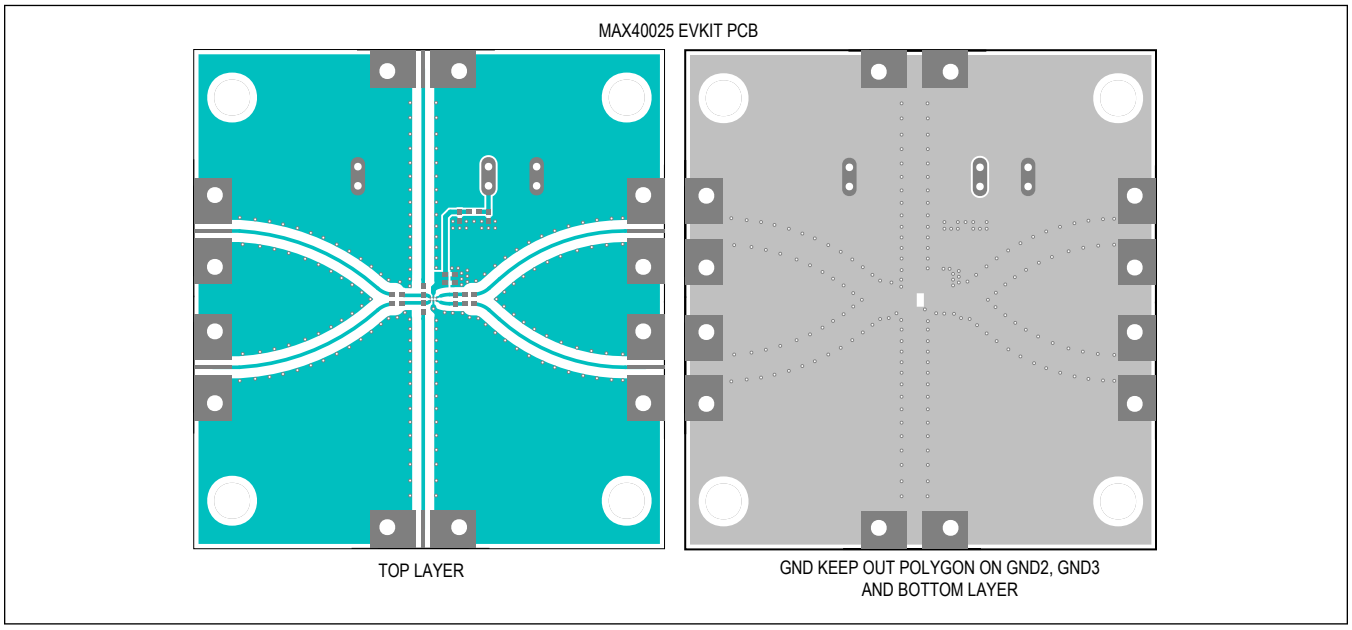


Figure 7. Layout Guidelines—Ground Keep-Out to Avoid Stubs.

Input Slew Rate

With slower slew rates, when the input voltage is near the threshold any parasitic feedback paths can cause oscillation. In addition, the comparator's input noise will cause the output to undergo transitions. Eliminating feedback paths will stop

oscillation. To avoid noise-induced chattering, the input slew rate should be greater than 1V/µs.

Typical Application Circuits

Receiver Section of Differential Time-of-Flight Measurement Circuit:

In Figure 8, the photodiode, shown at the far right, converts light incident upon it into current that drives the input of the MAX40658 Transimpedance Amplifier (TIA). The MAX40658 then converts photodiode current to voltage, amplifies it, and passes a replica of the incident light to input of the MAX40025 high-speed comparator. By default, the MAX40658 has -27mV differential output offset voltage when there is no input current. This offset can be adjusted using the MAX40658's offset pin. The MAX40025 produces differential output pulses whenever an incident light pulse has intensity sufficient to change the polarity of the comparator input signal.

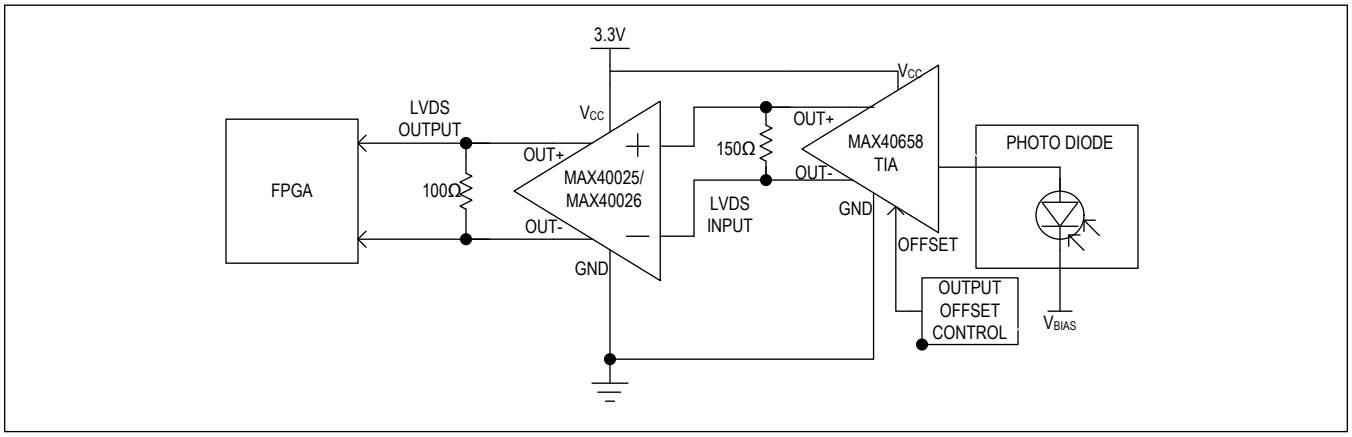


Figure 8. Differential-Ended Output Receiver

Receiver Section of Single-Ended Time-of-Flight Measurement Circuit:

Figure 9 has a single-ended output configuration on the transimpedance amplifier, which drives one input of the comparator. This functionality is the same as that of the differential configuration discussed above, except that the threshold voltage can be adjusted by selecting the values of R1 and R2.

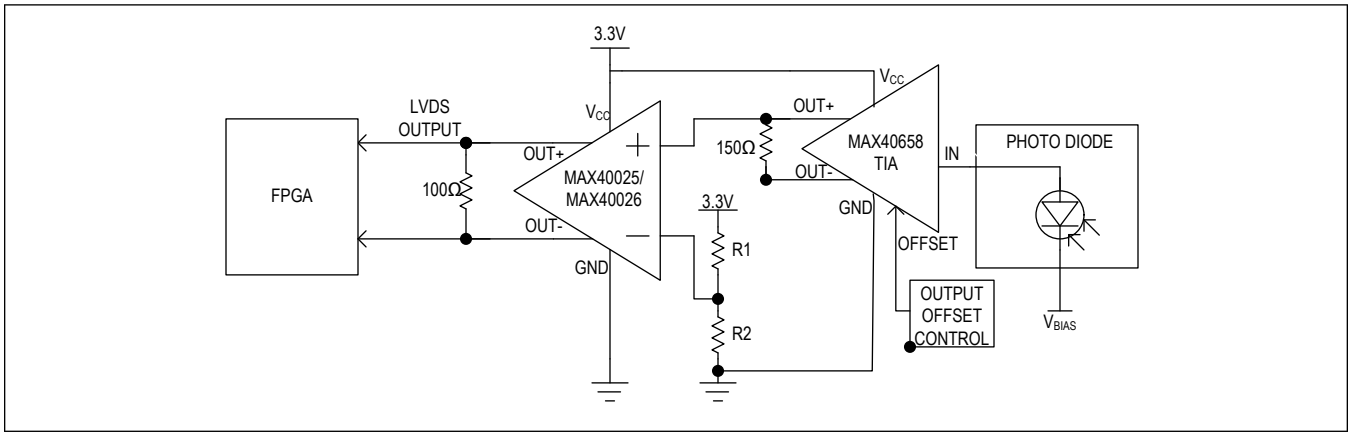


Figure 9. Single-Ended Output Receiver

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PIN-PACKAGE	TOP MARK	HYSTERESIS
MAX40025AAWT+	-40°C to +125°C	6-WLP	+AAC	2.5mv
MAX40025CAWT+	-40°C to +125°C	6-WLP	+AAB	No Hysterisis
MAX40026ATA/VY+	-40°C to +125°C	8-TDFN	+BSS	1.5mV
MAX40026ATA+	-40°C to +125°C	8-TDFN	+BTF	1.5mV

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	11/18	Initial release	—
1	12/18	Updated part numbers in title and equation in *Detailed Description*	1–17
2	1/19	Updated *Pin Configuration Diagram* and *Pin Description*	7
3	2/19	Updated data sheet for release of MAX40026	1–18
4	3/19	Updated data sheet for release of MAX40025A	1–18
5	9/19	Updated *Ordering Information* table	18

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