

Automotive-grade N-channel 40 V, 1.27 mΩ typ., 120 A STripFET™ F6 Power MOSFET in a PowerFLAT™ 5x6 DSC

Datasheet - production data

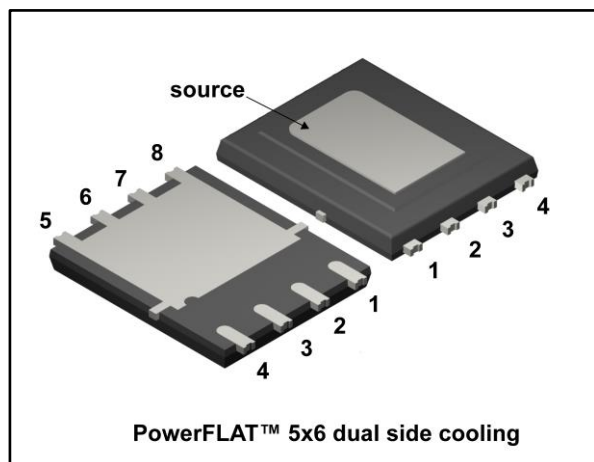
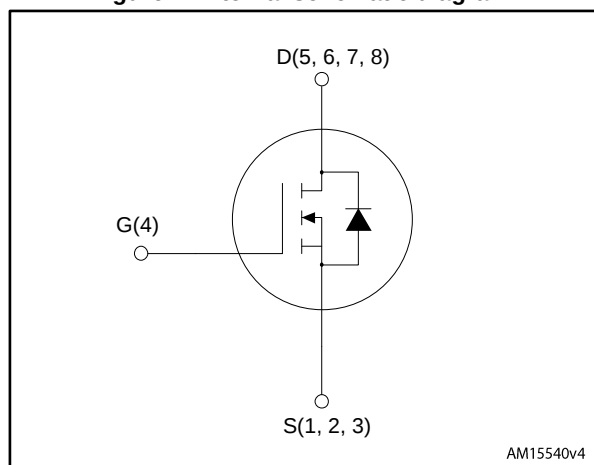


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max.	I _D
STLD200N4F6AG	40 V	1.50 mΩ	120 A

- AEC-Q101 qualified
- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss
- Wettable flank package



Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using the STripFET™ F6 technology with a new trench gate structure. The resulting Power MOSFET exhibits very low R_{DS(on)} in all packages.

Table 1: Device summary

Order code	Marking	Package	Packaging
STLD200N4F6AG	200	PowerFLAT™ 5x6 dual side cooling	Tape and reel

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	40	V
V_{GS}	Gate-source voltage	± 20	V
$I_D^{(1)(2)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	120	A
$I_D^{(1)(2)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	120	A
$I_{DM}^{(2)(3)}$	Drain current (pulsed)	480	A
$P_{TOT}^{(2)}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	158	W
T_J	Operating junction temperature range	-55 to 175	$^\circ\text{C}$
T_{stg}	Storage temperature range		

Notes:⁽¹⁾Limited by package⁽²⁾The value is rated according to R_{thj-c} bottom side.⁽³⁾Pulse width limited by safe operating area

Table 3: Thermal data

Symbol	Parameter	Value	Unit
R_{thj-c} top side	Thermal resistance junction-case top side	2.90	$^\circ\text{C/W}$
R_{thj-c} bottom side	Thermal resistance junction-case bottom side	0.95	
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	31.3	

Notes:⁽¹⁾When mounted on 1 inch² 2 Oz. Cu board, $t \leq 10\text{ s}$

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AV}	Avalanche current, repetitive or not repetitive (pulse width limited by maximum junction temperature)	90	A
E_{AS}	Single pulse avalanche energy ($T_J = 25\text{ }^\circ\text{C}$, $I_C = I_{AV}$, $V_{DD} = 16\text{ V}$)	400	mJ

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 5: On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	V _{GS} = 0 V, I _D = 1 mA	40			V
I _{DSS}	Zero gate voltage drain current	V _{GS} = 0 V, V _{DS} = 16 V			1	μA
		V _{GS} = 0 V, V _{DS} = 16 V, T _J = 125 °C ⁽¹⁾			10	μA
I _{GSS}	Gate-body leakage current	V _{DS} = 0 V, V _{GS} = ±20 V			±100	nA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 250 μA	2.5		3.5	V
R _{DS(on)}	Static drain-source on-resistance	V _{GS} = 10 V, I _D = 75 A		1.27	1.50	mΩ
		V _{GS} = 6.5 V, I _D = 75 A		1.48	2.00	

Notes:

⁽¹⁾Defined by design, not subject to production test.

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iss}	Input capacitance	V _{DS} = 10 V, f = 1 MHz, V _{GS} = 0 V	-	10700	-	pF
C _{oss}	Output capacitance		-	1530	-	pF
C _{rss}	Reverse transfer capacitance		-	1100	-	pF
Q _g	Total gate charge	V _{DD} = 32 V, I _D = 90 A, V _{GS} = 0 to 10 V (see Figure 14: "Test circuit for gate charge behavior")	-	172	-	nC
Q _{gs}	Gate-source charge		-	56	-	nC
Q _{gd}	Gate-drain charge		-	48	-	nC

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t _{d(on)}	Turn-on delay time	V _{DD} = 30 V, I _D = 75 A R _G = 30 Ω, V _{GS} = 10 V (see Figure 13: "Test circuit for resistive load switching times" and Figure 18: "Switching time waveform")	-	150	-	ns
t _r	Rise time		-	440	-	ns
t _{d(off)}	Turn-off-delay time		-	600	-	ns
t _f	Fall time		-	410	-	ns

Table 8: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}^{(1)}$	Source-drain current		-		120	A
$I_{SDM}^{(1)(2)}$	Source-drain current (pulsed)		-		480	A
$V_{SD}^{(3)}$	Forward on voltage	$V_{GS} = 0\text{ V}$, $I_{SD} = 90\text{ A}$	-		1.2	V
t_{rr}	Reverse recovery time	$I_{SD} = 90\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 20\text{ V}$ (see Figure 15: "Test circuit for inductive load switching and diode recovery times")	-	40		ns
Q_{rr}	Reverse recovery charge		-	53		nC
I_{RRM}	Reverse recovery current		-	2.5		A

Notes:

⁽¹⁾Limited by package.

⁽²⁾Pulse width is limited by safe operating area.

⁽³⁾Pulse test: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

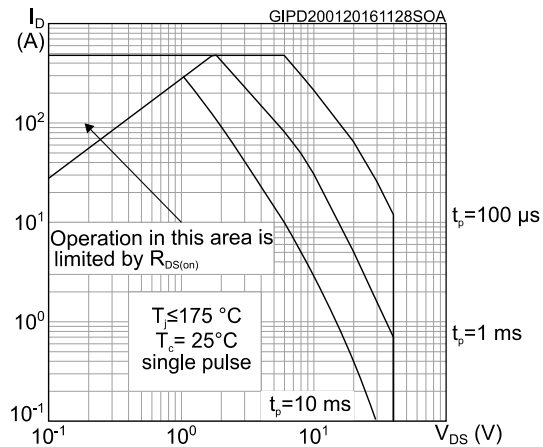


Figure 3: Thermal impedance

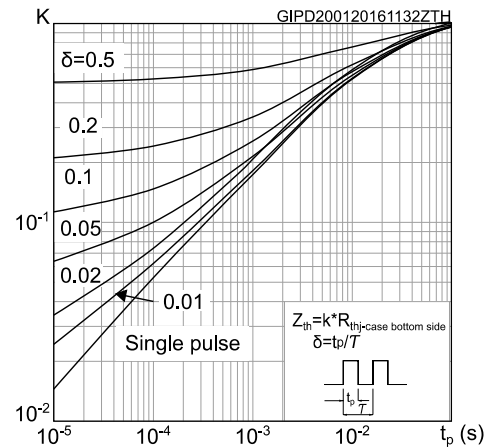


Figure 4: Output characteristics

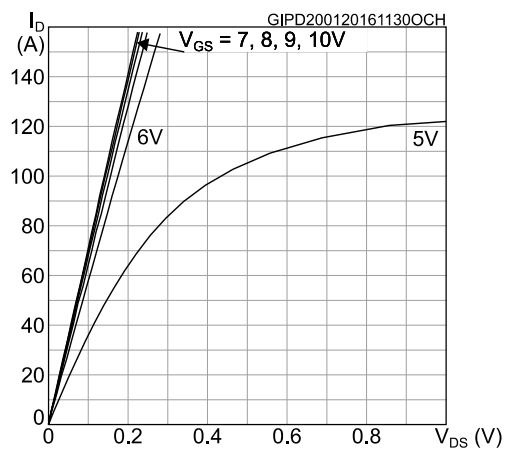


Figure 5: Transfer characteristics

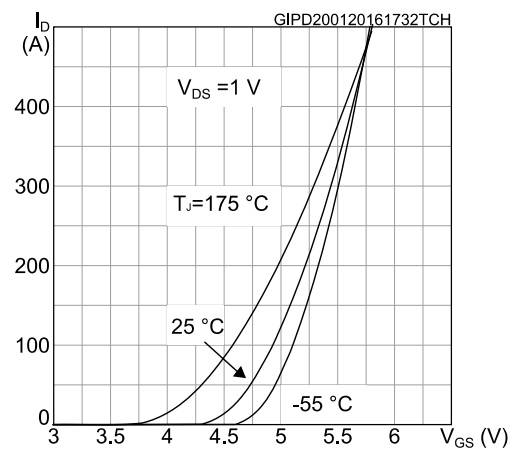


Figure 6: Gate charge vs gate-source voltage

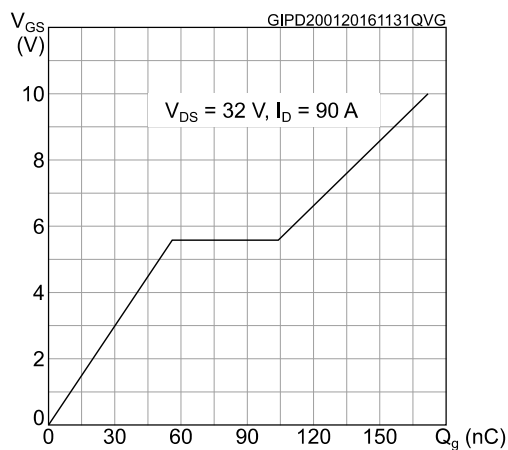


Figure 7: Static drain-source on-resistance

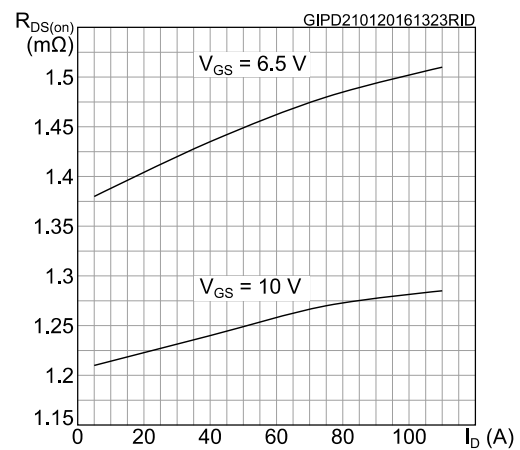


Figure 8: Capacitance variations

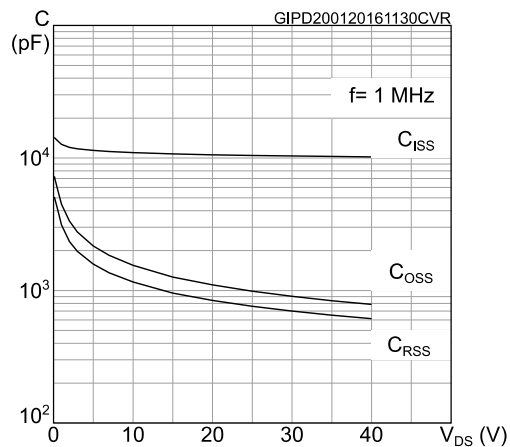


Figure 9: Normalized gate threshold voltage vs temperature

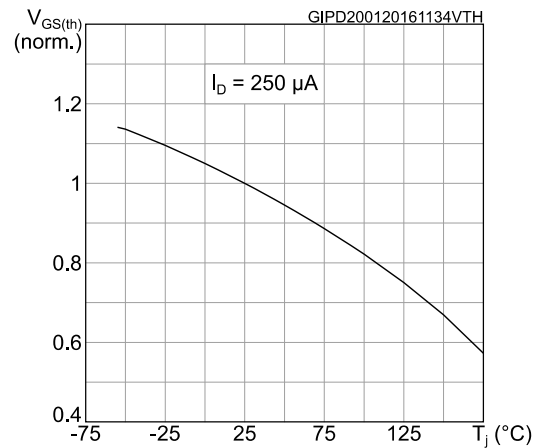


Figure 10: Normalized on-resistance vs temperature

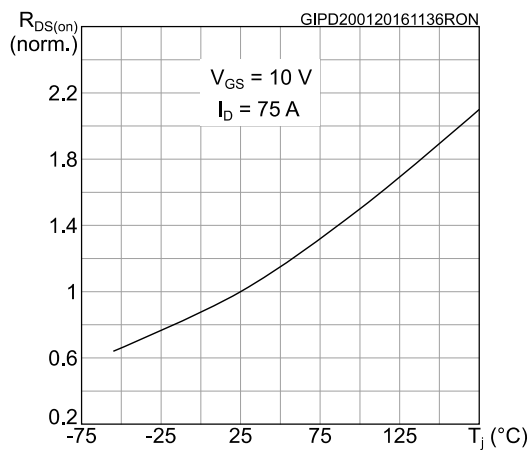
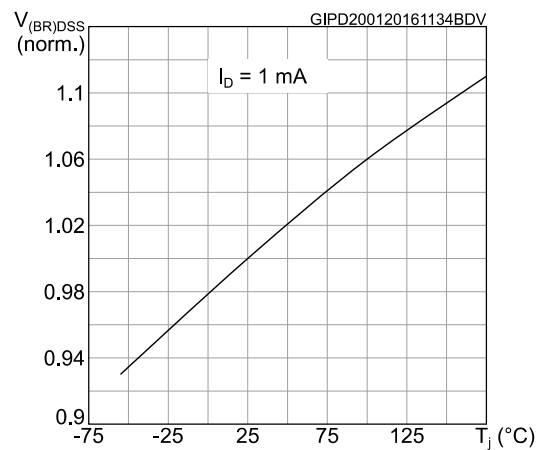
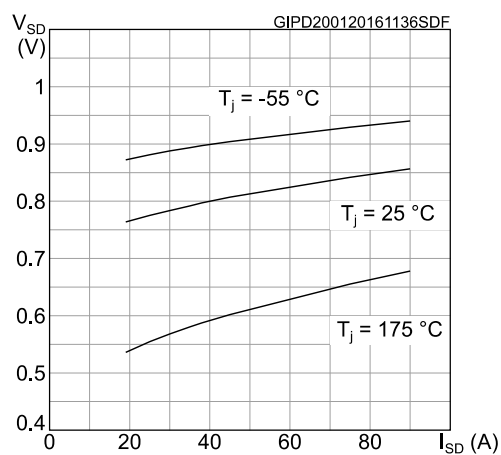
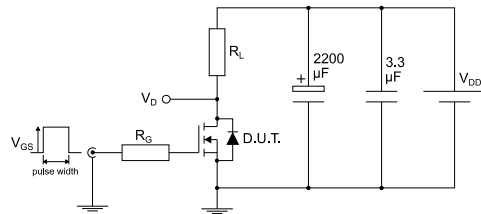
Figure 11: Normalized $V_{(BR)DSS}$ vs temperature

Figure 12: Source-drain diode forward characteristics



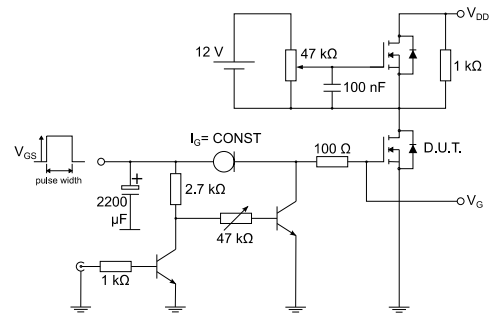
3 Test circuits

Figure 13: Test circuit for resistive load switching times



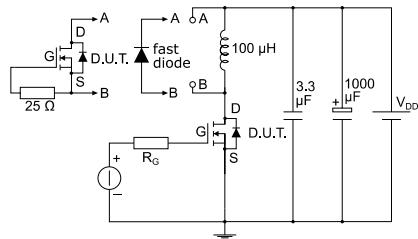
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Figure 14: Test circuit for gate charge behavior



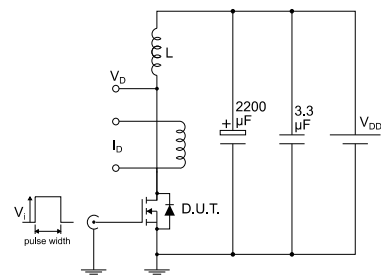
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Figure 15: Test circuit for inductive load switching and diode recovery times



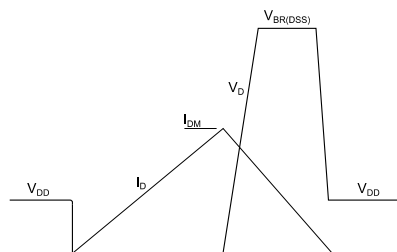
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Figure 16: Unclamped inductive load test circuit



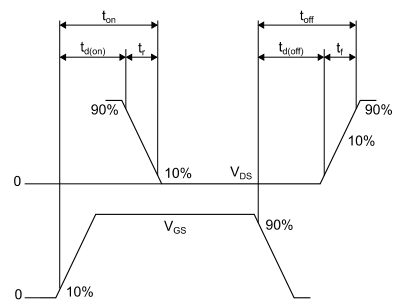
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Figure 17: Unclamped inductive waveform



AM01472v1

Figure 18: Switching time waveform



AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 PowerFLAT™ 5x6 dual side cooling package information

Figure 19: PowerFLAT™ 5x6 dual side cooling package outline

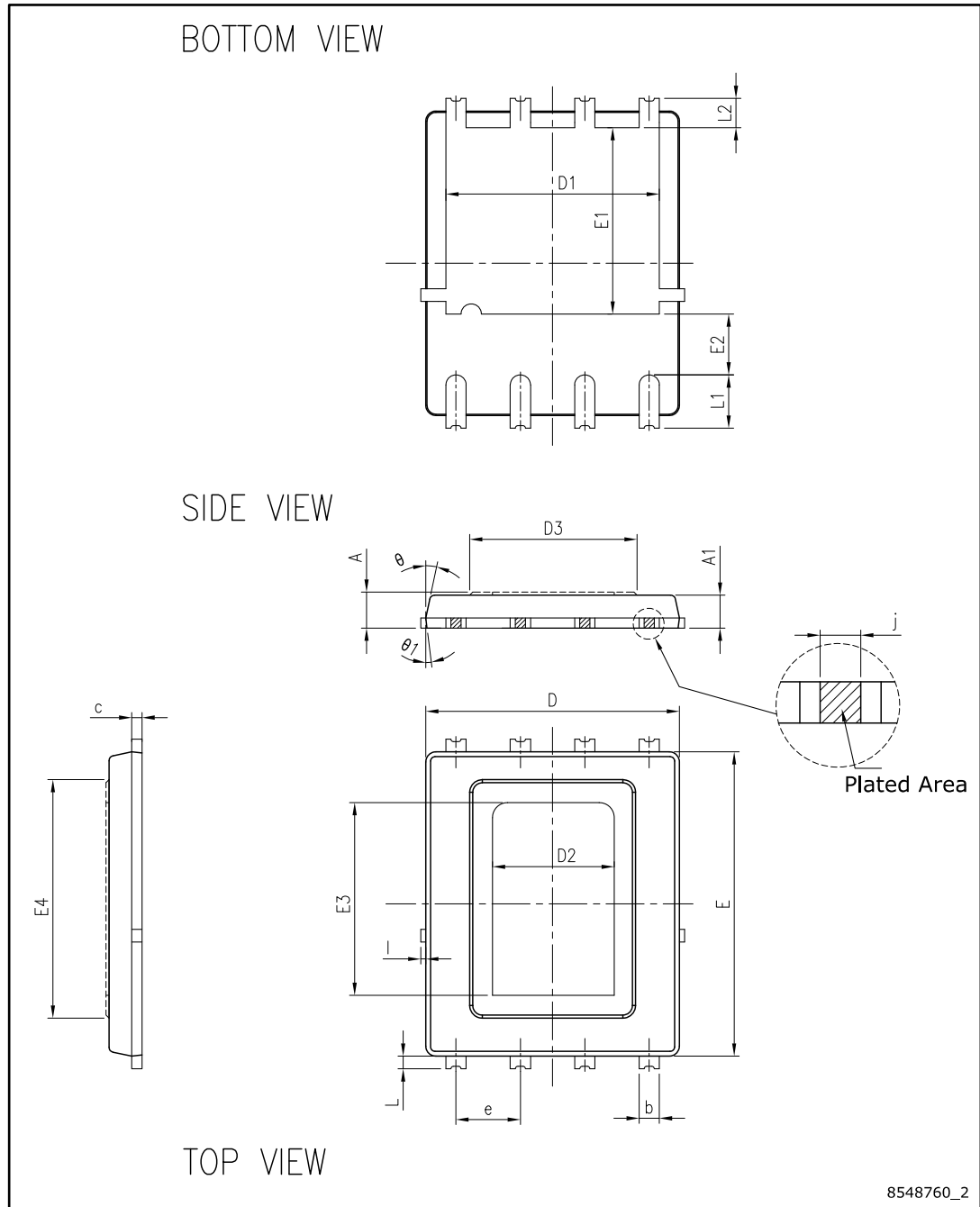
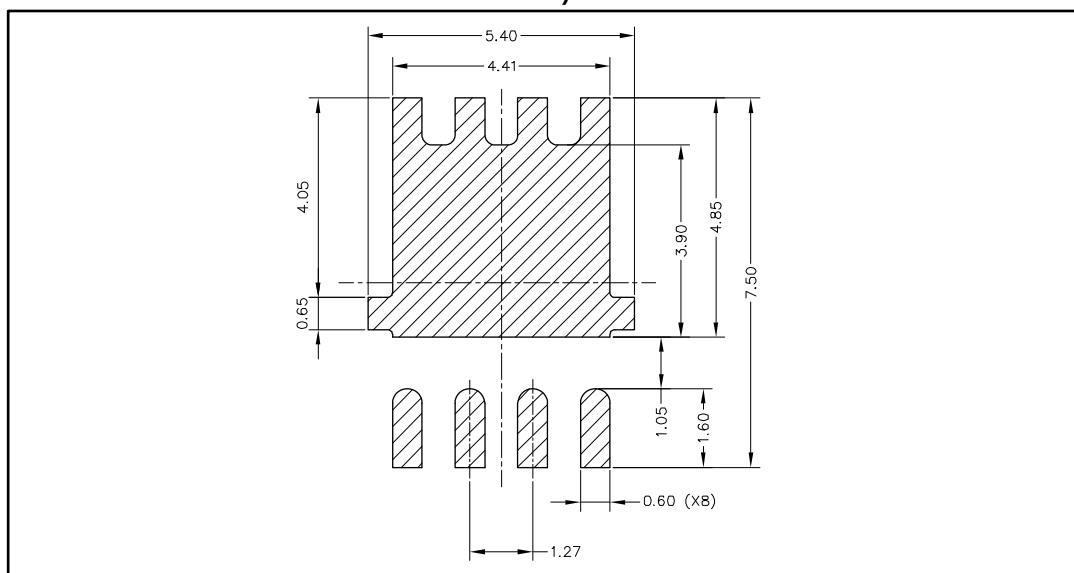


Table 9: PowerFLAT™ 5x6 dual side cooling mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.66	0.71	0.76
A1	0.60		0.75
b	0.33	0.43	0.53
c	0.15	0.203	0.30
D	5.00 BSC		
D1	4.06	4.21	4.36
D2	2.40 BSC		
D3	2.80	3.30	3.80
E	6.00 BSC		
E1	3.525	3.675	3.825
E2	1.05	1.20	1.35
E3	3.80 BSC		
E4	4.20	4.70	5.20
e	1.27 BSC		
l			0.15
L	0.15	0.25	0.35
L1	0.925	1.05	1.175
L2	0.45	0.575	0.70
ϑ	12° BSC		
ϑ1	7° BSC		
j	0.20 BSC		

Figure 20: PowerFLAT™ 5x6 dual side cooling recommended footprint (dimensions are in mm)



4.2 PowerFLAT™ 5x6 dual side cooling packing information

Figure 21: PowerFLAT™ 5x6 dual side cooling tape (dimensions are in mm)

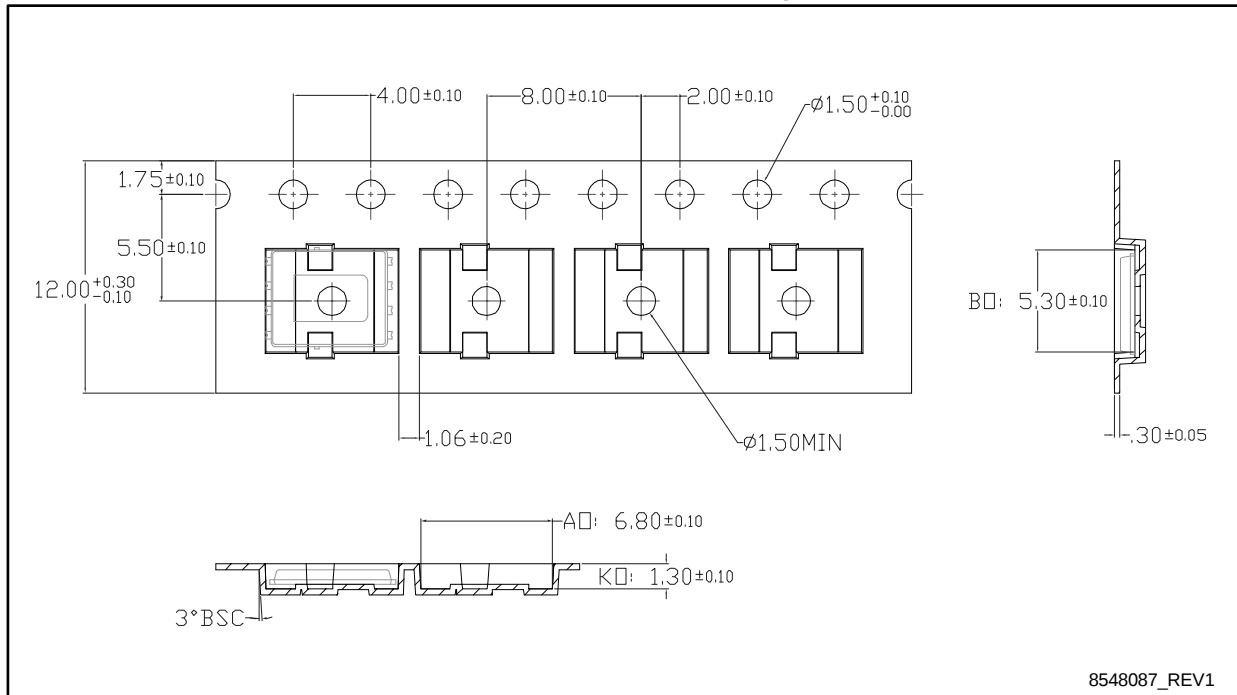
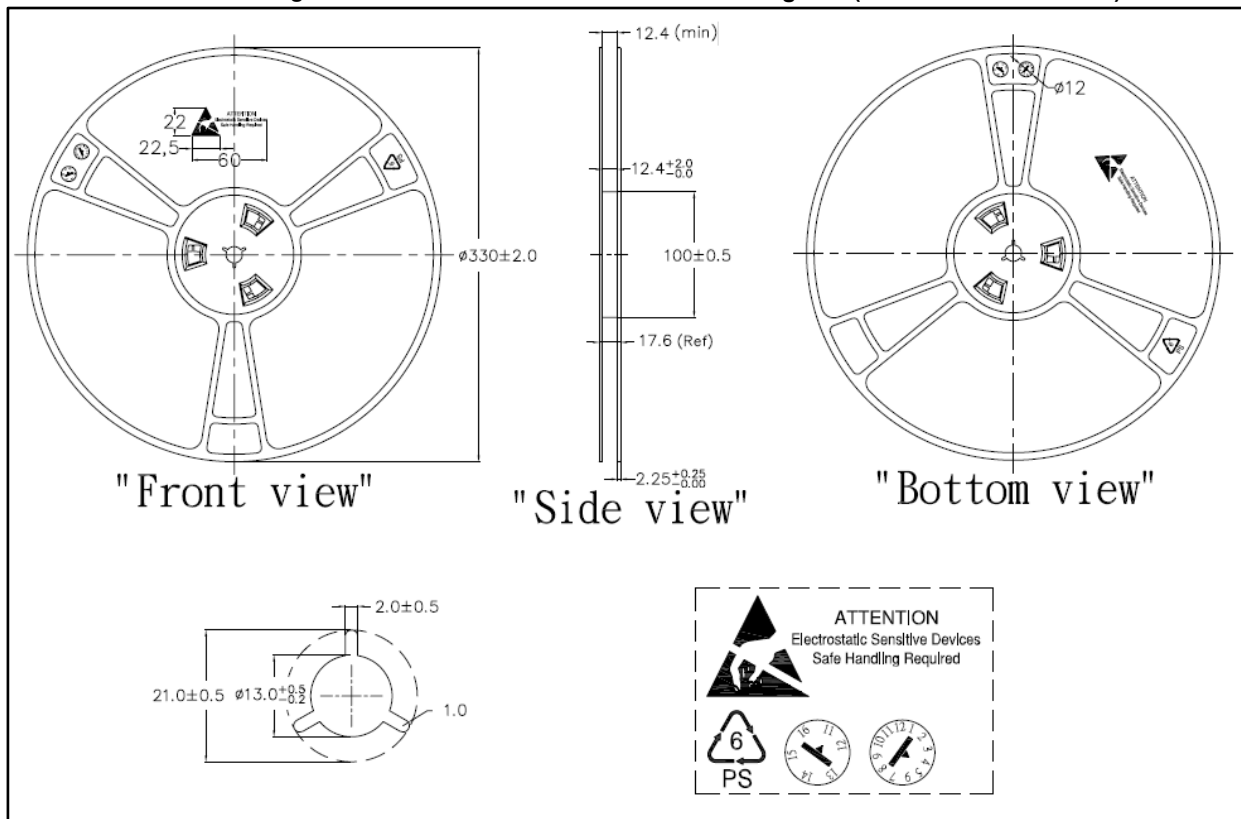


Figure 22: PowerFLAT™ 5x6 dual side cooling reel (dimensions are in mm)



5 Revision history

Table 10: Document revision history

Date	Revision	Changes
19-Jan-2016	1	First release
07-Feb-2017	2	Document status promoted from preliminary to production data. Updated <i>Table 3: "Thermal data"</i> and <i>Table 5: "On/off states"</i> . Minor text changes
23-Feb-2017	3	Updated features on cover page. Updated <i>Table 5: "On/off states"</i> and <i>Figure 9: "Normalized gate threshold voltage vs temperature"</i> Minor text changes
04-Apr-2017	4	Updated test conditions in <i>Table 7: "Switching times"</i> .
12-Jul-2017	5	Added Section 4.2: "PowerFLAT™ 5x6 dual side cooling packing information" .

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