

21-27GHz Down-Converter

GaAs Monolithic Microwave IC in SMD leadless package

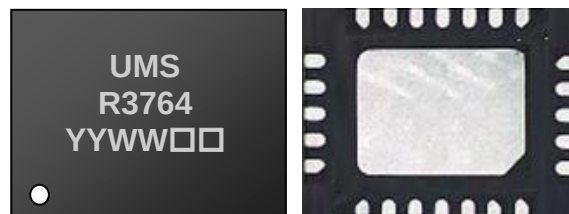
Description

The CHR3764-QEG is a multifunction monolithic circuit, which integrates a balanced cold FET mixer, a multiplier by two, and a RF LNA including gain control.

It is designed for a wide range of applications, typically ISM and commercial communication systems.

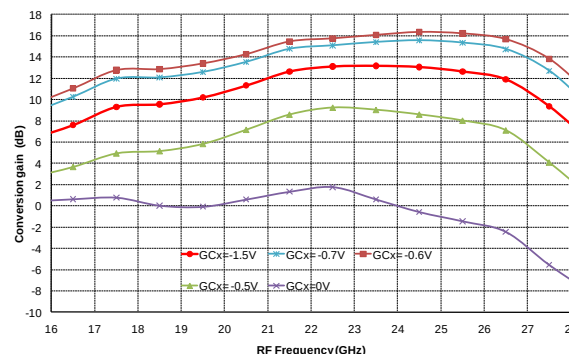
The circuit is manufactured with a pHEMT process, 0.25 μ m gate length, via holes through the substrate, air bridges and electron beam gate lithography.

It is supplied in RoHS compliant SMD package.



Main Features

- Broadband RF performance 21-26.5GHz
- 13dB conversion gain
- 3.1dB Noise Figure, for IF>0.1GHz
- 1dBm Input IP3
- 14dB Gain Control
- 15dBc Image Rejection
- DC bias: Vd=4Volt @ Id=320mA
- 24L-QFN4x5
- MSL1



Main Characteristics

Tamb.= +25°C, Vd = 4V

Symbol	Parameter	Min	Typ	Max	Unit
F _{RF}	RF frequency range	21		26.5	GHz
F _{OL}	LO frequency range	8.5		15	GHz
F _{IF}	IF frequency range	DC		3.5	GHz
NF	Noise Figure@ min. att., for IF>0.1GHz		3.0		dB

Electrical Characteristics

Tamb = +25°C, VD = VDL = 4V

Symbol	Parameter	Min	Typ	Max	Unit
F _{RF}	RF frequency range	21		26.5	GHz
F _{OL}	LO frequency range	8.5		15	GHz
F _{IF}	IF frequency range	DC		3.5	GHz
G _C	Conversion Gain @ min. attenuation	9	13		dB
ΔG	Gain control range		14		dB
NF	Noise Figure @ min. att. from 21 to 24GHz, for IF>0.1GHz		3.1	3.6	dB
	Noise Figure @ min. att. from 24 to 26.5GHz, for IF>0.1GHz		3.6	4.1	dB
Im_rej	Image rejection ⁽¹⁾		15		dBc
P _{LO}	LO Input power		0	5	dBm
IIP3	Input IP3 @ min. attenuation	0	2		dBm
	Input IP3 @ all gain range (ΔG)	-4	-2		dBm
2LO/RF	2LO leakage at RF port @ max. gain		30		dBc
RL _{RF}	RF Return loss		-10		dB
RL _{OL}	LO Return loss		-8		dB
VD, VDL	DC drain voltage		4		V
Id	Drain current (ID + IDL)		320		mA
VGL	LNA DC gate voltage ⁽²⁾		-0.6		V
GC2,3	Gain control DC voltage	-2	-1.5	0	V
VGM	Mixer DC gate voltage		-0.7		V

These values are representative of onboard measurements as defined on the drawing in paragraph "Evaluation mother board".

⁽¹⁾ An external combiner 90° is required on IF ports, I / Q.

⁽²⁾ Typical VGL value for IDL = 75mA

See in paragraph "biasing option" other possibility to optimise differently the performances

Note: Id is not affected by gain control (GC2, GC3).

Absolute Maximum Ratings ⁽¹⁾T_{amb.} = +25°C

Symbol	Parameter	Values	Unit
VD	Drain bias voltage	5	V
Id	Drain bias current	450	mA
VGL	LNA DC gate voltage	-2 to +0.4	V
VGM	Mixer DC gate voltage	-2 to +0.4	V
GC2,3	Gain control voltage	-2 to +0.8	V
P _{RF}	Maximum peak input power overdrive	10	dBm
P _{LO}	Maximum LO input power	10	dBm
T _j	Junction temperature ⁽²⁾	175	°C
Ta	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +150	°C

⁽¹⁾ Operation of this device above anyone of these parameters may cause permanent damage.

⁽²⁾ See "Device thermal performances"

Typical Bias ConditionsT_{amb.} = +25°C

Symbol	Pad N°	Parameter	Values	Unit
VDL, VD	10, 12	DC drain voltages	4	V
Id	10, 12	Total drain current	320	mA
VGL	9	DC gate voltage	-0.4	V
VGM	11	DC gate voltage	-0.7	V
GC2, GC3	7, 8	Gain control DC voltage	-2 to +0	V

Device thermal performances

All the figures given in this section are obtained assuming that the QFN device is cooled down only by conduction through the package thermal pad (no convection mode considered). The temperature is monitored at the package back-side interface (Tcase) as shown below. The system maximum temperature must be adjusted in order to guarantee that Tcase remains below than the maximum value specified in the next table. So, the system PCB must be designed to comply with this requirement.

A derating must be applied on the dissipated power if the Tcase temperature cannot be maintained below than the maximum temperature specified (see the curve Pdiss. Max) in order to guarantee the nominal device life time (MTTF).

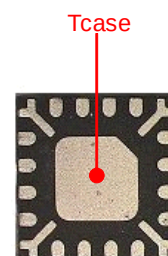
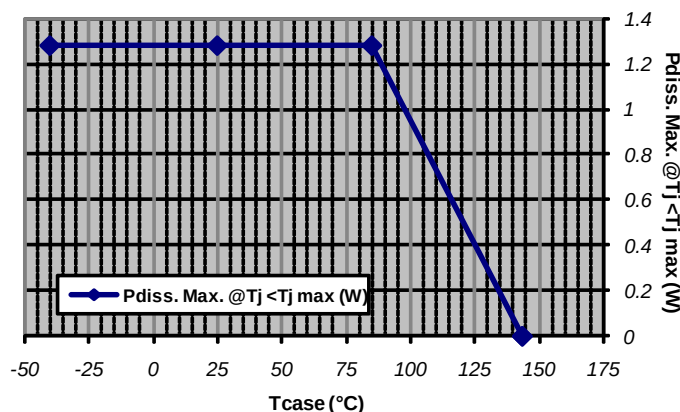
DEVICE THERMAL SPECIFICATION : CHR3764-QEG

Recommended max. junction temperature (Tj max)	:	143 °C
Junction temperature absolute maximum rating	:	175 °C
Max. continuous dissipated power (Pdiss. Max.)	:	1.3 W
=> Pdiss. Max. derating above Tcase ⁽¹⁾ = 85 °C	:	22 mW/°C
Junction-Case thermal resistance (Rth J-C) ⁽²⁾	:	<45 °C/W
Minimum Tcase operating temperature ⁽³⁾	:	-40 °C
Maximum Tcase operating temperature ⁽³⁾	:	85 °C
Minimum storage temperature	:	-55 °C
Maximum storage temperature	:	150 °C

(1) Derating at junction temperature constant = Tj max.

(2) Rth J-C is calculated for a worst case considering the **hottest junction** of the MMIC and all the devices biased.

(3) Tcase=Package back side temperature measured under the die-attach-pad (see the drawing below).



Example: QFN 16L 3x3
Location of temperature reference point (Tcase) on package's bottom side

6.0

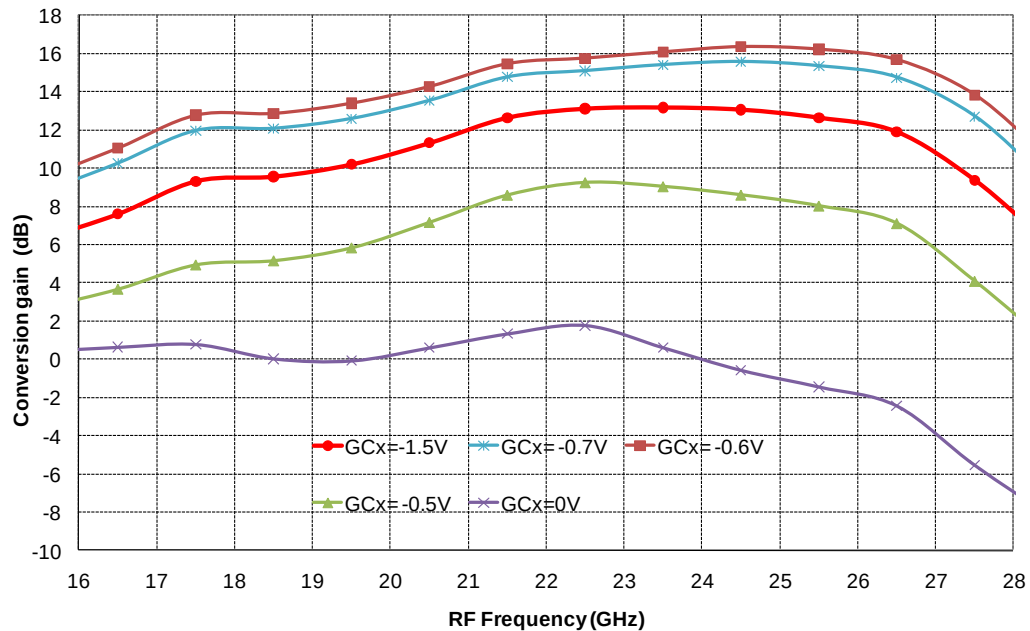
Typical Board Measurements

Tamb = +25°C, VD = VDL = 4V, VGL = -0.6V, VGM = -0.7V, P_LO = 0dBm

Board is defined on the drawing at paragraph "Evaluation mother board". The board losses are de-embedded. The results are given in the package access planes.

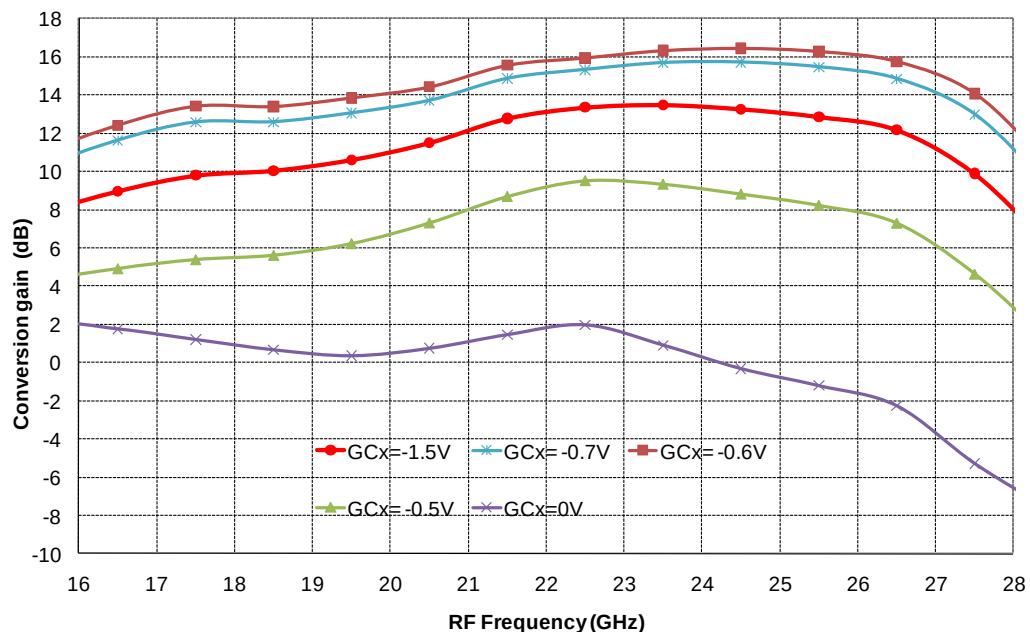
Conversion Gain in Supradyn Mode versus RF Frequency & GCx

$$F_{RF} = 2 \times F_{LO} + F_{IF}, F_{IF} = 1.5\text{GHz}$$



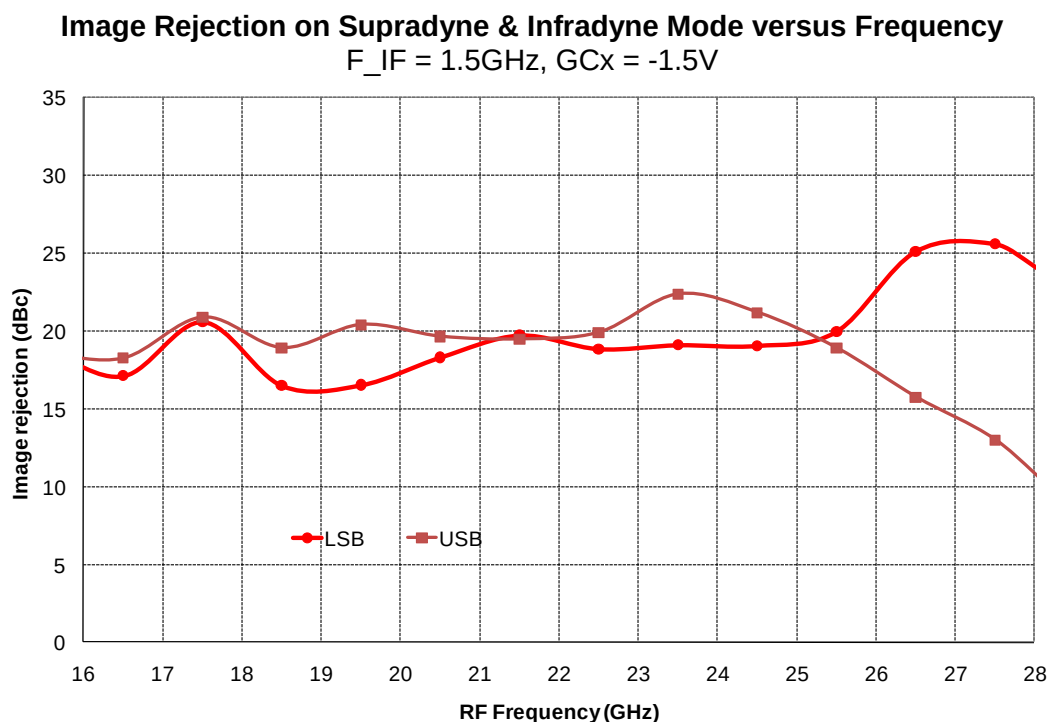
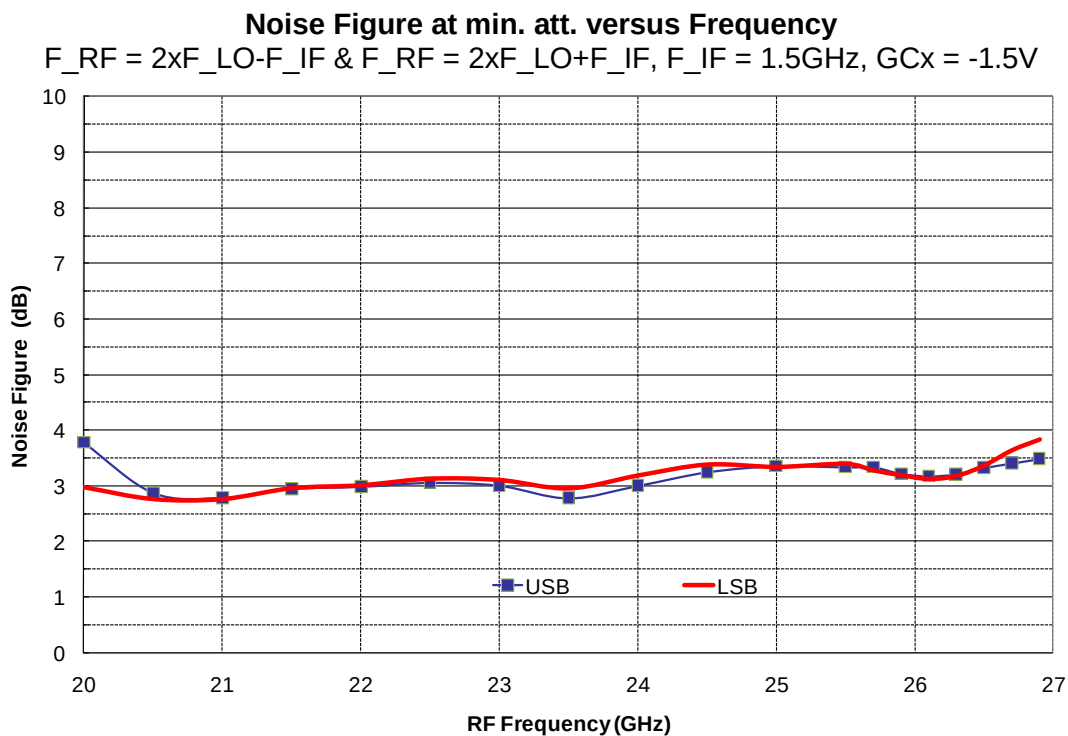
Conversion Gain in Infradyne Mode versus RF Frequency & GCx

$$RF = 2 \times F_{LO} - F_{IF}, F_{IF} = 1.5\text{GHz}$$



Typical Board Measurements

Tamb = +25°C, VD = VDL = 4V, VGL = -0.6V, VGM = -0.7V, P_LO = 0dBm

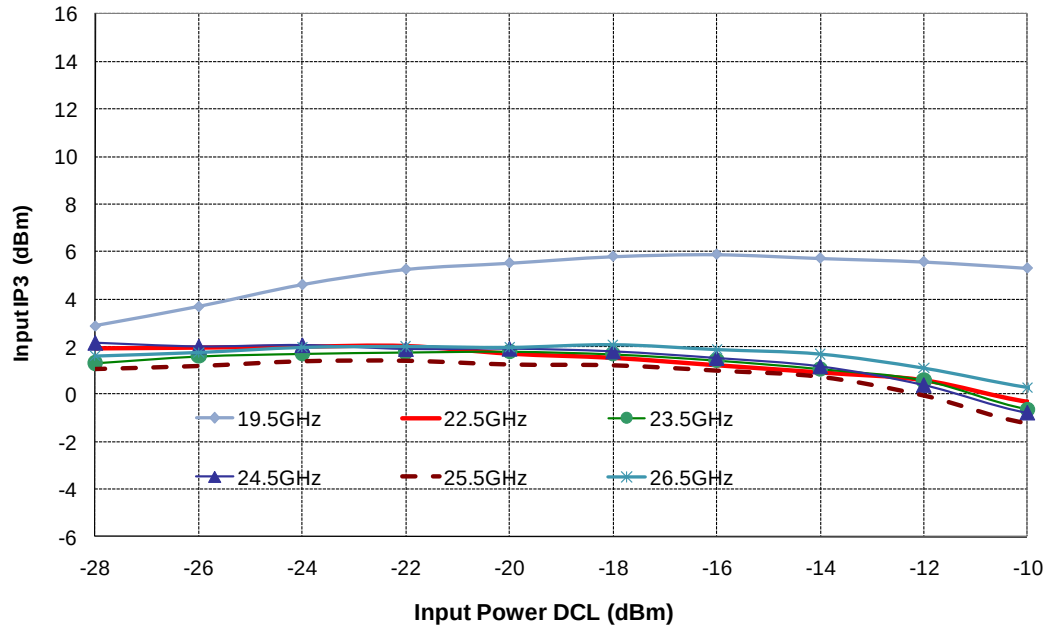


Typical Board Measurements

Tamb = +25°C, VD = VDL = 4V, VGL = -0.6V, VGM = -0.7V, P_LO = 0dBm

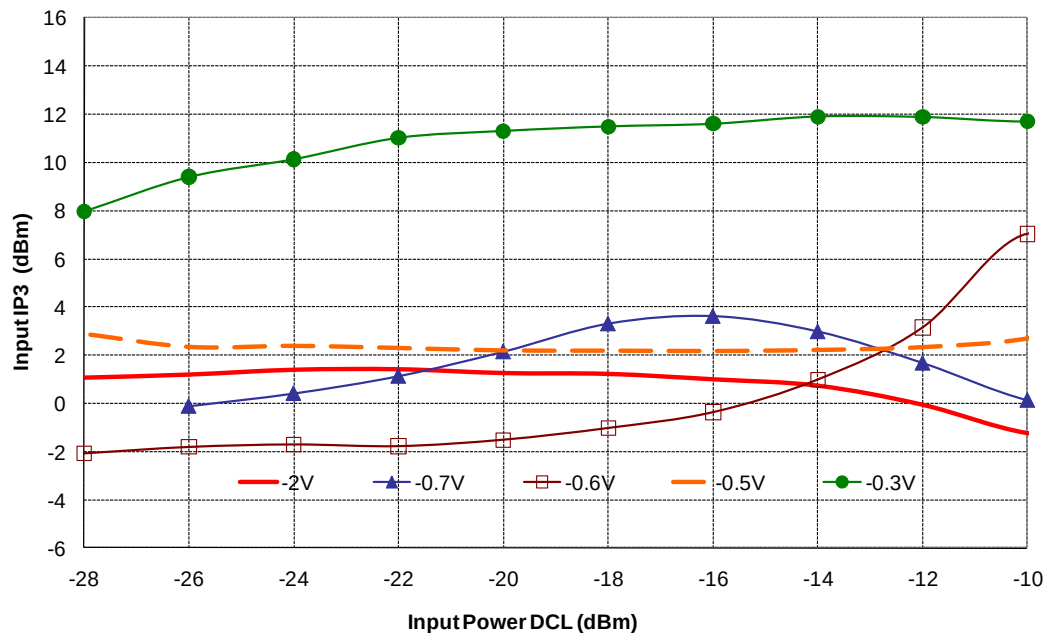
Input IP3 versus Frequency at GCx = -1.5V

$F_{RF} = 2 \times F_{LO} - F_{IF}$, $F_{IF} = 1.5\text{GHz}$



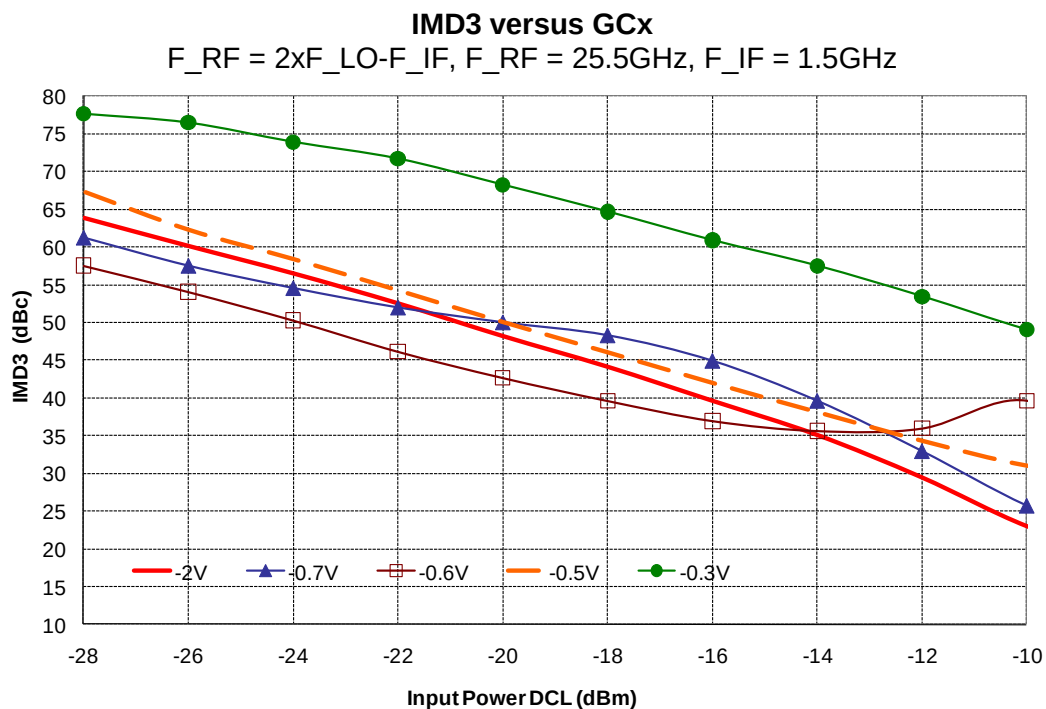
Input IP3 versus GCx

$F_{RF} = 2 \times F_{LO} - F_{IF}$, $F_{RF} = 25.5\text{GHz}$, $F_{IF} = 1.5\text{GHz}$

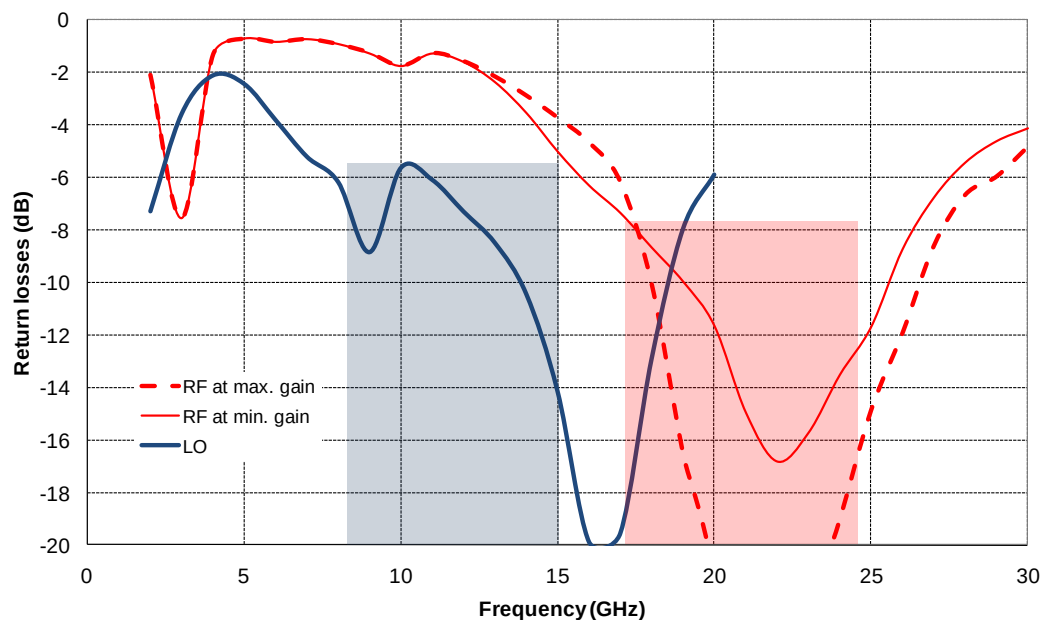


Typical Board Measurements

Tamb = +25°C, VD = VDL = 4V, VGL = -0.6V, VGM = -0.7V, P_LO = 0dBm



RF & LO return loss



Typical Board Measurements

Tamb = +25°C, VD = VDL = 4V, VGL = -0.6V, VGM = -0.7V, P_LO = 0dBm

Spurious on IF outputs

$$RF = 2LO + IF$$

$$P_{RF} = -20\text{dBm} / P_{LO} = 0\text{dBm @12GHz}$$

mRF	nLO				
	0	1	2	3	4
0	xx	37	20	41	37
1	26	49	>55	39	52
2	>50	>50	>55	>60	23

All values in dBc below IF power level (IF = 1.5GHz).

Data measured without external hybrid coupler.

Temperature Board Measurements

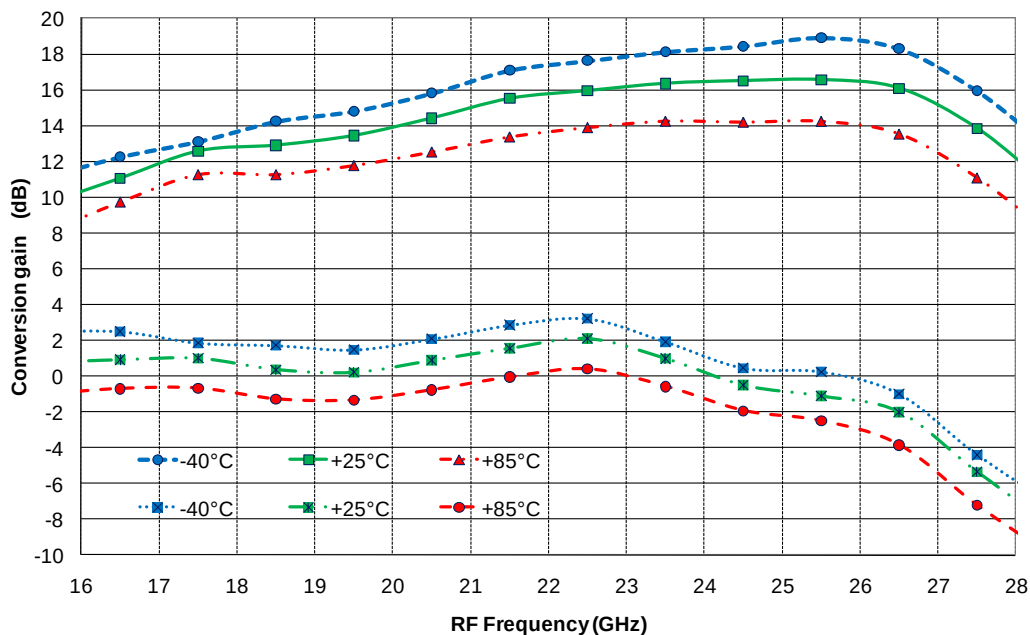
$T = [-40, +25, 85] ^\circ\text{C}$, $V_D = V_{DL} = 4\text{V}$, $V_{GL} = -0.6\text{V}$, $V_{GM} = -0.7\text{V}$, $P_{LO} = 0\text{dBm}$

Board is defined on the drawing at paragraph "Evaluation mother board". The board losses are de-embedded. The results are given in the package access planes.

Conversion Gain in Supradyn Mode versus Frequency

$F_{RF} = 2 \times F_{LO} + F_{IF}$, $F_{IF} = 1.5\text{GHz}$, $GCx = -1.5\text{V} \text{ \& } 0\text{V}$

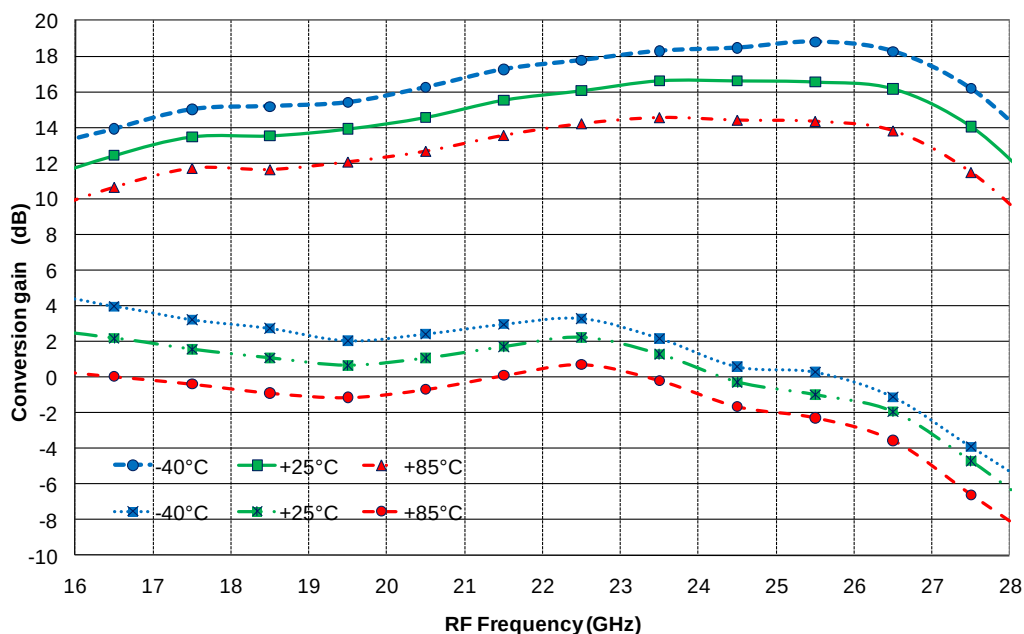
Board losses de-embedded (result given on package access planes)



Conversion Gain in Infradyne Mode versus Frequency

$F_{RF} = 2 \times F_{LO} - F_{IF}$, $F_{IF} = 2.0\text{GHz}$, $GCx = -1.5\text{V} \text{ \& } 0\text{V}$

Board losses de-embedded (result given on package access planes)



Temperature Board Measurements

$T = [-40, +25, 85] ^\circ\text{C}$, $V_D = V_{DL} = 4\text{V}$, $V_{GL} = -0.6\text{V}$, $V_{GM} = -0.7\text{V}$, $P_{LO} = 0\text{dBm}$

Noise Figure in Supradyn Mode at min. att. versus Frequency

$F_{RF} = 2 \times F_{LO} + F_{IF}$, $F_{IF} = 1.5\text{GHz}$, $GCx = -1.5\text{V}$

Board losses de-embedded (result given on package access planes)

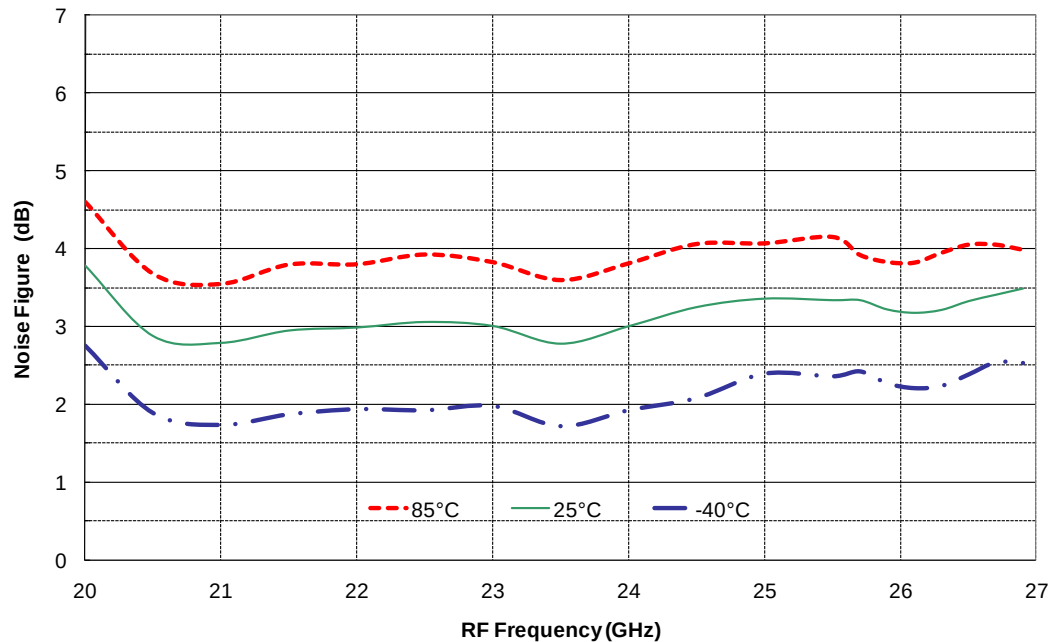
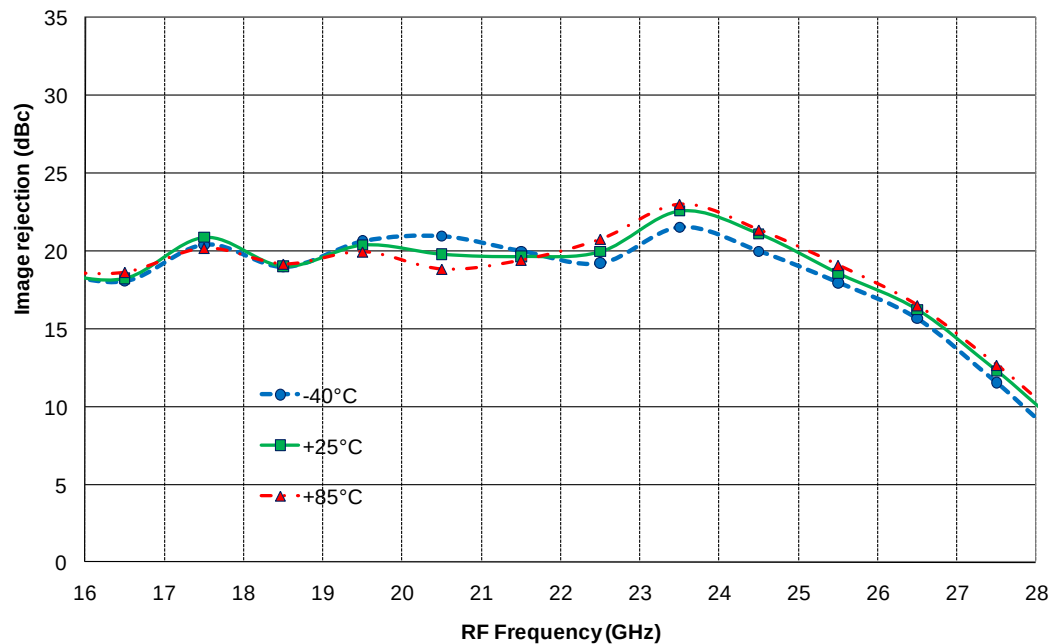


Image Rejection on Supradyn Mode versus Frequency

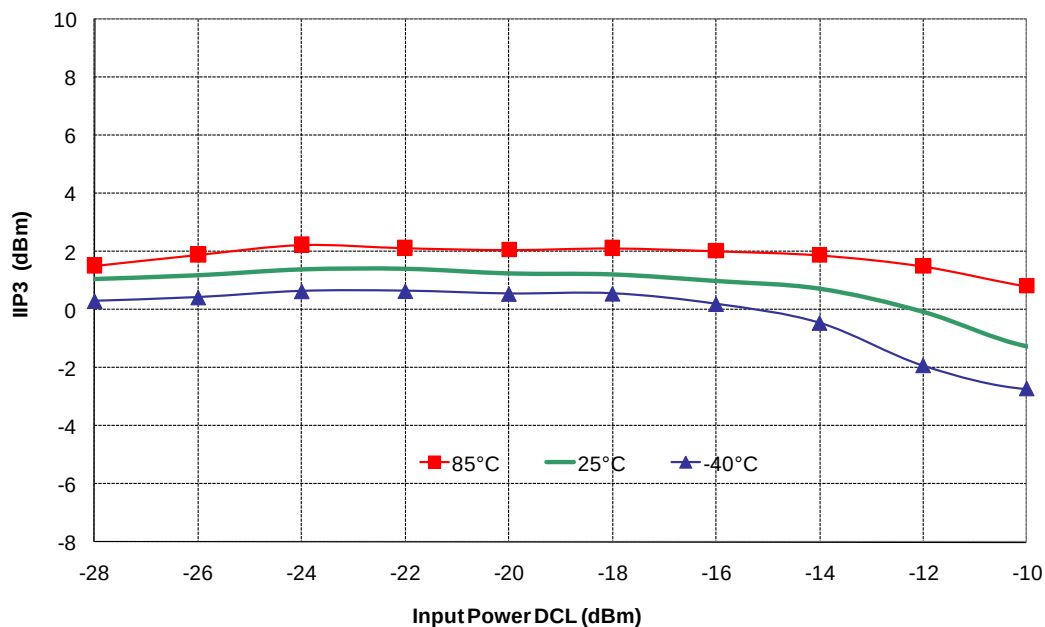
$F_{IF} = 1.5\text{GHz}$, $GCx = -1.5\text{V}$



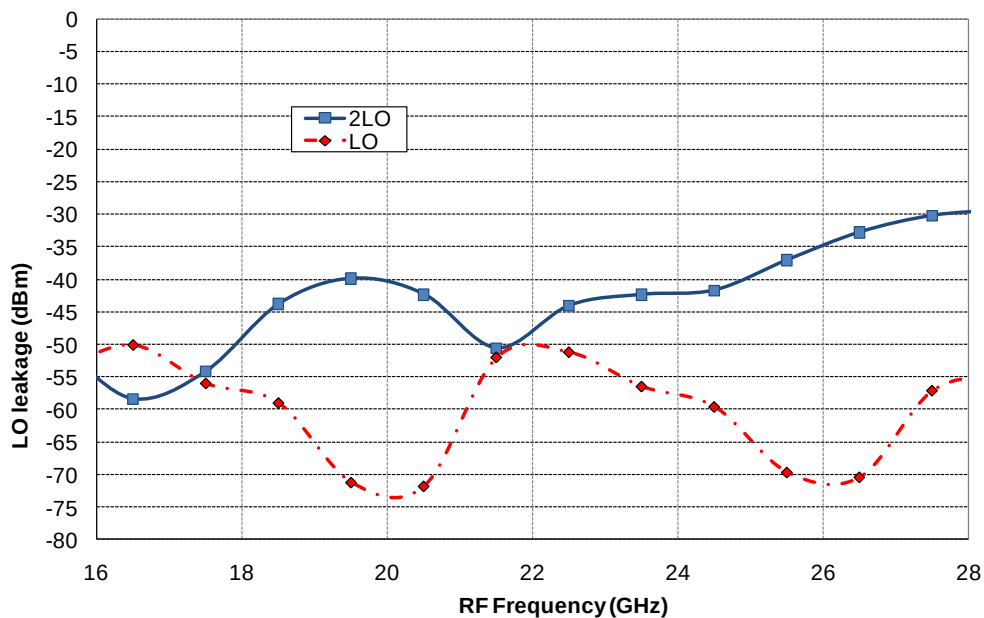
Temperature Board Measurements

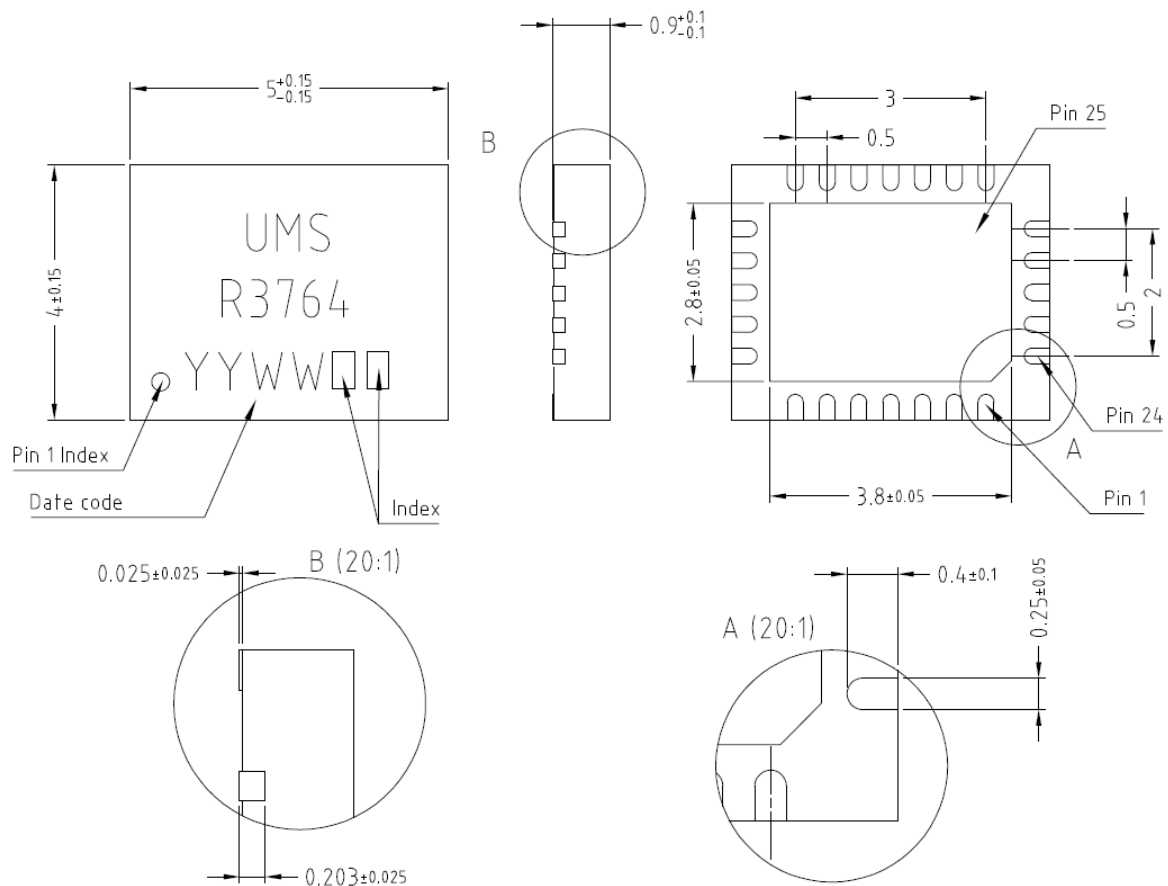
T = [-40, +25, 85] °C, VD = VDL = 4V, VGL = -0.6V, VGM = -0.7V, P_LO = 0dBm

Input IP3 versus Temperature at GCx = -1.5V
 $F_{RF} = 2 \times F_{LO} - F_{IF}$, $F_{RF} = 25.5\text{GHz}$, $F_{IF} = 1.5\text{GHz}$



LO & 2LO leakage at GCx = -1.5V
 At RF port and T= 25°C



Package outline ⁽¹⁾

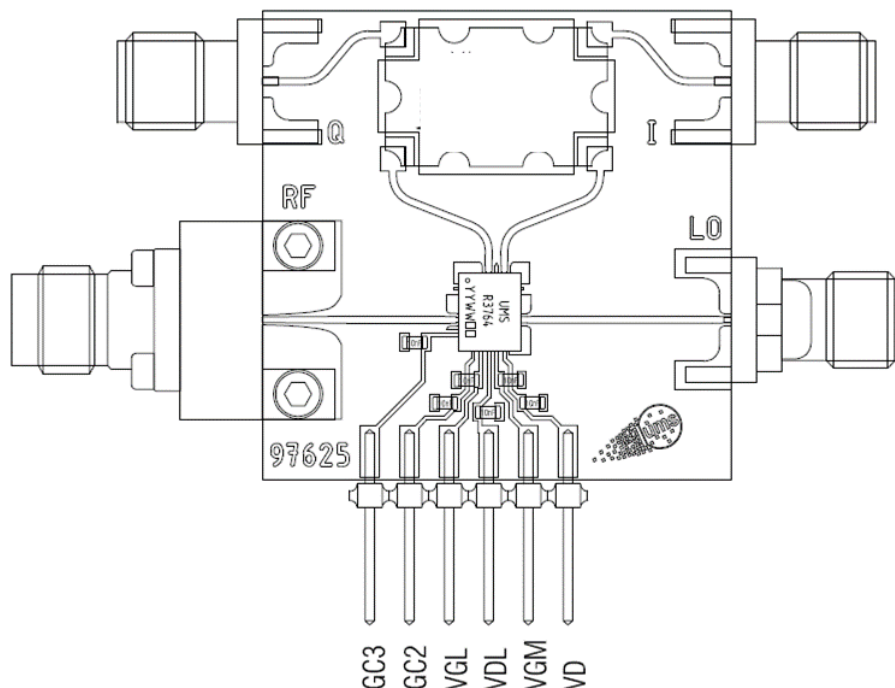
Matt tin, Lead Free (Green)	1- Nc	9- VGL	17- Nc
Units : mm	2- Nc	10- VDL	18- Nc
From the standard : JEDEC MO-220 (VGGD)	3- Nc	11- VGM	19- Nc
	4- GND ⁽²⁾	12- VD	20- IF_I out
25- GND	5- RF in	13- Nc	21- GND ⁽²⁾
	6- GND ⁽²⁾	14- GND ⁽²⁾	22- IF_Q out
	7- GC3	15- LO in	23- Nc
	8- GC2	16- GND ⁽²⁾	24- Nc

⁽¹⁾ The package outline drawing included to this data-sheet is given for indication. Refer to the application note AN0017 (<http://www.ums-gaas.com>) for exact package dimensions.

⁽²⁾ It is strongly recommended to ground all pins marked "Gnd" through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.

Evaluation mother board

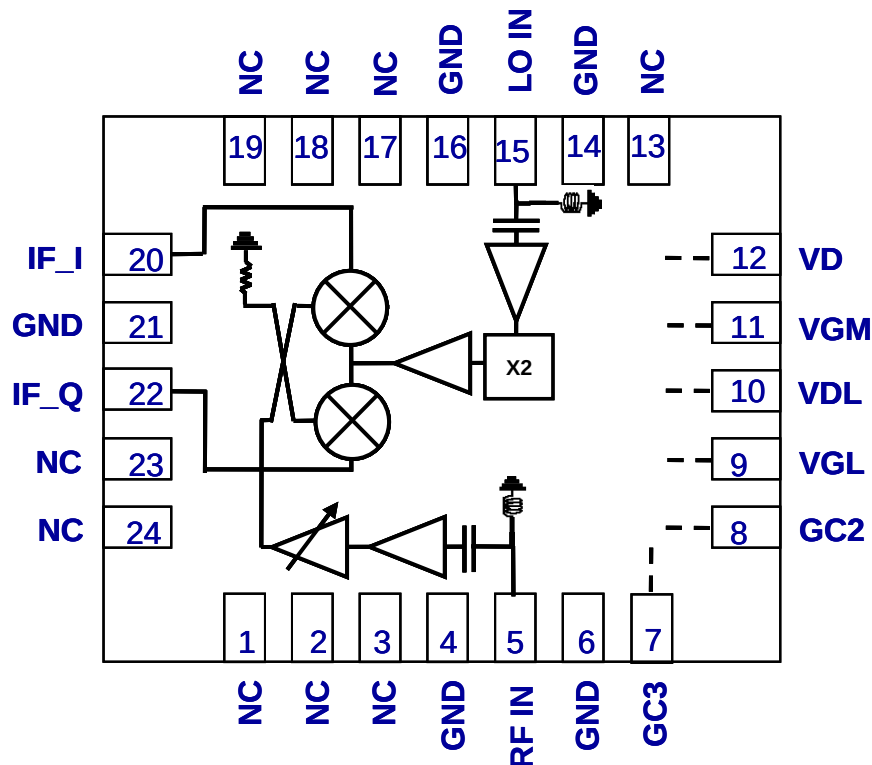
- Compatible with the proposed footprint.
- Based on typically Ro4003 / 8mils or equivalent.
- Using a micro-strip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of 10nF $\pm 10\%$ are recommended for all DC accesses.
- See application note AN0017 for details.



Hybrid coupler 90° 1-2GHz

Notes

Due to ESD protection circuits on RF and LO inputs, an external capacitance might be requested to isolate the product from external voltage that could be present on these accesses in the application.

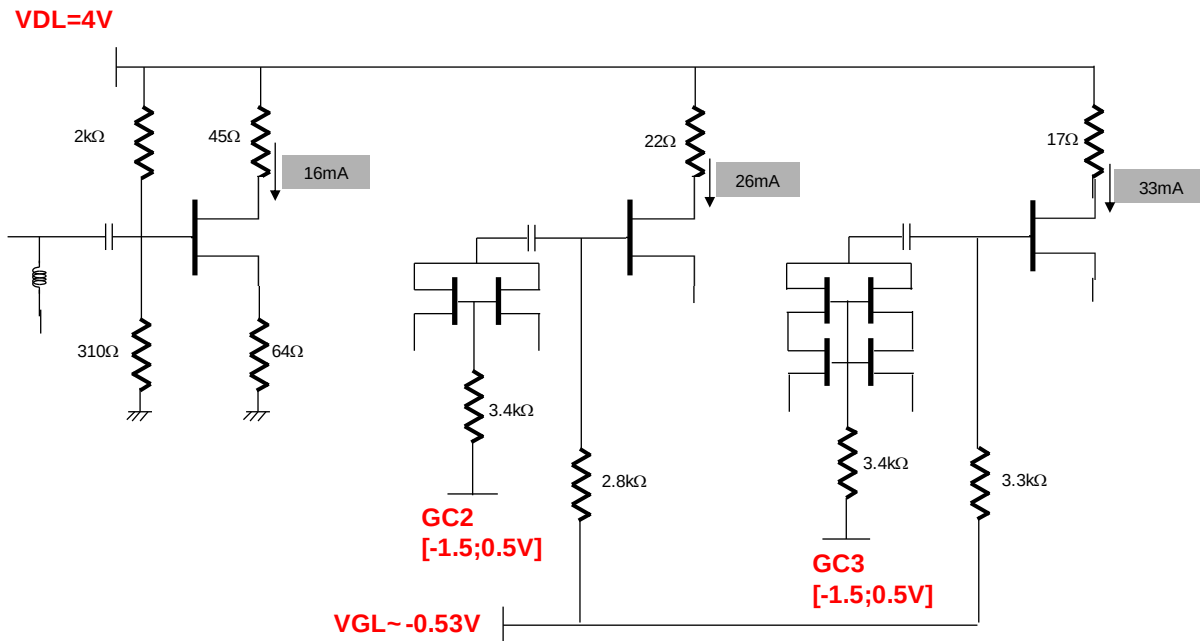


ESD protections are implemented on gate accesses.

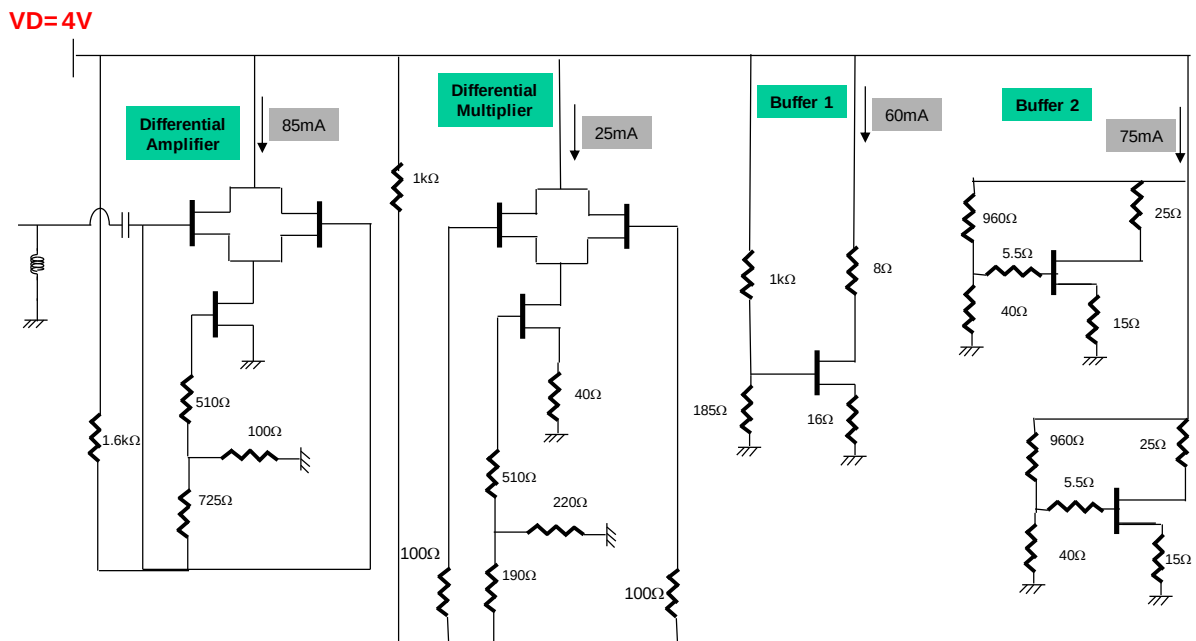
The DC connections do not include any decoupling capacitor in package, therefore it is mandatory to provide a good external DC decoupling on the PC board with SMT capacitor, as close as possible to the package. Recommended value is 10nF

DC Schematic

LNA (4V, 75mA)



LO Buffer (4V, 245mA)



Biasing Options

In order to improve the conversion gain and the noise figure, the biasing could be tuned.

VGL voltage allows controlling IDL current.

Table below gives the typical value for main characteristics.

Parameter	VD=VDL= 4.0V IDL= 75mA	VD=VDL= 4.5V IDL= 110mA
Conversion Gain@min. att. (dB)	13	14
Noise Figure@min. att. from 17 to 24GHz (dB)	3.1	3.0
Input IP3@min. att. (dBm)	1	2
VGL (V)	-0.6	-0.4
ID (mA)	245	250
ID + IDL (mA)	320	360
Total DC power consumption (mW)	1280	1620

Recommended package footprint

Refer to the application note AN0017 available at <http://www.ums-gaas.com> for package footprint recommendations.

SMD mounting procedure

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017.

Recommended environmental management

Refer to the application note AN0019 available at <http://www.ums-gaas.com> for environmental data on UMS package products.

Recommended ESD management

Refer to the application note AN0020 available at <http://www.ums-gaas.com> for ESD sensitivity and handling recommendations for the UMS package products.

Ordering Information

QFN 4x5 RoHS compliant package:

CHR3764-QEG/XY

Stick: XY = 20

Tape & reel: XY = 21

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