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August 2016

FDP12N50NZ / FDPF12N50NZ

N-Channel UniFETTM II MOSFET 500 V, 11.5 A, 520 m Ω

Features

- $R_{DS(on)}$ = 460 m Ω (Typ.) @ V_{GS} = 10 V, I_D = 5.75 A
- Low Gate Charge (Typ. 23 nC)
- Low C_{rss} (Typ. 14 pF)
- · 100% Avalanche Tested
- · ESD Improved Capability
- · RoHS Compliant

Applications

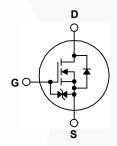
- LCD/LED/PDP TV
- Lighting
- · Uninterruptible Power Supply

Description

UniFETTM II MOSFET is Fairchild Semiconductor's high voltage MOSFET family based on advanced planar stripe and DMOS technology. This advanced MOSFET family has the smallest on-state resistance among the planar MOSFET, and also provides superior switching performance and higher avalanche energy strength. In addition, internal gate-source ESD diode allows UniFET II MOSFET to withstand over 2kV HBM surge stress. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.







MOSFET Maximum Ratings T_C = 25°C unless otherwise noted.

Symbol		Parameter		FDP12N50NZ	FDPF12N50NZ	Unit
V _{DSS}	Drain to Source Voltage			5	V	
V _{GSS}	Gate to Source Voltage			±	25	V
	Drain Current	- Continuous (T _C = 25°C)		11.5	11.5*	Α
ID	Drain Current	- Continuous (T _C = 100°C)		6.9	6.9*	А
I _{DM}	Drain Current	- Pulsed (Note 1)		1) 46 46*		Α
E _{AS}	Single Pulsed Avalanche Energy		(Note 2)	560		mJ
I _{AR}	Avalanche Current		(Note 1)	11.5		Α
E _{AR}	Repetitive Avalanche Energy		(Note 1)	17		mJ
dv/dt	MOSFET dv/dt Ruggedness			20		V/ns
av/at	Peak Diode Recovery dv/dt		(Note 3)	3) 10		V/ns
n	Dower Dissination	(T _C = 25°C)		170	42	W
P_{D}	Power Dissipation - Derate above 25°C		1.37	0.33	W/°C	
T _J , T _{STG}	Operating and Storage Temperature Range			-55 to	+150	°C
T _L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds			οС		

^{*}Drain current limited by maximum junction temperature

Thermal Characteristics

Symbol	Parameter	FDP12N50NZ	FDPF12N50NZ	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.73	3.0	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	62.5	C/VV

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDP12N50NZ	FDP12N50NZ	TO-220	Tube	N/A	50 units
FDPF12N50NZ	FDPF12N50NZ	TO-220F	Tube	N/A	50 units

Electrical Characteristics $T_C = 25^{\circ}C$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
Off Charac	eteristics					
BV _{DSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu A$, $V_{GS} = 0 V$, $T_J = 25 ^{\circ} C$	500	-	-	V
ΔBV _{DSS} / ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 250μA, Referenced to 25°C	-	0.5	-	V/°C
I	Zero Gate Voltage Drain Current	V _{DS} = 500V, V _{GS} = 0V	-	-	1	
IDSS	Zero Gate Voltage Drain Current	$V_{DS} = 400V, T_{C} = 125^{\circ}C$	-	-	10	μΑ
I _{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 25V, V_{DS} = 0V$	-	-	±10	μΑ

On Characteristics

V _{GS(th)}	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = 250 \mu A$	3.0	-	5.0	V
R _{DS(on)}	Static Drain to Source On Resistance	$V_{GS} = 10V, I_D = 5.75A$	-	0.46	0.52	Ω
9 _{FS}	Forward Transconductance	$V_{DS} = 20V, I_D = 5.75A$	-	12	-	S

Dynamic Characteristics

C _{iss}	Input Capacitance	V 051/ 1/ 01/		-	945	1235	pF
Coss	Output Capacitance	$V_{DS} = 25V, V_{GS} = 0V$ f = 1MHz		-\	155	205	pF
C _{rss}	Reverse Transfer Capacitance	1 = 111112		- \	14	20	pF
Qg	Total Gate Charge at 10V	V _{DS} = 400V, I _D = 11.5A		-	23	30	nC
Q _{gs}	Gate to Source Gate Charge	V _{GS} = 10V		-	5.5	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		(Note 4)	-	9.6	-	nC

Switching Characteristics

t _{d(on)}	Turn-On Delay Time	V _{DD} = 250V, I _D = 11.5A	-	20	50	ns
t _r	Turn-On Rise Time	$R_G = 25\Omega$	-	50	110	ns
t _{d(off)}	Turn-Off Delay Time		-	60	130	ns
t _f	Turn-Off Fall Time	(Note 4)	-	45	100	ns

Drain-Source Diode Characteristics

I _S	Maximum Continuous Drain to Source Diode Forward Current			-	11.5	Α
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	46	Α
V_{SD}	Drain to Source Diode Forward Voltage V _{GS} = 0V, I _{SD} = 11.5A		-	-	1.4	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0V, I _{SD} = 11.5A	-	315	/ -	ns
Q _{rr}	Reverse Recovery Charge	$dI_F/dt = 100A/\mu s$	-	2.0	-	μС

Notes

- Repetitive Rating: Pulse width limited by maximum junction temperature
- 2. L = 8.5mH, I $_{AS}$ = 11.5A, V $_{DD}$ = 50V, R $_{G}$ = 25 $\!\Omega$, Starting T $_{J}$ = 25°C
- 3. $I_{SD} \leq$ 11.5A, di/dt \leq 200A/ μ s, $V_{DD} \leq$ BV $_{DSS}$, Starting T $_{J}$ = 25°C
- 4. Essentially Independent of Operating Temperature Typical Characteristics

Typical Characteristics

Figure 1. On-Region Characteristics

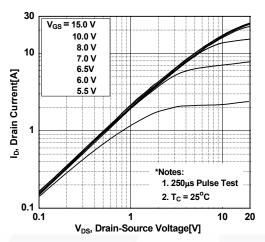


Figure 3. On-Resistance Variation vs.

Drain Current and Gate Voltage

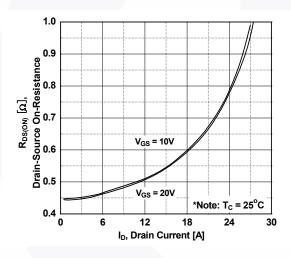


Figure 5. Capacitance Characteristics

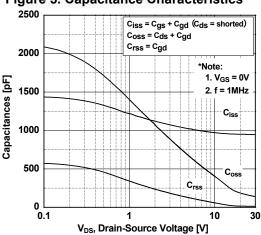


Figure 2. Transfer Characteristics

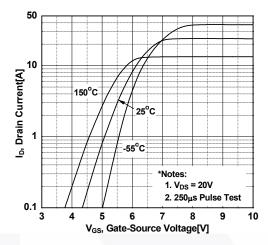


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

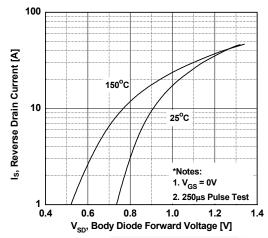
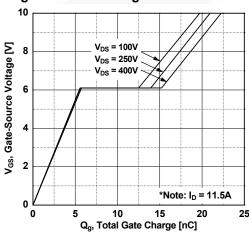


Figure 6. Gate Charge Characteristics



Typical Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

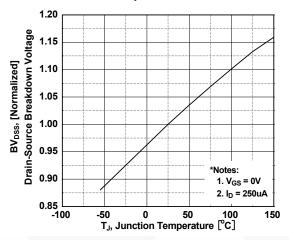


Figure 8. On-Resistance Variation vs. Temperature

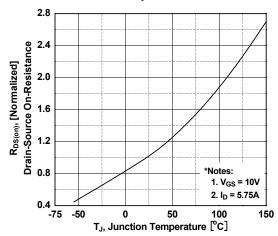


Figure 9. Maximum Safe Operating Area - FDPF12N50NZ

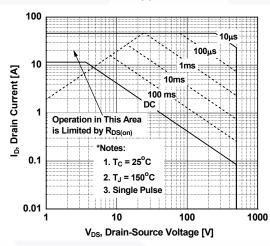


Figure 10.Maximum Safe Operating Area - FDP12N50NZ

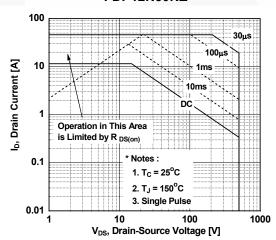
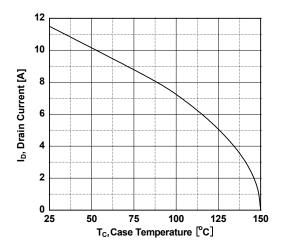


Figure 11. Maximum Drain Current vs. Case Temperature



Typical Characteristics (Continued)

Figure 12. Transient Thermal Response Curve - FDP12N50NZ

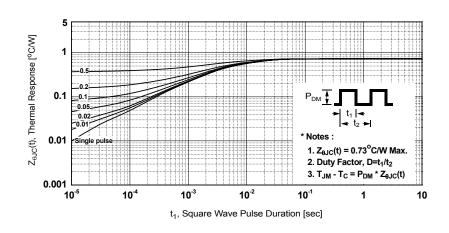


Figure 13. Transient Thermal Response Curve - FDPF12N50NZ

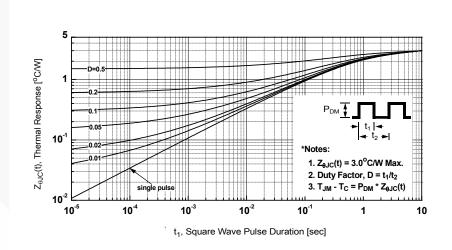


Figure 14. Gate Charge Test Circuit & Waveform

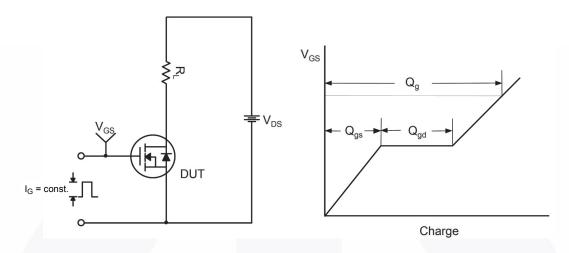


Figure 15. Resistive Switching Test Circuit & Waveforms

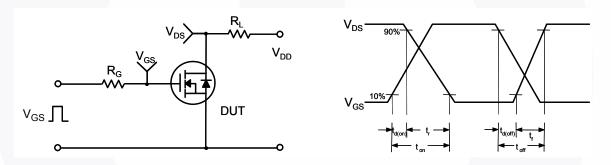
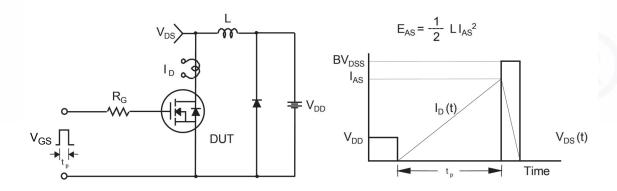


Figure 16. Unclamped Inductive Switching Test Circuit & Waveforms



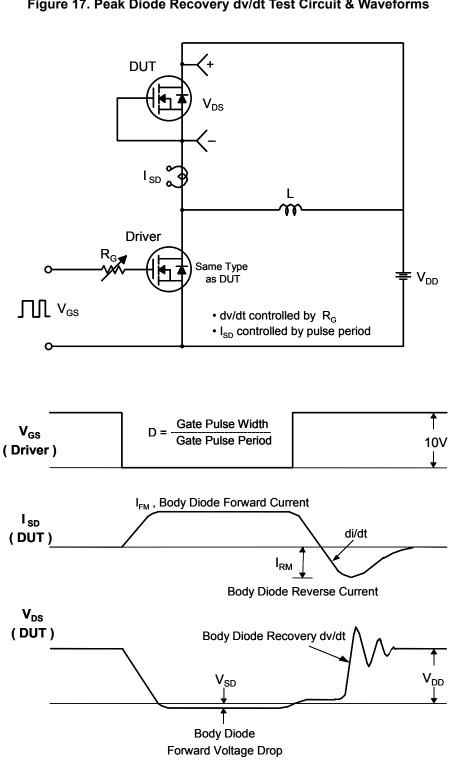
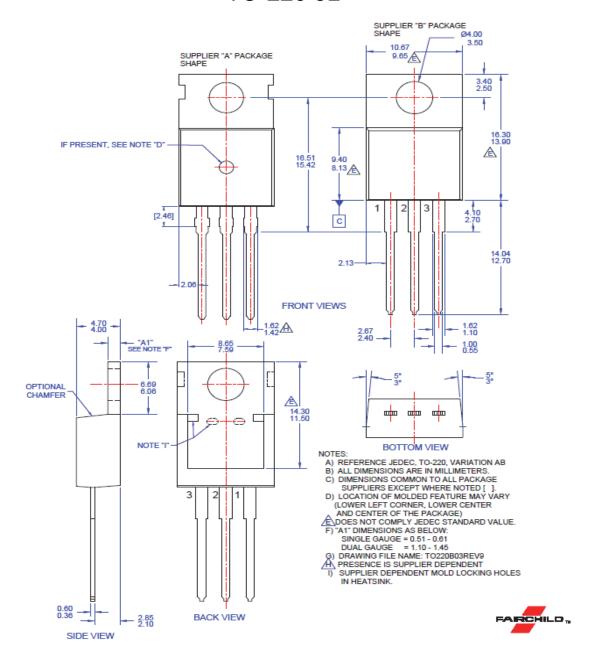
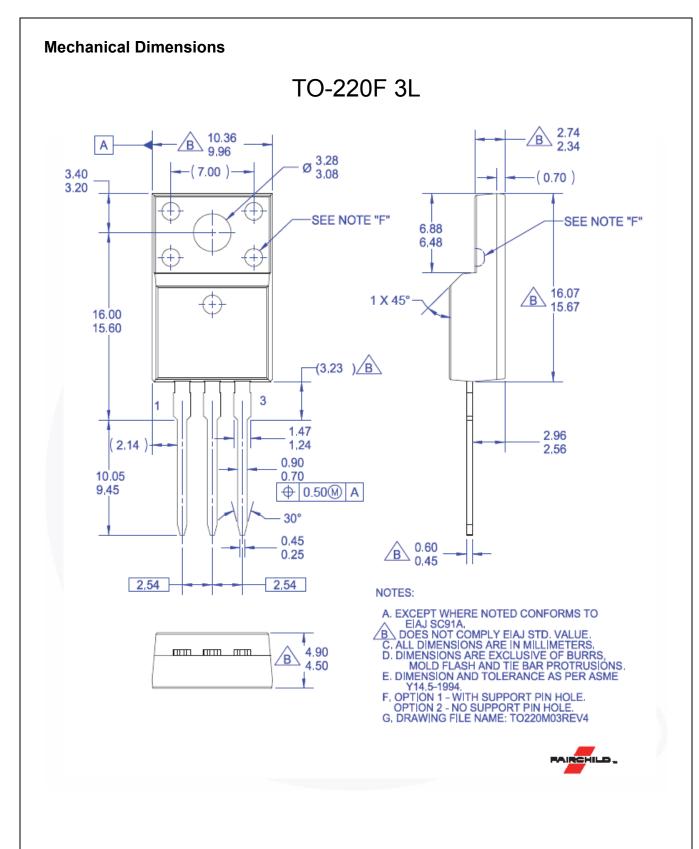


Figure 17. Peak Diode Recovery dv/dt Test Circuit & Waveforms

Mechanical Dimensions

TO-220 3L









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