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FDMD8630

Dual N-Channel PowerTrench® MOSFET 30 V, 167 A, 1.0 m Ω

Features

- Common Source Configuration to Eliminate PCB Routing
- Large Source Pad on Bottom of Package for Enhanced Thermals
- Max $r_{DS(on)}$ = 1.0 m Ω at V_{GS} = 10 V, I_D = 38 A
- Max $r_{DS(on)}$ = 1.3 m Ω at V_{GS} = 4.5 V, I_D = 33 A
- Ideal for Flexible Layout in Secondary Side Synchronous Rectification
- 100% UIL Tested
- Termination is Lead-free and RoHS Compliant

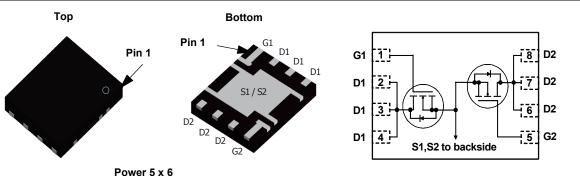


General Description

This package integrates two N-Channel devices connected internally in common-source configuration. This enables very low package parasitics and optimized thermal path to the common source pad on the bottom. Provides a very small footprint (5×6 mm) for higher power density.

Applications

- Isolated DC-DC Synchronous Rectifiers
- Common Ground Load Switches



MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted.

Symbol	Parame	eter		Ratings	Units
V _{DS}	Drain to Source Voltage			30	V
V _{GS}	Gate to Source Voltage			±20	V
	Drain Current -Continuous	T _C = 25 °C	(Note 5)	167	
	-Continuous	T _C = 100 °C	(Note 5)	106	^
ID	Drain Current -Continuous	T _A = 25 °C	(Note 1a)	38	Α
	-Pulsed		(Note 4)	1178	
E _{AS}	Single Pulse Avalanche Energy		(Note 3)	726	mJ
P_{D}	Power Dissipation $T_C = 25 ^{\circ}C$			43	W
	Power Dissipation	ower Dissipation $T_A = 25 ^{\circ}\text{C}$ (Note 1a)		2.3	VV
T _J , T _{STG}	Operating and Storage Junction Tempera	ture Range		-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	2.9	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	55	C/VV

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMD8630	FDMD8630	Power 5 x 6	13 "	12 mm	3000 units

Electrical Characteristics T_J = 25 °C unless otherwise noted.

Symbol	Parameter	Test Conditions		Тур.	Max.	Units
Off Chara	cteristics					
BV_{DSS}	Drain to Source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0 V	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_{J}}$	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, referenced to 25 °C		15		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 24 V, V _{GS} = 0 V			1	μΑ
I _{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$			±100	nA

On Characteristics

V _{GS(th)}	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = 250 \mu A$	1.0	1.6	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I _D = 250 μA, referenced to 25 °C		-6		mV/°C
r _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = 10 V, I _D = 38 A		0.6	1.0	
		$V_{GS} = 4.5 \text{ V}, I_D = 33 \text{ A}$		0.8	1.3	mΩ
		$V_{GS} = 10 \text{ V}, I_D = 38 \text{ A}, T_J = 125 ^{\circ}\text{C}$		0.9	1.5	
9 _{FS}	Forward Transconductance	V _{DD} = 5 V, I _D = 38 A		281		S

Dynamic Characteristics

C _{iss}	Input Capacitance	V _{DS} = 15 V, V _{GS} = 0 V f = 1 MHz		7090	9930	pF
C _{oss}	Output Capacitance			2025	2835	pF
C _{rss}	Reverse Transfer Capacitance			212	300	pF
R_g	Gate Resistance		0.1	1.9	3.8	Ω

Switching Characteristics

t _{d(on)}	Turn-On Delay Time		14	26	ns
t _r	Rise Time	V _{DD} = 15 V, I _D = 38 A	15	27	ns
t _{d(off)}	Turn-Off Delay Time	$V_{GS} = 10 \text{ V}, R_{GEN} = 6 \Omega$	66	105	ns
t _f	Fall Time		24	39	ns
$Q_{g(TOT)}$	Total Gate Charge	V _{GS} = 0 V to 10 V	97	142	nC
$Q_{g(TOT)}$	Total Gate Charge	V _{GS} = 0 V to 4.5 V V _{DD} = 15 V	46	74	nC
Q _{gs}	Gate to Source Charge	I _D = 38 A	17		nC
Q_{gd}	Gate to Drain "Miller" Charge		12		nC

Drain-Source Diode Characteristics

V_{SD}	Source to Drain Diode Forward Voltage	V _{GS} = 0 V, I _S = 38 A (Note 2)	0.8	1.3	V
V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0 V, I_S = 2 A$ (Note 2)	0.7	1.2	V
t _{rr}	Reverse Recovery Time	I _E = 38 A, di/dt = 100 A/μs	64	103	ns
Q _{rr}	Reverse Recovery Charge	ης – 30 A, αιναι – 100 A/μs	56	90	nC

NOTES

^{1.} R_{0JA} is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. R_{0JC} is guaranteed by design while R_{0CA} is determined by the user's board design.



a. 55 °C/W when mounted on a 1 in² pad of 2 oz copper



b.125 °C/W when mounted on a minimum pad of 2 oz copper

- 2. Pulse Test: Pulse Width < 300 $\mu s,$ Duty cycle < 2.0 %.
- 3. E_{AS} of 726 mJ is based on starting T_J = 25 °C, L = 3 mH, I_{AS} = 22 A, V_{DD} = 30 V, V_{GS} = 10 V. 100% tested at L = 0.1 mH, I_{AS} = 70 A
- 4. Pulsed Id please refer to Fig 11 SOA graph for more details.
- 5. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

Typical Characteristics $T_J = 25$ °C unless otherwise noted.

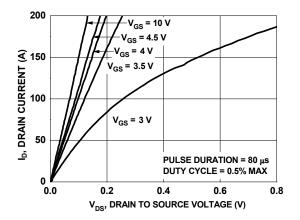


Figure 1. On-Region Characteristics

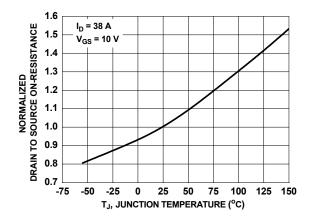


Figure 3. Normalized On Resistance vs. Junction Temperature

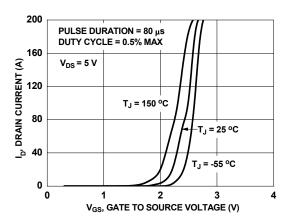


Figure 5. Transfer Characteristics

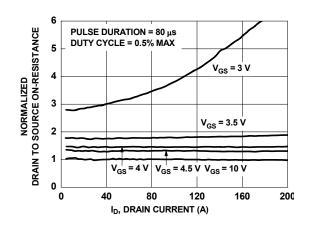


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

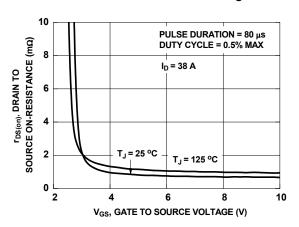


Figure 4. On Resistance vs. Gate to Source Voltage

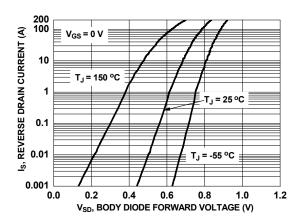


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

Typical Characteristics $T_J = 25$ °C unless otherwise noted.

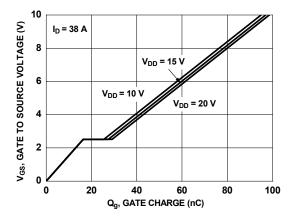


Figure 7. Gate Charge Characteristics

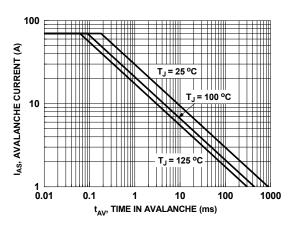


Figure 9. Unclamped Inductive Switching Capability

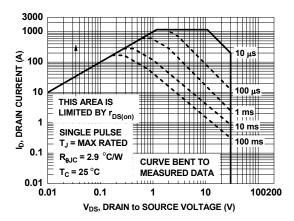


Figure 11. Forward Bias Safe Operating Area

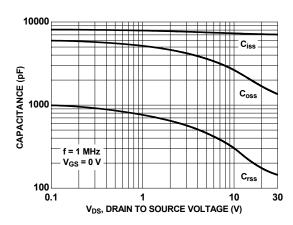


Figure 8. Capacitance vs. Drain to Source Voltage

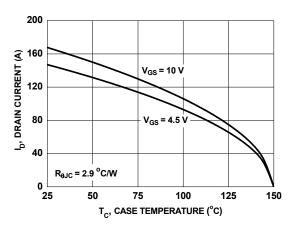


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

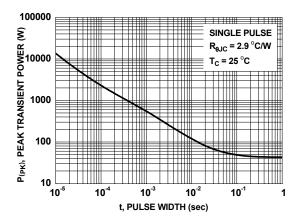


Figure 12. Single Pulse Maximum Power Dissipation



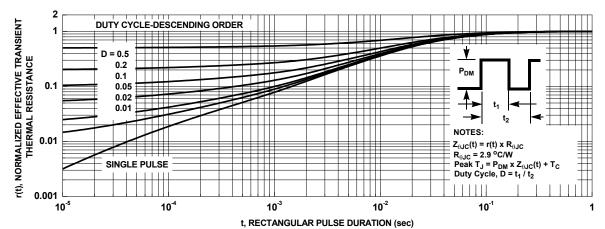
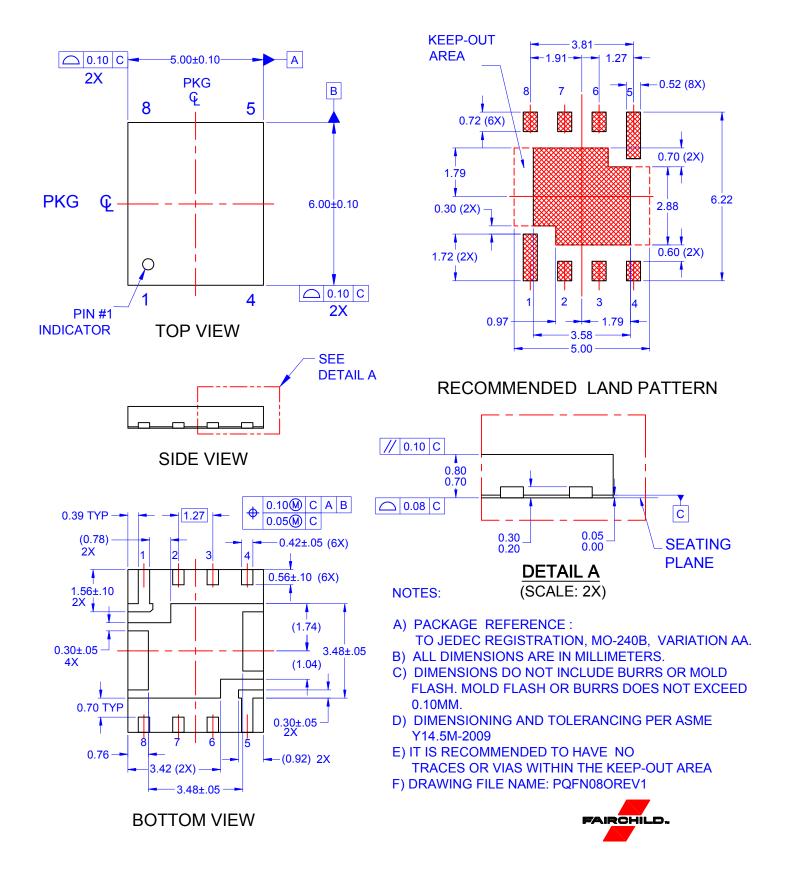


Figure 13. Junction-to-Case Transient Thermal Response Curve



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