

32-Channel Serial to Parallel Converter With Open Drain Outputs

Features

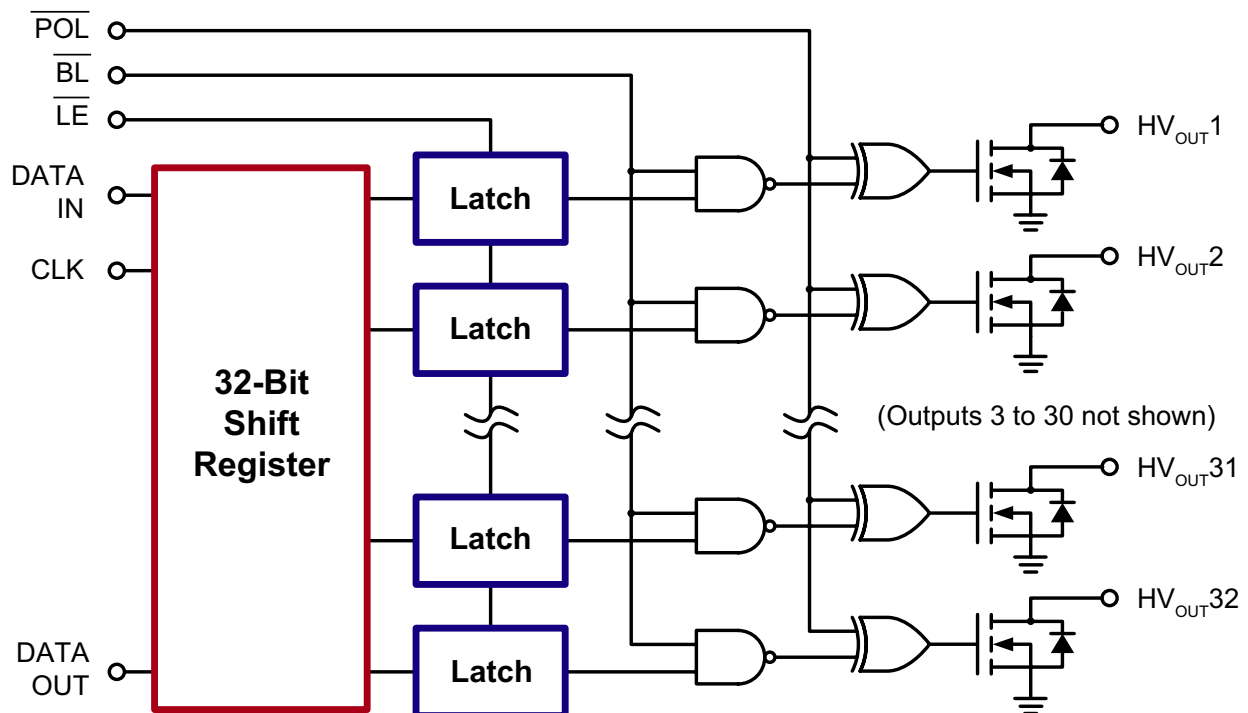
- ▶ Processed with HVCMOS® technology
- ▶ Sink current minimum 100mA
- ▶ Shift register speed 8.0MHz
- ▶ Polarity and Blanking inputs
- ▶ CMOS compatible inputs
- ▶ Forward and reverse shifting options
- ▶ Diode to VPP allows efficient power recovery

General Description

The HV5522 is a low-voltage serial to high-voltage parallel converter with open drain outputs. This device has been designed for use as a driver for AC-electroluminescent displays. It can also be used in any application requiring multiple output high voltage current sinking capabilities such as driving inkjet and electrostatic print heads, plasma panels, vacuum fluorescent, or large matrix LCD displays.

This device consists of a 32-bit shift register, 32 latches, and control logic to perform the polarity select and blanking of the outputs. Data is shifted through the shift register on the high to low transition of the clock. The HV5522 shifts in the counter clockwise direction when viewed from the top of the package. A data output buffer is provided for cascading devices. This output reflects the current status of the last bit of the shift register. Operation of the shift register is not affected by the \overline{LE} (latch enable), \overline{BL} (blanking), or the \overline{POL} (polarity) inputs. Transfer of data from the shift register to the latch occurs when the \overline{LE} (latch enable) input is high. The data in the latch is stored when \overline{LE} is low.

Functional Block Diagram



Ordering Information

| Device | Package Options | |
|--------|--|--|
| | 44-Lead Quad Plastic Gullwing 10.00x10.00mm body 2.45mm height (max) 0.80mm pitch | 44-Lead Quad Plastic Chip Carrier .653x.653in body .180in height (max) .050in pitch |
| HV5522 | HV5522PG-G | HV5522PJ-G |

-G indicates package is RoHS compliant ('Green')



Absolute Maximum Ratings

| Parameter | |
|---|--------------------------|
| Supply voltage, V_{DD}^1 | -0.5V to +15V |
| Output voltage, V_{PP}^1 | -0.5V to +230V |
| Logic input levels ¹ | -0.5V to $V_{DD} + 0.5V$ |
| Ground current ² | 1.5A |
| Continuous total power dissipation ³ | 1200mW |
| Operating temperature range | -40°C to +85°C |
| Storage temperature range | -65°C to +150°C |

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Notes:

- All voltages are referenced to V_{SS}
- Duty cycle is limited by the total power dissipated in the package
- For operation above 25°C ambient derate linearly to maximum operating temperature at 20mW/°C.

Recommended Operating Conditions

| Sym | Parameter | Min | Max | Units |
|------------|--------------------------------|----------------|----------|-------|
| V_{DD} | Logic voltage supply | 10.8 | 13.2 | V |
| HV_{OUT} | High voltage output | -0.3 | +220 | V |
| V_{IH} | Input high voltage | $V_{DD} - 2.0$ | V_{DD} | V |
| V_{IL} | Input low voltage | 0 | 2.0 | V |
| f_{CLK} | Clock frequency | - | 8.0 | MHz |
| T_A | Operating free-air temperature | -40 | +85 | °C |

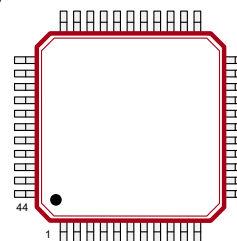
Power-Up Sequence

Power-up sequence should be the following:

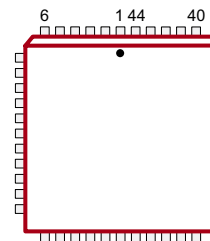
- Connect ground
- Apply V_{DD}
- Set all inputs to a known state

Power-down sequence should be the reverse of the above.

Pin Configurations



44-Lead PQFP (PG)
(top view)



44-Lead PLCC (PJ)
(top view)

Product Marking

Top Marking



YY = Year Sealed
WW = Week Sealed
L = Lot Number
C = Country of Origin*
A = Assembler ID*

Bottom Marking

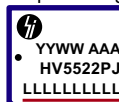


____ = "Green" Packaging
*May be part of top marking

Package may or may not include the following marks: Si or

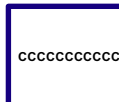
44-Lead PQFP (PG)

Top Marking



YY = Year Sealed
WW = Week Sealed
L = Lot Number
A = Assembler ID
C = Country of Origin*

Bottom Marking



____ = "Green" Packaging
*May be part of top marking

Package may or may not include the following marks: Si or

44-Lead PLCC (PJ)

Electrical Characteristics (over recommended operating conditions unless otherwise noted)

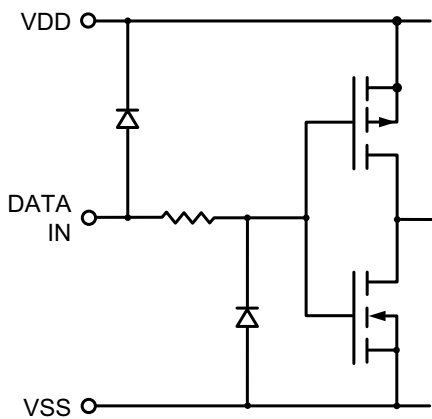
DC Characteristics

| Sym | Parameter | Min | Max | Units | Conditions | |
|--------------|-------------------------------------|------------------------|------|---------------|--|------------------------------|
| I_{DD} | V_{DD} supply current | - | 15 | mA | $f_{CLK} = 8.0\text{MHz}$, $F_{DATA} = 4.0\text{MHz}$ | |
| I_{DDQ} | V_{DD} supply current (quiescent) | - | 100 | μA | $V_{IN} = 0\text{V}$ | |
| $I_{O(OFF)}$ | Off state output current | - | 10 | μA | All outputs high, all SWS parallel | |
| I_{IH} | High-level logic input current | - | 1.0 | μA | $V_{IH} = V_{DD}$ | |
| I_{IL} | Low-level logic input current | - | -1.0 | μA | $V_{IL} = 0\text{V}$ | |
| V_{OH} | High-level output data out | $V_{DD} - 1.0\text{V}$ | - | V | $I_{DOUT} = -100\mu\text{A}$ | |
| V_{OL} | Low-level output voltage | HV _{OUT} | - | 15 | V | $I_{HVOUT} = +100\text{mA}$ |
| | | Data out | - | 1.0 | V | $I_{DOUT} = +100\mu\text{A}$ |
| V_{OC} | HV _{OUT} clamp voltage | - | -1.5 | V | $I_{OL} = -100\text{mA}$ | |

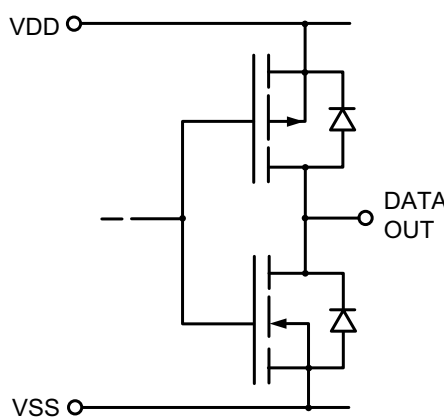
AC Characteristics ($V_{DD} = 12\text{V}$, $T_c = 25^\circ\text{C}$)

| Sym | Parameter | Min | Max | Units | Conditions |
|-----------|--|-----|-----|-------|--|
| f_{CLK} | Clock frequency | - | 8.0 | MHz | --- |
| t_w | Clock width, high or low | 62 | - | ns | --- |
| t_{SU} | Data set-up time before CLK falls | 25 | - | ns | --- |
| t_H | Data hold time after CLK falls | 10 | - | ns | --- |
| t_{ON} | Turn-on time, HV _{OUT} from enable | - | 500 | ns | $R_L = 2.0\text{K}\Omega$ to V_{pp} max. |
| t_{DHL} | Delay time clock to data high to low | - | 100 | ns | $C_L = 15\text{pF}$ |
| t_{DLH} | Delay time clock to data low to high | - | 100 | ns | $C_L = 15\text{pF}$ |
| t_{DLE} | Delay time clock to $\overline{\text{LE}}$ low to high | 50 | - | ns | --- |
| t_{WLE} | Width of $\overline{\text{LE}}$ pulse | 50 | - | ns | --- |
| t_{SLE} | $\overline{\text{LE}}$ setup time before clock falls | 50 | - | ns | --- |

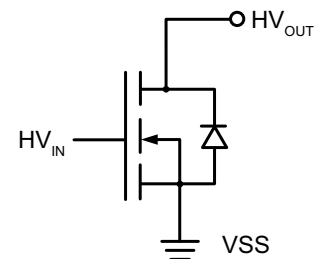
Input and Output Equivalent Circuits



Logic Inputs



Logic Data Output



High Voltage Outputs

Switching Waveforms



Functional Table

| Function | Inputs | | | | | Outputs | | | | |
|------------------------|--------|--------|-----------------|-----------------|------------------|-----------|--------|----------------|--------------------|------------|
| | Data | CLK | \overline{LE} | \overline{BL} | \overline{POL} | Shift Reg | | HV Outputs | | Data Out * |
| | | | | | | 1 | 2...32 | 1 | 2...32 | * |
| All on | X | X | X | L | L | * | *...* | On | On...On | * |
| All off | X | X | X | L | H | * | *...* | Off | Off...Off | * |
| Invert mode | X | X | L | H | L | * | *...* | $\overline{*}$ | $\overline{*...*}$ | * |
| Load S/R | H or L | ↓ | L | H | H | H or L | *...* | * | *...* | * |
| Load latches | X | H or L | ↑ | H | H | * | *...* | * | *...* | * |
| | X | H or L | ↑ | H | L | * | *...* | $\overline{*}$ | $\overline{*...*}$ | * |
| Transparent latch mode | L | ↓ | H | H | H | L | *...* | Off | *...* | * |
| | H | ↓ | H | H | H | H | *...* | On | *...* | * |

Notes:

H = high level, L = low level, X = irrelevant, ↓ = high-to-low transition, ↑ = low-to-high transition.

* dependent on previous stage's state before the last CLK ↓ or last \overline{LE} high.

44-Lead PQFP Pin Assignment (PG)

| Pin # | Function | Description |
|-------|-------------------------|--|
| 1 | HV _{OUT} 11 | High voltage outputs. |
| 2 | HV _{OUT} 12 | |
| 3 | HV _{OUT} 13 | |
| 4 | HV _{OUT} 14 | |
| 5 | HV _{OUT} 15 | |
| 6 | HV _{OUT} 16 | |
| 7 | HV _{OUT} 17 | |
| 8 | HV _{OUT} 18 | |
| 9 | HV _{OUT} 19 | |
| 10 | HV _{OUT} 20 | |
| 11 | HV _{OUT} 21 | |
| 12 | HV _{OUT} 22 | |
| 13 | HV _{OUT} 23 | |
| 14 | HV _{OUT} 24 | |
| 15 | HV _{OUT} 25 | |
| 16 | HV _{OUT} 26 | |
| 17 | HV _{OUT} 27 | |
| 18 | HV _{OUT} 28 | |
| 19 | HV _{OUT} 29 | |
| 20 | HV _{OUT} 30 | |
| 21 | HV _{OUT} 31 | |
| 22 | HV _{OUT} 32 | |
| 23 | DATA OUT | Data output pin. |
| 24 | N/C | No internal connection. |
| 25 | N/C | |
| 26 | N/C | |
| 27 | $\overline{\text{POL}}$ | Inverts the polarity of the HV _{OUT} pins |
| 28 | CLK | Clock pin, shift registers shifts data on falling edge of input clock. |
| 29 | VSS | Reference voltage, usually ground. |
| 30 | VDD | Logic supply voltage. |
| 31 | $\overline{\text{LE}}$ | Latch enable pin, data is shifted from shift register to latches on logic input high. |
| 32 | DATA IN | Data input pin. |
| 33 | $\overline{\text{BL}}$ | Blanking pin sets all HV _{OUT} pins low or high depending upon state of polarity. See function table. |
| 34 | N/C | No internal connection. |
| 35 | HV _{OUT} 1 | High voltage outputs. |
| 36 | HV _{OUT} 2 | |
| 37 | HV _{OUT} 3 | |
| 38 | HV _{OUT} 4 | |
| 39 | HV _{OUT} 5 | |
| 40 | HV _{OUT} 6 | |
| 41 | HV _{OUT} 7 | |
| 42 | HV _{OUT} 8 | |
| 43 | HV _{OUT} 9 | |
| 44 | HV _{OUT} 10 | |

44-Lead PLCC Pin Assignment (PJ)

| Pin # | Function | Description |
|-------|-------------------------|--|
| 1 | HV _{OUT} 16 | High voltage outputs. |
| 2 | HV _{OUT} 17 | |
| 3 | HV _{OUT} 18 | |
| 4 | HV _{OUT} 19 | |
| 5 | HV _{OUT} 20 | |
| 6 | HV _{OUT} 21 | |
| 7 | HV _{OUT} 22 | |
| 8 | HV _{OUT} 23 | |
| 9 | HV _{OUT} 24 | |
| 10 | HV _{OUT} 25 | |
| 11 | HV _{OUT} 26 | |
| 12 | HV _{OUT} 27 | |
| 13 | HV _{OUT} 28 | |
| 14 | HV _{OUT} 29 | |
| 15 | HV _{OUT} 30 | |
| 16 | HV _{OUT} 31 | |
| 17 | HV _{OUT} 32 | |
| 18 | DATA OUT | Data output pin. |
| 19 | N/C | No internal connection. |
| 20 | N/C | |
| 21 | N/C | |
| 22 | $\overline{\text{POL}}$ | Inverts the polarity of the HV _{OUT} pins |
| 23 | CLK | Clock pin, shift registers shifts data on falling edge of input clock. |
| 24 | VSS | Reference voltage, usually ground. |
| 25 | VDD | Logic supply voltage. |
| 26 | $\overline{\text{LE}}$ | Latch enable pin, data is shifted from shift register to latches on logic input high. |
| 27 | DATA IN | Data input pin. |
| 28 | $\overline{\text{BL}}$ | Blanking pin sets all HV _{OUT} pins low or high depending upon state of polarity. See function table. |
| 29 | N/C | No internal connection. |
| 30 | HV _{OUT} 1 | High voltage outputs. |
| 31 | HV _{OUT} 2 | |
| 32 | HV _{OUT} 3 | |
| 33 | HV _{OUT} 4 | |
| 34 | HV _{OUT} 5 | |
| 35 | HV _{OUT} 6 | |
| 36 | HV _{OUT} 7 | |
| 37 | HV _{OUT} 8 | |
| 38 | HV _{OUT} 9 | |
| 39 | HV _{OUT} 10 | |
| 40 | HV _{OUT} 11 | |
| 41 | HV _{OUT} 12 | |
| 42 | HV _{OUT} 13 | |
| 43 | HV _{OUT} 14 | |
| 44 | HV _{OUT} 15 | |

44-Lead PQFP Package Outline (PG)

10.00x10.00mm body, 2.35mm height (max), 0.80mm pitch



Note:
 1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.

| Symbol | A | A1 | A2 | b | D | D1 | E | E1 | e | L | L1 | L2 | θ | |
|----------------|-----|-------|------|------|------|--------|--------|--------|--------|----------|----------|----------|------|------|
| Dimension (mm) | MIN | 1.95* | 0.00 | 1.95 | 0.30 | 13.65* | 9.80* | 13.65* | 9.80* | 0.80 BSC | 1.95 REF | 0.25 BSC | 0° | |
| | NOM | - | - | 2.00 | - | 13.90 | 10.00 | 13.90 | 10.00 | | | | 0.73 | 3.5° |
| | MAX | 2.35 | 0.25 | 2.10 | 0.45 | 14.15* | 10.20* | 14.15* | 10.20* | | | | 0.88 | 7° |

JEDEC Registration MO-112, Variation AA-2, Issue B, Sep. 1995.

* This dimension is not specified in the JEDEC drawing.

Drawings not to scale.

Supertex Doc. #: DSPD-44PQFP, Version C041309.

44-Lead PLCC Package Outline (PJ)

.653x.653in body, .180in height (max), .050in pitch



Notes:

1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.
2. Actual shape of this feature may vary.

| Symbol | A | A1 | A2 | b | b1 | D | D1 | E | E1 | e | R | |
|--------------------|-----|------|------|------|------|-------|------|------|------|------|----------|------|
| Dimension (inches) | MIN | .165 | .090 | .062 | .013 | .026 | .685 | .650 | .685 | .650 | .050 BSC | .025 |
| | NOM | .172 | .105 | - | - | - | .690 | .653 | .690 | .653 | | .035 |
| | MAX | .180 | .120 | .083 | .021 | .036† | .695 | .656 | .695 | .656 | | .045 |

JEDEC Registration MS-018, Variation AC, Issue A, June, 1993.

† This dimension differs from the JEDEC drawing.

Drawings not to scale.

Supertex Doc. #: DSPD-44PLCCPJ, Version F031111.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

Supertex inc. does not recommend the use of its products in life support applications, and will not knowingly sell them for use in such applications unless it receives an adequate "product liability indemnification insurance agreement." Supertex inc. does not assume responsibility for use of devices described, and limits its liability to the replacement of the devices determined defective due to workmanship. No responsibility is assumed for possible omissions and inaccuracies. Circuitry and specifications are subject to change without notice. For the latest product specifications refer to the Supertex inc. (website: <http://www.supertex.com>)

Данный компонент на территории Российской Федерации

Вы можете приобрести в компании MosChip.

Для оперативного оформления запроса Вам необходимо перейти по данной ссылке:

<http://moschip.ru/get-element>

Вы можете разместить у нас заказ для любого Вашего проекта, будь то серийное производство или разработка единичного прибора.

В нашем ассортименте представлены ведущие мировые производители активных и пассивных электронных компонентов.

Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

Офис по работе с юридическими лицами:

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:

moschip.ru

moschip.ru_4

moschip.ru_6

moschip.ru_9