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May 2014



FDMC5614P

P-Channel PowerTrench® MOSFET

-60V, -13.5A, 100mΩ

Features

- Max $r_{DS(on)}$ = 100m Ω at V_{GS} = -10V, I_D = -5.7A
- Max $r_{DS(on)}$ = 135m Ω at V_{GS} = -4.5V, I_D = -4.4A
- Low gate charge
- Fast switching speed
- High performance trench technology for extremely low r_{DS(on)}
- High power and current handling capability
- RoHS Compliant

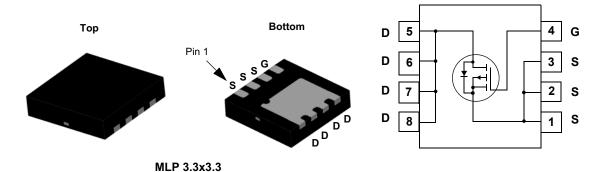


General Description

This P-Channel MOSFET is a rugged gate version of Fairchild Semiconductor's advanced PowerTrench® process. It has been optimized for power management applications requiring a wide range of gate drive voltage ratings (4.5V-20V).

Application

- Power management
- Load switch
- Battery protection



$\textbf{MOSFET Maximum Ratings} \ \, \text{T_A = 25°C unless otherwise noted}$

Symbol	Parameter			Ratings	Units	
V_{DS}	Drain to Source Voltage			-60	V	
V _{GS}	Gate to Source Voltage			±20	V	
	Drain Current -Continuous (Package limited)	T _C = 25°C		-13.5		
	-Continuous (Silicon limited)	T _C = 25°C		-14	^	
ID	-Continuous	T _A = 25°C	(Note 1a)	-5.7	_ A	
	-Pulsed			-23		
D	Power Dissipation	T _C = 25°C		42	١٨/	
P_{D}	Power Dissipation	T _A = 25°C	(Note 1a)	2.1	W	
T _J , T _{STG}	Operating and Storage Junction Temperature Ra	nge		-55 to +150	°C	

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	3.0	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	60	C/VV

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
5614P	FDMC5614P	Power 33	7"	8mm	3000 units

Electrical Characteristics $T_J = 25^{\circ}C$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Chara	octeristics					
BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = -250 \mu A, V_{GS} = 0 V$	-60			V
$\frac{\Delta BV_{DSS}}{\Delta T_{J}}$	Breakdown Voltage Temperature Coefficient	I_D = -250 μ A, referenced to 25°C		-54		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = -48V, V _{GS} = 0V			-1	μΑ
I _{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20V, V_{DS} = 0V$			±100	nA

On Characteristics

V _{GS(th)}	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = -250 \mu A$	-1	-1.95	-3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = -250 μ A, referenced to 25°C		4.7		mV/°C
		$V_{GS} = -10V, I_D = -5.7A$		84	100	
r _{DS(on)}	Static Drain to Source On Resistance	$V_{GS} = -4.5V, I_D = -4.4A$		108	135	mΩ
, ,		$V_{GS} = -10V$, $I_D = -5.7A$, $T_J = 125$ °C		140	168	
g _{FS}	Forward Transconductance	$V_{DS} = -15V, I_{D} = -5.7A$		11		S

Dynamic Characteristics

C _{iss}	Input Capacitance	V _{DS} = -30V, V _{GS} = 0V, f = 1MHz	795	1055	pF
C _{oss}	Output Capacitance		140	185	pF
C _{rss}	Reverse Transfer Capacitance	1 - 11/11/2	60	90	pF

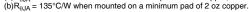
Switching Characteristics

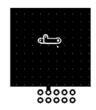
t _{d(on)}	Turn-On Delay Time		10	21	ns
t _r	Rise Time	V_{DD} = -30V, I_{D} = -1A V_{GS} = -10V, R_{GEN} = 6Ω	11	23	ns
$t_{d(off)}$	Turn-Off Delay Time	VGS = -10V, NGEN = 052	32	65	ns
t_f	Fall Time	1	11	22	ns
$Q_{g(TOT)}$	Total Gate Charge at 10V	V _{GS} = -10V	15	20	nC
Q_{gs}	Gate to Source Gate Charge	V _{DD} = -30V	1.6	2.1	nC
Q_{gd}	Gate to Drain "Miller" Charge	I _D = -5.7A	2.7	3.5	nC

Drain-Source Diode Characteristics

V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0V, I_S = -3.2A$	-0.8	-1.2	V
t _{rr}	Reverse Recovery Time	I _F = -3.2A, di/dt = 100A/μs		36	ns
Q _{rr}	Reverse Recovery Charge			29	nC

(a) $R_{0,lA}=60^{\circ}\text{C/W}$ when mounted on a 1 in² pad of 2 oz copper, 1.5'x1.5'x0.062' thick PCB. (b) $R_{0,lA}=135^{\circ}\text{C/W}$ when mounted on a minimum pad of 2 oz copper.





a. 60°C/W when mounted on a 1 in² pad of 2 oz copper



b.135°C/W when mounted on a minimum pad of 2 oz copper

2: Pulse Test: Pulse Width < 300μ s, Duty cycle < 2.0%.

Notes:

1: R_{0JA} is determined with the device mounted on a 1 in² oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. R_{0JC} is guaranteed by design while R_{0JA} is determined by the user's board design.

Typical Characteristics T_J = 25°C unless otherwise noted

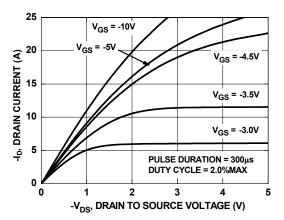


Figure 1. On-Region Characteristics

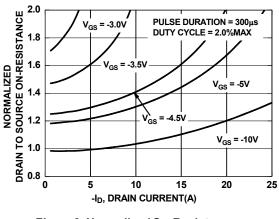


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

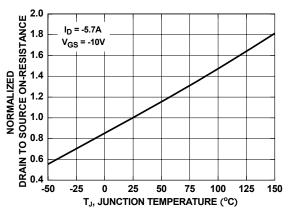


Figure 3. Normalized On-Resistance vs Junction Temperature

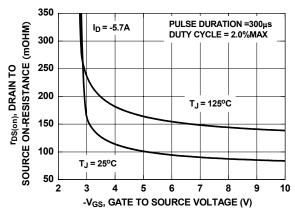


Figure 4. On-Resistance vs Gate to Source Voltage

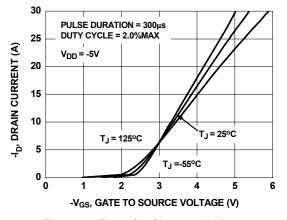


Figure 5. Transfer Characteristics

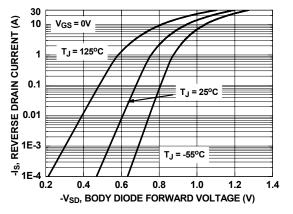


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics T_J = 25°C unless otherwise noted

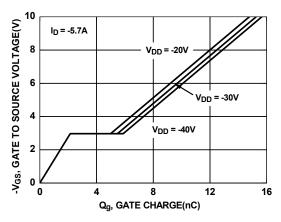


Figure 7. Gate Charge Characteristics

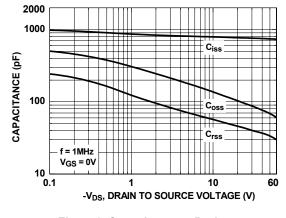


Figure 8. Capacitance vs Drain to Source Voltage

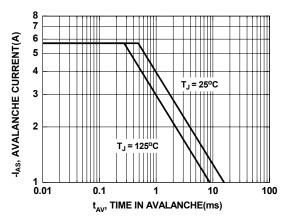


Figure 9. Unclamped Inductive Switching Capability

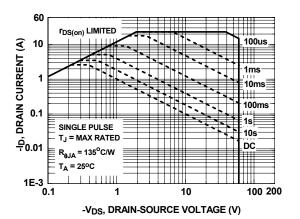
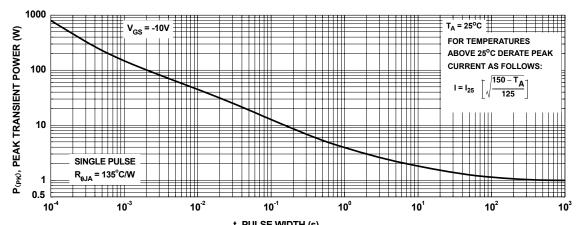


Figure 10. Forward Bias Safe Operating Area



t, PULSE WIDTH (s)
Figure 11. Single Pulse Maximum Power Dissipation

Typical Characteristics T_J = 25°C unless otherwise noted

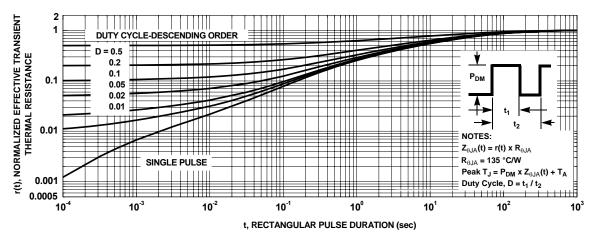
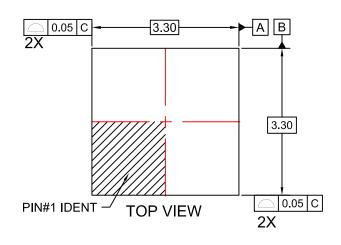
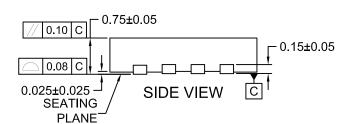
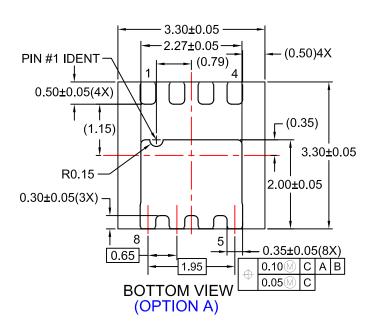
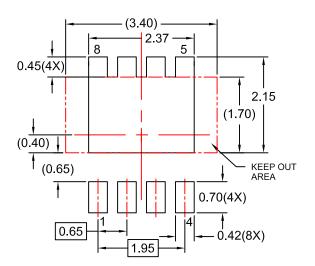


Figure 12. Transient Thermal Response Curve

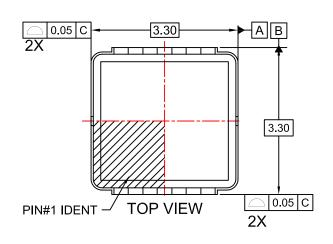


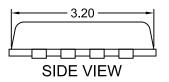


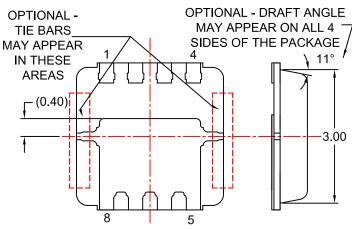






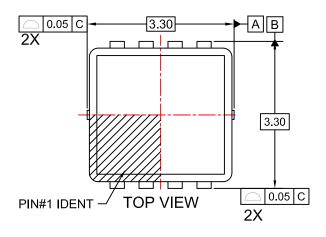


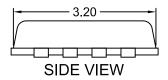


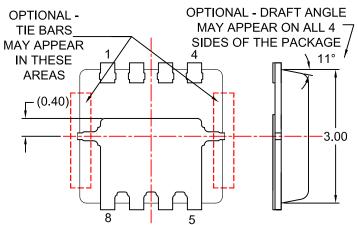


ALL DIMENSIONS AS PER OPTION A
UNLESS SPECIFIED
BOTTOM VIEW
(OPTION B)









ALL DIMENSIONS AS PER OPTION A
UNLESS SPECIFIED
BOTTOM VIEW
(OPTION C)

NOTES:

- A. PACKAGE DOES NOT FULLY CONFORM TO JEDEC REGISTRATION MO-240.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN
- E. DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. BURRS OR MOLD FLASH SHALL NOT EXCEED 0.10MM.
- F. DRAWING FILENAME: MKT-MLP08Wrev3.
- G. OPTION A SAWN MLP, OPTIONS B & C PUNCH MLP.



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