

Le79R70

Ringing Subscriber Line Interface Circuit VE580 Series

APPLICATIONS

- Integrated Access Devices (IADs)
- Network Interface Units (NIUs)
- Cable Modems
- DSL Modems
- Set Top / House Side Boxes
- Intelligent PBX
- Pain Gain
- FXS Cards
- Voice over ISDN or T1/E1
- Smart Residential Gateways
- WLL, APON, FITL, NGN, and all other short-loop CPE/ Enterprise telephony applications

FEATURES

- Ideal for ISDN-TA and set top applications
- On-chip ringing with on-chip ring-trip detector
- Low Standby state power
- Battery operation:
 - VBAT1: -40 V to -67 V
 - VBAT2: -19 V to VBAT1
- On-chip battery switching and feed selection
- On-hook transmission
- Polarity reversal option
- Programmable constant-current feed
- Programmable open circuit voltage
- Programmable loop-detect threshold
- Current gain = 1000
- Two-wire impedance set by single component
- Ground-key detector
- Tip Open state for ground-start lines
- Internal VEE regulator (no external -5 V power supply required)
- Two on-chip relay drivers and snubber circuits
- Space-saving package options (8x8 QFN)

RELATED LITERATURE

- 080917 VE790 Series RSLIC Device Product Brief
- 080158 Le79R70/79/100/101 Ringing SLIC Devices Technical Overview
- 080255 Le71HE0040J Evaluation Board User's Guide
- 080753 Le58QL02/021/031 QLSLAC™ Data Sheet

ORDERING INFORMATION

| Device ¹ | Package Type ^{2, 3} | Packing ⁴ |
|---------------------|-------------------------------------------|----------------------|
| Le79R70DJC | 32-pin PLCC, No Pol. Rev. (Green package) | Tube |
| Le79R70-1DJC | 32-pin PLCC, Pol. Rev. (Green package) | Tube |
| Le79R70-1FQC | 32-pin QFN, Pol. Rev. (Green package) | Tray |

1. Zarlink reserves the right to fulfill all orders for this device with parts marked with the "Am" part number prefix until all inventory bearing this mark has been depleted. Note that parts marked with either the "Am" or the "Le" part number prefix are equivalent devices in terms of form, fit, and function—the prefix appearing on the topside mark is the only difference.
2. The green package meets RoHS Directive 2002/95/EC of the European Council to minimize the environmental impact of electrical equipment.
3. Due to size constraints, QFN devices are marked by omitting the "Le" prefix and the performance grade dash character. For example, Le79R70-1QC is marked 79R701QC.
4. For delivery using a tape and reel packing system, add a "T" suffix to the OPN (Ordering Part Number) when placing an order.

DESCRIPTION

The Le79R70 Ringing Subscriber Line Interface Circuit (RSLIC) device is a bipolar monolithic SLIC that offers on-chip ringing. Designers can achieve significant cost reductions at the system level for short-loop applications by integrating the ringing function on chip. Examples of such applications would be ISDN Terminal Adaptors and set top boxes. Using a CMOS-compatible input waveform and wave shaping R-C network, the Le79R70 Ringing SLIC device can provide trapezoidal wave ringing to meet various design requirements.

See the [Le79R70 Block Diagram, on page 3](#).

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PRODUCT DESCRIPTION

The Zarlink family of subscriber line interface circuit (SLIC) products provide the telephone interface functions required throughout the worldwide market. Zarlink SLIC devices address all major telephony markets including central office (CO), private branch exchange (PBX), digital loop carrier (DLC), fiber-in-the-loop (FITL), radio-in-the-loop (RITL), hybrid fiber coax (HFC), and video telephony applications.

The Zarlink SLIC devices offer support of BORSHT (battery feed, over voltage protection, ringing, supervision, hybrid, and test) functions with features including current limiting, on-hook transmission, polarity reversal, tip-open, and loop-current detection. These features allow reduction of line card cost by minimizing component count, conserving board space, and supporting automated manufacturing.

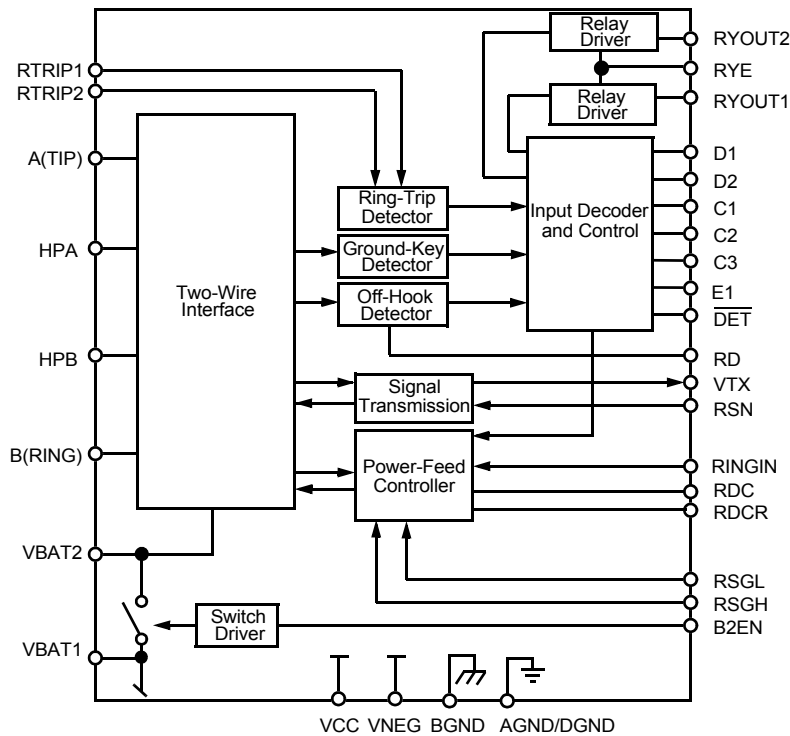
The Zarlink SLIC devices provide the two- to four-wire hybrid function, DC loop feed, and two-wire supervision. Two-wire termination is programmed by a scaled impedance network. Transhybrid balance can be achieved with an external balance circuit or simply programmed using a companion Zarlink codec/filter, such as the Le58QL0xx Quad SLAC (QLSLAC™) device.

The Le79R70 Ringing SLIC device is a bipolar monolithic SLIC that offers on-chip ringing. Now designers can achieve significant cost reductions at the system level for short-loop applications by integrating the ringing function on chip. Examples of such applications would be ISDN Terminal Adaptors and set top boxes. Using a CMOS-compatible input waveform and wave shaping R-C network, the Le79R70 Ringing SLIC can provide trapezoidal wave ringing to meet various design requirements.

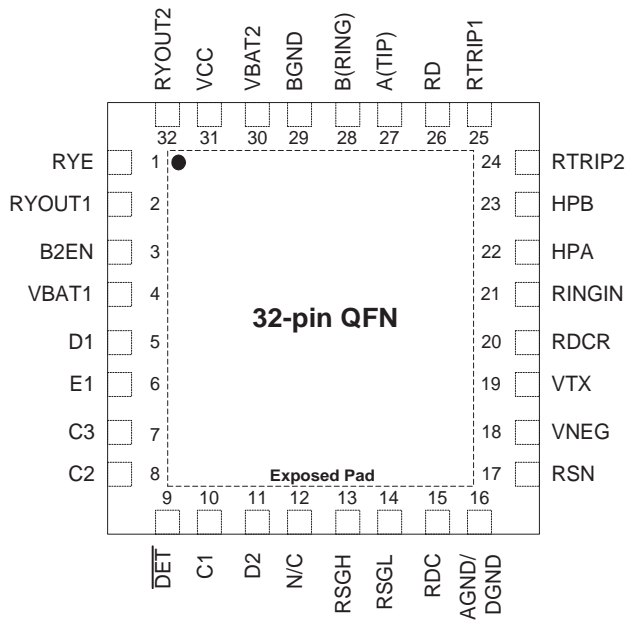
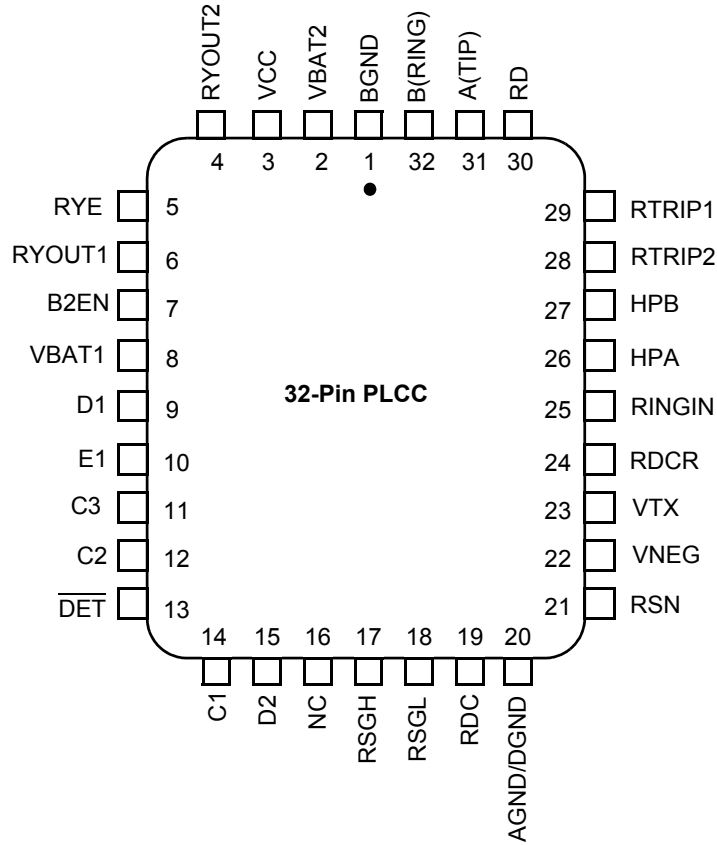
In order to further enhance the suitability of this device in short-loop, distributed switching applications, Zarlink has maximized power savings by incorporating battery switching on chip. The Le79R70 Ringing SLIC device switches between two battery supplies such that in the Off-hook (active) state, a low battery is used to save power. In order to meet the Open Circuit voltage requirements of fax machines and maintenance termination units (MTU), the SLIC automatically switches to a higher voltage in the On-hook (standby) state.

Like all of the Zarlink SLIC devices, the Le79R70 Ringing SLIC device supports on-hook transmission, ring-trip detection and programmable loop-detect threshold. The Le79R70 Ringing SLIC device is a programmable constant-current feed device with two on-chip relay drivers to operate external relays. This unique device is available in the proven Zarlink 75 V bipolar process.

Figure 1. Le79R70 Block Diagram



CONNECTION DIAGRAM



Notes:

1. Pin 1 is marked for orientation.
2. NC = No connect
3. RSVD = Reserved. Do not connect to this pin.
4. The thermally enhanced QFN package features an exposed pad on the underside which must be electrically tied to VBAT1.

Pin Descriptions

| Pin Names | Type | Description |
|-------------|-----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| AGND/DGND | Gnd | Analog and digital ground are connected internally to a single pin. |
| A(TIP) | Output | Output of A(TIP) power amplifier. |
| B2EN | Input | V _{BAT2} enable. Logic Low enables operation from V _{BAT2} . Logic High enables operation from V _{BAT1} . TTL compatible. |
| BGND | Gnd | Battery (power) ground |
| B(RING) | Output | Output of B(RING) power amplifier. |
| C3–C1 | Input | Decoder. TTL compatible. C3 is MSB and C1 is LSB. |
| D1 | Input | Relay1 control. TTL compatible. Logic Low activates the Relay1 relay driver. |
| D2 | Input | (Option) Relay2 control. TTL compatible. Logic Low activates the Relay2 relay driver. |
| DET | Output | Detector. Logic Low indicates that the selected detector is tripped. Logic inputs C3–C1 and E1 select the detector. Open-collector with a built-in 15 k Ω pull-up resistor. |
| E1 | Input | (Option) A logic High selects the off-hook detector. A logic Low selects the ground-key detector. TTL compatible. |
| HPA | Capacitor | High-pass filter capacitor. A(TIP) side of high-pass filter capacitor. |
| HPB | Capacitor | High-pass filter capacitor. B(RING) side of high-pass filter capacitor. |
| RD | Resistor | Detect resistor. Threshold modification and filter point for the off-hook detector. |
| RDC | Resistor | DC feed resistor. Connection point for the DC-feed current programming network, which also connects to the receiver summing node (RSN). V _{RDC} is negative for normal polarity and positive for reverse polarity. |
| RDCR | — | Connection point for feedback during ringing. |
| RINGIN | Input | Ring Signal Input. Pin for ring signal input. Square-wave shaped by external RC filter. Requires 50% duty cycle. CMOS-compatible input. |
| RSGH | Input | Saturation Guard High. Pin for resistor to adjust Open Circuit voltage when operating from V _{BAT1} . |
| RSGL | Input | Saturation Guard Low. Pin for resistor to adjust the anti-saturation cut-in voltage when operating from both V _{BAT1} and V _{BAT2} . |
| RSN | Input | The metallic current (AC and DC) between A(TIP) and B(RING) is equal to 1000 x the current into this pin. The networks that program receive gain, two-wire impedance, and feed resistance all connect to this node. |
| RTRIP1 | Input | Ring-trip detector. Ring-trip detector threshold set and filter pin. |
| RTRIP2 | Input | Ring-trip detector threshold offset (switch to V _{BAT1}). For power conservation in any non-ringing state, this switch is open. |
| RYE | Output | Common Emitter of RYOUT1/RYOUT2. Emitter output of RYOUT1 and RYOUT2. Normally connected to relay ground. |
| RYOUT1 | Output | Relay/switch driver. Open-collector driver with emitter internally connected to RYE. |
| RYOUT2 | Output | (Option) Relay/switch driver. Open-collector driver with emitter internally connected to RYE. |
| VBAT1 | Battery | Battery supply and connection to substrate. |
| VBAT2 | Battery | Power supply to output amplifiers. Connect to off-hook battery through a diode. |
| VCC | Power | Positive analog power supply. |
| VNEG | Power | Negative analog power supply. This pin is the return for the internal VEE regulator. |
| VTX | Output | Transmit Audio. This output is a 0.5066 gain version of the A(TIP) and B(RING) metallic AC voltage. VTX also sources the two-wire input impedance programming network. |
| Exposed Pad | Battery | This must be electrically tied to VBAT1. |

ABSOLUTE MAXIMUM RATINGS

Stresses above those listed under *Absolute Maximum Ratings* can cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

| | |
|-----------------------------------------------------------------|-----------------------------------|
| Storage temperature | -55 to +150°C |
| Ambient temperature under bias | 0 to +70°C |
| V _{CC} with respect to AGND/DGND | 0.4 to + 7 V |
| V _{NEG} with respect to AGND/DGND | 0.4 V to V _{BAT2} |
| V _{BAT2} | V _{BAT2} to GND |
| V _{BAT1} with respect to AGND/DGND: | |
| Continuous | +0.4 to -80 V |
| 10 ms | +0.4 to -85 V |
| BGND with respect to AGND/DGND | +3 to -3 V |
| A (TIP) or B (RING) to BGND: | |
| Continuous | V _{BAT1} - 5 V+ 1 V |
| 10 ms (F = 0.1 Hz) | V _{BAT1} - 10 V+ 5 V |
| 1 μs (F = 0.1 Hz) | V _{BAT1} - 15 V+ 8 V |
| 250 ns (F = 0.1 Hz) | V _{BAT1} - 20 V+ 12 V |
| Current from A (TIP) or B (RING) | ± 150 mA |
| RYOUT1, RYOUT2 current | 75 mA |
| RYOUT1, RYOUT2 voltage | RYE to +7 V |
| RYOUT1, RYOUT2 transient | RYE to +10 V |
| RYE voltage | BGND to V _{BAT1} |
| C3-C1, D2-D1, E1, B2EN and RINGIN: | |
| Input voltage | -0.4 V to V _{CC} + 0.4 V |
| Maximum continuous power dissipation, TA = 70° C ¹ : | |
| In 32-pin PLCC package | 1.67 W |
| In 32-pin QFN package | 3.00 W |
| Thermal Data: | θ _{JA} |
| In 32-pin PLCC package | 45° C/W |
| In 32-pin QFN package ² | 25° C/W |
| ESD Immunity (Human Body Model) | JESD22 Class 1C compliant |

Note:

1. Thermal limiting circuitry on the chip will shut down the circuit at a junction temperature of about 165°C. Continuous operation above 145°C junction temperature may degrade device reliability.
2. The thermal performance of a thermally enhanced package is assured through optimized printed circuit board layout. Specified performance requires that the exposed thermal pad be soldered to an equally sized exposed copper surface, which, in turn, conducts heat through multiple vias to a large internal copper plane.

Package Assembly

Green package devices are assembled with enhanced, environmental compatible lead-free, halogen-free, and antimony-free materials. The leads possess a matte-tin plating which is compatible with conventional board assembly processes or newer lead-free board assembly processes. The peak soldering temperature should not exceed 245°C during printed circuit board assembly.

Refer to IPC/JEDEC J-Std-020B Table 5-2 for the recommended solder reflow temperature profile.

OPERATING RANGES

Environmental Ranges

Zarlink guarantees the performance of this device over the commercial (0° C to 70° C) temperature range by conducting electrical characterization and by conducting a production test with single insertion coupled to periodic sampling. These characterization and test procedures comply with section 4.6.2 of Bellcore GR-357-CORE Component Reliability Assurance Requirements for Telecommunications Equipment.

Environmental Ranges

| | |
|---------------------|------------|
| Ambient Temperature | 0 to 70° C |
|---------------------|------------|

Electrical Ranges

| | |
|--------------------------------|-----------------------|
| V_{CC} | 4.75 V to 5.25 V |
| V_{NEG} | -4.75 V to V_{BAT2} |
| V_{BAT1} | -40 to -67 V |
| V_{BAT2} | -19 V to V_{BAT1} |
| AGND/DGND | 0 V |
| BGND with respect to AGND/DGND | -100 mV to +100 mV |
| Load resistance on VTX to GND | 20 k Ω min |

Note:

The Operating Ranges define those limits between which the functionality of the device is guaranteed.

ELECTRICAL CHARACTERISTICS

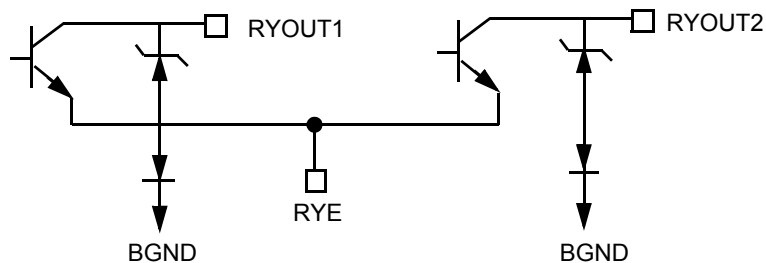
| Description | Test Conditions (See Note 1) | Min | Typ | Max | Unit | Note |
|------------------------------------------------------------------------------------------------|-------------------------------------------------|----------------------------------------|----------------|-------|---------------------|---------------|
| Transmission Performance | | | | | | |
| 2-wire return loss | 200 Hz to 3.4 kHz (Test Circuit D) | 26 | | | dB | 1, 4, 6 |
| Z_{VTX} , analog output impedance | | | 3 | 20 | Ω | 4 |
| V_{VTX} , analog output offset voltage | | -50 | | +50 | mV | |
| Z_{RSN} , analog input impedance | | | 1 | 20 | Ω | 4 |
| Overload level, 2-wire and 4-wire, off hook | Active state | 2.5 | | | Vpk | 2a |
| Overload level, 2-wire | On hook, $R_{LAC} = 600 \Omega$ | 0.88 | | | Vrms | 2b |
| THD (Total Harmonic Distortion) | +3 dBm, BAT2 = -24 V | | -64 | -50 | dB | 5 |
| THD, on hook, OHT state | 0 dBm, $R_{LAC} = 600 \Omega$, BAT1 = -67 V | | | -40 | | |
| Longitudinal Performance (See Test Circuit C) | | | | | | |
| Longitudinal to metallic L-T, L-4 balance | 200 Hz to 3.4 kHz | 40 | | | dB | |
| Longitudinal signal generation 4-L | 200 Hz to 800 Hz, Normal polarity | 40 | | | | |
| Longitudinal current per pin (A or B) | Active or OHT state | 12 | 28 | | mArms | 4 |
| Longitudinal impedance at A or B | 0 to 100 Hz, $T_A = +25^\circ\text{C}$ | | 25 | | Ω/pin | |
| Idle Channel Noise | | | | | | |
| C-message weighted noise | | | +7 | +14 | dBrnC | |
| Psophometric weighted noise | | | -83 | -76 | dBmp | 4 |
| Insertion Loss and Four- to Four-Wire Balance Return Signal (See Test Circuits A and B) | | | | | | |
| Gain accuracy | 4- to 2-wire | 0 dBm, 1 kHz | -0.20 | 0 | +0.20 | dB |
| Gain accuracy | 2- to 4-wire and 4- to 4-wire | 0 dBm, 1 kHz | -6.22 | -6.02 | -5.82 | |
| Gain accuracy | 4- to 2-wire | OHT state, on hook | -0.35 | 0 | +0.35 | |
| Gain accuracy | 2- to 4-wire and 4- to 4-wire | OHT state, on hook | -6.37 | -6.02 | -5.77 | |
| Gain accuracy over frequency | | 300 to 3400 Hz relative to 1 kHz | -0.10 | | +0.10 | |
| Gain tracking | | +3 dBm to -55 dBm relative to 0 dBm | -0.10 | | +0.10 | |
| Gain tracking OHT state, on hook | | 0 dBm to -37 dBm +3 dBm to 0 dBm | -0.10 -0.35 | | +0.10 +0.35 | |
| Group delay | | 0 dBm, 1 kHz | | 3 | | μs |

ELECTRICAL CHARACTERISTICS (CONTINUED)

| Description | Test Conditions (See Note 1) | Min | Typ | Max | Unit | Note |
|---------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------|--------------------|----------|----------|---------------|------|
| Line Characteristics | | | | | | |
| I_L , Loop-current accuracy | I_L in constant-current region, B2EN = 0 | $0.87I_L$ | I_L | $1.1I_L$ | mA | |
| I_L , Long loops, Active state | $R_{LDC} = 600 \Omega$, RSGL = open $R_{LDC} = 750 \Omega$, RSGL = short | 20 20 | 21.7 | | | |
| I_L , Accuracy, Standby state | $I_L = \frac{ V_{BAT1} - 10 \text{ V}}{R_L + 400}$ | $0.8I_L$ | I_L | $1.2I_L$ | | |
| | I_L = constant-current region $T_A = 25^\circ\text{C}$ | 18 | 27 | 39 | | |
| $I_{L\text{LIM}}$ | Active, A and B to ground OHT, A and B to ground | | 55 55 | 110 | | 4 |
| I_L , Loop current, Open Circuit state | $R_L = 0$ | | | 100 | μA | |
| I_A , Pin A leakage, Tip Open state | $R_L = 0$ | | | 100 | | |
| I_B , Pin B current, Tip Open state | B to ground | | 34 | | mA | |
| V_A , Standby, ground-start signaling | A to $-48 \text{ V} = 7 \text{ k}\Omega$, B to ground = 100Ω | -7.5 | -5 | | | V |
| V_{AB} , Open Circuit voltage | | 42 | | | | |
| Power Supply Rejection Ratio ($V_{\text{RIPPLE}} = 100 \text{ mVrms}$), Active Normal State | | | | | | |
| V_{CC} | 50 Hz to 3400 Hz | 33 | 50 | | dB | 5 |
| V_{NEG} | 50 Hz to 3400 Hz | 30 | 40 | | | |
| V_{BAT1} | 50 Hz to 3400 Hz | 30 | 50 | | | |
| V_{BAT2} | 50 Hz to 3400 Hz | 30 | 50 | | | |
| Power Dissipation | | | | | | |
| On hook, Open Circuit state | V_{BAT1} | | 48 | 100 | mW | |
| On hook, Standby state | V_{BAT2} | | 55 | 80 | | 9 |
| On hook, OHT state | V_{BAT1} | | 200 | 300 | | |
| On hook, Active state | V_{BAT1} | | 220 | 350 | | |
| Off hook, Standby state | V_{BAT1} or V_{BAT2} | $R_L = 300 \Omega$ | 2000 | 2800 | | 9 |
| Off hook, OHT state | V_{BAT1} | $R_L = 300 \Omega$ | 2000 | 2200 | | |
| Off hook, Active state | V_{BAT2} | $R_L = 300 \Omega$ | 550 | 750 | | |
| Supply Currents | | | | | | |
| I_{CC} , On-hook V_{CC} supply current | Open Circuit state | | 3.0 | 4.5 | mA | |
| | Standby state | | 3.2 | 5.5 | | |
| | OHT state | | 6.2 | 8.0 | | |
| | Active state–normal | | 6.5 | 9.0 | | |
| I_{NEG} , On-hook V_{NEG} supply current | Open Circuit state | | 0.1 | 0.2 | | |
| | Standby state | | 0.1 | 0.2 | | |
| | OHT state | | 0.7 | 1.1 | | |
| | Active state–normal | | 0.7 | 1.1 | | |
| I_{BAT} , On-hook V_{BAT} supply current | Open Circuit state | | 0.45 | 1.0 | | |
| | Standby state | | 0.6 | 1.5 | | |
| | OHT state | | 2.0 | 4.0 | | |
| | Active state–normal | | 2.7 | 5.0 | | |

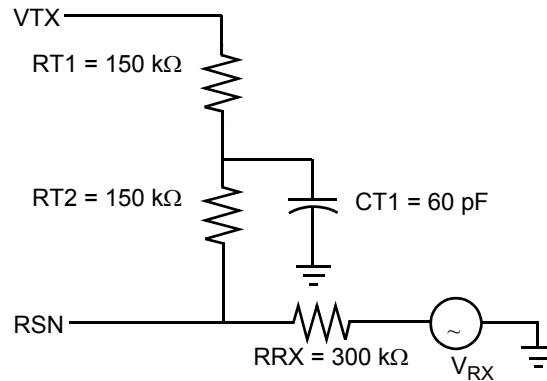
ELECTRICAL CHARACTERISTICS (continued)

| Description | Test Conditions (See Note 1) | Min | Typ | Max | Unit | Note |
|------------------------------------------------------|-------------------------------------------------------------------------|-------------------|-------|----------------|-----------------|------|
| Logic Inputs (C3–C1, D2–D1, E1, and B2EN) | | | | | | |
| V _{IH} , Input High voltage | | 2.0 | | | V | |
| V _{IL} , Input Low voltage | | | | 0.8 | | |
| I _{IH} , Input High current | | –75 | | 40 | μA | |
| I _{IL} , Input Low current | | –400 | | | | |
| Logic Output DET | | | | | | |
| V _{OL} , Output Low voltage | I _{OUT} = 0.8 mA, 15 kΩ to V _{CC} | | | 0.40 | V | |
| V _{OH} , Output High voltage | I _{OUT} = –0.1 mA, 15 kΩ to V _{CC} | 2.4 | | | | |
| Ring-Trip Detector Input | | | | | | |
| Ring detect accuracy | $I_{RTD} = \left(\frac{ BAT1 - 1}{RRT1} + 24 \mu A \right) \cdot 335$ | –10 | | +10 | % | |
| Ring Signal | | | | | | |
| V _{AB} , Ringing | Bat1 = –67 V, ringload = 1570 Ω | 57 | 61 | | V _{pk} | |
| V _{AB} Ringing offset | V _{RINGIN} = 2.5 V | | 0 | | V | |
| ΔV _{AB} /ΔV _{RINGIN} (RINGIN gain) | | | 180 | | — | |
| Ground-Key Detector Thresholds | | | | | | |
| Ground-key resistive threshold | B to ground | 2 | 5 | 10 | kΩ | |
| Ground-key current threshold | B to ground | | 11 | | mA | |
| Loop Detector | | | | | | |
| R _{LTH} , Loop-resistance detect threshold | Active, V _{BAT1} Active, V _{BAT2} Standby | –20 –20 –12 | | 20 20 12 | % | 8 |
| Relay Driver Output (RELAY1 and 2) | | | | | | |
| V _{OL} , On voltage (each output) | I _{OL} = 30 mA | | +0.25 | +0.4 | V | |
| V _{OL} , On voltage (each output) | I _{OL} = 40 mA | | +0.30 | +0.8 | V | 4 |
| I _{OH} , Off leakage (each output) | V _{OH} = +5 V | | | 100 | μA | |
| Zener breakover (each output) | I _Z = 100 μA | 6.6 | 7.9 | | V | |
| Zener on voltage (each output) | I _Z = 30 mA | | 11 | | | |

RELAY DRIVER SCHEMATIC

Notes:

1. Unless otherwise noted, test conditions are $BAT1 = -67\text{ V}$, $BAT2 = -24\text{ V}$, $V_{CC} = +5\text{ V}$, $V_{NEG} = -5\text{ V}$, $R_L = 600\ \Omega$, $R_{DC1} = 80\text{ k}\Omega$, $R_{DC2} = 20\text{ k}\Omega$, $R_D = 75\text{ k}\Omega$, no fuse resistors, $C_{HP} = 0.018\ \mu\text{F}$, $C_{DC} = 1.2\ \mu\text{F}$, $D_1 = D_2 = 1\text{N}400\text{x}$, two-wire AC input impedance (ZSL) is a $600\ \Omega$ resistance synthesized by the programming network shown below. $R_{SGL} = \text{open}$, $R_{SGH} = \text{open}$, $R_{DCR} = 2\text{ k}\Omega$, $R_{RT1} = 430\text{ k}\Omega$, $R_{RT2} = 12\text{ k}\Omega$, $C_{RT} = 1.5\ \mu\text{F}$, $R_{SLEW} = 150\text{ k}\Omega$, $C_{SLEW} = 0.33\ \mu\text{F}$.



2. a. Overload level is defined when $THD = 1\%$.
b. Overload level is defined when $THD = 1.5\%$.
3. Balance return signal is the signal generated at V_{TX} by V_{RX} . This specification assumes that the two-wire AC load impedance matches the programmed impedance.
4. Not tested in production. This parameter is guaranteed by characterization or correlation to other tests.
5. This parameter is tested at 1 kHz in production. Performance at other frequencies is guaranteed by characterization.
6. Group delay can be greatly reduced by using a Z_T network such as that shown in Note 1 above. The network reduces the group delay to less than $2\ \mu\text{s}$ and increases 2WRL . The effect of group delay on line card performance may also be compensated for by synthesizing complex impedance with the QSLAC or DSLAC device.
7. Open Circuit V_{AB} can be modified using RSGH.
8. R_D must be greater than $56\text{ k}\Omega$. Refer to [Table 2](#) for typical value of R_{LTH} .
9. Lower power is achieved by switching into low-battery state in standby. Standby loop current is returned to V_{BAT1} regardless of the battery selected.

Table 1. SLIC Decoding

| State | C3 C2 C1 | 2-Wire Status | (DET) Output | | Battery Selection |
|-------|----------|--------------------------|---------------|------------|-------------------|
| | | | E1 = 1 | E1 = 0 | |
| 0 | 0 0 0 | Open Circuit | Ring trip | Ring trip | B2EN |
| 1 | 0 0 1 | Ringing | Ring trip | Ring trip | |
| 2 | 0 1 0 | Active | Loop detector | Ground key | |
| 3 | 0 1 1 | On-hook TX (OHT) | Loop detector | Ground key | |
| 4 | 1 0 0 | Tip Open | Loop detector | Ground key | B2EN = 1** |
| 5 | 1 0 1 | Standby | Loop detector | Ground key | V_{BAT1} |
| 6* | 1 1 0 | Active Polarity Reversal | Loop detector | Ground key | B2EN |
| 7* | 1 1 1 | OHT Polarity Reversal | Loop detector | Ground key | |

Notes:

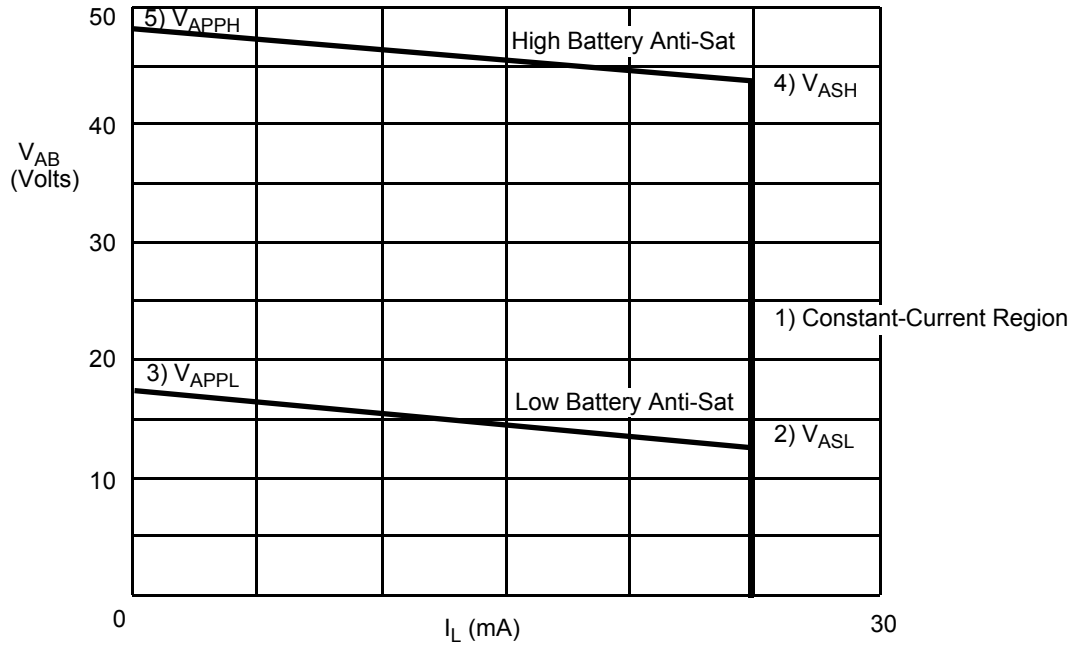
* Only -1 performance grade devices support polarity reversal.

** For correct ground-start operation using Tip Open, V_{BAT1} on-hook battery must be used.

Table 2. User-Programmable Components

| | |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| $Z_T = 500(Z_{2WIN} - 2R_F)$ | <p>Z_T is connected between the VTX and RSN pins. The fuse resistors are R_F, and Z_{2WIN} is the desired 2-wire AC input impedance. When computing Z_T, the internal current amplifier pole and any external stray capacitance between VTX and RSN must be taken into account.</p> |
| $Z_{RX} = \frac{Z_L}{G_{42L}} \cdot \frac{1000 \cdot Z_T}{Z_T + 500(Z_L + 2R_F)}$ | <p>Z_{RX} is connected from V_{RX} to R_{SN}. Z_T is defined above, and G_{42L} is the desired receive gain.</p> |
| $R_{DC1} + R_{DC2} = \frac{2500}{I_{LOOP}}$ $R_{DCR1} + R_{DCR2} = \frac{3000}{I_{ringlim}}$ $C_{DC} = 19 \text{ ms} \cdot \frac{R_{DC1} + R_{DC2}}{R_{DC1}R_{DC2}}$ $C_{DCR} = \frac{R_{DCR1} + R_{DCR2}}{R_{DCR1}R_{DCR2}} \cdot 150 \mu\text{s}$ | <p>R_{DC1}, R_{DC2}, and C_{DC} form the network connected to the RDC pin. I_{LOOP} is the desired loop current in the constant-current region.</p> <p>R_{DCR1}, R_{DCR2}, and C_{DCR} form the network connected to the RDCR pin. See Applications Circuit for these components.</p> <p>C_{DCR} sets the ringing time constant, which can be between 15 μs and 150 μs.</p> |
| $R_D = R_{LTH} \cdot 12.67 \text{ for high battery state}$ | <p>R_D is the resistor connected from the RD pin to GND and R_{LTH} is the loop-resistance threshold between on-hook and off-hook detection. R_D should be greater than 56 kΩ to guarantee detection will occur in the Standby state. Choose the value of R_D for high battery state; then use the equation for R_{LTH} to find where the threshold is for low battery.</p> |
| Loop-Threshold Detect Equations | |
| $R_{LTH} = \frac{R_D}{12.67} \text{ for high battery}$ | <p>This is the same equation as for R_D in the preceding equation, except solved for R_{LTH}.</p> |
| $R_{LTH} = \frac{R_D}{11.37} \text{ for low battery}$ | <p>For low battery, the detect threshold is slightly higher, which will avoid oscillating between states.</p> |
| $R_{LTH} = \frac{ V_{BAT1} - 10}{915} \cdot R_D - 400 - 2R_F$ | <p>$R_{LTH} \text{ standby} < R_{LTH} \text{ active} < V_{BAT1} < R_{LTH} \text{ active} < V_{BAT2}$, which will guarantee no unstable states under all operating conditions. This equation will show at what resistance the standby threshold will be; it is actually a current threshold rather than a resistance threshold, which is shown by the Vbat dependency.</p> |

DC FEED CHARACTERISTICS

Figure 1. Typical V_{AB} vs. I_L DC Feed Characteristics

$$R_{DC} = R_{DC1} + R_{DC2} = 20 \text{ k}\Omega + 80 \text{ k}\Omega = 100 \text{ k}\Omega$$

$$(V_{BAT1} = -67 \text{ V}, V_{BAT2} = -24 \text{ V})$$

Notes:

1. Constant-current region: $V_{AB} = I_L R_L = \frac{2500}{R_{DC}} R_L$; where $R_L = R_L + 2R_F$

2. Low battery $V_{ASL} = \frac{1000 \cdot (104 \cdot 10^3 + R_{SGL})}{6720 \cdot 10^3 + (80 \cdot R_{SGL})}$; where R_{SGL} = resistor to GND, B2EN = logic Low.

Anti-sat region: $V_{ASL} = \frac{1000 \cdot (R_{SGL} - 56 \cdot 10^3)}{6720 \cdot 10^3 + (80 \cdot R_{SGL})}$; where R_{SGL} = resistor to V_{CC} , B2EN = logic Low.

R_{SGL} to V_{CC} must be greater than 100 k Ω .

3. $V_{APPL} = 4.17 + V_{ASL}$

$$I_{LOOP} = \frac{V_{APPL}}{\frac{(R_{DC1} + R_{DC2})}{600} + 2R_F + R_{LOOP}}$$

4. High battery $V_{ASH} = V_{ASHH} + V_{ASL}$

Anti-sat region: $V_{ASHH} = \frac{1000 \cdot (70 \cdot 10^3 + R_{SGH})}{1934 \cdot 10^3 + (31.75 \cdot R_{SGH})}$; where R_{SGH} = resistor to GND, B2EN = logic High.

$$V_{ASHH} = \frac{1000 \cdot (R_{SGH} + 2.75 \cdot 10^3)}{1934 \cdot 10^3 + (31.75 \cdot R_{SGH})}$$
; where R_{SGH} = resistor to V_{CC} , B2EN = logic High.

R_{SGH} to V_{CC} must be greater than 100 k Ω .

5. $V_{APPH} = 4.17 + V_{ASH}$

$$I_{LOPH} = \frac{V_{APPH}}{\frac{(R_{DC1} + R_{DC2})}{600} + 2R_F + R_{LOOP}}$$

RING-TRIP COMPONENTS

$R_{RT2} = 12 \text{ k}\Omega$

$C_{RT} = 1.5 \text{ }\mu\text{F}$

$$R_{RT1} = 320 \cdot CF \cdot \frac{V_{BAT1}}{V_{BAT1} - 5 - (24 \text{ }\mu\text{A} \cdot 320 \cdot CF \cdot (R_{LRT} + 150 + 2R_F))} \cdot (R_{LRT} + 150 + 2R_F)$$

where R_{LRT} = Loop-detection threshold resistance for ring trip and CF = Crest factor of ringing signal (≈ 1.25)

R_{SLEW} , C_{SLEW}

Ring waveform rise time $\approx 0.214 \cdot (R_{SLEW} \cdot C_{SLEW}) \approx tr$.

For a 1.25 crest factor @ 20 Hz, $tr \approx 10 \text{ mS}$.

$\therefore (R_{SLEW} = 150 \text{ k}\Omega, C_{SLEW} = 0.33 \text{ }\mu\text{F})$

C_{SLEW} should be changed if a different crest factor is desired.

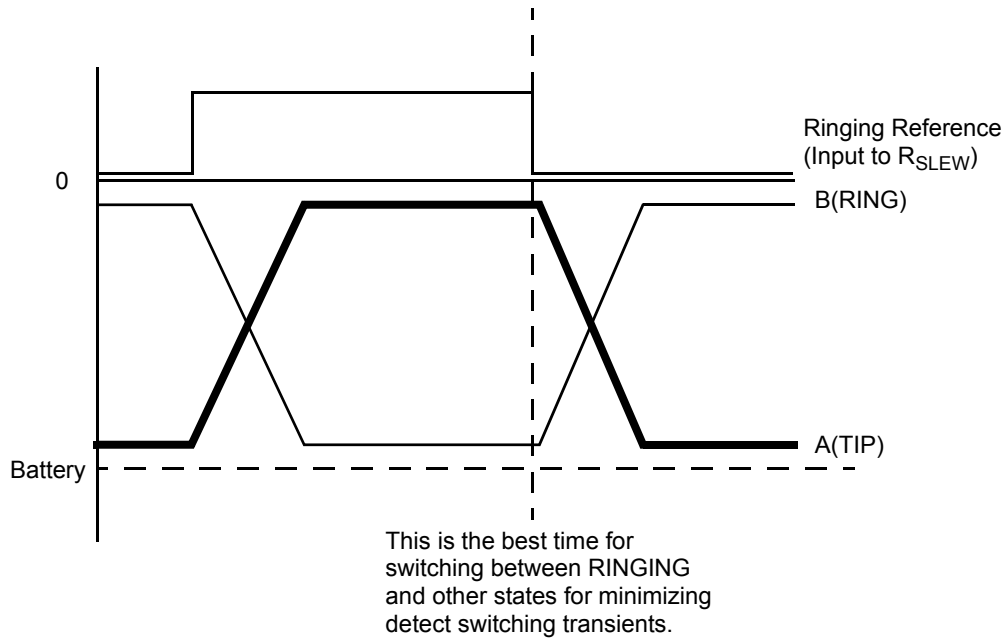
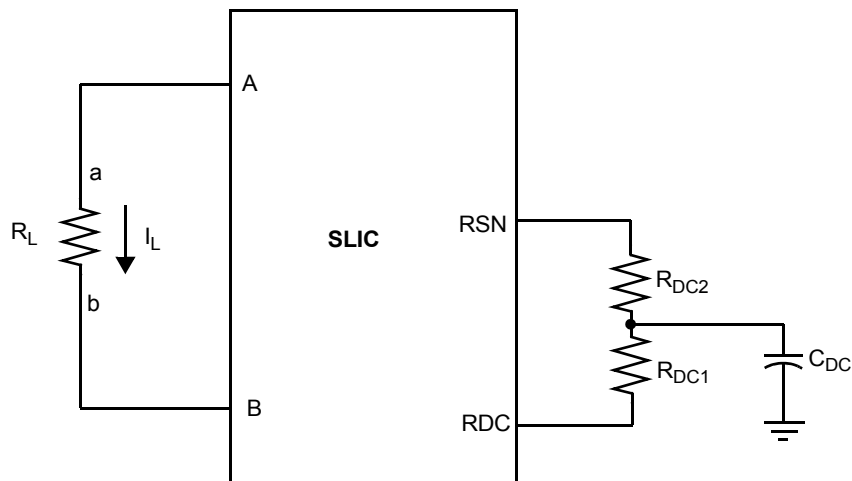


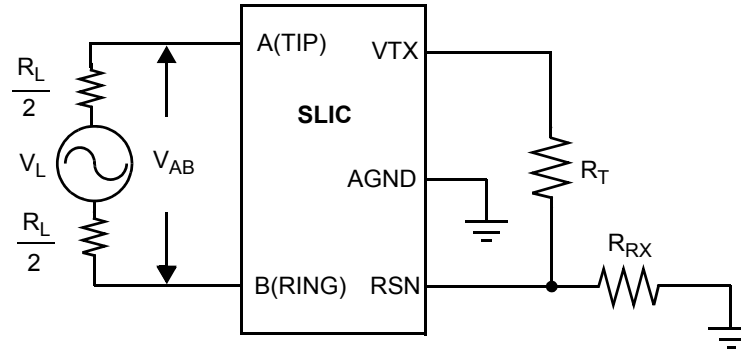
Figure 2. Ringing Waveforms



Feed current programmed by R_{DC1} and R_{DC2}

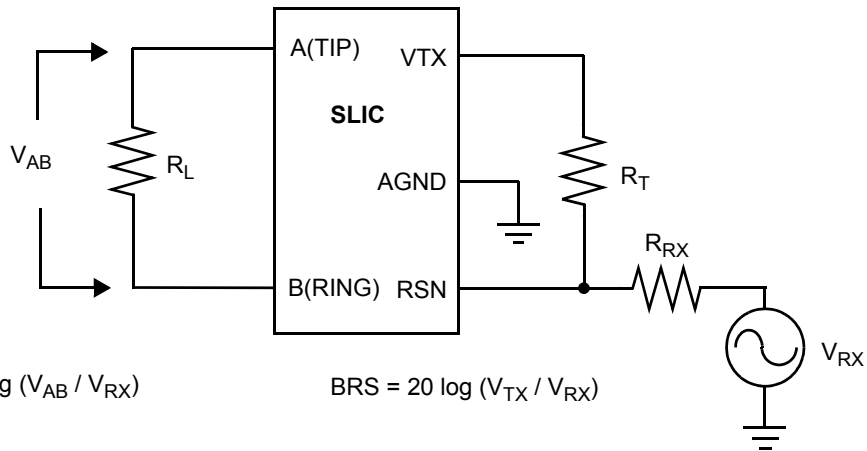
Figure 3. Feed Programming

TEST CIRCUITS



$$I_{L2-4} = 20 \log (V_{TX} / V_{AB})$$

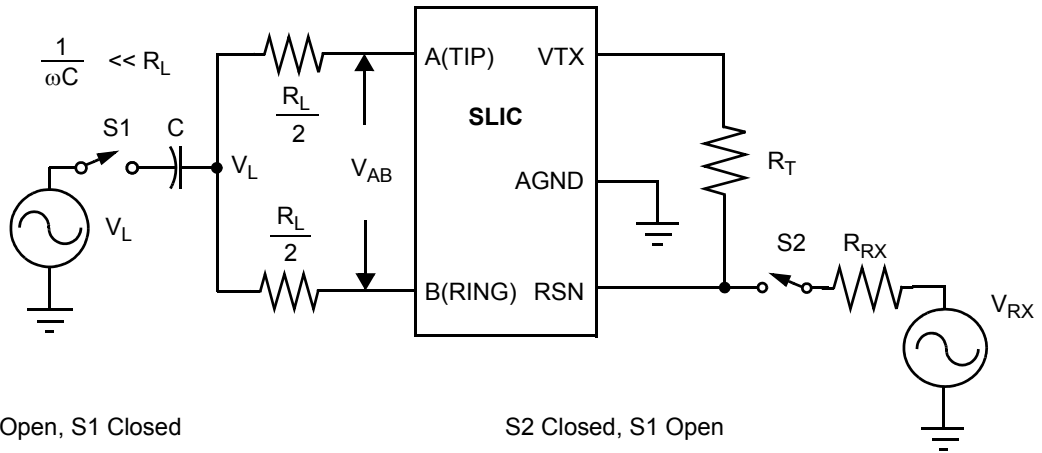
A. Two- to Four-Wire Insertion Loss



$$I_{L4-2} = 20 \log (V_{AB} / V_{RX})$$

$$BRS = 20 \log (V_{TX} / V_{RX})$$

B. Four- to Two-Wire Insertion Loss and Four- to Four-Wire Balance Return Signal



S2 Open, S1 Closed

$$L-T \text{ Long. Bal.} = 20 \log (V_{AB} / V_L)$$

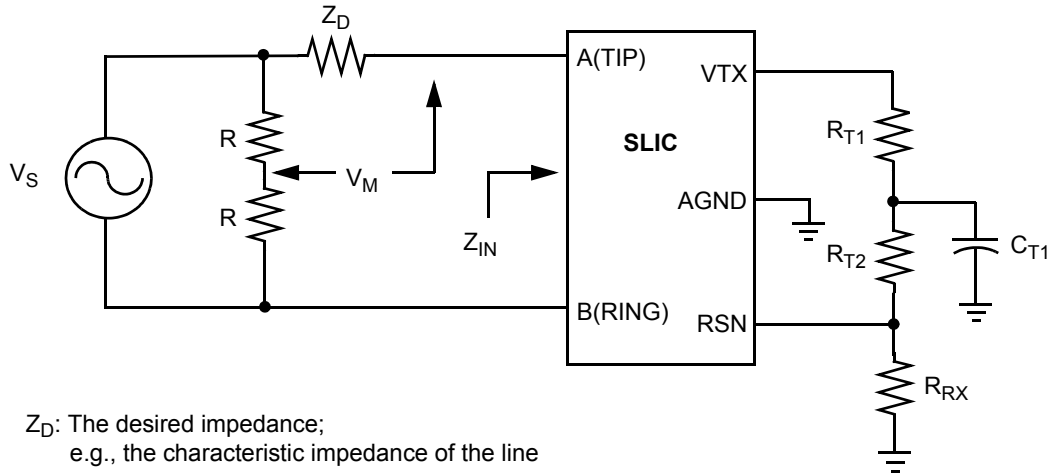
$$L-4 \text{ Long. Bal.} = 20 \log (V_{TX} / V_L)$$

S2 Closed, S1 Open

$$4-L \text{ Long. Sig. Gen.} = 20 \log (V_L / V_{RX})$$

C. Longitudinal Balance

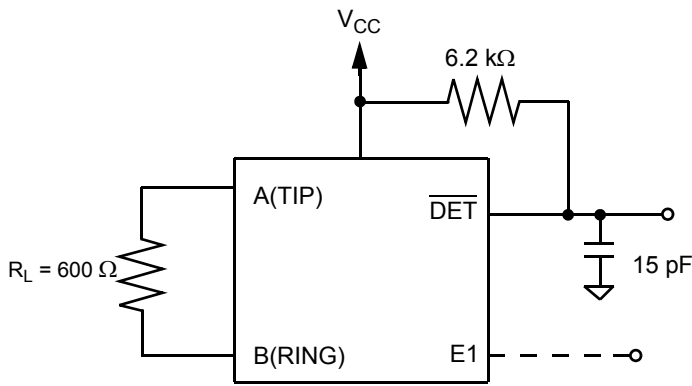
TEST CIRCUITS (continued)



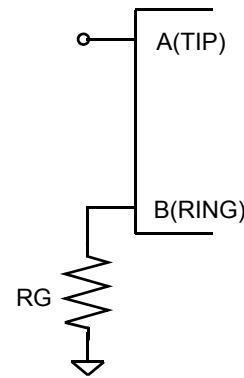
Z_D : The desired impedance;
e.g., the characteristic impedance of the line

$$\text{Return loss} = -20 \log (2 V_M / V_S)$$

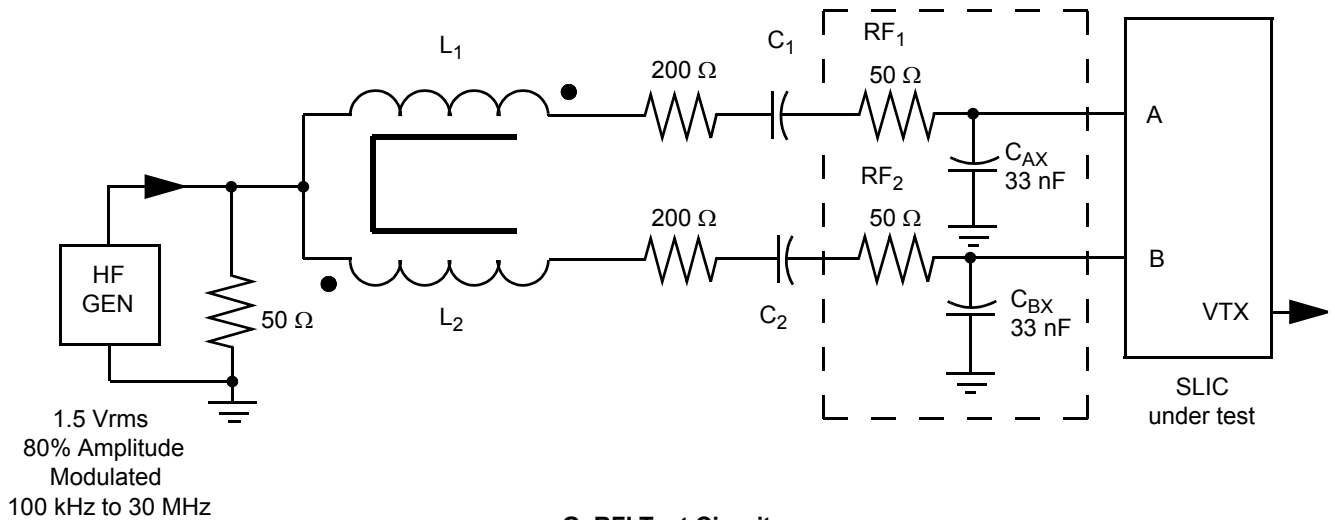
D. Two-Wire Return Loss Test Circuit



E. Loop-Detector Switching

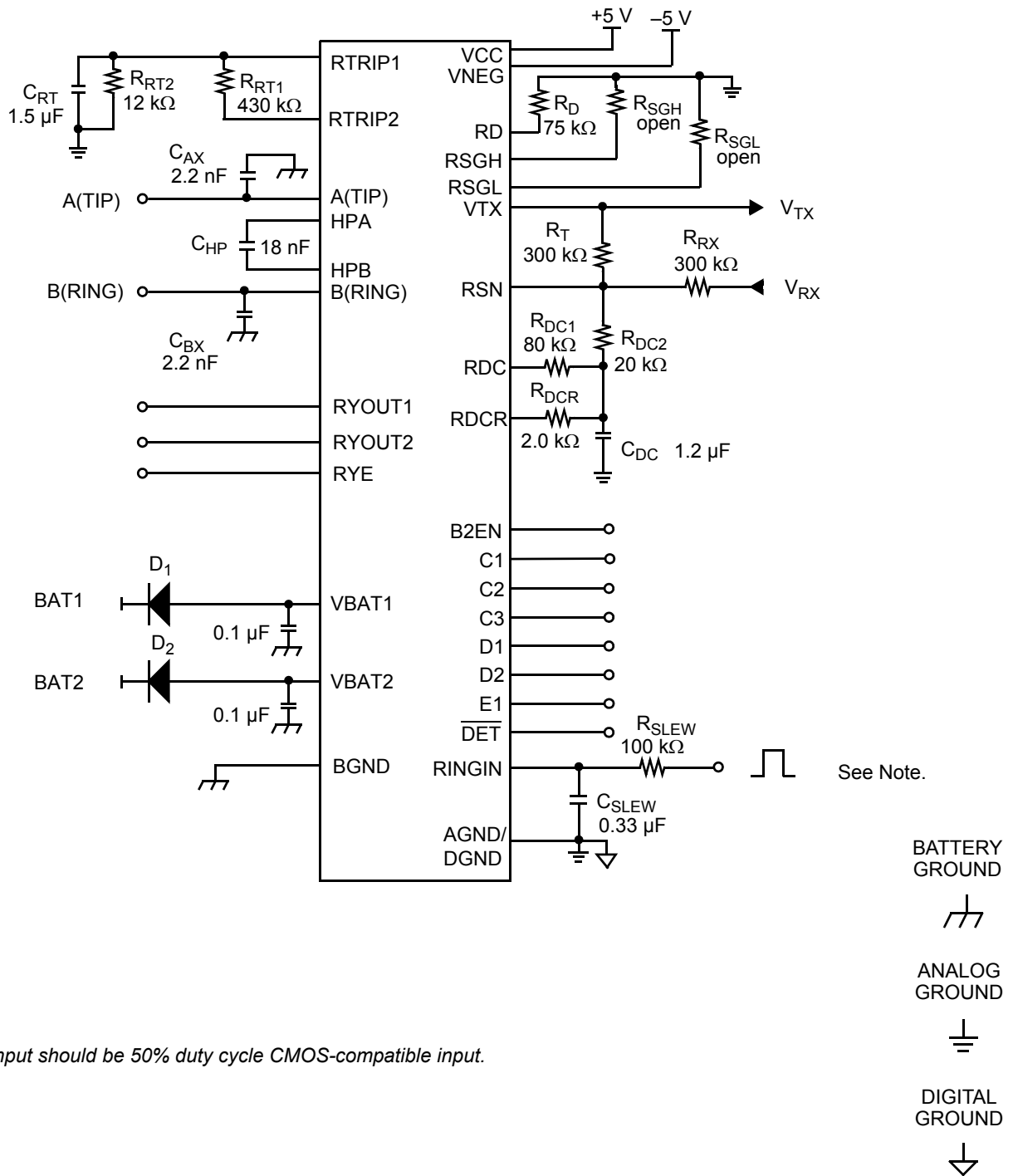


F. Ground-Key Switching



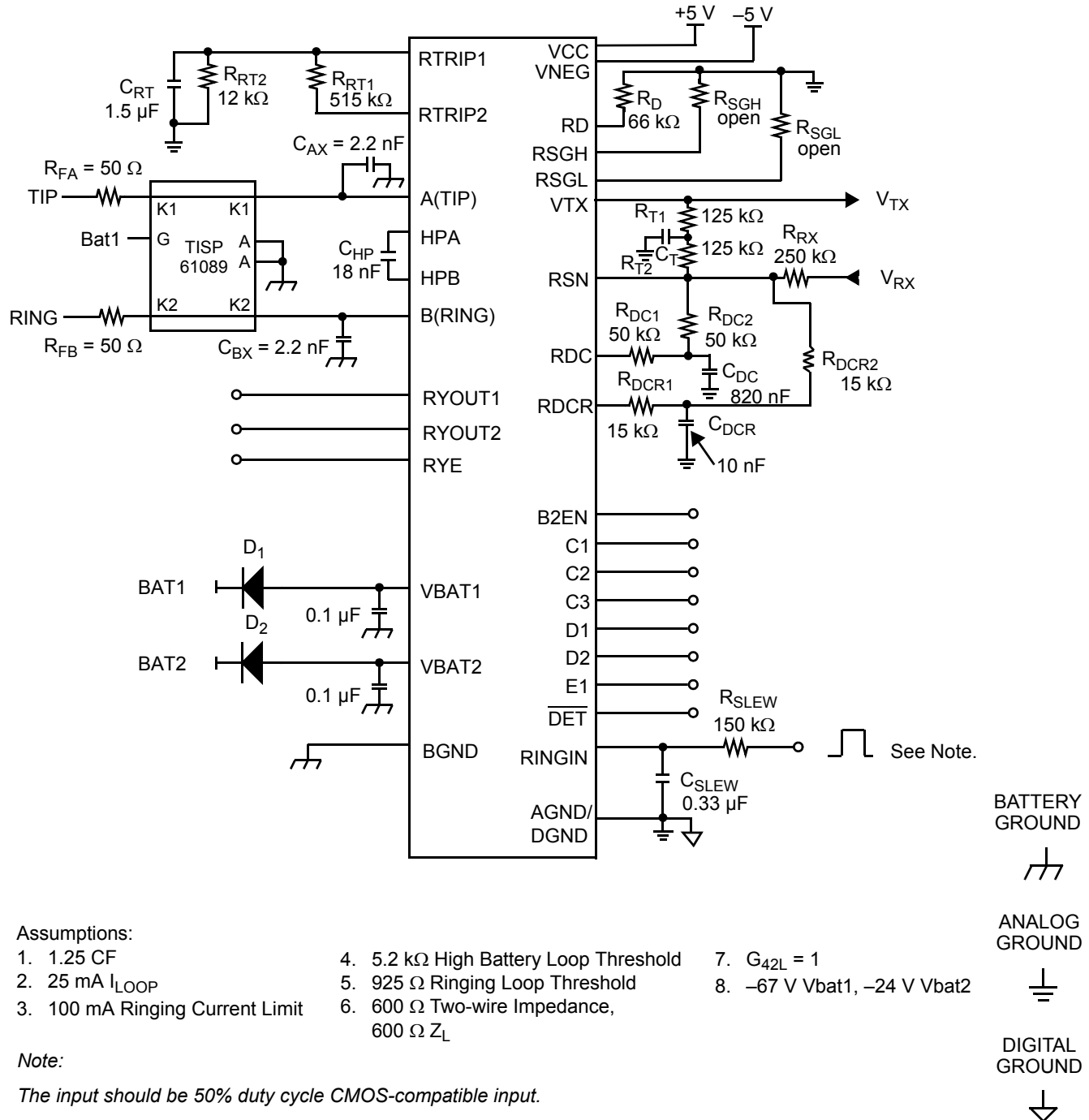
G. RFI Test Circuit

TEST CIRCUITS (continued)



H. Le79R70 Test Circuit

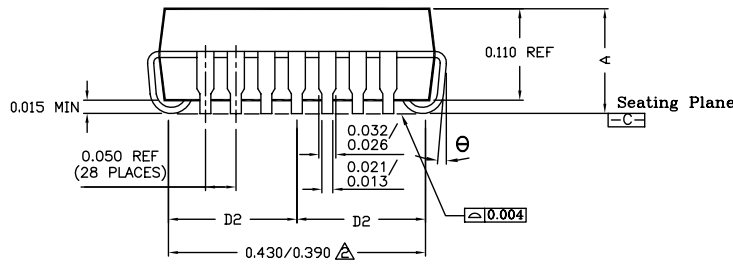
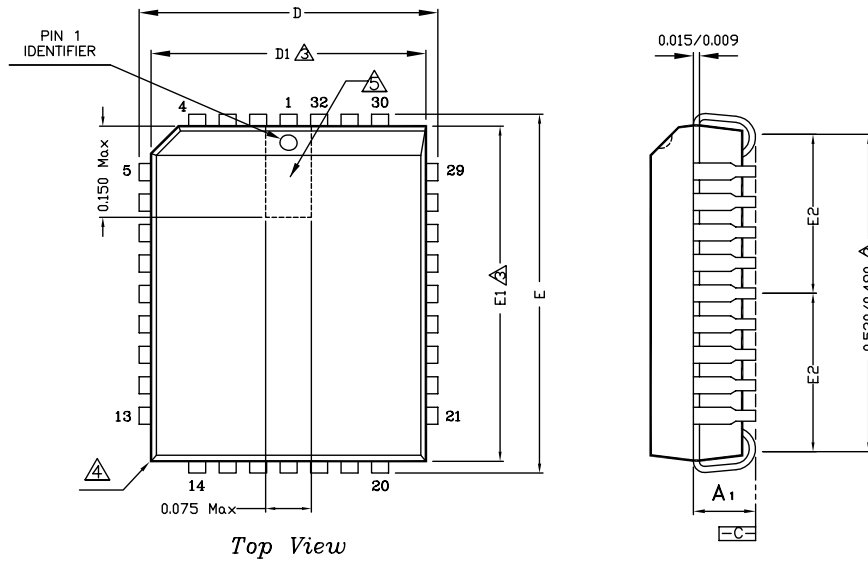
APPLICATION CIRCUIT



I. Application Circuit

PHYSICAL DIMENSIONS

32-Pin PLCC



NOTES:

| 32-Pin PLCC | | | |
|----------------|-----------|-------|--------|
| JEDEC # MS-016 | | | |
| Symbol | Min | Nom | Max |
| A | 0.125 | -- | 0.140 |
| A1 | 0.075 | 0.090 | 0.095 |
| D | 0.485 | 0.490 | 0.495 |
| D1 | 0.447 | 0.450 | 0.453 |
| D2 | 0.205 REF | | |
| E | 0.585 | 0.590 | 0.595 |
| E1 | 0.547 | 0.550 | 0.553 |
| E2 | 0.255 REF | | |
| θ | 0 deg | -- | 10 deg |

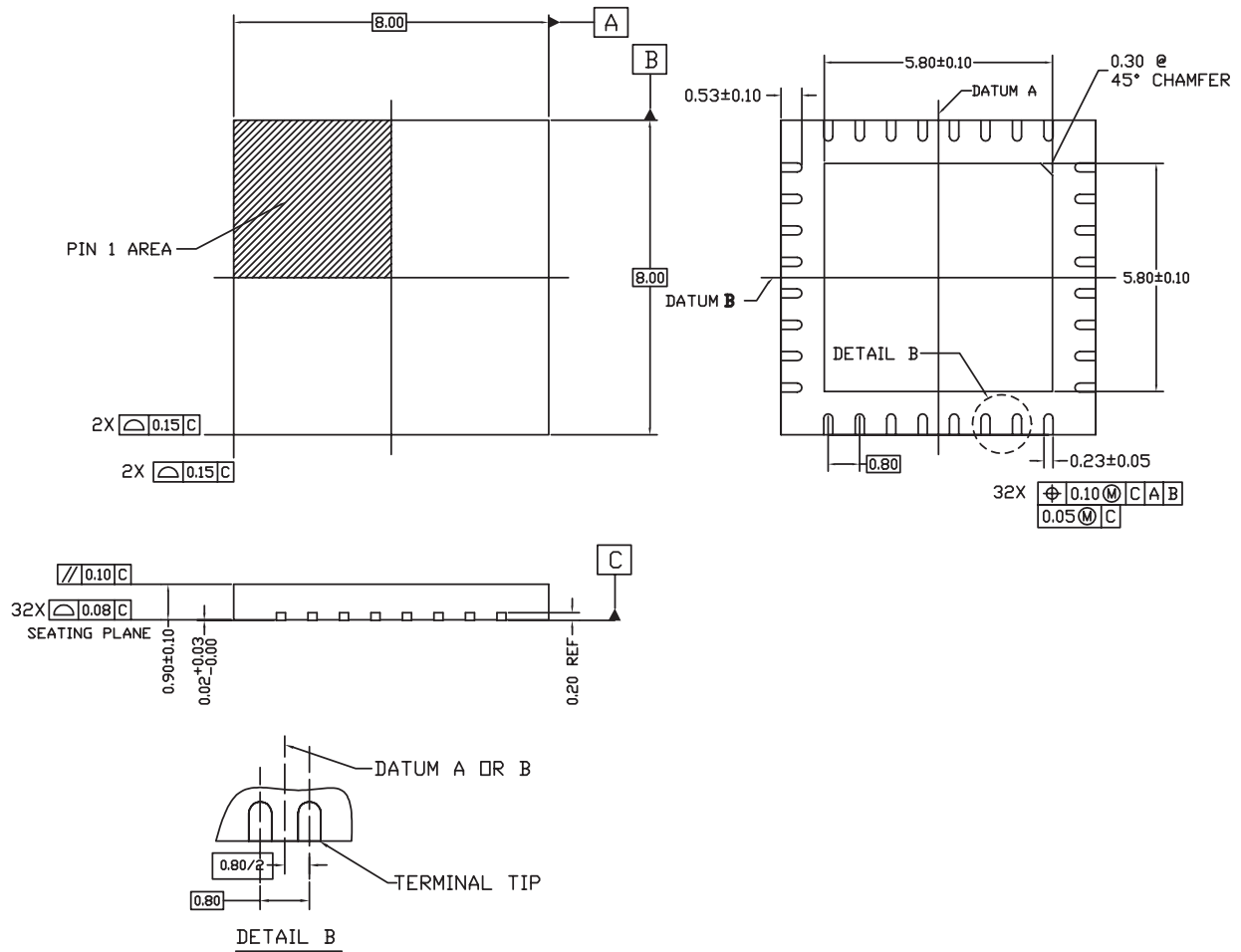
- 1 Dimensioning and tolerancing conform to ASME Y14,5M-1994.
- 2 To be measured at seating plan $\square-C$ contact point.
- 3 Dimensions "D1" and "E1" do not include mold protrusion. Allowable mold protrusion is 0.010 inch per side. Dimensions "D" and "E" include mold mismatch and determined at the parting line; that is "D1" and "E1" are measured at the extreme material condition at the upper or lower parting line.
- 4 Exact shape of this feature is optional.
- 5 Details of pin 1 identifier are optional but must be located within the zone indicated.
- 6 Sum of DAM bar protrusions to be 0.007 max per lead.
- 7 Controlling dimension : Inch.
- 8 Reference document : JEDEC MS-016

32-Pin PLCC

Note:

Packages may have mold tooling markings on the surface. These markings have no impact on the form, fit or function of the device. Markings will vary with the mold tool used in manufacturing.

32-Pin QFN



| Symbol | 32 LEAD QFN | | |
|--------|-------------|------|------|
| | Min | Nom | Max |
| A | 0.80 | 0.90 | 1.00 |
| A2 | 0.57 REF | | |
| b | 0.18 | 0.23 | 0.28 |
| D | 8.00 BSC | | |
| D2 | 5.70 | 5.80 | 5.90 |
| E | 8.00 BSC | | |
| E2 | 5.70 | 5.80 | 5.90 |
| e | 0.80 BSC | | |
| L | 0.43 | 0.53 | 0.63 |
| N | 32 | | |
| A1 | 0.00 | 0.02 | 0.05 |
| A3 | 0.20 REF | | |
| aaa | 0.20 | | |
| bbb | 0.10 | | |
| ccc | 0.10 | | |

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5M-1994.
2. All dimensions are in millimeters. \oplus is in degrees.
3. N is the total number of terminals.
4. \triangle The Terminal #1 identifier and terminal numbering convention shall conform to JEP 95-1 and SSP-012. Details of the Terminal #1 identifier are optional, but must be located within the zone indicated. The Terminal #1 identifier may be either a mold or marked feature.
5. \triangle Coplanarity applies to the exposed pad as well as the terminals.
6. Reference Document: JEDEC MO-220.
7. \triangle Lead width deviates from the JEDEC MO-220 standard.

32-Pin QFN

Note:

Packages may have mold tooling markings on the surface. These markings have no impact on the form, fit or function of the device. Markings will vary with the mold tool used in manufacturing.

REVISION HISTORY

Revision A to B

- Minor changes were made to the data sheet style and format to conform to Zarlink standards.

Revision B to C

- The 28-pin SOIC information and package was added to the Ordering Information and the Connection Diagrams sections.
- The physical dimensions (PL032 and SOW28) were added to the Physical Dimensions section.
- Updated the Pin Description table to correct inconsistencies.

Revision C to D

- Changed Ring-Trip Components equation from:

$$R_{RT1} = 300 \cdot CF \cdot \frac{V_{BAT1}}{V_{bat} - 3.5 - (15 \mu A \cdot 300 \cdot CF \cdot (R_{LRT} + 150 + 2R_F))} \cdot (R_{LRT} + 150 + 2R_F)$$

To:

$$R_{RT1} = 320 \cdot CF \cdot \frac{V_{BAT1}}{V_{bat} - 5 - (24 \mu A \cdot 320 \cdot CF \cdot (R_{LRT} + 150 + 2R_F))} \cdot (R_{LRT} + 150 + 2R_F)$$

Revision D to E

- In "Ordering Information" section, added description for wafer foundry facility optional character.

Revision E to F

- Updated device name from "Am79R70" to "Le79R70" throughout document.
- Added QFN package to "Connection Diagram," "Absolute Maximum Ratings," and "Physical Dimensions."
- Removed reference to PLCC package type in "General Description."
- Ordering Information: Temperature statement updated to standard.
- Absolute Maximum Ratings: Notes updated to standard.
- Operating Ranges: Temperature statement updated to standard.

Revision F to G1

- Added green package OPNs to [Ordering Information, on page 1](#)
- Added [Package Assembly, on page 6](#)

Revision G1 to H1

- Added "Packing" column and Note 5 to [Ordering Information, on page 1](#)
- Updated 32QFN drawing in [Physical Dimensions, on page 19](#)

Revision H1 to I1

- Added green package OPNs and removed OPN for SOIC package in [Ordering Information, on page 1](#)
- Removed SOIC drawing in [Physical Dimensions, on page 19](#)
- Added note to [Physical Dimensions, on page 19](#)

Revision I1 to J1

- Removed the following OPNs from [Ordering Information, on page 1](#): Le79R70JC, Le79R70-1JC, Le79R70QC, Le79R70-1QC.
- Changed I_L Loop-Current Accuracy from 0.9 to 0.871 in [Electrical Characteristics](#).

Revision J1 to J2

- Enhanced format of package drawings in [Physical Dimensions, on page 19](#)
- Added new headers/footers due to Zarlink purchase of Legerity on August 3, 2007



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