

N-Channel Power MOSFET

60V, 54A, 12mΩ

FEATURES

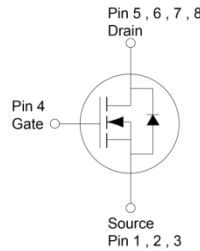
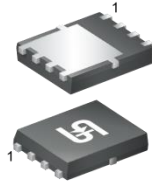
- Low $R_{DS(ON)}$ to minimize conductive losses
- Logic level
- Low gate charge for fast power switching
- 100% UIS and R_g tested
- Compliant to RoHS directive 2011/65/EU and in accordance to WEEE 2002/96/EC
- Halogen-free according to IEC 61249-2-21

KEY PERFORMANCE PARAMETERS

PARAMETER	VALUE	UNIT
V_{DS}	60	V
$R_{DS(on)}$ (max)	$V_{GS} = 10V$	12
	$V_{GS} = 4.5V$	15
Q_g	18	nC

APPLICATIONS

- BLDC Motor Control
- Battery Power Management
- DC-DC converter
- Secondary Synchronous Rectification


PDFN56


Note: MSL 1 (Moisture Sensitivity Level) per J-STD-020

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ^(Note 1)	I_D	$T_C = 25^\circ\text{C}$	54
		$T_A = 25^\circ\text{C}$	10
Pulsed Drain Current	I_{DM}	216	A
Single Pulse Avalanche Current ^(Note 2)	I_{AS}	19	A
Single Pulse Avalanche Energy ^(Note 2)	E_{AS}	54	mJ
Total Power Dissipation	P_D	$T_C = 25^\circ\text{C}$	69
		$T_C = 125^\circ\text{C}$	14
Total Power Dissipation	P_D	$T_A = 25^\circ\text{C}$	2.6
		$T_A = 125^\circ\text{C}$	0.5
Operating Junction and Storage Temperature Range	T_J, T_{STG}	- 55 to +150	$^\circ\text{C}$

THERMAL PERFORMANCE

PARAMETER	SYMBOL	LIMIT	UNIT
Junction to Case Thermal Resistance	$R_{\theta JC}$	1.8	$^\circ\text{C/W}$
Junction to Ambient Thermal Resistance	$R_{\theta JA}$	48	$^\circ\text{C/W}$

Thermal Performance Note: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case-thermal reference is defined at the solder mounting surface of the drain pins. $R_{\theta JA}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

ELECTRICAL SPECIFICATIONS (T _A = 25°C unless otherwise noted)						
PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Static						
Drain-Source Breakdown Voltage	V _{GS} = 0V, I _D = 250μA	BV _{DSS}	60	--	--	V
Gate Threshold Voltage	V _{GS} = V _{DS} , I _D = 250μA	V _{GS(TH)}	1.2	1.7	2.5	V
Gate-Source Leakage Current	V _{GS} = ±20V, V _{DS} = 0V	I _{GSS}	--	--	±100	nA
Drain-Source Leakage Current	V _{GS} = 0V, V _{DS} = 60V	I _{DSS}	--	--	1	μA
	V _{GS} = 0V, V _{DS} = 60V T _J = 125°C		--	--	100	
Drain-Source On-State Resistance (Note 3)	V _{GS} = 10V, I _D = 10A	R _{DS(on)}	--	9.6	12	mΩ
	V _{GS} = 4.5V, I _D = 9A		--	11	15	
Forward Transconductance (Note 3)	V _{DS} = 5V, I _D = 10A	g _{fs}	--	36	--	S
Dynamic (Note 4)						
Total Gate Charge	V _{GS} = 10V, V _{DS} = 30V, I _D = 10A	Q _g	--	36.5	--	nC
Total Gate Charge	V _{GS} = 4.5V, V _{DS} = 30V, I _D = 9A	Q _g	--	18	--	
Gate-Source Charge		Q _{gs}	--	6	--	
Gate-Drain Charge		Q _{gd}	--	7.5	--	
Input Capacitance	V _{GS} = 0V, V _{DS} = 30V f = 1.0MHz	C _{iss}	--	2116	--	pF
Output Capacitance		C _{oss}	--	136	--	
Reverse Transfer Capacitance		C _{rss}	--	85	--	
Gate Resistance	f = 1.0MHz	R _g	0.5	1.6	3.2	Ω
Switching (Note 4)						
Turn-On Delay Time	V _{GS} = 10V, V _{DS} = 30V, I _D = 10A, R _G = 2Ω,	t _{d(on)}	--	6.5	--	ns
Turn-On Rise Time		t _r	--	13	--	
Turn-Off Delay Time		t _{d(off)}	--	26	--	
Turn-Off Fall Time		t _f	--	7	--	
Source-Drain Diode						
Forward Voltage (Note 3)	V _{GS} = 0V, I _S = 10A	V _{SD}	--	--	1	V
Reverse Recovery Time	I _S = 10A , dI/dt = 100A/μs	t _{rr}	--	18	--	ns
Reverse Recovery Charge		Q _{rr}	--	14	--	nC

Notes:

1. Silicon limited current only.
2. $L = 0.3\text{mH}$, $V_{GS} = 10V$, $V_{DD} = 30V$, $R_G = 25\Omega$, $I_{AS} = 19A$, Starting $T_J = 25^\circ\text{C}$
3. Pulse test: Pulse Width $\leq 300\mu s$, duty cycle $\leq 2\%$.
4. Switching time is essentially independent of operating temperature.

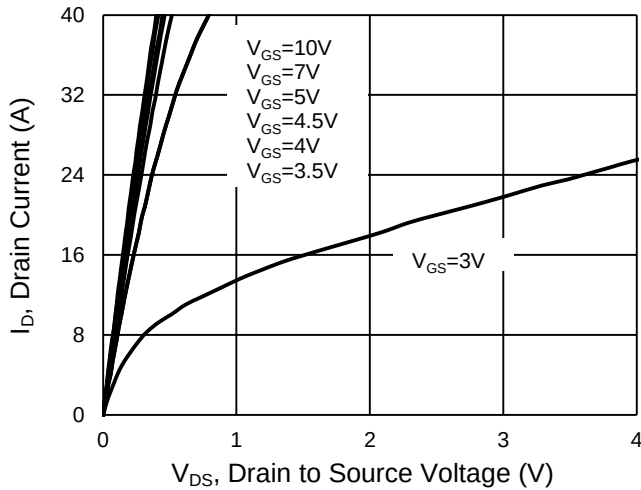
ORDERING INFORMATION

PART NO.	PACKAGE	PACKING
TSM120N06LCR RLG	PDFN56	2500pcs / 13" Reel

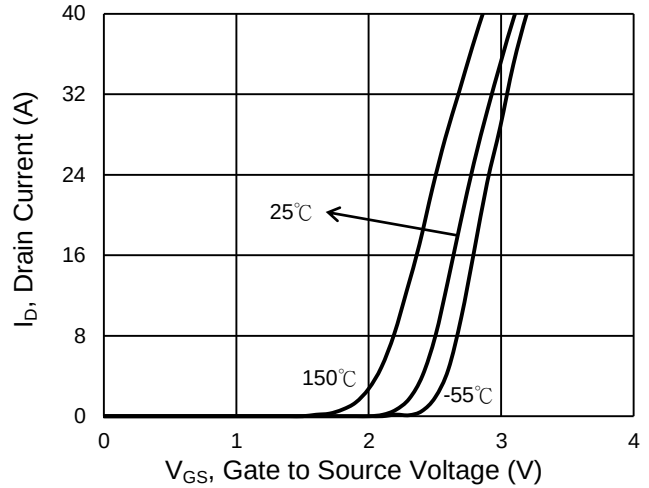
CHARACTERISTICS CURVES

($T_A = 25^\circ\text{C}$ unless otherwise noted)

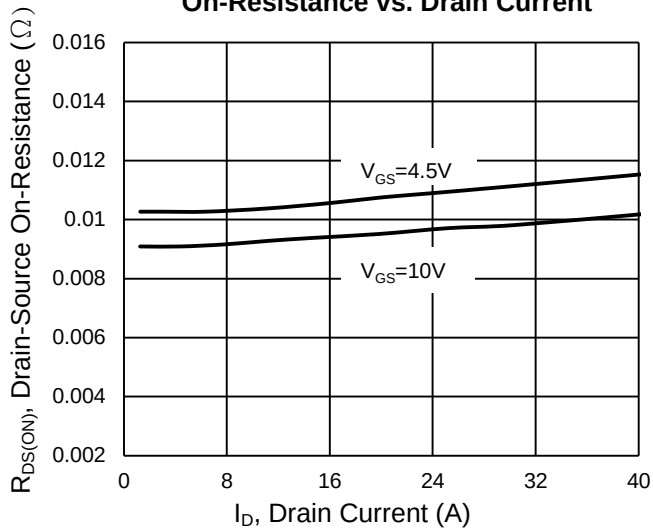
Output Characteristics



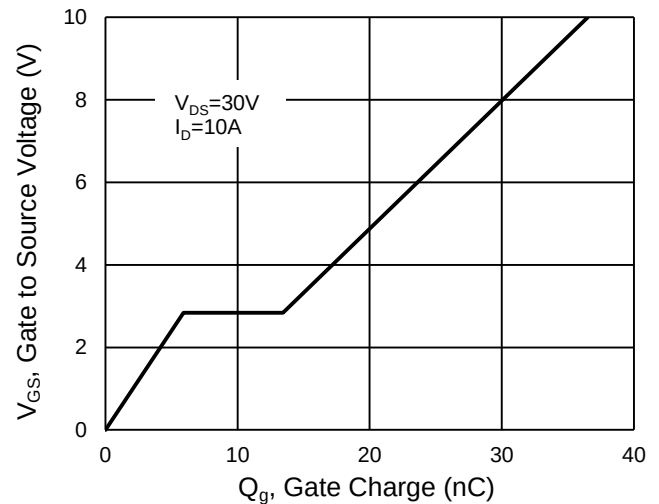
Transfer Characteristics



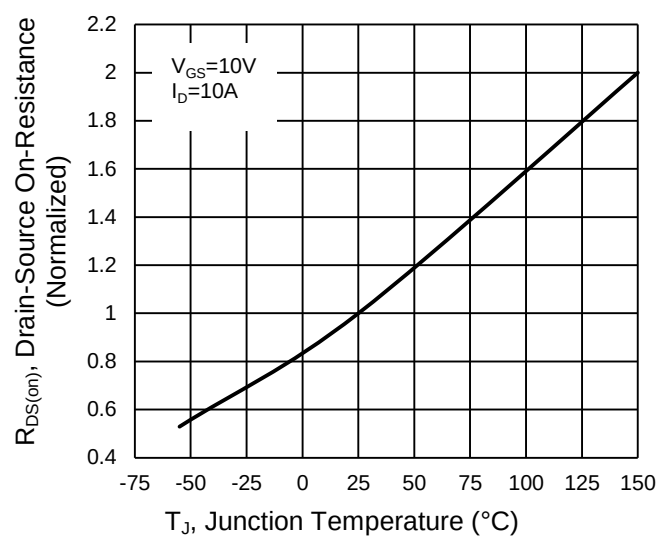
On-Resistance vs. Drain Current



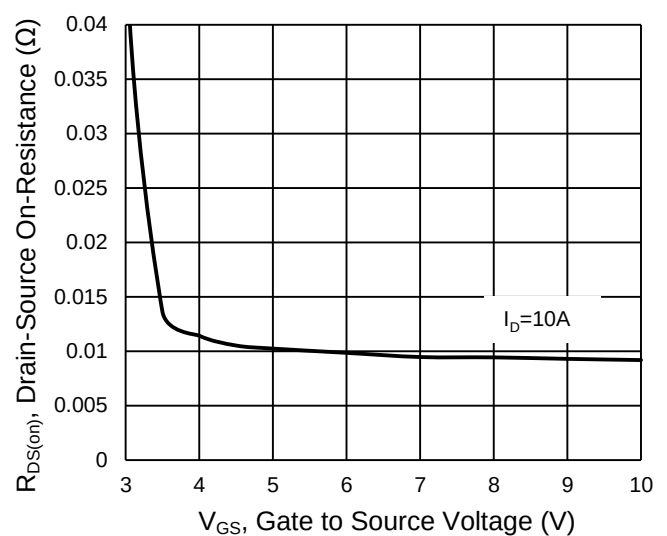
Gate-Source Voltage vs. Gate Charge



On-Resistance vs. Junction Temperature



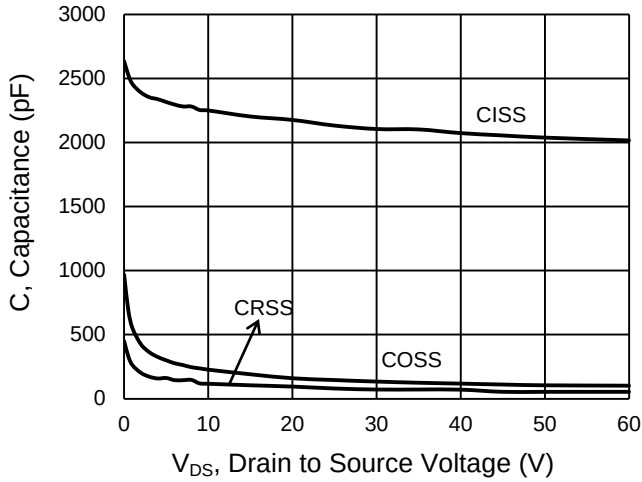
On-Resistance vs. Gate-Source Voltage



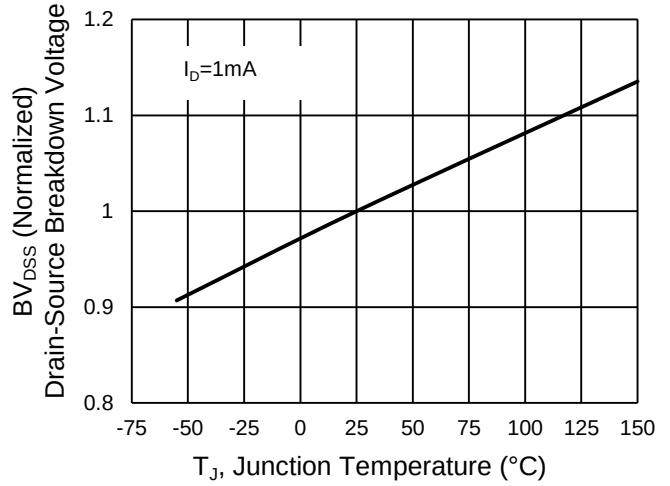
CHARACTERISTICS CURVES

($T_A = 25^\circ\text{C}$ unless otherwise noted)

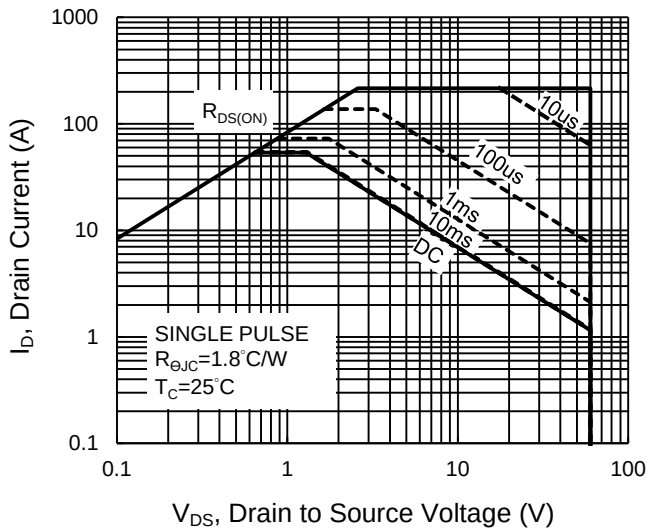
Capacitance vs. Drain-Source Voltage



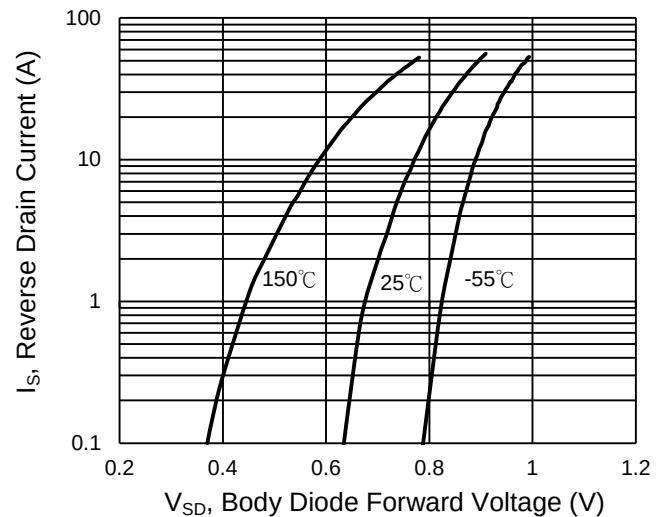
BV_{DSS} vs. Junction Temperature



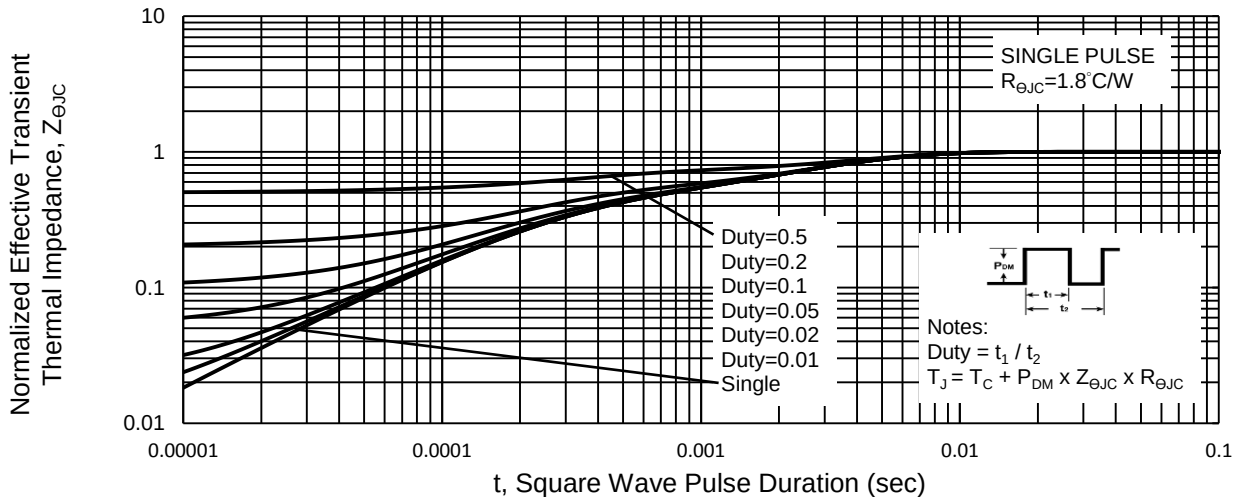
Maximum Safe Operating Area, Junction-to-Case



Source-Drain Diode Forward Current vs. Voltage

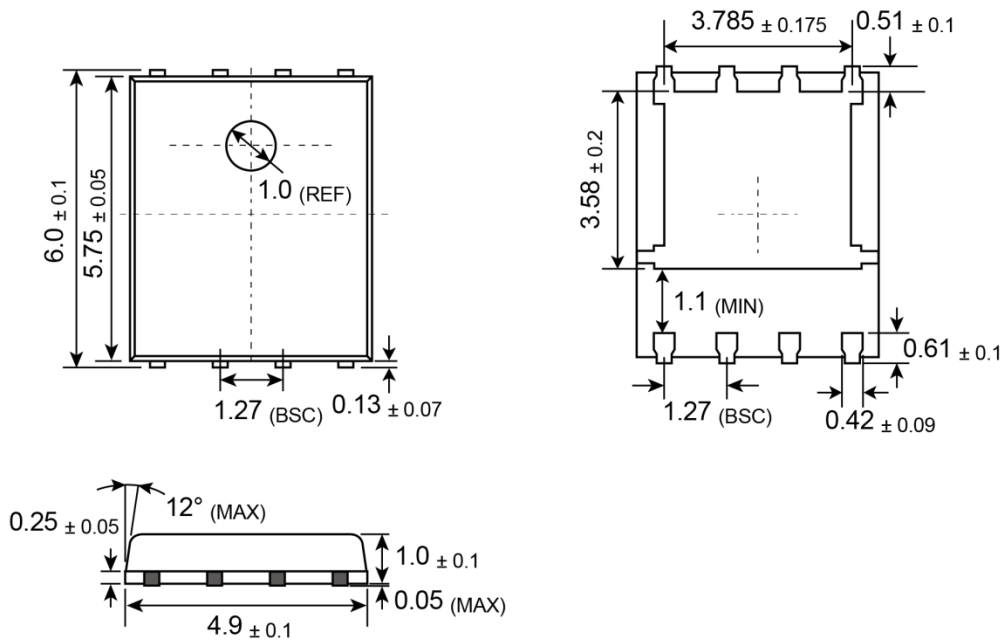


Normalized Thermal Transient Impedance, Junction-to-Case

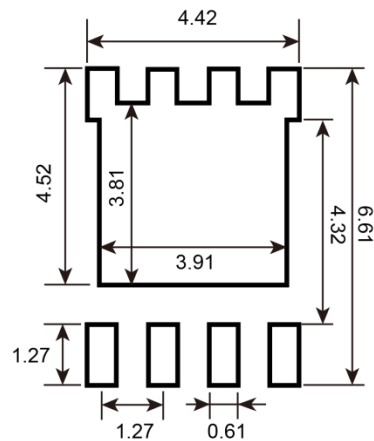


PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

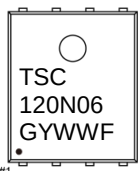
PDFN56



SUGGESTED PAD LAYOUT (Unit: Millimeters)



MARKING DIAGRAM



- G** = Halogen Free
- Y** = Year Code
- WW** = Week Code (01~52)
- F** = Factory Code

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