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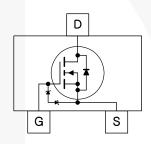
September 2014

2N7002K N-Channel Enhancement Mode Field Effect Transistor

Features

- Low On-Resistance
- Low Gate Threshold Voltage
- Low Input Capacitance
- Fast Switching Speed
- Low Input / Output Leakage
- Ultra-Small Surface Mount Package
- Pb Free / RoHS Compliant
- ESD HBM = 2000 V (Typical: 3000 V) as per JESD22 A114 and ESD CDM = 2000 V as per JESD22 C101





Ordering Information

Part Number	Top Mark	Package	Packing Method
2N7002K	7K	SOT-23 3L	Tape and Reel

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. Values are at $T_A = 25^{\circ}$ C unless otherwise noted.

Symbol	Parameter		Value	Unit
V _{DSS}	Drain-Source Voltage		60	V
V _{DGR}	Drain-Gate Voltage ($R_{GS} \le 1.0 \text{ M}\Omega$)		60	V
V _{GSS}	Gate-Source Voltage		±20	V
1	Drain Current	Continuous	300	- mA
I _D Drain		Pulsed	800	
TJ	Operating Junction Temperature Range		-55 to +150	°C
T _{STG}	Storage Temperature Range		-55 to +150	°C

Thermal Characteristics

Values are at $T_A = 25^{\circ}C$ unless otherwise noted.

Symbol	Parameter	Value	Unit
р	Total Power Dissipation	350	mW
P _D	Derate Above T _A = 25°C	2.8	mW/°C
$R_{ extsf{ heta}JA}$	Thermal Resistance, Junction-to-Ambient ⁽¹⁾	350	°C/W

Note:

1. Device mounted on FR-4 PCB, 1 inch x 0.85 inch x 0.062 inch. Minimum land pad size.

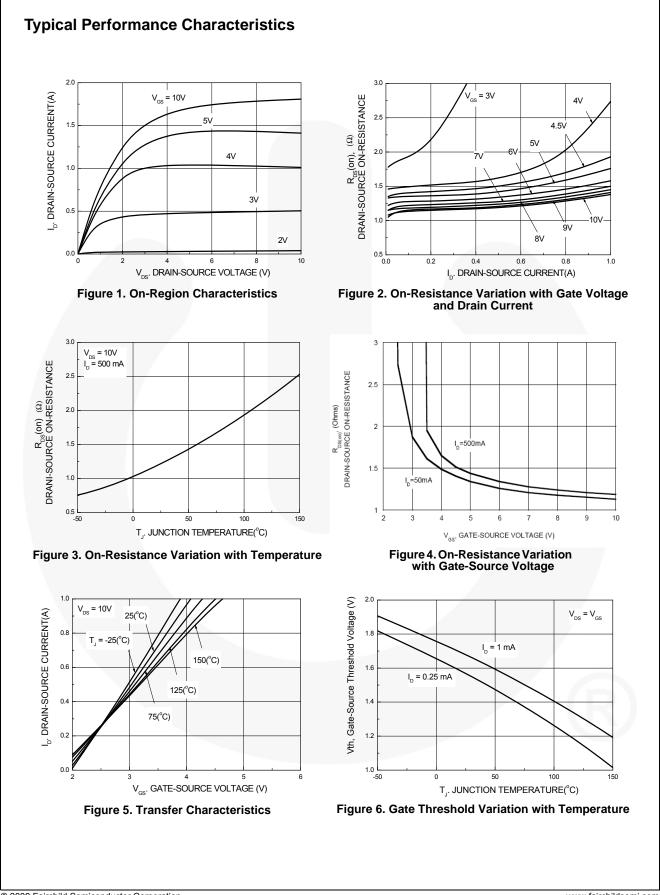
Electrical Characteristics

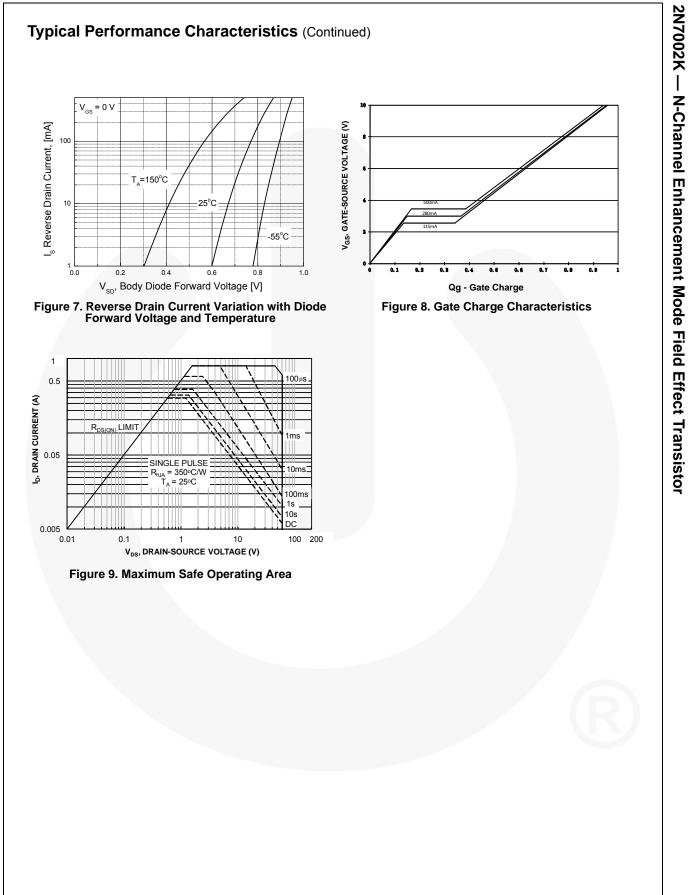
Values are at $T_A = 25^{\circ}C$ unless otherwise noted.

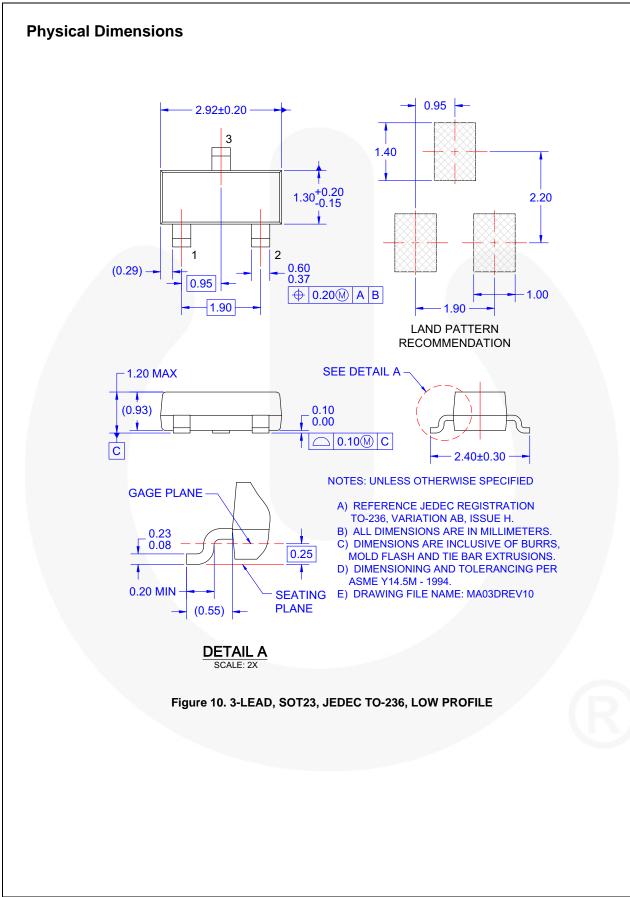
Symbol	Parameter	Conditions	Min.	Max.	Unit
Off Characte	eristics ⁽²⁾				
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0 V, I _D = 10 μA	60		V
		V _{DS} = 60 V, V _{GS} = 0 V		1.0	μΑ
I _{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 60 V, V_{GS} = 0 V,$ T _J = 125°C		500	
I _{GSS}	Gate-Body Leakage	V_{GS} = ±20 V, V_{DS} = 0 V		±10	μA
On Characte	eristics ⁽²⁾				
V _{GS(th)}	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	1.0	2.5	V
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} = 10 V, I _D = 0.5 A		2	Ω
		V _{GS} = 4.5 V, I _D = 200 mA		4	
I _{D(ON)}	On-State Drain Current	V _{GS} = 10 V, V _{DS} = 7.5 V	1.5		Α
9 _{FS}	Forward Transconductance	V _{DS} = 10 V, I _D = 0.2 A	200		mS
Dynamic Ch	aracteristics				
C _{iss}	Input Capacitance			50	pF
C _{oss}	Output Capacitance	V _{DS} = 25 V, V _{GS} = 0 V, f = 1.0 MHz		15	pF
C _{rss}	Reverse Transfer Capacitance			6	pF
	haracteristics	·			
t _{D(ON)}	Turn-On Delay Time	V _{DD} = 30 V, I _{DSS} = 200 mA,		5	ns
t _{D(OFF)}	Turn-Off Delay Time	$R_{G} = 10 \Omega, V_{GS} = 10 V$		30	ns

Note:

2. Short duration test pulse used to minimize self-heating effect.







2N7002K — N-Channel Enhancement Mode Field Effect Transistor

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