

CBTL05023

Multiplexer/demultiplexer switch for Thunderbolt applications

Rev. 5 — 15 July 2013

Product data sheet

1. General description

The CBTL05023 is a multiplexer/demultiplexer switch chip for DisplayPort v1.2 signals and the control signals of a 10 Gbit/s channel. The 10 Gbit/s channel does not pass through this switch. This chip provides BIASOUT output control signal, and the DC-biasing pull-down resistors to facilitate an external 10 Gbit/s channel.

The AUX MUX is a 2 : 1 switch with CA_DETect pin selecting between AUX and DDC (Direct Display Control) signals.

The DP MUX is a 2 : 1 switch that selects between DPML (DisplayPort Main Link) and LSTX/LSRX signals.

This chip also includes three control signal buffers: HPDOUT, CA_DETOUT and BIASOUT.

CBTL05023 is powered by a 3.3 V supply and it is available in 3 mm × 3 mm HVQFN24 package with 0.4 mm pitch.

2. Features and benefits

2.1 AUX MUX 2 : 1 switch

- This 2 : 1 switch is controlled by CA_DET signal multiplexing of the 1 Mbit/s differential AUX and DDC (Direct Display Control) signals
 - ◆ When CA_DET is HIGH, DDC path is selected
- Differential AUX channel:
 - ◆ Low insertion loss: -0.5 dB at 5 MHz
 - ◆ Low return loss: -19 dB at 5 MHz
 - ◆ Low ON-state resistance: 7.5 Ω
 - ◆ Bandwidth: 5 GHz
 - ◆ Low off-state isolation: -75 dB at 5 MHz
 - ◆ Low crosstalk: -40 dB at 5 MHz
 - ◆ Common-mode input voltage V_{IC} : 0 V to 3.3 V
 - ◆ Differential input voltage V_{ID} : 1.4 V (maximum)
- DDC channel has DDC_CLK and DDC_DAT I²C signals
 - ◆ 100 kHz 3.3 V voltage swing
- Both AUXIO+ and AUXIO- outputs have 900 Ω (± 20 %) pull-down resistor that is enabled by the status of the BIASOUT output pin
 - ◆ These pull-down resistors provide DC bias for the 10 Gbit/s channel



2.2 DP MUX 2 : 1 switch

The DP MUX is a 2:1 switch that is controlled by DP_PD pin multiplexing of a differential DPML signal and LSTX/LSRX signals

- The DPML (DisplayPort Main Link) runs up to HBR2 data rate of 5.4 Gbit/s
- The low speed DC coupled signals LSTX and LSRX are 3.3 V single-ended signals that operated at 1 Mbit/s
- 5.4 Gbit/s DPML channel:
 - ◆ Low insertion loss for DP-DPMLO path: -2.0 dB at 2.5 GHz
 - ◆ Low insertion loss for LS-DPMLO path: -2.0 dB at 2.5 GHz
 - ◆ Low return loss for DP-DPMLO path: -15 dB at 2.5 GHz
 - ◆ Low return loss for LS-DPMLO path: -14 dB at 2.5 GHz
 - ◆ Low ON-state resistance for DP-DPMLO path: 9 Ω
 - ◆ Low ON-state resistance for LS-DPMLO path: 13 Ω
 - ◆ High bandwidth: 7 GHz
 - ◆ Low off-state isolation: -20 dB at 2.5 GHz
 - ◆ Low crosstalk: -25 dB at 2.5 GHz
 - ◆ Common-mode input voltage V_{IC} : 0 V to 3.3 V
 - ◆ Differential input voltage V_{ID} : 1.4 V (maximum)

2.3 General

- The input of the HPDOUT (Hot Plug Detect output) buffer is 5 V tolerant
- HPDOUT, CA_DETOUT and BIASOUT buffers
 - ◆ CA_DET input leakage current < 0.1 μ A to prevent driving the 1 M Ω pull-down to a HIGH level
 - ◆ BIASOUT buffer is able to provide enough current to drive the bias circuit for the PIN diode path
 - ◆ BIASOUT buffer can drive up to six sets of bias circuits for the 10 Gbit/s paths
- When AUXIO_EN is LOW or (BIASIN = 0 and DP_PD = 1), this chip is in Sleep mode
 - ◆ AUXIO+ and AUXIO- of AUX MUX are disabled
 - ◆ CA_DETOUT and HPDOUT buffers are on
 - ◆ When the chip is in Sleep mode, CBTL05023 consumes < 3.5 mW
- Patent-pending high-bandwidth analog pass-gate technology
- Very low intra-pair differential skew (5 ps typical)
- All channels have back current protection
- All channels support rail-to-rail input voltage
- CMOS input buffer with hysteresis
- Single 3.3 V \pm 10 % power supply
- HVQFN24 3 mm \times 3 mm package, 0.4 mm pitch, with exposed center pad for thermal relief and electrical ground
- ESD: 2500 V HBM, 1250 V CDM
- Operating temperature range: 0 $^{\circ}$ C to 85 $^{\circ}$ C

3. Ordering information

Table 1. Ordering information

| Type number | Topside marking | Package | | Version |
|-------------|-----------------|---------|---|----------|
| | | Name | Description | |
| CBTL05023BS | 023 | HVQFN24 | plastic thermal enhanced very thin quad flat package; no leads; 24 terminals; body 3 × 3 × 0.85 mm ^[1] | SOT905-1 |

[1] Maximum package height is 1 mm.

3.1 Ordering options

Table 2. Ordering options

| Type number | Orderable part number | Package | Packing method | Minimum order quantity | Temperature |
|-------------|-----------------------|---------|--------------------------------------|------------------------|-----------------------------------|
| CBTL05023BS | CBTL05023BS,118 | HVQFN24 | Reel 13" Q1/T1 *standard mark SMD | 6000 | T _{amb} = 0 °C to +85 °C |

4. Block diagram

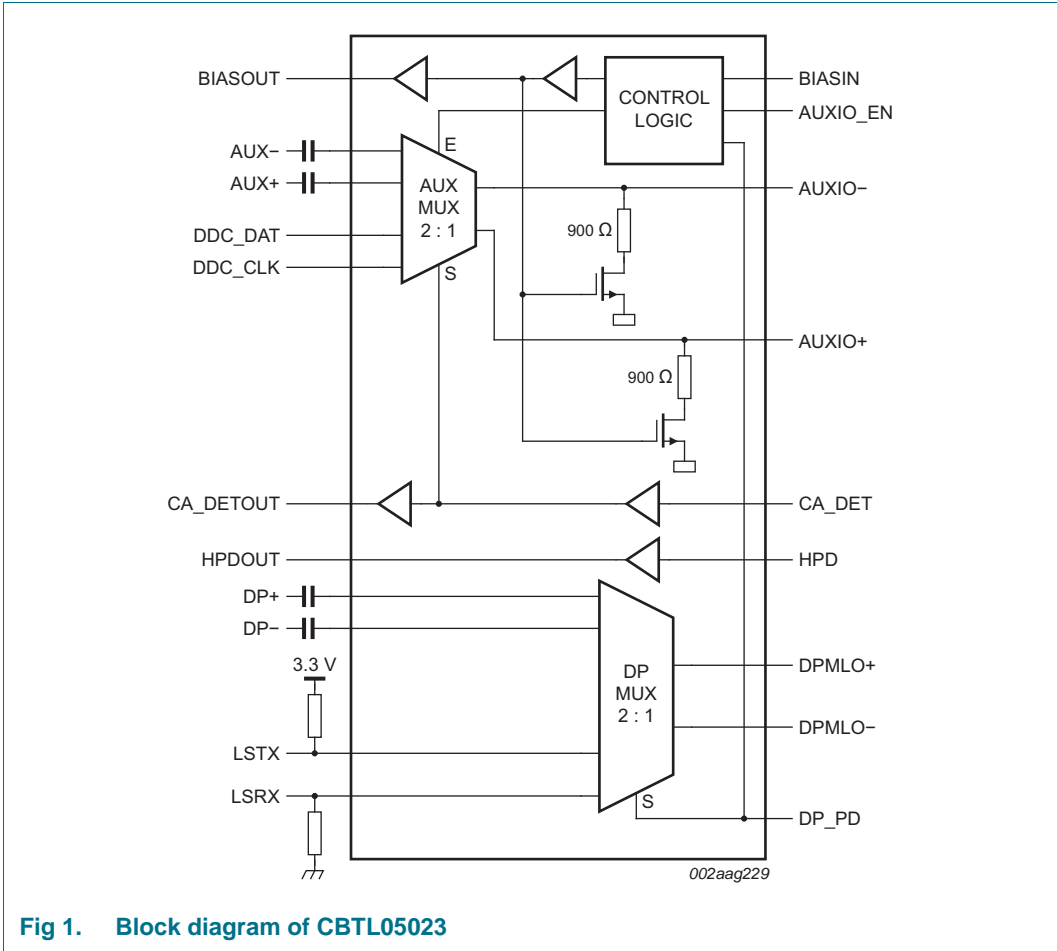
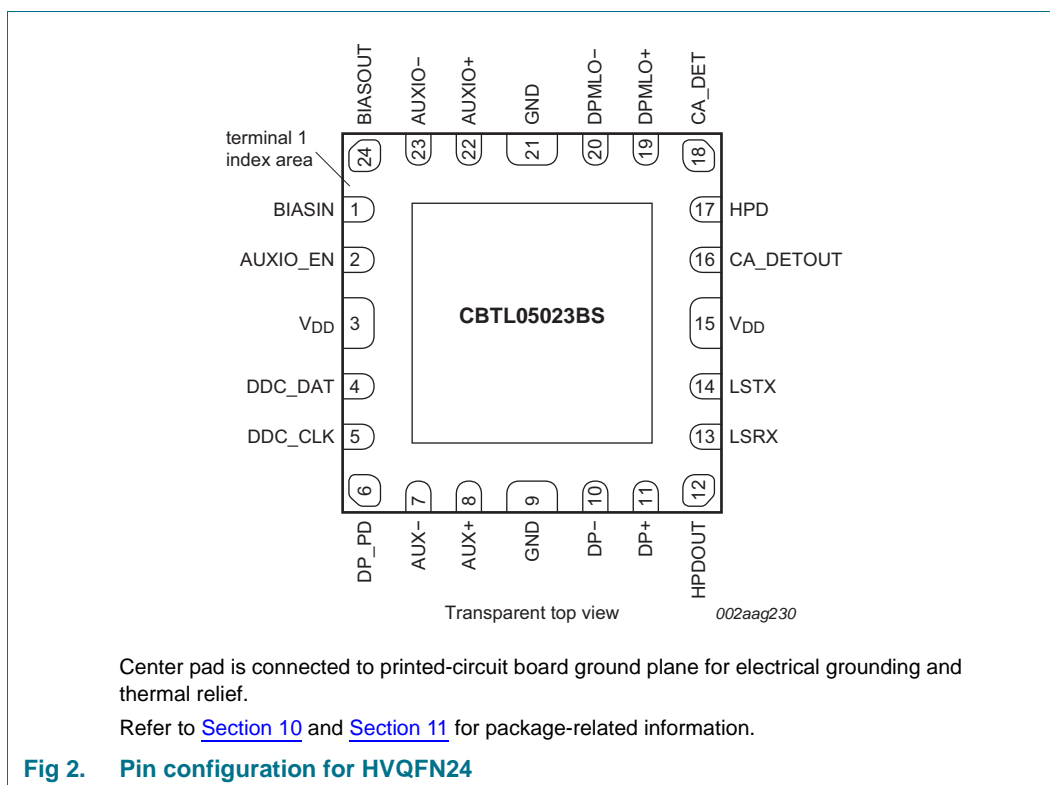


Fig 1. Block diagram of CBTL05023

5. Pinning information

5.1 Pinning



5.2 Pin description

Table 3. Pin description

| Symbol | Pin | Type | Description |
|--------------------------|-----|------------------|--|
| Data path signals | | | |
| AUX- | 7 | differential I/O | AUX differential signals. The input to this pin must be AC-coupled externally. |
| AUX+ | 8 | differential I/O | |
| AUXIO- | 23 | differential I/O | Differential pairs that are DC-coupled to 3.3 V and ground. |
| AUXIO+ | 22 | differential I/O | These two pins are internally connected to 1 k Ω pull-down resistors that are enabled by the status of BIASOUT output pin (see Table 18 for details). |
| DDC_CLK | 5 | single-ended I/O | Pair of single-ended terminals for DDC clock and data signals. |
| DDC_DAT | 4 | single-ended I/O | |
| DP- | 10 | differential I/O | High speed differential pair. The input to this pin must be AC-coupled externally. |
| DP+ | 11 | differential I/O | |
| DPMLO- | 20 | differential I/O | Differential pair that is DC-coupled to 3.3 V and ground. |
| DPMLO+ | 19 | differential I/O | |
| LSRX | 13 | single-ended I/O | Single-ended signal with DC coupled to 3.3 V. |
| LSTX | 14 | single-ended I/O | Single-ended signal with DC coupled to ground. |

Table 3. Pin description ...continued

| Symbol | Pin | Type | Description |
|----------------------------|----------------------|-------------|---|
| Control signals | | | |
| HPDOUT | 12 | CMOS output | 3.3 V CMOS output buffer for HPD. |
| HPD | 17 | CMOS input | CMOS input with 5 V tolerance. |
| CA_DET | 18 | CMOS input | When CA_SET is HIGH, the DDC_CLK and DDC_DAT replace AUX differential pair. |
| CA_DETOUT | 16 | CMOS output | 3.3 V CMOS output buffer for CA_DET. |
| BIASIN | 1 | CMOS input | CMOS input buffer. |
| BIASOUT | 24 | CMOS output | This output enables the 1 k Ω pull-down resistors for both AUXIO+ and AUXIO-. It enables the DC bias of the 10 Gbit/s data path. It provides power through six sets of 3.2 k Ω bias circuits for 10 Gbit/s paths. |
| AUXIO_EN | 2 | CMOS input | If AUXIO_EN is LOW, then AUXIO+ and AUXIO- are in high-impedance state for Sleep mode. |
| DP_PD | 6 | CMOS input | If DP_PD is LOW, then DPMLO+ and DPMLO- are connected to DP+ and DP-. If DP_PD is HIGH, then DPMLO+ and DPMLO- are connected to LSTX and LSRX. This multiplexer must work during initial power-up that might have $V_{DD} = 2.3$ V. |
| 3.3 V supply option | | | |
| V_{DD} | 3, 15 | power | 3.3 V supply. Both pin 3 and pin 15 must be connected to system power supply. |
| Ground connections | | | |
| GND | 9, 21 ^[1] | ground | 0 V (ground). |
| GND | center pad | ground | The center pad must be connected to GND plane for both electrical grounding and thermal relief. |

- [1] HVQFN24 package die supply ground is connected to both GND pins and exposed center pad. GND pins and the exposed center pad must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board level performance, the exposed pad needs to be soldered to the board using a corresponding thermal pad on the board and for proper heat conduction through the board, thermal vias need to be incorporated in the printed-circuit board in the thermal pad region.

6. Functional description

Refer to [Figure 1 “Block diagram of CBTL05023”](#).

The following sections describe the individual block functions and capabilities of the device in more detail.

6.1 Buffer function tables

Table 4. BIASOUT buffer

X = don't care.

| AUXIO_EN | BIASIN | BIASOUT |
|----------|--------|---------|
| 0 | X | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

Table 5. HPD buffer

| HPD input | HPDOUT output |
|-----------|---------------|
| 0 | 0 |
| 1 | 1 |

Table 6. CA_DET buffer

| CA_DET input | CA_DETOUT output |
|--------------|------------------|
| 0 | 0 |
| 1 | 1 |

6.2 AUX MUX state and function tables

The 2 : 1 AUXIO+ and AUXIO– are controlled by three signals: AUXIO_EN, CA_DET and BIASIN.

Table 7. AUX MUX state

X = don't care.

| AUXIO_EN input | BIASIN input | DP_PD input | AUX MUX | State |
|----------------|--------------|-------------|---------|----------------|
| 0 | X | X | 3-state | sleep |
| 1 | 0 | 0 | ON | DP/DP++ |
| 1 | 0 | 1 | 3-state | sleep |
| 1 | 1 | 0 | 3-state | illegal |
| 1 | 1 | 1 | 3-state | 10 Gbit/s mode |

Table 8. AUX MUX function

| CA_DET input | AUXIO |
|--------------|-------|
| 0 | AUX |
| 1 | DDC |

6.3 Operation modes of both DPML MUX and AUX MUX

Table 9. DPML MUX function

| DP_PD input | DPMLO outputs |
|-------------|---------------|
| 0 | DP+ and DP– |
| 1 | LSRX and LSTX |

Table 10. Operation modes

X = don't care.

| AUXIO_EN | BIASIN | DP_PD | CA_DET | BIASOUT | AUXIO | DPMLO | State |
|----------|--------|-------|--------|---------|------------------------|----------|----------------|
| 0 | X | 0 | X | 0 | 3-state | DP input | sleep |
| 0 | X | 1 | X | 0 | 3-state | LS | sleep |
| 1 | 0 | 0 | 0 | 0 | AUX input | DP input | DP mode |
| 1 | 0 | 0 | 1 | 0 | DDC | DP input | DP++ mode |
| 1 | 0 | 1 | X | 0 | 3-state | LS | detect |
| 1 | 1 | 0 | X | 1 | 1 k Ω pull-down | DP input | illegal |
| 1 | 1 | 1 | X | 1 | 1 k Ω pull-down | LS | 10 Gbit/s mode |

7. Limiting values

Table 11. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------|---------------------------------|------------|----------|------|------|
| V_{DD} | supply voltage | | [1] -0.3 | +4.6 | V |
| V_I | input voltage | | [1] -0.3 | +5.5 | V |
| T_{stg} | storage temperature | | -65 | +150 | °C |
| V_{ESD} | electrostatic discharge voltage | HBM | [2] - | 2500 | V |
| | | CDM | [3] - | 1250 | V |

[1] All voltage values, except differential voltages, are with respect to network ground terminal.

[2] Human Body Model: ANSI/EOS/ESD-S5.1-1994, standard for ESD sensitivity testing, Human Body Model - Component level; Electrostatic Discharge Association, Rome, NY, USA.

[3] Charged Device Model: ANSI/EOS/ESD-S5.3-1-1999, standard for ESD sensitivity testing, Charged Device Model - Component level; Electrostatic Discharge Association, Rome, NY, USA.

8. Recommended operating conditions

Table 12. Operating conditions

Over operating free-air temperature range, unless specified otherwise.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------|---------------------|---|---------|-----|----------------|------|
| V_{DD} | supply voltage | 3.3 V supply option | 3.0 | 3.3 | 3.6 | V |
| | | initial supply voltage before power supply negotiation done | [1] 2.3 | - | - | V |
| V_I | input voltage | CMOS inputs | -0.3 | - | $V_{DD} + 0.3$ | V |
| | | MUX I/O pins | -0.3 | - | $V_{DD} + 0.3$ | V |
| T_{amb} | ambient temperature | operating in free air | 0 | - | 85 | °C |

[1] During power supply negotiation only a limited supply voltage is available. The control logic and multiplexers must be in full function with degraded performance. The channel between LSTX/LSRX and DPMLO+/DPMLO- must work. The initial R_{on} of DP MUX in [Table 15](#) should be < 50 Ω .

9. Characteristics

9.1 Device general characteristics

Table 13. General characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------|----------------------|---|-------|-----|-----|---------------|
| I_{DD} | supply current | $V_{DD} = 3.6\text{ V}$ with no load on BIASOUT | - | - | 2.8 | mA |
| P_{cons} | power consumption | $V_{DD} = 3.6\text{ V}$ with no load on BIASOUT | - | - | 10 | mW |
| | | Sleep mode; AUXIO_EN = 0 or (BIASIN = 0 and DP_PD = 1) | - | - | 3.5 | mW |
| $t_{startup}$ | start-up time | supply voltage valid to channel specified operating characteristics | - | - | 10 | ms |
| t_{rcfg} | reconfiguration time | DP_PD, AUXIO_EN, BIASIN or CA_DET state change to channel specified operating characteristics | [1] - | 2 | 4 | μs |

[1] Outputs are undefined during reconfiguration, including enable and disable time of the multiplexers.

9.2 AUX/DDC channel characteristics

Table 14. AUX/DDC channel characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------|----------------------------------|---|-----|------|-----------|---------------|
| DDIL | differential insertion loss | channel is OFF; $f = 5\text{ MHz}$ | - | -75 | - | dB |
| | | channel is ON; $f = 5\text{ MHz}$ | - | -0.5 | - | dB |
| DDRL | differential return loss | $f = 5\text{ MHz}$ | - | -19 | - | dB |
| DDNEXT | differential near-end crosstalk | adjacent channels are ON; $f = 5\text{ MHz}$ | - | -40 | - | dB |
| R_{on} | ON-state resistance | $V_{DD} = 3.3\text{ V}$; $V_I = 3.3\text{ V}$; $I_I = 20\text{ mA}$ | - | 7.5 | - | Ω |
| B_{-3dB} | -3 dB bandwidth | | - | 5 | - | GHz |
| t_{PD} | propagation delay | from DDC to AUXIO | - | 70 | - | ps |
| | | from AUX to AUXIO | - | 70 | - | ps |
| $t_{sk(dif)}$ | differential skew time | intra-pair | - | 5 | - | ps |
| V_I | input voltage | AUX+/AUX- and AUXIO+/AUXIO- | 0 | - | V_{DD} | V |
| V_{IC} | common-mode input voltage | AUX+/AUX- and AUXIO+/AUXIO- | 0 | - | V_{DD} | V |
| V_{ID} | differential input voltage | AUX+/AUX- and AUXIO+/AUXIO-; peak-to-peak value | - | - | 1.4 | V |
| I_{LIH} | HIGH-level input leakage current | $V_{DD} = \text{max.}$; $V_I = V_{DD}$ | - | - | ± 0.5 | μA |
| I_{LIL} | LOW-level input leakage current | $V_{DD} = \text{max.}$; $V_I = \text{GND}$ | - | - | ± 0.5 | μA |

9.3 DisplayPort Main Link (DPML) channel characteristics

Table 15. DPML channel characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------------|----------------------------------|---|------|------|-----------------------|------|
| DDIL | differential insertion loss | DP-DPMLO path; channel is OFF | | | | |
| | | f = 2.5 GHz | - | -20 | - | dB |
| | | f = 1.35 GHz | - | -26 | - | dB |
| | | DP-DPMLO path; channel is ON | | | | |
| | | f = 2.5 GHz | - | -2.0 | - | dB |
| | | f = 1.35 GHz | - | -1.0 | - | dB |
| | | f = 100 MHz | - | -0.5 | - | dB |
| | | LS-DPMLO path; channel is OFF | | | | |
| | | f = 2.5 GHz | - | -20 | - | dB |
| | | f = 1.35 GHz | - | -26 | - | dB |
| | | LS-DPMLO path; channel is ON | | | | |
| | | f = 2.5 GHz | - | -2.0 | - | dB |
| | | f = 1.35 GHz | - | -1.5 | - | dB |
| | | f = 100 MHz | - | -1.5 | - | dB |
| DDRL | differential return loss | DP-DPMLO path | | | | |
| | | f = 2.5 GHz | - | -15 | - | dB |
| | | f = 100 MHz | - | -24 | - | dB |
| | | LS-DPMLO path | | | | |
| | | f = 2.5 GHz | - | -14 | - | dB |
| DDNEXT | differential near-end crosstalk | adjacent channels are ON | | | | |
| | | f = 2.5 GHz | - | -25 | - | dB |
| | | f = 100 MHz | - | -60 | - | dB |
| R _{on} | ON-state resistance | V _{DD} = 3.3 V; V _I = 3.3 V; I _I = 10 mA | | | | |
| | | DP-DPMLO path | - | 9 | - | Ω |
| | | LS-DPMLO path | - | 13 | - | Ω |
| | | initial ON-state resistance before power supply negotiation done; V _{DD} = 2.3 V; V _I = 2.3 V; I _I = 10 mA | - | - | 50 | Ω |
| B _{-3dB} | -3 dB bandwidth | | - | 7.0 | - | GHz |
| t _{PD} | propagation delay | from DP+/DP- to DPMLO+/DPMLO- | - | 100 | - | ps |
| t _{sk(dif)} | differential skew time | intra-pair | - | 5 | - | ps |
| V _I | input voltage | LSTX/LSRX to DPMLO+/DPMLO- channel | -0.3 | - | V _{DD} + 0.6 | V |
| V _{IC} | common-mode input voltage | DP+/DP- and DPMLO+/DPMLO- | 0 | - | V _{DD} | V |
| V _{ID} | differential input voltage | DP+/DP- and DPMLO+/DPMLO- channel; peak-to-peak value | - | - | 1.4 | V |
| I _{LIH} | HIGH-level input leakage current | V _{DD} = max.; V _I = V _{DD} | - | - | ±0.5 | μA |
| I _{LIL} | LOW-level input leakage current | V _{DD} = max.; V _I = GND | - | - | ±0.5 | μA |

9.4 Control signals characteristics

Table 16. CA_DET input buffer characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------|--------------------------|--|---------------------|-----|---------------------|---------|
| V_{IH} | HIGH-level input voltage | | $0.7 \times V_{DD}$ | - | - | V |
| V_{IL} | LOW-level input voltage | | - | - | $0.3 \times V_{DD}$ | V |
| I_{LI} | input leakage current | measured with input at $V_{IH(max)}$ and $V_{IL(min)}$ | [1] - | - | 0.1 | μA |

[1] The leakage current on CA_DET pin must not drive the 1 M Ω pull-down to a HIGH level.

Table 17. HPD, BIASIN, DP_PD, AUXIO_EN input buffer characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------|--------------------------|--|---------------------|-----|---------------------|---------|
| V_{IH} | HIGH-level input voltage | CMOS inputs | $0.7 \times V_{DD}$ | - | - | V |
| V_{IL} | LOW-level input voltage | CMOS inputs | - | - | $0.3 \times V_{DD}$ | V |
| I_{LI} | input leakage current | measured with input at $V_{IH(max)}$ and $V_{IL(min)}$ | - | - | 1 | μA |

Table 18. BIASOUT output buffer characteristics

This buffer provides the power supply current for the PIN diode bias path and it drives six sets of bias resistors for the 10 Gbit/s signal paths.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------|-------------------|------------------------|-----|-----|-----|------|
| I_{pd} | pull-down current | $V_O = 0.4 V$ | 5 | - | - | mA |
| I_{pu} | pull-up current | $V_O = V_{DD} - 0.4 V$ | - | - | -9 | mA |
| t_{PD} | propagation delay | | - | 40 | 60 | ns |

Table 19. CA_DETOUT, HPDOUT output buffer characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------|-------------------|------------------------|-----|-----|-----|------|
| I_{pd} | pull-down current | $V_O = 0.4 V$ | 2 | - | - | mA |
| I_{pu} | pull-up current | $V_O = V_{DD} - 0.4 V$ | - | - | -2 | mA |
| t_{PD} | propagation delay | | - | 70 | 100 | ns |

Table 20. AUXIO+ and AUXIO- pins in 10 Gbit/s mode (AUXIO_EN = BIASIN = DP_PD = 1) characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------|--------------------------|--------------|----------|------|-----|------|
| V_{OL} | LOW-level output voltage | $I_O = 1 mA$ | [1] 0.72 | 0.90 | 1.1 | V |

[1] This V_{OL} is contributed from the 900 Ω pull-down resistors on these two pins.

10. Package outline

HVQFN24: plastic thermal enhanced very thin quad flat package; no leads;
 24 terminals; body 3 x 3 x 0.85 mm

SOT905-1

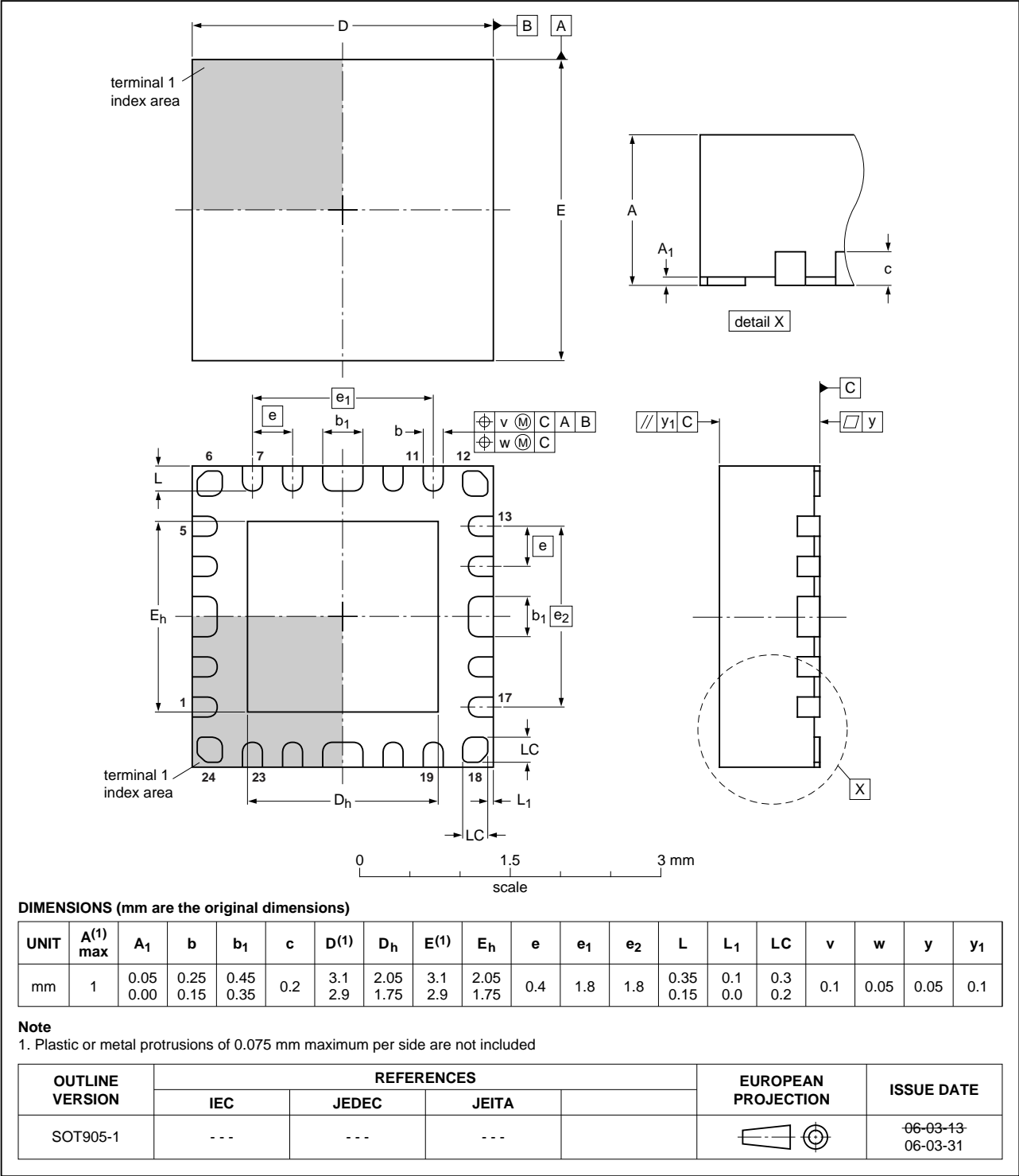


Fig 3. Package outline SOT905-1 (HVQFN24)

11. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

11.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

11.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

11.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

11.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 4](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 21](#) and [22](#)

Table 21. SnPb eutectic process (from J-STD-020D)

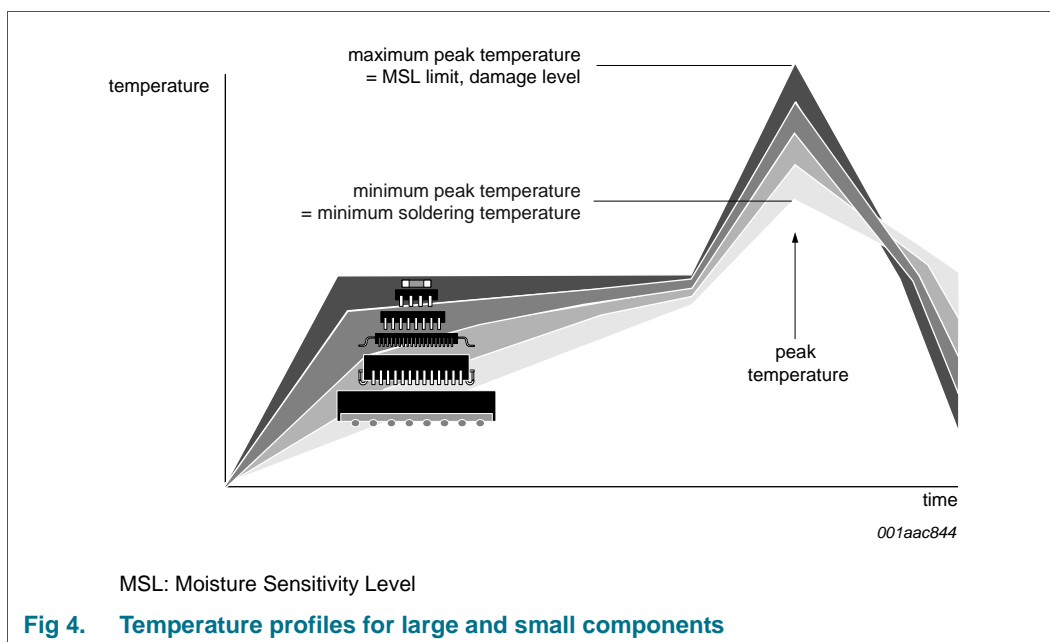
| Package thickness (mm) | Package reflow temperature (°C) | |
|------------------------|---------------------------------|-------|
| | Volume (mm ³) | |
| | < 350 | ≥ 350 |
| < 2.5 | 235 | 220 |
| ≥ 2.5 | 220 | 220 |

Table 22. Lead-free process (from J-STD-020D)

| Package thickness (mm) | Package reflow temperature (°C) | | |
|------------------------|---------------------------------|-------------|--------|
| | Volume (mm ³) | | |
| | < 350 | 350 to 2000 | > 2000 |
| < 1.6 | 260 | 260 | 260 |
| 1.6 to 2.5 | 260 | 250 | 245 |
| > 2.5 | 250 | 245 | 245 |

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 4](#).



For further information on temperature profiles, refer to Application Note *AN10365* “Surface mount reflow soldering description”.

12. Abbreviations

Table 23. Abbreviations

| Acronym | Description |
|---------|---|
| CDM | Charged-Device Model |
| CMOS | Complementary Metal-Oxide Semiconductor |
| DDC | Direct Display Control |
| DP | DisplayPort |
| DPML | DisplayPort Main Link |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| HBR2 | High Bit Rate 2 |
| ML | Main Link |
| MUX | Multiplexer |
| PIN | P-type, Intrinsic, N-type |

13. Revision history

Table 24. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|----------------|--|--------------------|---------------|---------------|
| CBTL05023 v.5 | 20130715 | Product data sheet | - | CBTL05023 v.4 |
| Modifications: | <ul style="list-style-type: none"> • Section 2.3 “General”, first bullet item: corrected term from “Hug Plug Detect” to “Hot Plug Detect” • Table 1 “Ordering information”: added column “Topside marking” • Added Section 3.1 “Ordering options” • De-activated hyper links in previous revision history | | | |
| CBTL05023 v.4 | 20121031 | Product data sheet | - | CBTL05023 v.3 |
| Modifications: | <ul style="list-style-type: none"> • Descriptive title of data sheet changed from “Multiplexer/demultiplexer switch chip” to “Multiplexer/demultiplexer switch for Thunderbolt applications” • Table 13 “AUX/DDC channel characteristics”: <ul style="list-style-type: none"> – I_{LH} Max value changed from “$\pm 5 \mu A$” to “$\pm 0.5 \mu A$” – I_{LL} Max value changed from “$\pm 5 \mu A$” to “$\pm 0.5 \mu A$” • Table 14 “DPML channel characteristics”: <ul style="list-style-type: none"> – I_{LH} Max value changed from “$\pm 5 \mu A$” to “$\pm 0.5 \mu A$” – I_{LL} Max value changed from “$\pm 5 \mu A$” to “$\pm 0.5 \mu A$” • Table 16 “HPD, BIASIN, DP_PD, AUXIO_EN input buffer characteristics”: <ul style="list-style-type: none"> – I_L Max value changed from “$10 \mu A$” to “$1 \mu A$” | | | |
| CBTL05023 v.3 | 20120621 | Product data sheet | - | CBTL05023 v.2 |
| Modifications: | <ul style="list-style-type: none"> • Table 2 “Pin description”, last row: “Type” for Pin “center pad” corrected from “power” to “ground” | | | |
| CBTL05023 v.2 | 20120515 | Product data sheet | - | CBTL05023 v.1 |
| Modifications: | <ul style="list-style-type: none"> • Section 2.2 “DP MUX 2 : 1 switch”, third bullet, ninth sub-bullet: changed from “–50 dB” to “–25 dB” • Section 2.3 “General”, fourth bullet: inserted “Patent-pending” • Table 14 “DPML channel characteristics”, DDNEXT characteristic: <ul style="list-style-type: none"> – Typ value for condition $f = 2.5 \text{ GHz}$ changed from “–50 dB” to “–25 dB” – Typ value for condition $f = 100 \text{ MHz}$ changed from “–65 dB” to “–60 dB” | | | |
| CBTL05023 v.1 | 20111104 | Product data sheet | - | - |

14. Legal information

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|-----------------------------------|-------------------------------|---|
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16. Contents

| | | |
|-----------|---|-----------|
| 1 | General description | 1 |
| 2 | Features and benefits | 1 |
| 2.1 | AUX MUX 2 : 1 switch | 1 |
| 2.2 | DP MUX 2 : 1 switch | 2 |
| 2.3 | General | 2 |
| 3 | Ordering information | 3 |
| 3.1 | Ordering options | 3 |
| 4 | Block diagram | 3 |
| 5 | Pinning information | 4 |
| 5.1 | Pinning | 4 |
| 5.2 | Pin description | 4 |
| 6 | Functional description | 6 |
| 6.1 | Buffer function tables | 6 |
| 6.2 | AUX MUX state and function tables | 6 |
| 6.3 | Operation modes of both DPML MUX and AUX MUX | 7 |
| 7 | Limiting values | 8 |
| 8 | Recommended operating conditions | 8 |
| 9 | Characteristics | 9 |
| 9.1 | Device general characteristics | 9 |
| 9.2 | AUX/DDC channel characteristics | 9 |
| 9.3 | DisplayPort Main Link (DPML) channel characteristics | 10 |
| 9.4 | Control signals characteristics | 11 |
| 10 | Package outline | 12 |
| 11 | Soldering of SMD packages | 13 |
| 11.1 | Introduction to soldering | 13 |
| 11.2 | Wave and reflow soldering | 13 |
| 11.3 | Wave soldering | 13 |
| 11.4 | Reflow soldering | 14 |
| 12 | Abbreviations | 15 |
| 13 | Revision history | 16 |
| 14 | Legal information | 17 |
| 14.1 | Data sheet status | 17 |
| 14.2 | Definitions | 17 |
| 14.3 | Disclaimers | 17 |
| 14.4 | Trademarks | 18 |
| 15 | Contact information | 18 |
| 16 | Contents | 19 |

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