# Kinetis KV30F 64 KB/128 KB Flash
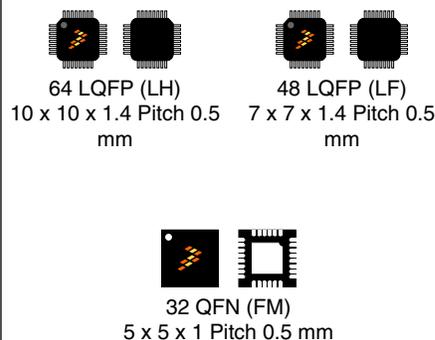
**100 MHz ARM® Cortex®-M4 Based Microcontroller with FPU**

The KV30 MCU family is a highly scalable member of the Kinetis V series and provides a high-performance, cost-competitive motor-control solution. Built on the ARM® Cortex®-M4 core running at 100 MHz, combined with floating point and DSP capability, it delivers a highly capable platform enabling customers to build a highly scalable solution portfolio. Additional features include:

- Dual 16-bit ADCs sampling at up to 1.2 MS/s in 12-bit mode
- Highly accurate and flexible motor control timers
- Excellent processing efficiency, 100 MHz ARM® Cortex®-M4-based device with Floating-Point Unit in a tiny form factor
- Enabled to support Kinetis Motor Suite (KMS), a bundled hardware and software solution that enables rapid configuration of BLDC and PMSM motor drive systems.

MKV30F128Vxx10
MKV30F64Vxx10
MKV30F128Vxx10P
MKV30F64Vxx10P

64 LQFP (LH)
10 x 10 x 1.4 Pitch 0.5 mm

48 LQFP (LF)
7 x 7 x 1.4 Pitch 0.5 mm

32 QFN (FM)
5 x 5 x 1 Pitch 0.5 mm

**Performance**
- 100 MHz ARM Cortex-M4 core with DSP instructions delivering 1.25 Dhrystone MIPS per MHz

**Memories and memory interfaces**
- Up to 128 KB of embedded flash and 16 KB of RAM
- Preprogrammed Kinetis flashloader for one-time, in-system factory programming

**System peripherals**
- 4-channel DMA controller
- Independent External and Software Watchdog monitor

**Clocks**
- Crystal oscillator: 32-40 kHz or 3-32 MHz
- Three internal oscillators: 32 kHz, 4 MHz, and 48 MHz
- Multi-purpose clock generator with FLL

**Security and integrity modules**
- Hardware CRC module
- 128-bit unique identification (ID) number per chip
- Flash access control to protect proprietary software

**Human-machine interface**
- Up to 46 general-purpose I/O (GPIO)

**Analog modules**
- Two 16-bit SAR ADCs (1.2 MS/s in 12bit mode)
- One 12-bit DAC
- Two analog comparators (CMP) with 6- bit DAC
- Accurate internal voltage reference (not available in 32-pin QFN package)

**Communication interfaces**
- One SPI module
- Two UART modules
- One I2C: Support for up to 1 Mbps operation

**Timers**
- One 6-channel motor-control general-purpose/PWM timer
- Two 2-channel motor-control general-purpose timers with quadrature decoder functionality

**Operating Characteristics**
- Voltage range (including flash writes): 1.71 to 3.6 V
- Temperature range (ambient): -40 to 105°C

**Kinetis Motor Suite**
- Supports Velocity and Position control of BLDC & PMSM motors

- Implements Field Orient Control (FOC) using Back EMF to improve motor efficiency
- Utilizes SpinTAC control theory that improves overall system performance and reliability

## Ordering Information

| Part Number | Memory | | Number of GPIOs |
| --- | --- | --- | --- |
| | Flash (KB) | SRAM (KB) | |
| MKV30F128VLH10 | 128 | 16 | 46 |
| MKV30F128VLF10 | 128 | 16 | 35 |
| MKV30F128VFM10 | 128 | 16 | 26 |
| MKV30F64VLH10 | 64 | 16 | 46 |
| MKV30F64VLF10 | 64 | 16 | 35 |
| MKV30F64VFM10 | 64 | 16 | 26 |
| MKV30F128VLF10P | 120 | 16 | 35 |
| MKV30F64VLH10P[1] | 56 | 16 | 46 |
| MKV30F64VLF10P[1] | 56 | 16 | 35 |

1. This part number is subject to removal

## Related Resources

| Type | Description | Resource |
| --- | --- | --- |
| Selector Guide | The Freescale Solution Advisor is a web-based tool that features interactive application wizards and a dynamic product selector. | Product Selector |
| Product Brief | The Product Brief contains concise overview/summary information to enable quick evaluation of a device for design suitability. | KV30FKV31FPB |
| Reference Manual | The Reference Manual contains a comprehensive description of the structure and function (operation) of a device. | KV30P64M100SFARM |
| Data Sheet | The Data Sheet includes electrical characteristics and signal connections. | This document. |
| KMS User Guide | The KMS User Guide provides a comprehensive description of the features and functions of the Kinetis Motor Suite solution. | Kinetis Motor Suite User's Guide (KMS100UG)[1] |
| KMS API Reference Manual | The KMS API reference manual provides a comprehensive description of the API of the Kinetis Motor Suite function blocks. | Kinetis Motor Suite API Reference Manual (KMS100RM)[1] |
| Chip Errata | The chip mask set Errata provides additional or corrective information for a particular device mask set. | Kinetis_V_0N36M |
| Package drawing | Package dimensions are provided by the part number:<br>• MKV30F64VLF10P<br>• MKV30F64VLH10P<br>• MKV30F128VLH10<br>• MKV30F128VLF10<br>• MKV30F128VFM10<br>• MKV30F128VLF10P | • 98ASH00962A<br>• 98ASS23234W<br>• 98ASS23234W<br>• 98ASH00962A<br>• 98ARE10566D<br>• 98ASH00962A |

1. To find the associated resource, go to freescale.com and perform a search using Document ID
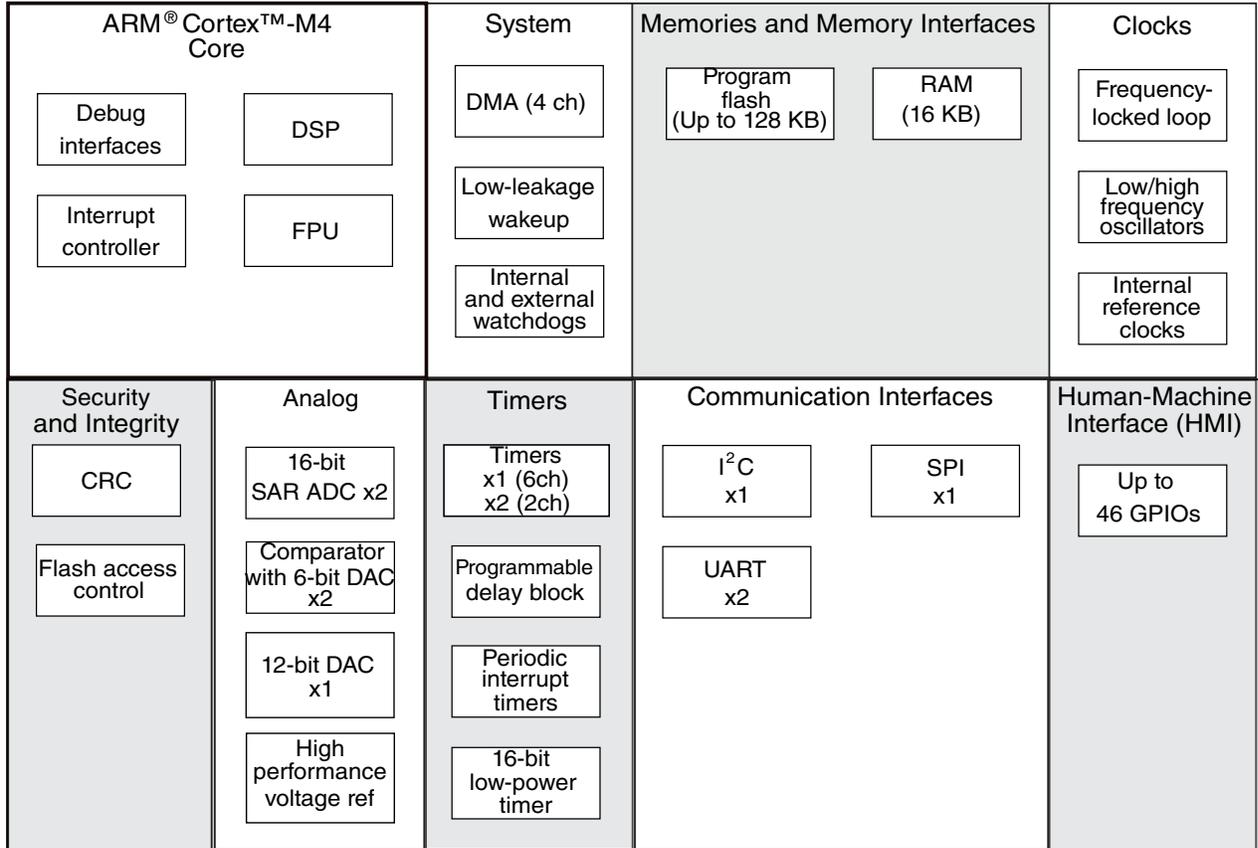
Figure 1 shows the functional modules in the chip.

| ARM® Cortex™-M4 Core | System | Memories and Memory Interfaces | Clocks |
|---|---|---|---|
| Debug interfaces · DSP · Interrupt controller · FPU | DMA (4 ch) · Low-leakage wakeup · Internal and external watchdogs | Program flash (Up to 128 KB) · RAM (16 KB) | Frequency-locked loop · Low/high frequency oscillators · Internal reference clocks |

| Security and Integrity | Analog | Timers | Communication Interfaces | Human-Machine Interface (HMI) |
|---|---|---|---|---|
| CRC · Flash access control | 16-bit SAR ADC x2 · Comparator with 6-bit DAC x2 · 12-bit DAC x1 · High performance voltage ref | Timers x1 (6ch) x2 (2ch) · Programmable delay block · Periodic interrupt timers · 16-bit low-power timer | I²C x1 · SPI x1 · UART x2 | Up to 46 GPIOs |

**Figure 1. Functional block diagram**

# Table of Contents

# 1  Ratings

## 1.1  Thermal handling ratings

| Symbol | Description | Min. | Max. | Unit | Notes |
|--------|-------------|------|------|------|-------|
| $T_{STG}$ | Storage temperature | −55 | 150 | °C | 1 |
| $T_{SDR}$ | Solder temperature, lead-free | — | 260 | °C | 2 |

1.  Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2.  Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

## 1.2  Moisture handling ratings

| Symbol | Description | Min. | Max. | Unit | Notes |
|--------|-------------|------|------|------|-------|
| MSL | Moisture sensitivity level | — | 3 | — | 1 |

1.  Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

## 1.3  ESD handling ratings

| Symbol | Description | Min. | Max. | Unit | Notes |
|--------|-------------|------|------|------|-------|
| $V_{HBM}$ | Electrostatic discharge voltage, human body model | -2000 | +2000 | V | 1 |
| $V_{CDM}$ | Electrostatic discharge voltage, charged-device model | -500 | +500 | V | 2 |
| $I_{LAT}$ | Latch-up current at ambient temperature of 105°C | -100 | +100 | mA | 3 |

1.  Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2.  Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3.  Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

## 1.4  Voltage and current operating ratings

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{DD}$ | Digital supply voltage | −0.3 | 3.8 | V |
| $I_{DD}$ | Digital supply current | — | 145 | mA |
| $V_{DIO}$ | Digital input voltage | −0.3 | $V_{DD} + 0.3$ | V |
| $V_{AIO}$ | Analog[1] | −0.3 | $V_{DD} + 0.3$ | V |
| $I_D$ | Maximum current single pin limit (applies to all digital pins) | −25 | 25 | mA |
| $V_{DDA}$ | Analog supply voltage | $V_{DD} - 0.3$ | $V_{DD} + 0.3$ | V |

1. Analog pins are defined as pins that do not have an associated general purpose I/O port function.

# 2  General

## 2.1  AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.
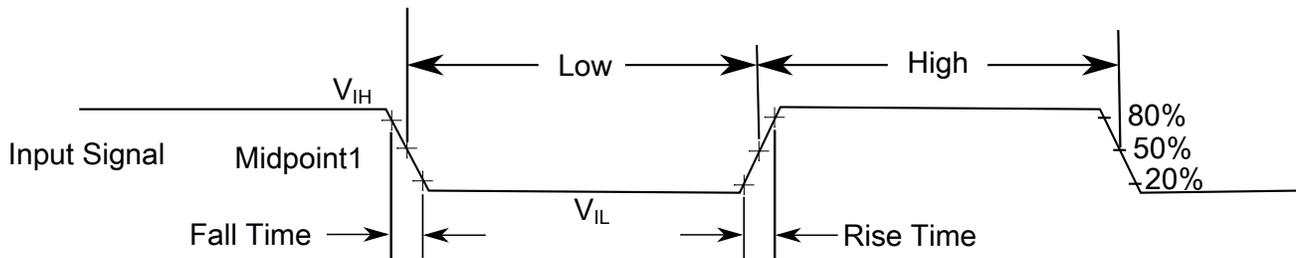


The midpoint is $V_{IL} + (V_{IH} - V_{IL}) / 2$

**Figure 2. Input signal measurement reference**

## 2.2  Nonswitching electrical specifications

### 2.2.1  Voltage and current operating requirements

**Table 1.  Voltage and current operating requirements**

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | 1.71 | 3.6 | V | |

*Table continues on the next page...*

**Table 1. Voltage and current operating requirements (continued)**

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $V_{DDA}$ | Analog supply voltage | 1.71 | 3.6 | V | |
| $V_{DD} - V_{DDA}$ | $V_{DD}$-to-$V_{DDA}$ differential voltage | −0.1 | 0.1 | V | |
| $V_{SS} - V_{SSA}$ | $V_{SS}$-to-$V_{SSA}$ differential voltage | −0.1 | 0.1 | V | |
| $V_{IH}$ | Input high voltage | $0.7 \times V_{DD}$ | — | V | |
| | • 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | $0.75 \times V_{DD}$ | — | V | |
| | • 1.7 V ≤ $V_{DD}$ ≤ 2.7 V | | | | |
| $V_{IL}$ | Input low voltage | — | $0.35 \times V_{DD}$ | V | |
| | • 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | — | $0.3 \times V_{DD}$ | V | |
| | • 1.7 V ≤ $V_{DD}$ ≤ 2.7 V | | | | |
| $V_{HYS}$ | Input hysteresis | $0.06 \times V_{DD}$ | — | V | |
| $I_{ICIO}$ | Analog and I/O pin DC injection current — single pin | | | | 1 |
| | • $V_{IN}$ < $V_{SS}$-0.3V (Negative current injection) | -3 | — | mA | |
| $I_{ICcont}$ | Contiguous pin DC injection current —regional limit, includes sum of negative injection currents or sum of positive injection currents of 16 contiguous pins | | | | |
| | • Negative current injection | -25 | — | mA | |
| $V_{ODPU}$ | Open drain pullup voltage level | $V_{DD}$ | $V_{DD}$ | V | 2 |
| $V_{RAM}$ | $V_{DD}$ voltage required to retain RAM | 1.2 | — | V | |

1. All analog and I/O pins are internally clamped to $V_{SS}$ through ESD protection diodes. If $V_{IN}$ is less than $V_{IO\_MIN}$ or greater than $V_{IO\_MAX}$, a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as $R=(V_{IO\_MIN}-V_{IN})/|I_{ICIO}|$.
2. Open drain outputs must be pulled to VDD.

## 2.2.2 LVD and POR operating requirements

**Table 2. $V_{DD}$ supply LVD and POR operating requirements**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $V_{POR}$ | Falling VDD POR detect voltage | 0.8 | 1.1 | 1.5 | V | |
| $V_{LVDH}$ | Falling low-voltage detect threshold — high range (LVDV=01) | 2.48 | 2.56 | 2.64 | V | |
| | Low-voltage warning thresholds — high range | | | | | 1 |
| $V_{LVW1H}$ | • Level 1 falling (LVWV=00) | 2.62 | 2.70 | 2.78 | V | |
| $V_{LVW2H}$ | • Level 2 falling (LVWV=01) | 2.72 | 2.80 | 2.88 | V | |
| $V_{LVW3H}$ | • Level 3 falling (LVWV=10) | 2.82 | 2.90 | 2.98 | V | |
| $V_{LVW4H}$ | • Level 4 falling (LVWV=11) | 2.92 | 3.00 | 3.08 | V | |

*Table continues on the next page...*

### Table 2. V$_{DD}$ supply LVD and POR operating requirements (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| V$_{HYSH}$ | Low-voltage inhibit reset/recover hysteresis — high range | — | 80 | — | mV | |
| V$_{LVDL}$ | Falling low-voltage detect threshold — low range (LVDV=00) | 1.54 | 1.60 | 1.66 | V | |
| | Low-voltage warning thresholds — low range | | | | | 1 |
| V$_{LVW1L}$ | • Level 1 falling (LVWV=00) | 1.74 | 1.80 | 1.86 | V | |
| V$_{LVW2L}$ | • Level 2 falling (LVWV=01) | 1.84 | 1.90 | 1.96 | V | |
| V$_{LVW3L}$ | • Level 3 falling (LVWV=10) | 1.94 | 2.00 | 2.06 | V | |
| V$_{LVW4L}$ | • Level 4 falling (LVWV=11) | 2.04 | 2.10 | 2.16 | V | |
| V$_{HYSL}$ | Low-voltage inhibit reset/recover hysteresis — low range | — | 60 | — | mV | |
| V$_{BG}$ | Bandgap voltage reference | 0.97 | 1.00 | 1.03 | V | |
| t$_{LPO}$ | Internal low power oscillator period — factory trimmed | 900 | 1000 | 1100 | µs | |

1. Rising threshold is the sum of falling threshold and hysteresis voltage

## 2.2.3 Voltage and current operating behaviors

### Table 3. Voltage and current operating behaviors

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| V$_{OH}$ | Output high voltage — Normal drive pad except RESET_B | | | | | |
| | 2.7 V ≤ V$_{DD}$ ≤ 3.6 V, I$_{OH}$ = -5 mA | V$_{DD}$ – 0.5 | — | — | V | 1 |
| | 1.71 V ≤ V$_{DD}$ ≤ 2.7 V, I$_{OH}$ = -2.5 mA | V$_{DD}$ – 0.5 | — | — | V | |
| V$_{OH}$ | Output high voltage — High drive pad except RESET_B | | | | | |
| | 2.7 V ≤ V$_{DD}$ ≤ 3.6 V, I$_{OH}$ = -20 mA | V$_{DD}$ – 0.5 | — | — | V | 1 |
| | 1.71 V ≤ V$_{DD}$ ≤ 2.7 V, I$_{OH}$ = -10 mA | V$_{DD}$ – 0.5 | — | — | V | |
| I$_{OHT}$ | Output high current total for all ports | — | — | 100 | mA | |
| V$_{OL}$ | Output low voltage — Normal drive pad except RESET_B | | | | | |
| | 2.7 V ≤ V$_{DD}$ ≤ 3.6 V, I$_{OL}$ = 5 mA | — | — | 0.5 | V | 1 |
| | 1.71 V ≤ V$_{DD}$ ≤ 2.7 V, I$_{OL}$ = 2.5 mA | — | — | 0.5 | V | |
| V$_{OL}$ | Output low voltage — High drive pad except RESET_B | | | | | |
| | 2.7 V ≤ V$_{DD}$ ≤ 3.6 V, I$_{OL}$ = 20 mA | — | — | 0.5 | V | 1 |
| | 1.71 V ≤ V$_{DD}$ ≤ 2.7 V, I$_{OL}$ = 10 mA | — | — | 0.5 | V | |
| V$_{OL}$ | Output low voltage — RESET_B | | | | | |

*Table continues on the next page...*

**Table 3. Voltage and current operating behaviors (continued)**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|--------|-------------|------|------|------|------|-------|
| | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, $I_{OL}$ = 3 mA | — | — | 0.5 | V | |
| | 1.71 V ≤ $V_{DD}$ ≤ 2.7 V, $I_{OL}$ = 1.5 mA | — | — | 0.5 | V | |
| $I_{OLT}$ | Output low current total for all ports | — | — | 100 | mA | |
| $I_{IN}$ | Input leakage current (per pin) for full temperature range | | | | | |
| | All pins other than high drive port pins | — | 0.002 | 0.5 | µA | 1, 2 |
| | High drive port pins | — | 0.004 | 0.5 | µA | |
| $I_{IN}$ | Input leakage current (total all pins) for full temperature range | — | — | 1.0 | µA | 2 |
| $R_{PU}$ | Internal pullup resistors | 20 | — | 50 | kΩ | 3 |
| $R_{PD}$ | Internal pulldown resistors | 20 | — | 50 | kΩ | 4 |

1. PTB0, PTB1, PTC3, PTC4, PTD4, PTD5, PTD6, and PTD7 I/O have both high drive and normal drive capability selected by the associated PTx_PCRn[DSE] control bit. All other GPIOs are normal drive only.
2. Measured at VDD=3.6V
3. Measured at $V_{DD}$ supply voltage = $V_{DD}$ min and Vinput = $V_{SS}$
4. Measured at $V_{DD}$ supply voltage = $V_{DD}$ min and Vinput = $V_{DD}$

## 2.2.4  Power mode transition operating behaviors

All specifications except $t_{POR}$, and VLLSx→RUN recovery times in the following table assume this clock configuration:

- CPU and system clocks = 72 MHz
- Bus clock = 36 MHz
- Flash clock = 24 MHz
- MCG mode: FEI

**Table 4. Power mode transition operating behaviors**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|--------|-------------|------|------|------|------|-------|
| $t_{POR}$ | After a POR event, amount of time from the point $V_{DD}$ reaches 1.71 V to execution of the first instruction across the operating temperature range of the chip. | — | — | 300 | µs | 1 |
| | • VLLS0 → RUN | — | — | 135 | µs | |
| | • VLLS1 → RUN | — | — | 135 | µs | |
| | • VLLS2 → RUN | — | — | 75 | µs | |

*Table continues on the next page...*

**Table 4. Power mode transition operating behaviors (continued)**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| | • VLLS3 → RUN | — | — | 75 | µs | |
| | • VLPS → RUN | — | — | 5.7 | µs | |
| | • STOP → RUN | — | — | 5.7 | µs | |

1. Normal boot (FTFA_OPT[LPBOOT]=1)

## 2.2.5 Power consumption operating behaviors

The current parameters in the table below are derived from code executing a while(1) loop from flash, unless otherwise noted.

The IDD typical values represent the statistical mean at 25°C, and the IDD maximum values for RUN, WAIT, VLPR, and VLPW represent data collected at 125°C junction temperature unless otherwise noted. The maximum values represent characterized results equivalent to the mean plus three times the standard deviation (mean + 3 sigma).

**Table 5. Power consumption operating behaviors**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $I_{DDA}$ | Analog supply current | — | — | See note | mA | 1 |
| $I_{DD\_HSRUN}$ | High Speed Run mode current - all peripheral clocks disabled, CoreMark benchmark code executing from flash | | | | | |
| | @ 1.8V | — | 18.70 | 19.37 | mA | 2, 3, 4 |
| | @ 3.0V | — | 18.71 | 19.38 | mA | |
| $I_{DD\_HSRUN}$ | High Speed Run mode current - all peripheral clocks disabled, code executing from flash | | | | | |
| | @ 1.8V | — | 18.13 | 18.80 | mA | 4 |
| | @ 3.0V | — | 18.19 | 18.86 | mA | |
| $I_{DD\_HSRUN}$ | High Speed Run mode current — all peripheral clocks enabled, code executing from flash | | | | | |
| | @ 1.8V | — | 22.2 | 22.87 | mA | 5 |
| | @ 3.0V | — | 22.4 | 23.07 | mA | |
| $I_{DD\_RUN}$ | Run mode current in Compute operation — CoreMark benchmark code executing from flash | | | | | |
| | @ 1.8V | — | 12.74 | 13.41 | mA | 2, 3, 6 |
| | @ 3.0V | — | 12.82 | 13.49 | mA | |

*Table continues on the next page...*

## Table 5.  Power consumption operating behaviors (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| I$_{DD\_RUN}$ | Run mode current in Compute operation — code executing from flash | | | | | 6 |
| | @ 1.8V | — | 12.10 | 13.10 | mA | |
| | @ 3.0V | — | 12.20 | 13.37 | mA | |
| I$_{DD\_RUN}$ | Run mode current — all peripheral clocks disabled, code executing from flash | | | | | 7 |
| | @ 1.8V | — | 12.8 | 13.47 | mA | |
| | @ 3.0V | — | 12.9 | 13.57 | mA | |
| I$_{DD\_RUN}$ | Run mode current — all peripheral clocks enabled, code executing from flash | | | | | 8 |
| | @ 1.8V | — | 14.8 | 15.47 | mA | |
| | @ 3.0V | | | | | |
| | • @ 25°C | — | 14.9 | 15.57 | mA | |
| | • @ 70°C | — | 14.9 | 15.57 | mA | |
| | • @ 85°C | — | 14.9 | 15.57 | mA | |
| | • @ 105°C | — | 15.5 | 16.20 | mA | |
| I$_{DD\_RUN}$ | Run mode current — Compute operation, code executing from flash | | | | | 9 |
| | @ 1.8V | — | 12.1 | 12.77 | mA | |
| | @ 3.0V | | | | | |
| | • @ 25°C | — | 12.2 | 12.87 | mA | |
| | • @ 70°C | — | 12.2 | 12.87 | mA | |
| | • @ 85°C | — | 12.2 | 12.87 | mA | |
| | • @ 105°C | — | 12.7 | 13.37 | mA | |
| I$_{DD\_WAIT}$ | Wait mode high frequency current at 3.0 V — all peripheral clocks disabled | — | 5.5 | 6.17 | mA | 7 |
| I$_{DD\_WAIT}$ | Wait mode reduced frequency current at 3.0 V — all peripheral clocks disabled | — | 3.5 | 4.17 | mA | 10 |
| I$_{DD\_VLPR}$ | Very-low-power run mode current in Compute operation — CoreMark benchmark code executing from flash | | | | | 2, 11, 3 |
| | @ 1.8V | — | 0.58 | 0.86 | mA | |
| | @ 3.0V | — | 0.59 | 0.87 | mA | |
| I$_{DD\_VLPR}$ | Very-low-power run mode current in Compute operation, code executing from flash | | | | | 11 |
| | @ 1.8V | — | 0.47 | 0.75 | mA | |
| | @ 3.0V | — | 0.47 | 0.75 | mA | |
| I$_{DD\_VLPR}$ | Very-low-power run mode current at 3.0 V — all peripheral clocks disabled | — | 0.62 | 0.90 | mA | 12 |

*Table continues on the next page...*

## Table 5.  Power consumption operating behaviors (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $I_{DD\_VLPR}$ | Very-low-power run mode current at 3.0 V — all peripheral clocks enabled | — | 0.76 | 1.04 | mA | 13 |
| $I_{DD\_VLPW}$ | Very-low-power wait mode current at 3.0 V — all peripheral clocks disabled | — | 0.28 | 0.56 | mA | 14 |
| $I_{DD\_STOP}$ | Stop mode current at 3.0 V | | | | | |
| | @ -40°C to 25°C | — | 0.26 | 0.33 | mA | |
| | @ 70°C | — | 0.30 | 0.47 | mA | |
| | @ 85°C | — | 0.35 | 0.52 | mA | |
| | @ 105°C | — | 0.43 | 0.60 | mA | |
| $I_{DD\_VLPS}$ | Very-low-power stop mode current at 3.0 V | | | | | |
| | @ -40°C to 25°C | — | 2.80 | 8.30 | µA | |
| | @ 70°C | — | 13.30 | 29.90 | µA | |
| | @ 85°C | — | 26.90 | 46.45 | µA | |
| | @ 105°C | — | 56.80 | 67.05 | µA | |
| $I_{DD\_VLLS3}$ | Very low-leakage stop mode 3 current at 3.0 V | | | | | |
| | @ -40°C to 25°C | — | 1.3 | 1.71 | µA | |
| | @ 70°C | — | 3.8 | 5.35 | µA | |
| | @ 85°C | — | 7.6 | 8.50 | µA | |
| | @ 105°C | — | 15.1 | 19.05 | µA | |
| $I_{DD\_VLLS2}$ | Very low-leakage stop mode 2 current at 3.0 V | | | | | |
| | @ -40°C to 25°C | — | 1.3 | 1.55 | µA | |
| | @ 70°C | — | 3.1 | 4.05 | µA | |
| | @ 85°C | — | 7.2 | 8.60 | µA | |
| | @ 105°C | — | 12.0 | 14.10 | µA | |
| $I_{DD\_VLLS1}$ | Very low-leakage stop mode 1 current at 3.0 V | | | | | |
| | @ -40°C to 25°C | — | 0.63 | 0.87 | µA | |
| | @ 70°C | — | 1.70 | 2.35 | µA | |
| | @ 85°C | — | 2.8 | 3.40 | µA | |
| | @ 105°C | — | 7.6 | 8.80 | µA | |
| $I_{DD\_VLLS0}$ | Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit enabled | | | | | |
| | @ -40°C to 25°C | — | 0.35 | 0.46 | µA | |
| | @ 70°C | — | 1.38 | 1.94 | µA | |
| | @ 85°C | — | 2.4 | 2.95 | µA | |
| | @ 105°C | — | 7.3 | 8.45 | µA | |
| $I_{DD\_VLLS0}$ | Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit disabled | | | | | |
| | @ -40°C to 25°C | — | 0.07 | 0.16 | µA | |
| | @ 70°C | — | 1.05 | 1.78 | µA | |
| | @ 85°C | — | 2.1 | 2.80 | µA | |

*Table continues on the next page...*

## Table 5. Power consumption operating behaviors (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|--------|-------------|------|------|------|------|-------|
|        | @ 105°C     | —    | 6.9  | 8.25 | µA   |       |

1. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
2. Cache on and prefetch on, low compiler optimization
3. CoreMark benchmark compiled using IAR 7.2 with optimization level low
4. 100 MHz core and system clock, 50 MHz bus clock, and 25 MHz flash clock. MCG configured for FEE mode. All peripheral clocks disabled.
5. 100 MHz core and system clock, 50 MHz bus clock, and 25 MHz flash clock. MCG configured for FEI mode. All peripheral clocks enabled.
6. 72 MHz core and system clock, 36 MHz bus clock and 24 MHz flash clock. MCG configured for FEE mode. All peripheral clocks disabled. Compute operation.
7. 72 MHz core and system clock, 36 MHz bus clock, and 24 MHz flash clock. MCG configured for FEI mode. All peripheral clocks disabled.
8. 72 MHz core and system clock, 36 MHz bus clock, and 24 MHz flash clock. MCG configured for FEI mode. All peripheral clocks enabled.
9. 72MHz core and system clock, 36MHz bus clock, and 24MHz flash clock. MCG configured for FEI mode. Compute operation.
10. 25 MHz core and system clock, 25 MHz bus clock, and 25 MHz flash clock. MCG configured for FEI mode.
11. 4 MHz core, system, and bus clock, and 1 MHz flash clock. MCG configured for BLPE mode. Compute operation. Code executing from flash.
12. 4 MHz core, system, and bus clock, and 1 MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled. Code executing from flash.
13. 4 MHz core, system, and bus clock, and 1 MHz flash clock. MCG configured for BLPE mode. All peripheral clocks enabled, but peripherals are not in active operation. Code executing from flash.
14. 4 MHz core, system, and bus clock, and 1 MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled.

## Table 6. Low power mode peripheral adders—typical value

| Symbol | Description | Temperature (°C) | | | | | | Unit |
|--------|-------------|-----|-----|-----|-----|-----|-----|------|
|        |             | -40 | 25  | 50  | 70  | 85  | 105 |      |
| $I_{IREFSTEN4MHz}$ | 4 MHz internal reference clock (IRC) adder. Measured by entering STOP or VLPS mode with 4 MHz IRC enabled. | 56 | 56 | 56 | 56 | 56 | 56 | µA |
| $I_{IREFSTEN32KHz}$ | 32 kHz internal reference clock (IRC) adder. Measured by entering STOP mode with the 32 kHz IRC enabled. | 52 | 52 | 52 | 52 | 52 | 52 | µA |
| $I_{EREFSTEN4MHz}$ | External 4 MHz crystal clock adder. Measured by entering STOP or VLPS mode with the crystal enabled. | 206 | 228 | 237 | 245 | 251 | 258 | uA |
| $I_{EREFSTEN32KHz}$ | External 32 kHz crystal clock adder by means of the OSC0_CR[EREFSTEN and EREFSTEN] bits. Measured by entering all modes with the crystal enabled. | | | | | | | |
| | VLLS1 | 440 | 490 | 540 | 560 | 570 | 580 | nA |
| | VLLS3 | 440 | 490 | 540 | 560 | 570 | 580 | |
| | LLS | 490 | 490 | 540 | 560 | 570 | 680 | |

*Table continues on the next page...*

**Table 6.  Low power mode peripheral adders—typical value (continued)**

| Symbol | Description | Temperature (°C) | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | -40 | 25 | 50 | 70 | 85 | 105 | |
| | VLPS | 510 | 560 | 560 | 560 | 610 | 680 | |
| | STOP | 510 | 560 | 560 | 560 | 610 | 680 | |
| $I_{48MIRC}$ | 48 Mhz internal reference clock | 350 | 350 | 350 | 350 | 350 | 350 | µA |
| $I_{CMP}$ | CMP peripheral adder measured by placing the device in VLLS1 mode with CMP enabled using the 6-bit DAC and a single external input for compare. Includes 6-bit DAC power consumption. | 22 | 22 | 22 | 22 | 22 | 22 | µA |
| $I_{UART}$ | UART peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source waiting for RX data at 115200 baud rate. Includes selected clock source power consumption. | | | | | | | |
| | MCGIRCLK (4 MHz internal reference clock) | 66 | 66 | 66 | 66 | 66 | 66 | µA |
| | >OSCERCLK (4 MHz external crystal) | 214 | 237 | 246 | 254 | 260 | 268 | |
| $I_{BG}$ | Bandgap adder when BGEN bit is set and device is placed in VLPx, LLS, or VLLSx mode. | 45 | 45 | 45 | 45 | 45 | 45 | µA |
| $I_{ADC}$ | ADC peripheral adder combining the measured values at $V_{DD}$ and $V_{DDA}$ by placing the device in STOP or VLPS mode. ADC is configured for low power mode using the internal clock and continuous conversions. | 42 | 42 | 42 | 42 | 42 | 42 | µA |

## 2.2.5.1  Diagram: Typical IDD_RUN operating behavior

The following data was measured under these conditions:

- MCG in FBE mode for 50 MHz and lower frequencies. MCG in FEE mode at frequencies between 50 MHz and 100MHz.
- No GPIOs toggled
- Code execution from flash with cache enabled
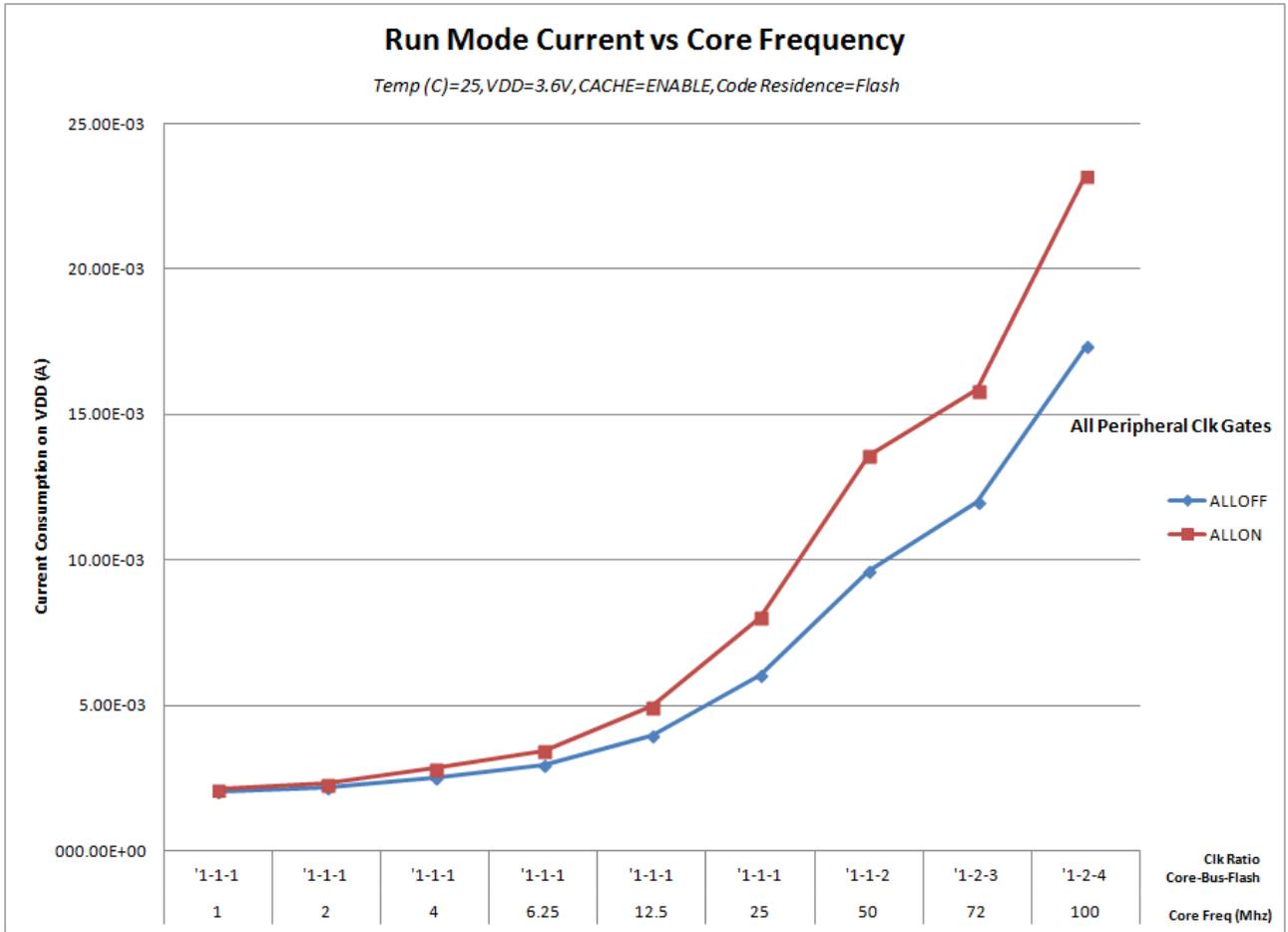- For the ALLOFF curve, all peripheral clocks are disabled except FTFA
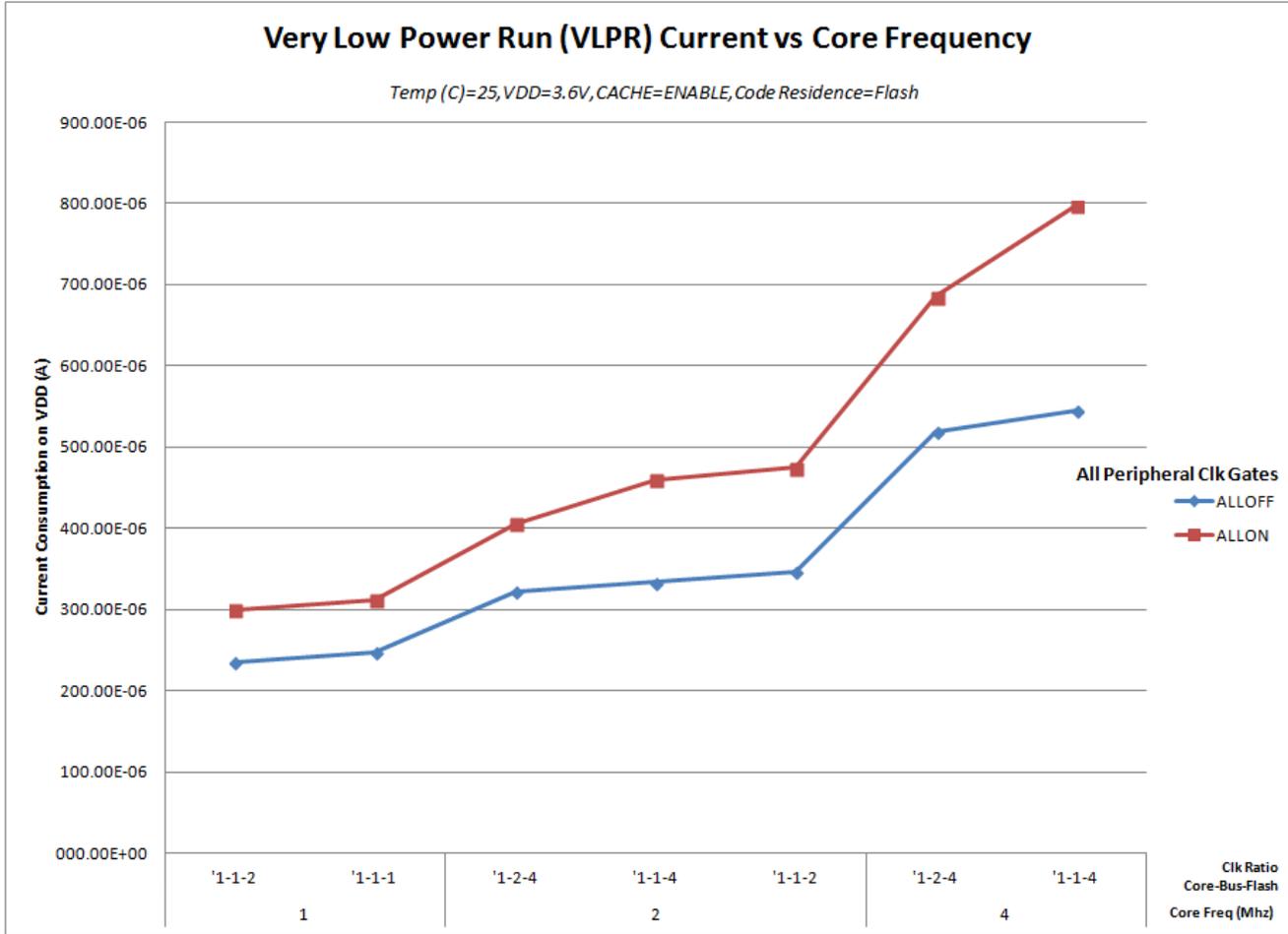
**Figure 3. Run mode supply current vs. core frequency**

**Figure 4. VLPR mode supply current vs. core frequency**

## 2.2.6   EMC radiated emissions operating behaviors

### Table 7.   EMC radiated emissions operating behaviors for 64 LQFP package

| Parameter | Conditions | Clocks | Frequency range | Level (Typ.) | Unit | Notes |
|---|---|---|---|---|---|---|
| $V_{EME}$ | Device configuration, test conditions and EM testing per standard IEC 61967-2.<br><br>Supply voltage: VDD = 3.3 V<br><br>Temp = 25°C | FSYS = 100 MHz<br><br>FBUS = 50 MHz<br><br>External crystal = 10 MHz | 150 kHz–50 MHz | 11 | dBuV | 1, 2, 3 |
| | | | 50 MHz–150 MHz | 12 | | |
| | | | 150 MHz–500 MHz | 11 | | |
| | | | 500 MHz–1000 MHz | 8 | | |
| | | | IEC level | N | | 4 |

1. Measurements were made per IEC 61967-2 while the device was running typical application code.
2. Measurements were performed on the 64LQFP device, MKV30F128VLH10.
3. The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.

4.  IEC Level Maximums: N ≤ 12dBmV, M ≤ 18dBmV, L ≤ 24dBmV, K ≤ 30dBmV, I ≤ 36dBmV .

## 2.2.7  Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:
1.  Go to www.freescale.com.
2.  Perform a keyword search for "EMC design."

## 2.2.8  Capacitance attributes

**Table 8.  Capacitance attributes**

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $C_{IN\_A}$ | Input capacitance: analog pins | — | 7 | pF |
| $C_{IN\_D}$ | Input capacitance: digital pins | — | 7 | pF |

## 2.3  Switching specifications

## 2.3.1  Device clock specifications

**Table 9.  Device clock specifications**

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| High Speed run mode | | | | | |
| $f_{SYS}$ | System and core clock | — | 100 | MHz | |
| $f_{BUS}$ | Bus clock | — | 50 | MHz | |
| Normal run mode (and High Speed run mode unless otherwise specified above) | | | | | |
| $f_{SYS}$ | System and core clock | — | 72 | MHz | |
| $f_{BUS}$ | Bus clock | — | 50 | MHz | |
| $f_{FLASH}$ | Flash clock | — | 25 | MHz | |
| $f_{LPTMR}$ | LPTMR clock | — | 25 | MHz | |
| VLPR mode[1] | | | | | |
| $f_{SYS}$ | System and core clock | — | 4 | MHz | |
| $f_{BUS}$ | Bus clock | — | 4 | MHz | |
| $f_{FLASH}$ | Flash clock | — | 1 | MHz | |
| $f_{ERCLK}$ | External reference clock | — | 16 | MHz | |

*Table continues on the next page...*

### Table 9. Device clock specifications (continued)

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $f_{LPTMR\_pin}$ | LPTMR clock | — | 25 | MHz | |
| $f_{LPTMR\_ERCLK}$ | LPTMR external reference clock | — | 16 | MHz | |

1. The frequency limitations in VLPR mode here override any frequency specification listed in the timing specification for any other module.

## 2.3.2 General switching specifications

These general purpose specifications apply to all signals configured for GPIO, UART, and timers.

### Table 10. General switching specifications

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| | GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path | 1.5 | — | Bus clock cycles | 1, 2 |
| | External RESET and NMI pin interrupt pulse width — Asynchronous path | 100 | — | ns | 3 |
| | GPIO pin interrupt pulse width (digital glitch filter disabled, passive filter disabled) — Asynchronous path | 50 | — | ns | 4 |
| | Port rise and fall time<br><br>• Slew disabled<br><br>  • $1.71 \le V_{DD} \le 2.7V$<br><br>  • $2.7 \le V_{DD} \le 3.6V$<br><br>• Slew enabled<br><br>  • $1.71 \le V_{DD} \le 2.7V$<br><br>  • $2.7 \le V_{DD} \le 3.6V$ | <br><br>—<br><br>—<br><br><br><br>—<br><br> | <br><br><br><br>10<br><br>5<br><br><br><br>30<br><br>16 | <br><br><br><br>ns<br><br>ns<br><br><br><br>ns<br><br>ns | 5 |

1. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In Stop, VLPS, LLS, and VLLSx modes, the synchronizer is bypassed so shorter pulses can be recognized in that case.
2. The greater of synchronous and asynchronous timing must be met.
3. These pins have a passive filter enabled on the inputs. This is the shortest pulse width that is guaranteed to be recognized.
4. These pins do not have a passive filter on the inputs. This is the shortest pulse width that is guaranteed to be recognized.
5. 25 pF load

## 2.4 Thermal specifications

## 2.4.1 Thermal operating requirements

### Table 11. Thermal operating requirements

| Symbol | Description | Min. | Max. | Unit | Notes |
|--------|-------------|------|------|------|-------|
| $T_J$ | Die junction temperature | −40 | 125 | °C | |
| $T_A$ | Ambient temperature | −40 | 105 | °C | 1 |

1. Maximum $T_A$ can be exceeded only if the user ensures that $T_J$ does not exceed maximum $T_J$. The simplest method to determine $T_J$ is: $T_J = T_A + R_{\Theta JA} \times$ chip power dissipation.

## 2.4.2 Thermal attributes

| Board type | Symbol | Description | 64 LQFP | 48 LQFP | 32 QFN | Unit | Notes |
|------------|--------|-------------|---------|---------|--------|------|-------|
| Single-layer (1s) | $R_{\theta JA}$ | Thermal resistance, junction to ambient (natural convection) | 66 | 79 | 97 | °C/W | 1 |
| Four-layer (2s2p) | $R_{\theta JA}$ | Thermal resistance, junction to ambient (natural convection) | 48 | 55 | 33 | °C/W | 1 |
| Single-layer (1s) | $R_{\theta JMA}$ | Thermal resistance, junction to ambient (200 ft./min. air speed) | 54 | 67 | 81 | °C/W | 1 |
| Four-layer (2s2p) | $R_{\theta JMA}$ | Thermal resistance, junction to ambient (200 ft./min. air speed) | 41 | 49 | 28 | °C/W | 1 |
| — | $R_{\theta JB}$ | Thermal resistance, junction to board | 30 | 33 | 13 | °C/W | 2 |
| — | $R_{\theta JC}$ | Thermal resistance, junction to case | 17 | 23 | 2.0 | °C/W | 3 |

*Table continues on the next page...*

| Board type | Symbol | Description | 64 LQFP | 48 LQFP | 32 QFN | Unit | Notes |
|---|---|---|---|---|---|---|---|
| — | $\Psi_{JT}$ | Thermal characterization parameter, junction to package top outside center (natural convection) | 3 | 5 | 6 | °C/W | 4 |

1. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*, or EIA/JEDEC Standard JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)*.
2. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*.
3. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
4. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*.

# 3  Peripheral operating requirements and behaviors

## 3.1  Core modules

### 3.1.1  SWD electricals

**Table 12.  SWD full voltage range electricals**

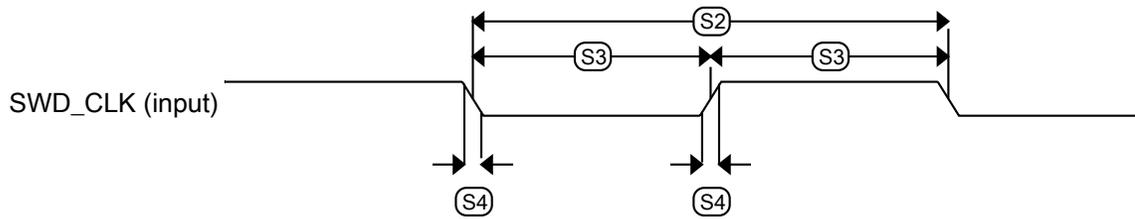| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
|  | Operating voltage | 1.71 | 3.6 | V |
| S1 | SWD_CLK frequency of operation |  |  |  |
|  | • Serial wire debug | 0 | 33 | MHz |
| S2 | SWD_CLK cycle period | 1/S1 | — | ns |
| S3 | SWD_CLK clock pulse width |  |  |  |
|  | • Serial wire debug | 15 | — | ns |
| S4 | SWD_CLK rise and fall times | — | 3 | ns |
| S9 | SWD_DIO input data setup time to SWD_CLK rise | 8 | — | ns |
| S10 | SWD_DIO input data hold time after SWD_CLK rise | 1.4 | — | ns |
| S11 | SWD_CLK high to SWD_DIO data valid | — | 25 | ns |
| S12 | SWD_CLK high to SWD_DIO high-Z | 5 | — | ns |

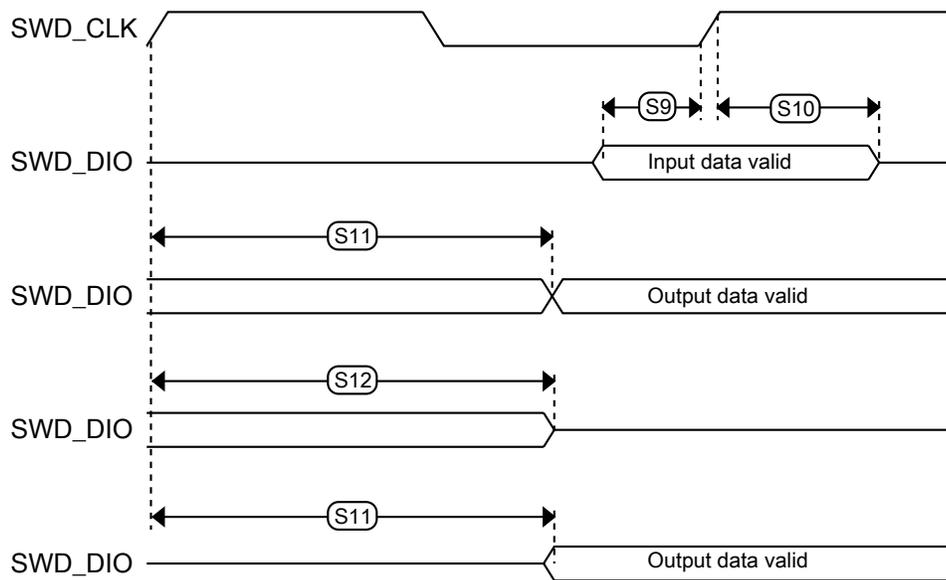**Figure 5. Serial wire clock input timing**



**Figure 6. Serial wire data timing**

## 3.1.2   JTAG electricals

**Table 13.   JTAG limited voltage range electricals**

| Symbol | Description | Min. | Max. | Unit |
|--------|-------------|------|------|------|
|  | Operating voltage | 2.7 | 3.6 | V |
| J1 | TCLK frequency of operation |  |  | MHz |
|  | • Boundary Scan | 0 | 10 |  |
|  | • JTAG and CJTAG | 0 | 20 |  |
| J2 | TCLK cycle period | 1/J1 | — | ns |
| J3 | TCLK clock pulse width |  |  |  |

*Table continues on the next page...*

**Table 13.  JTAG limited voltage range electricals (continued)**

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
|  | • Boundary Scan | 50 | — | ns |
|  | • JTAG and CJTAG | 25 | — | ns |
| J4 | TCLK rise and fall times | — | 3 | ns |
| J5 | Boundary scan input data setup time to TCLK rise | 20 | — | ns |
| J6 | Boundary scan input data hold time after TCLK rise | 1 | — | ns |
| J7 | TCLK low to boundary scan output data valid | — | 25 | ns |
| J8 | TCLK low to boundary scan output high-Z | — | 25 | ns |
| J9 | TMS, TDI input data setup time to TCLK rise | 8 | — | ns |
| J10 | TMS, TDI input data hold time after TCLK rise | 1 | — | ns |
| J11 | TCLK low to TDO data valid | — | 19 | ns |
| J12 | TCLK low to TDO high-Z | — | 19 | ns |
| J13 | $\overline{TRST}$ assert time | 100 | — | ns |
| J14 | $\overline{TRST}$ setup time (negation) to TCLK high | 8 | — | ns |

**Table 14.  JTAG full voltage range electricals**

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
|  | Operating voltage | 1.71 | 3.6 | V |
| J1 | TCLK frequency of operation |  |  | MHz |
|  | • Boundary Scan | 0 | 10 |  |
|  | • JTAG and CJTAG | 0 | 15 |  |
| J2 | TCLK cycle period | 1/J1 | — | ns |
| J3 | TCLK clock pulse width |  |  |  |
|  | • Boundary Scan | 50 | — | ns |
|  | • JTAG and CJTAG | 33 | — | ns |
| J4 | TCLK rise and fall times | — | 3 | ns |
| J5 | Boundary scan input data setup time to TCLK rise | 20 | — | ns |
| J6 | Boundary scan input data hold time after TCLK rise | 1.4 | — | ns |
| J7 | TCLK low to boundary scan output data valid | — | 27 | ns |
| J8 | TCLK low to boundary scan output high-Z | — | 27 | ns |
| J9 | TMS, TDI input data setup time to TCLK rise | 8 | — | ns |
| J10 | TMS, TDI input data hold time after TCLK rise | 1.4 | — | ns |
| J11 | TCLK low to TDO data valid | — | 26.2 | ns |
| J12 | TCLK low to TDO high-Z | — | 26.2 | ns |
| J13 | $\overline{TRST}$ assert time | 100 | — | ns |
| J14 | $\overline{TRST}$ setup time (negation) to TCLK high | 8 | — | ns |
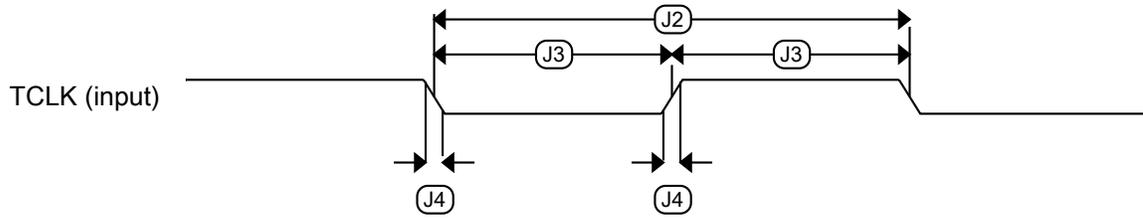
**Figure 7. Test clock input timing**
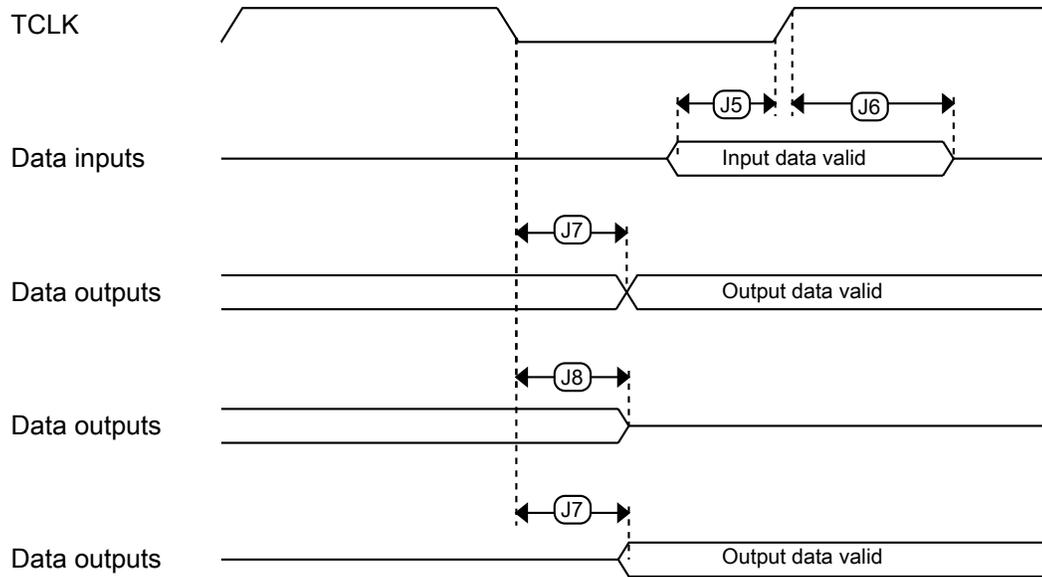


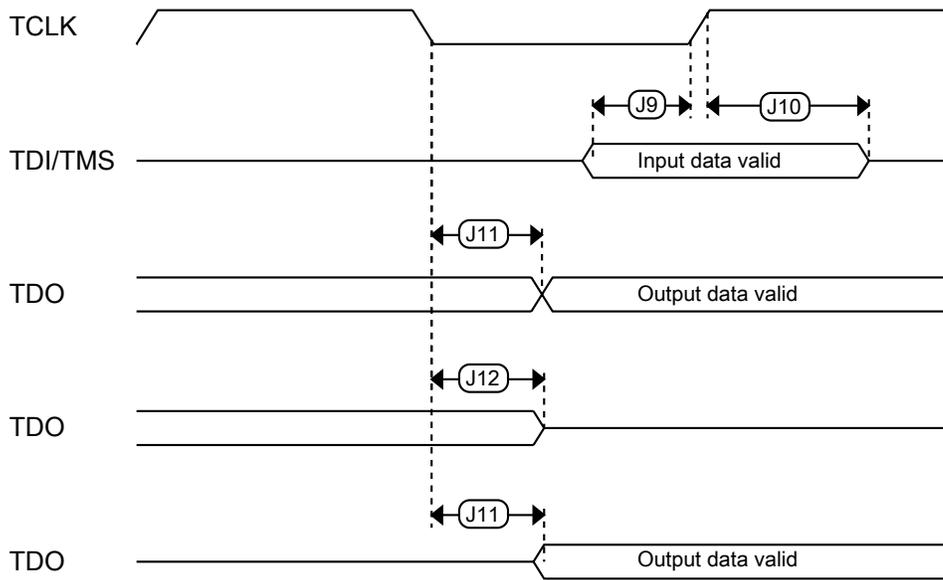**Figure 8. Boundary scan (JTAG) timing**

**Figure 9. Test Access Port timing**



**Figure 10. $\overline{\text{TRST}}$ timing**
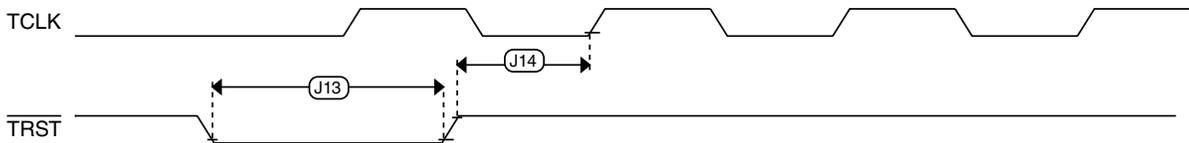
## 3.2  System modules

There are no specifications necessary for the device's system modules.

## 3.3  Clock modules

## 3.3.1 MCG specifications

### Table 15.  MCG specifications

| Symbol | Description | | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|---|
| $f_{ints\_ft}$ | Internal reference frequency (slow clock) — factory trimmed at nominal VDD and 25 °C | | — | 32.768 | — | kHz | |
| $\Delta f_{ints\_t}$ | Total deviation of internal reference frequency (slow clock) over voltage and temperature | | — | +0.5/-0.7 | ± 2 | % | |
| $f_{ints\_t}$ | Internal reference frequency (slow clock) — user trimmed | | 31.25 | — | 39.0625 | kHz | |
| $\Delta f_{dco\_res\_t}$ | Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM and SCFTRIM | | — | ± 0.3 | ± 0.6 | %$f_{dco}$ | 1 |
| $\Delta f_{dco\_t}$ | Total deviation of trimmed average DCO output frequency over voltage and temperature | | — | +0.5/-0.7 | ± 2 | %$f_{dco}$ | 1, 2 |
| $\Delta f_{dco\_t}$ | Total deviation of trimmed average DCO output frequency over fixed voltage and temperature range of 0–70°C | | — | ± 0.3 | ± 1.5 | %$f_{dco}$ | 1 |
| $f_{intf\_ft}$ | Internal reference frequency (fast clock) — factory trimmed at nominal VDD and 25°C | | — | 4 | — | MHz | |
| $\Delta f_{intf\_ft}$ | Frequency deviation of internal reference clock (fast clock) over temperature and voltage — factory trimmed at nominal VDD and 25 °C | | — | +1/-2 | ± 5 | %$f_{intf\_ft}$ | |
| $f_{intf\_t}$ | Internal reference frequency (fast clock) — user trimmed at nominal VDD and 25 °C | | 3 | — | 5 | MHz | |
| $f_{loc\_low}$ | Loss of external clock minimum frequency — RANGE = 00 | | (3/5) x $f_{ints\_t}$ | — | — | kHz | |
| $f_{loc\_high}$ | Loss of external clock minimum frequency — RANGE = 01, 10, or 11 | | (16/5) x $f_{ints\_t}$ | — | — | kHz | |
| FLL | | | | | | | |
| $f_{fll\_ref}$ | FLL reference frequency range | | 31.25 | — | 39.0625 | kHz | |
| $f_{dco}$ | DCO output frequency range | Low range (DRS=00) $640 \times f_{fll\_ref}$ | 20 | 20.97 | 25 | MHz | 3, 4 |
| | | Mid range (DRS=01) $1280 \times f_{fll\_ref}$ | 40 | 41.94 | 50 | MHz | |
| | | Mid-high range (DRS=10) $1920 \times f_{fll\_ref}$ | 60 | 62.91 | 75 | MHz | |
| | | High range (DRS=11) $2560 \times f_{fll\_ref}$ | 80 | 83.89 | 100 | MHz | |
| $f_{dco\_t\_DMX32}$ | DCO output frequency | Low range (DRS=00) $732 \times f_{fll\_ref}$ | — | 23.99 | — | MHz | 5, 6 |
| | | Mid range (DRS=01) $1464 \times f_{fll\_ref}$ | — | 47.97 | — | MHz | |
| | | Mid-high range (DRS=10) | — | 71.99 | — | MHz | |

*Table continues on the next page...*

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**Table 15.  MCG specifications (continued)**

| Symbol | Description | | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|---|
| | | $2197 \times f_{fll\_ref}$ | | | | | |
| | | High range (DRS=11) | — | 95.98 | — | MHz | |
| | | $2929 \times f_{fll\_ref}$ | | | | | |
| $J_{cyc\_fll}$ | FLL period jitter • $f_{VCO}$ = 48 MHz • $f_{VCO}$ = 98 MHz | | — — | — 180 150 | — — | ps | |
| $t_{fll\_acquire}$ | FLL target frequency acquisition time | | — | — | 1 | ms | 7 |

1. This parameter is measured with the internal reference (slow clock) being used as a reference to the FLL (FEI clock mode).
2. 2.0 V <= VDD <= 3.6 V.
3. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=0.
4. The resulting system clock frequencies should not exceed their maximum specified values. The DCO frequency deviation ($\Delta f_{dco\_t}$) over voltage and temperature should be considered.
5. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=1.
6. The resulting clock frequency must not exceed the maximum specified clock frequency of the device.
7. This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bits are changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

## 3.3.2  IRC48M specifications

**Table 16.  IRC48M specifications**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | 1.71 | — | 3.6 | V | |
| $I_{DD48M}$ | Supply current | — | 400 | 500 | µA | |
| $f_{irc48m}$ | Internal reference frequency | — | 48 | — | MHz | |
| $\Delta f_{irc48m\_hv}$ | Total deviation of IRC48M frequency at high voltage (VDD=1.89V-3.6V) over full temperature | — | ± 0.5 | ± 1.5 | $\%f_{irc48m}$ | |
| $\Delta f_{irc48m\_hv}$ | Total deviation of IRC48M frequency at high voltage (VDD=1.89V-3.6V) over -40°C to 85°C | — | ± 0.5 | ± 1.0 | $\%f_{irc48m}$ | |
| $\Delta f_{irc48m\_lv}$ | Total deviation of IRC48M frequency at low voltage (VDD=1.71V-1.89V) over full temperature | — | ± 0.5 | ± 2.0 | $\%f_{irc48m}$ | |
| $J_{cyc\_irc48m}$ | Period Jitter (RMS) | — | 35 | 150 | ps | |
| $t_{irc48mst}$ | Startup time | — | 2 | 3 | µs | 1 |

1. IRC48M startup time is defined as the time between clock enablement and clock availability for system use. Enable the clock by one of the following settings:
    • MCG operating in an external clocking mode and MCG_C7[OSCSEL]=10 or MCG_C5[PLLCLKEN0]=1, or
    • SIM_SOPT2[PLLFLLSEL]=11

### 3.3.3   Oscillator electrical specifications

#### 3.3.3.1   Oscillator DC electrical specifications

**Table 17.   Oscillator DC electrical specifications**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|--------|-------------|------|------|------|------|-------|
| $V_{DD}$ | Supply voltage | 1.71 | — | 3.6 | V | |
| $I_{DDOSC}$ | Supply current — low-power mode (HGO=0) | | | | | 1 |
| | • 32 kHz | — | 500 | — | nA | |
| | • 4 MHz | — | 200 | — | µA | |
| | • 8 MHz (RANGE=01) | — | 300 | — | µA | |
| | • 16 MHz | — | 950 | — | µA | |
| | • 24 MHz | — | 1.2 | — | mA | |
| | • 32 MHz | — | 1.5 | — | mA | |
| $I_{DDOSC}$ | Supply current — high-gain mode (HGO=1) | | | | | 1 |
| | • 32 kHz | — | 25 | — | µA | |
| | • 4 MHz | — | 400 | — | µA | |
| | • 8 MHz (RANGE=01) | — | 500 | — | µA | |
| | • 16 MHz | — | 2.5 | — | mA | |
| | • 24 MHz | — | 3 | — | mA | |
| | • 32 MHz | — | 4 | — | mA | |
| $C_x$ | EXTAL load capacitance | — | — | — | | 2, 3 |
| $C_y$ | XTAL load capacitance | — | — | — | | 2, 3 |
| $R_F$ | Feedback resistor — low-frequency, low-power mode (HGO=0) | — | — | — | MΩ | 2, 4 |
| | Feedback resistor — low-frequency, high-gain mode (HGO=1) | — | 10 | — | MΩ | |
| | Feedback resistor — high-frequency, low-power mode (HGO=0) | — | — | — | MΩ | |
| | Feedback resistor — high-frequency, high-gain mode (HGO=1) | — | 1 | — | MΩ | |
| $R_S$ | Series resistor — low-frequency, low-power mode (HGO=0) | — | — | — | kΩ | |
| | Series resistor — low-frequency, high-gain mode (HGO=1) | — | 200 | — | kΩ | |
| | Series resistor — high-frequency, low-power mode (HGO=0) | — | — | — | kΩ | |
| | Series resistor — high-frequency, high-gain mode (HGO=1) | — | 0 | — | kΩ | |

*Table continues on the next page...*

## Table 17.   Oscillator DC electrical specifications (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $V_{pp}$[5] | Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode (HGO=0) | — | 0.6 | — | V | |
| | Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO=1) | — | $V_{DD}$ | — | V | |
| | Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode (HGO=0) | — | 0.6 | — | V | |
| | Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode (HGO=1) | — | $V_{DD}$ | — | V | |

1. $V_{DD}$=3.3 V, Temperature =25 °C
2. See crystal or resonator manufacturer's recommendation
3. $C_x$ and $C_y$ can be provided by using either integrated capacitors or external components.
4. When low-power mode is selected, $R_F$ is integrated and must not be attached externally.
5. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other device.

## 3.3.3.2   Oscillator frequency specifications
### Table 18.   Oscillator frequency specifications

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $f_{osc\_lo}$ | Oscillator crystal or resonator frequency — low-frequency mode (MCG_C2[RANGE]=00) | 32 | — | 40 | kHz | |
| $f_{osc\_hi\_1}$ | Oscillator crystal or resonator frequency — high-frequency mode (low range) (MCG_C2[RANGE]=01) | 3 | — | 8 | MHz | |
| $f_{osc\_hi\_2}$ | Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x) | 8 | — | 32 | MHz | |
| $f_{ec\_extal}$ | Input clock frequency (external clock mode) | — | — | 50 | MHz | 1, 2 |
| $t_{dc\_extal}$ | Input clock duty cycle (external clock mode) | 40 | 50 | 60 | % | |
| $t_{cst}$ | Crystal startup time — 32 kHz low-frequency, low-power mode (HGO=0) | — | 750 | — | ms | 3, 4 |
| | Crystal startup time — 32 kHz low-frequency, high-gain mode (HGO=1) | — | 250 | — | ms | |
| | Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), low-power mode (HGO=0) | — | 0.6 | — | ms | |
| | Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), high-gain mode (HGO=1) | — | 1 | — | ms | |

1. Other frequency limits may apply when external clock is being used as a reference for the FLL

2. When transitioning from FEI or FBI to FBE mode, restrict the frequency of the input clock so that, when it is divided by FRDIV, it remains within the limits of the DCO input clock frequency.
3. Proper PC board layout procedures must be followed to achieve specifications.
4. Crystal startup time is defined as the time between the oscillator being enabled and the OSCINIT bit in the MCG_S register being set.

# 3.4  Memories and memory interfaces

## 3.4.1  Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

### 3.4.1.1  Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

**Table 19.  NVM program/erase timing specifications**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $t_{hvpgm4}$ | Longword Program high-voltage time | — | 7.5 | 18 | µs | — |
| $t_{hversscr}$ | Sector Erase high-voltage time | — | 13 | 113 | ms | 1 |
| $t_{hversall}$ | Erase All high-voltage time | — | 104 | 904 | ms | 1 |

1. Maximum time based on expectations at cycling end-of-life.

### 3.4.1.2  Flash timing specifications — commands
**Table 20.  Flash command timing specifications**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $t_{rd1sec2k}$ | Read 1s Section execution time (flash sector) | — | — | 60 | µs | 1 |
| $t_{pgmchk}$ | Program Check execution time | — | — | 45 | µs | 1 |
| $t_{rdrsrc}$ | Read Resource execution time | — | — | 30 | µs | 1 |
| $t_{pgm4}$ | Program Longword execution time | — | 65 | 145 | µs | — |
| $t_{ersscr}$ | Erase Flash Sector execution time | — | 14 | 114 | ms | 2 |
| $t_{rd1all}$ | Read 1s All Blocks execution time | — | — | 0.9 | ms | 1 |
| $t_{rdonce}$ | Read Once execution time | — | — | 30 | µs | 1 |
| $t_{pgmonce}$ | Program Once execution time | — | 100 | — | µs | — |
| $t_{ersall}$ | Erase All Blocks execution time | — | 140 | 1150 | ms | 2 |
| $t_{vfykey}$ | Verify Backdoor Access Key execution time | — | — | 30 | µs | 1 |

1. Assumes 25 MHz flash clock frequency.

2. Maximum times for erase parameters based on expectations at cycling end-of-life.

### 3.4.1.3 Flash high voltage current behaviors

**Table 21. Flash high voltage current behaviors**

| Symbol | Description | Min. | Typ. | Max. | Unit |
|--------|-------------|------|------|------|------|
| $I_{DD\_PGM}$ | Average current adder during high voltage flash programming operation | — | 2.5 | 6.0 | mA |
| $I_{DD\_ERS}$ | Average current adder during high voltage flash erase operation | — | 1.5 | 4.0 | mA |

### 3.4.1.4 Reliability specifications

**Table 22. NVM reliability specifications**

| Symbol | Description | Min. | Typ.[1] | Max. | Unit | Notes |
|--------|-------------|------|---------|------|------|-------|
| Program Flash | | | | | | |
| $t_{nvmretp10k}$ | Data retention after up to 10 K cycles | 5 | 50 | — | years | — |
| $t_{nvmretp1k}$ | Data retention after up to 1 K cycles | 20 | 100 | — | years | — |
| $n_{nvmcycp}$ | Cycling endurance | 10 K | 50 K | — | cycles | 2 |

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25 °C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at $-40\ °C \le T_j \le 125\ °C$.

## 3.5 Security and integrity modules

There are no specifications necessary for the device's security and integrity modules.

## 3.6 Analog

### 3.6.1 ADC electrical specifications

The 16-bit accuracy specifications listed in Table 23 and Table 24 are achievable on the differential pins ADCx_DPx, ADCx_DMx.

All other ADC channels meet the 13-bit differential/12-bit single-ended accuracy specifications.

## 3.6.1.1   16-bit ADC operating conditions
### Table 23.   16-bit ADC operating conditions

| Symbol | Description | Conditions | Min. | Typ.[1] | Max. | Unit | Notes |
|---|---|---|---|---|---|---|---|
| $V_{DDA}$ | Supply voltage | Absolute | 1.71 | — | 3.6 | V | |
| $\Delta V_{DDA}$ | Supply voltage | Delta to $V_{DD}$ ($V_{DD} - V_{DDA}$) | -100 | 0 | +100 | mV | 2 |
| $\Delta V_{SSA}$ | Ground voltage | Delta to $V_{SS}$ ($V_{SS} - V_{SSA}$) | -100 | 0 | +100 | mV | 2 |
| $V_{REFH}$ | ADC reference voltage high | | 1.13 | $V_{DDA}$ | $V_{DDA}$ | V | |
| $V_{REFL}$ | ADC reference voltage low | | $V_{SSA}$ | $V_{SSA}$ | $V_{SSA}$ | V | |
| $V_{ADIN}$ | Input voltage | • 16-bit differential mode<br><br>• All other modes | VREFL<br><br>VREFL | —<br><br>— | 31/32 * VREFH<br><br>VREFH | V | |
| $C_{ADIN}$ | Input capacitance | • 16-bit mode<br>• 8-bit / 10-bit / 12-bit modes | —<br>— | 8<br>4 | 10<br>5 | pF | |
| $R_{ADIN}$ | Input series resistance | | — | 2 | 5 | kΩ | |
| $R_{AS}$ | Analog source resistance (external) | 13-bit / 12-bit modes<br>$f_{ADCK} < 4$ MHz | — | — | 5 | kΩ | 3 |
| $f_{ADCK}$ | ADC conversion clock frequency | ≤ 13-bit mode | 1.0 | — | 24.0 | MHz | 4 |
| $f_{ADCK}$ | ADC conversion clock frequency | 16-bit mode | 2.0 | — | 12.0 | MHz | 4 |
| $C_{rate}$ | ADC conversion rate | ≤ 13-bit modes<br>No ADC hardware averaging<br>Continuous conversions enabled, subsequent conversion time | 20 | — | 1200 | Ksps | 5 |
| $C_{rate}$ | ADC conversion rate | 16-bit mode<br>No ADC hardware averaging<br>Continuous conversions enabled, subsequent conversion time | 37 | — | 461 | Ksps | 5 |

1. Typical values assume $V_{DDA}$ = 3.0 V, Temp = 25 °C, $f_{ADCK}$ = 1.0 MHz, unless otherwise stated. Typical values are for reference only, and are not tested in production.
2. DC potential difference.
3. This resistance is external to MCU. To achieve the best results, the analog source resistance must be kept as low as possible. The results in this data sheet were derived from a system that had < 8 Ω analog source resistance. The $R_{AS}/C_{AS}$ time constant should be kept to < 1 ns.
4. To use the maximum ADC conversion clock frequency, CFG2[ADHSC] must be set and CFG1[ADLPC] must be clear.
5. For guidelines and examples of conversion rate calculation, download the ADC calculator tool.
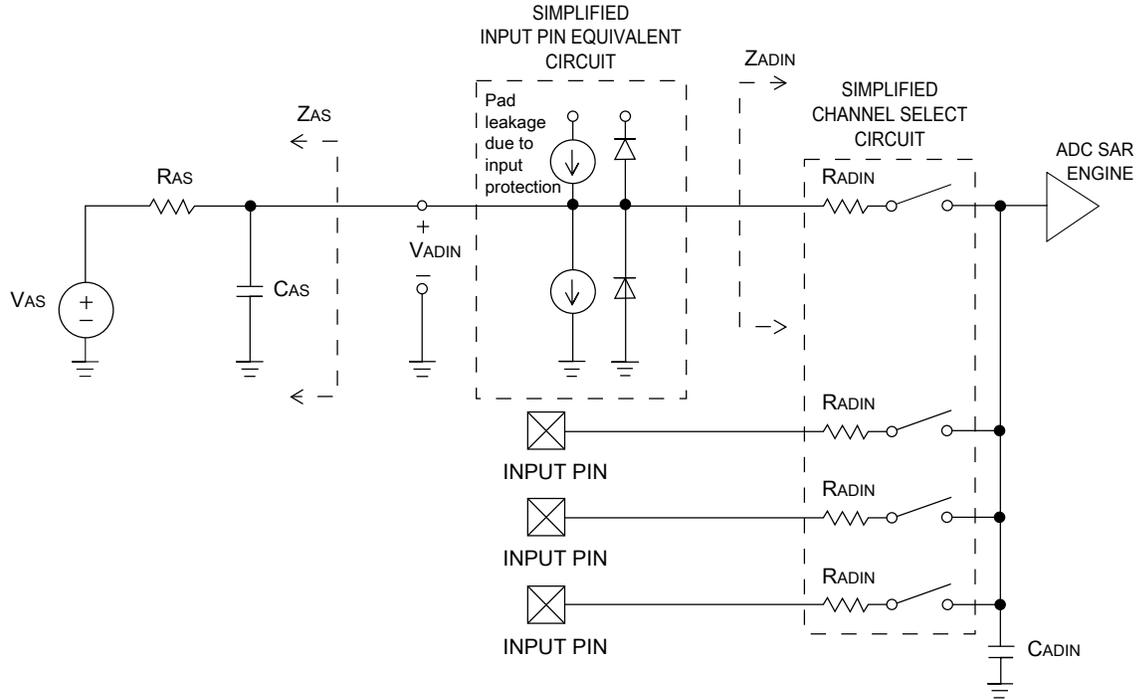
**Figure 11. ADC input impedance equivalency diagram**

## 3.6.1.2   16-bit ADC electrical characteristics

**Table 24.   16-bit ADC characteristics (V$_{REFH}$ = V$_{DDA}$, V$_{REFL}$ = V$_{SSA}$)**

| Symbol | Description | Conditions[1] | Min. | Typ.[2] | Max. | Unit | Notes |
|---|---|---|---|---|---|---|---|
| I$_{DDA\_ADC}$ | Supply current | | 0.215 | — | 1.7 | mA | 3 |
| f$_{ADACK}$ | ADC asynchronous clock source | • ADLPC = 1, ADHSC = 0 | 1.2 | 2.4 | 3.9 | MHz | t$_{ADACK}$ = 1/ f$_{ADACK}$ |
| | | • ADLPC = 1, ADHSC = 1 | 2.4 | 4.0 | 6.1 | MHz | |
| | | • ADLPC = 0, ADHSC = 0 | 3.0 | 5.2 | 7.3 | MHz | |
| | | • ADLPC = 0, ADHSC = 1 | 4.4 | 6.2 | 9.5 | MHz | |
| | Sample Time | See Reference Manual chapter for sample times | | | | | |
| TUE | Total unadjusted error | • 12-bit modes | — | ±4 | ±6.8 | LSB[4] | 5 |
| | | • <12-bit modes | — | ±1.4 | ±2.1 | | |
| DNL | Differential non-linearity | • 12-bit modes | — | ±0.7 | −1.1 to +1.9 | LSB[4] | 5 |
| | | • <12-bit modes | — | ±0.2 | −0.3 to 0.5 | | |
| INL | Integral non-linearity | • 12-bit modes | — | ±1.0 | −2.7 to +1.9 | LSB[4] | 5 |

*Table continues on the next page...*

## Table 24.   16-bit ADC characteristics ($V_{REFH}$ = $V_{DDA}$, $V_{REFL}$ = $V_{SSA}$) (continued)

| Symbol | Description | Conditions[1] | Min. | Typ.[2] | Max. | Unit | Notes |
|---|---|---|---|---|---|---|---|
| | | • <12-bit modes | — | ±0.5 | −0.7 to +0.5 | | |
| $E_{FS}$ | Full-scale error | • 12-bit modes | — | −4 | −5.4 | LSB[4] | $V_{ADIN}$ = $V_{DDA}$[5] |
| | | • <12-bit modes | — | −1.4 | −1.8 | | |
| $E_Q$ | Quantization error | • 16-bit modes | — | −1 to 0 | — | LSB[4] | |
| | | • ≤13-bit modes | — | — | ±0.5 | | |
| ENOB | Effective number of bits | 16-bit differential mode | | | | | 6 |
| | | • Avg = 32 | 12.8 | 14.5 | — | bits | |
| | | • Avg = 4 | 11.9 | 13.8 | — | bits | |
| | | 16-bit single-ended mode | | | | | |
| | | • Avg = 32 | 12.2 | 13.9 | — | bits | |
| | | • Avg = 4 | 11.4 | 13.1 | — | bits | |
| SINAD | Signal-to-noise plus distortion | See ENOB | | 6.02 × ENOB + 1.76 | | dB | |
| THD | Total harmonic distortion | 16-bit differential mode | | | | dB | 7 |
| | | • Avg = 32 | — | -94 | — | dB | |
| | | 16-bit single-ended mode | | | | | |
| | | • Avg = 32 | — | -85 | — | | |
| SFDR | Spurious free dynamic range | 16-bit differential mode | | | | dB | 7 |
| | | • Avg = 32 | 82 | 95 | — | dB | |
| | | 16-bit single-ended mode | | | | | |
| | | • Avg = 32 | 78 | 90 | — | | |
| $E_{IL}$ | Input leakage error | | | $I_{In}$ × $R_{AS}$ | | mV | $I_{In}$ = leakage current (refer to the MCU's voltage and current operating ratings) |
| | Temp sensor slope | Across the full temperature range of the device | 1.55 | 1.62 | 1.69 | mV/°C | 8 |
| $V_{TEMP25}$ | Temp sensor voltage | 25 °C | 706 | 716 | 726 | mV | 8 |

1.  All accuracy numbers assume the ADC is calibrated with $V_{REFH}$ = $V_{DDA}$
2.  Typical values assume $V_{DDA}$ = 3.0 V, Temp = 25 °C, $f_{ADCK}$ = 2.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
3.  The ADC supply current depends on the ADC conversion clock speed, conversion rate and ADC_CFG1[ADLPC] (low power). For lowest power operation, ADC_CFG1[ADLPC] must be set, the ADC_CFG2[ADHSC] bit must be clear with 1 MHz ADC conversion clock speed.

4.  1 LSB = $(V_{REFH} - V_{REFL})/2^N$
5.  ADC conversion clock < 16 MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
6.  Input data is 100 Hz sine wave. ADC conversion clock < 12 MHz.
7.  Input data is 1 kHz sine wave. ADC conversion clock < 12 MHz.
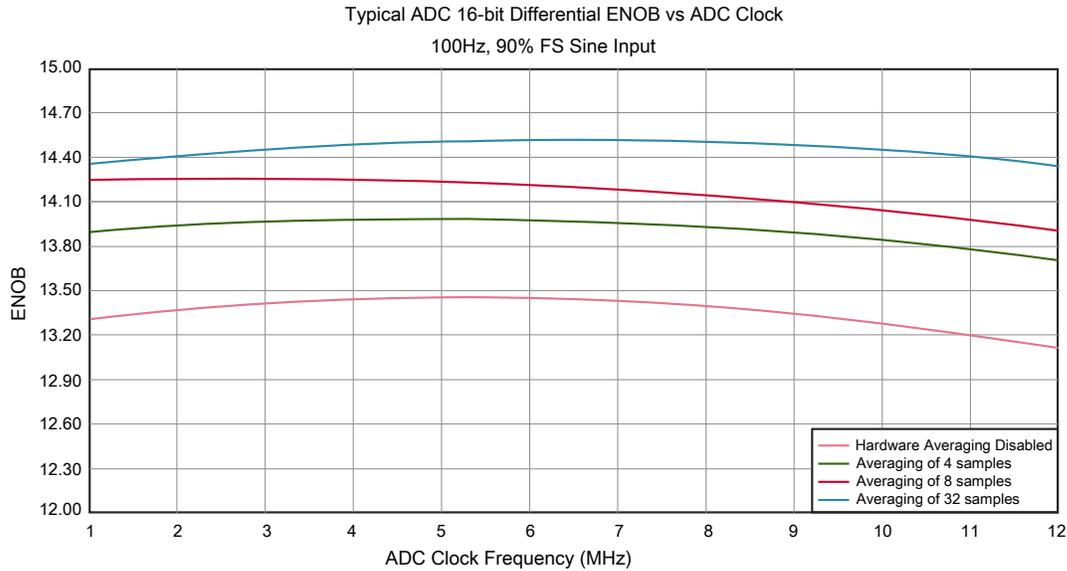8.  ADC conversion clock < 3 MHz



**Figure 12. Typical ENOB vs. ADC_CLK for 16-bit differential mode**
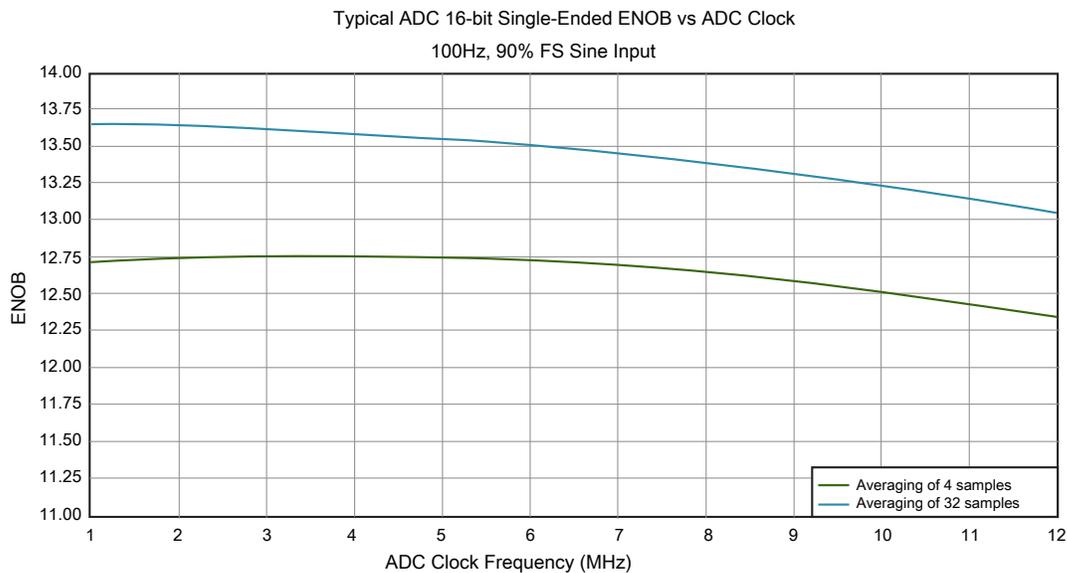


**Figure 13. Typical ENOB vs. ADC_CLK for 16-bit single-ended mode**

## 3.6.2  CMP and 6-bit DAC electrical specifications

### Table 25.  Comparator and 6-bit DAC electrical specifications

| Symbol | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | 1.71 | — | 3.6 | V |
| $I_{DDHS}$ | Supply current, High-speed mode (EN=1, PMODE=1) | — | — | 200 | μA |
| $I_{DDLS}$ | Supply current, low-speed mode (EN=1, PMODE=0) | — | — | 20 | μA |
| $V_{AIN}$ | Analog input voltage | $V_{SS} - 0.3$ | — | $V_{DD}$ | V |
| $V_{AIO}$ | Analog input offset voltage | — | — | 20 | mV |
| $V_H$ | Analog comparator hysteresis[1] | | | | |
| | • CR0[HYSTCTR] = 00 | — | 5 | — | mV |
| | • CR0[HYSTCTR] = 01 | — | 10 | — | mV |
| | • CR0[HYSTCTR] = 10 | — | 20 | — | mV |
| | • CR0[HYSTCTR] = 11 | — | 30 | — | mV |
| $V_{CMPOh}$ | Output high | $V_{DD} - 0.5$ | — | — | V |
| $V_{CMPOl}$ | Output low | — | — | 0.5 | V |
| $t_{DHS}$ | Propagation delay, high-speed mode (EN=1, PMODE=1) | 20 | 50 | 200 | ns |
| $t_{DLS}$ | Propagation delay, low-speed mode (EN=1, PMODE=0) | 80 | 250 | 600 | ns |
| | Analog comparator initialization delay[2] | — | — | 40 | μs |
| $I_{DAC6b}$ | 6-bit DAC current adder (enabled) | — | 7 | — | μA |
| INL | 6-bit DAC integral non-linearity | −0.5 | — | 0.5 | LSB[3] |
| DNL | 6-bit DAC differential non-linearity | −0.3 | — | 0.3 | LSB |

1.  Typical hysteresis is measured with input voltage range limited to 0.6 to $V_{DD}$–0.6 V.
2.  Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to CMP_DACCR[DACEN], CMP_DACCR[VRSEL], CMP_DACCR[VOSEL], CMP_MUXCR[PSEL], and CMP_MUXCR[MSEL]) and the comparator output settling to a stable level.
3.  1 LSB = $V_{reference}/64$
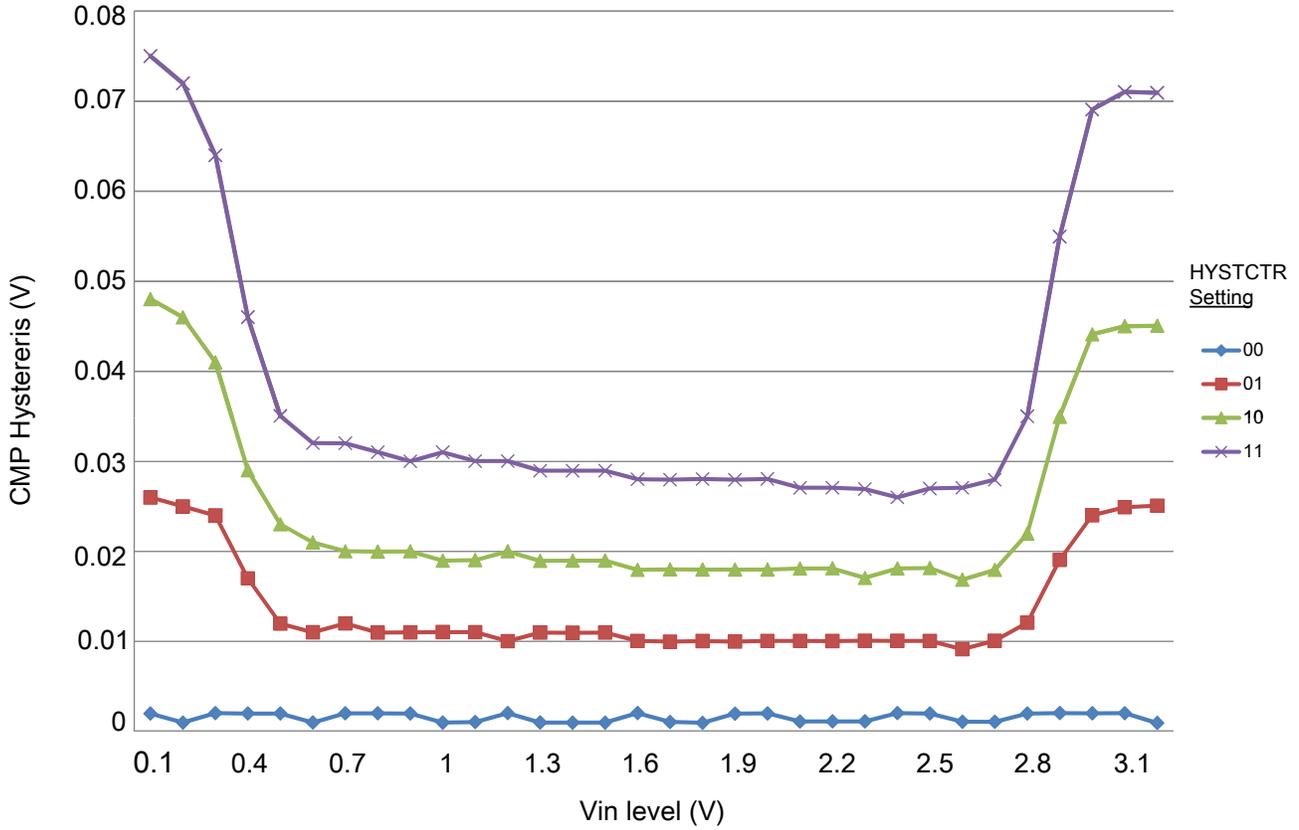
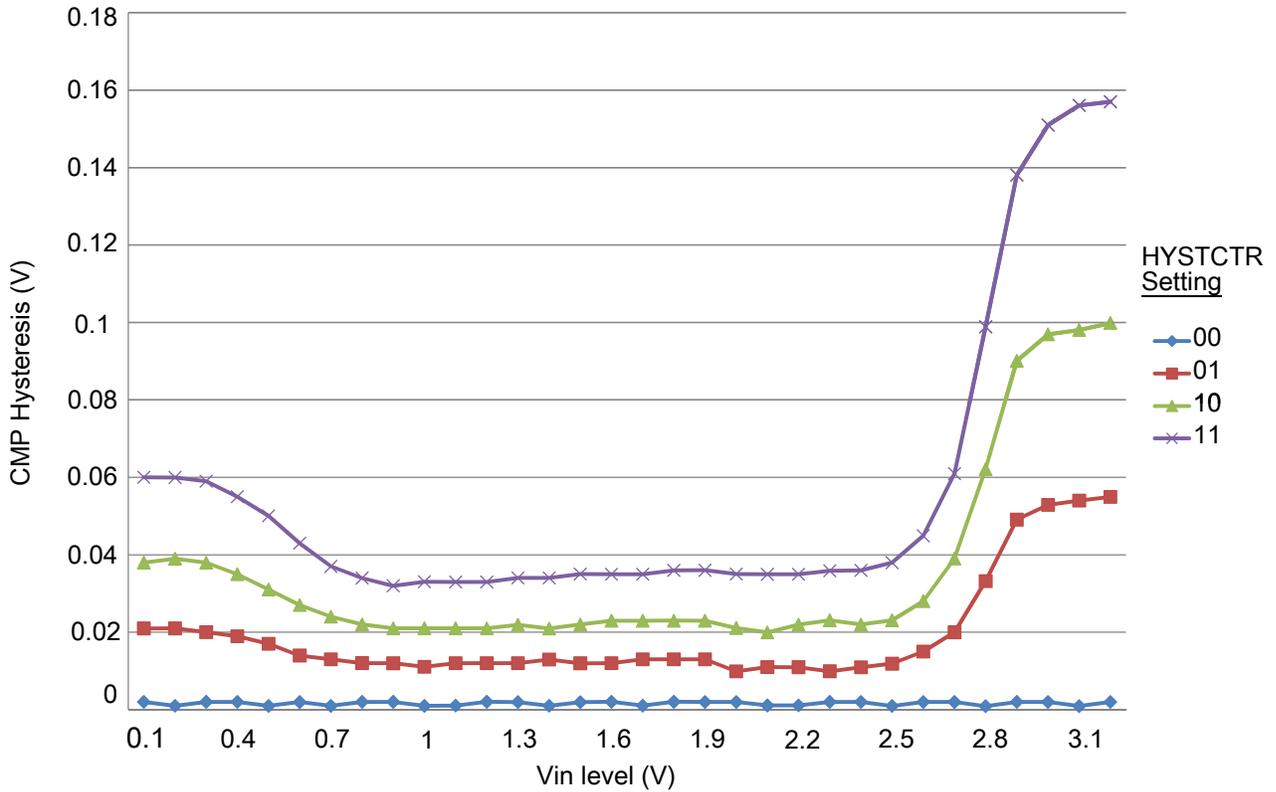**Figure 14. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 0)**

**Figure 15. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 1)**

# 3.6.3   12-bit DAC electrical characteristics

## 3.6.3.1   12-bit DAC operating requirements

**Table 26.   12-bit DAC operating requirements**

| Symbol | Desciption | Min. | Max. | Unit | Notes |
|--------|-----------|------|------|------|-------|
| $V_{DDA}$ | Supply voltage | 1.71 | 3.6 | V | |
| $V_{DACR}$ | Reference voltage | 1.13 | 3.6 | V | 1 |
| $C_L$ | Output load capacitance | — | 100 | pF | 2 |
| $I_L$ | Output load current | — | 1 | mA | |

1.  The DAC reference can be selected to be $V_{DDA}$ or $V_{REFH}$.
2.  A small load capacitance (47 pF) can improve the bandwidth performance of the DAC.

## 3.6.3.2 12-bit DAC operating behaviors
### Table 27. 12-bit DAC operating behaviors

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $I_{DDA\_DACLP}$ | Supply current — low-power mode | — | — | 330 | µA | |
| $I_{DDA\_DACHP}$ | Supply current — high-speed mode | — | — | 1200 | µA | |
| $t_{DACLP}$ | Full-scale settling time (0x080 to 0xF7F) — low-power mode | — | 100 | 200 | µs | 1 |
| $t_{DACHP}$ | Full-scale settling time (0x080 to 0xF7F) — high-power mode | — | 15 | 30 | µs | 1 |
| $t_{CCDACLP}$ | Code-to-code settling time (0xBF8 to 0xC08) — low-power mode and high-speed mode | — | 0.7 | 1 | µs | 1 |
| $V_{dacoutl}$ | DAC output voltage range low — high-speed mode, no load, DAC set to 0x000 | — | — | 100 | mV | |
| $V_{dacouth}$ | DAC output voltage range high — high-speed mode, no load, DAC set to 0xFFF | $V_{DACR}$ −100 | — | $V_{DACR}$ | mV | |
| INL | Integral non-linearity error — high speed mode | — | — | ±8 | LSB | 2 |
| DNL | Differential non-linearity error — $V_{DACR}$ > 2 V | — | — | ±1 | LSB | 3 |
| DNL | Differential non-linearity error — $V_{DACR}$ = VREF_OUT | — | — | ±1 | LSB | 4 |
| $V_{OFFSET}$ | Offset error | — | ±0.4 | ±0.8 | %FSR | 5 |
| $E_G$ | Gain error | — | ±0.1 | ±0.6 | %FSR | 5 |
| PSRR | Power supply rejection ratio, $V_{DDA} \geq 2.4$ V | 60 | — | 90 | dB | |
| $T_{CO}$ | Temperature coefficient offset voltage | — | 3.7 | — | µV/C | 6 |
| $T_{GE}$ | Temperature coefficient gain error | — | 0.000421 | — | %FSR/C | |
| Rop | Output resistance (load = 3 kΩ) | — | — | 250 | Ω | |
| SR | Slew rate -80h→ F7Fh→ 80h | | | | V/µs | |
| | • High power ($SP_{HP}$) | 1.2 | 1.7 | — | | |
| | • Low power ($SP_{LP}$) | 0.05 | 0.12 | — | | |
| BW | 3dB bandwidth | | | | kHz | |
| | • High power ($SP_{HP}$) | 550 | — | — | | |
| | • Low power ($SP_{LP}$) | 40 | — | — | | |

1. Settling within ±1 LSB
2. The INL is measured for 0 + 100 mV to $V_{DACR}$ −100 mV
3. The DNL is measured for 0 + 100 mV to $V_{DACR}$ −100 mV
4. The DNL is measured for 0 + 100 mV to $V_{DACR}$ −100 mV with $V_{DDA}$ > 2.4 V
5. Calculated by a best fit curve from $V_{SS}$ + 100 mV to $V_{DACR}$ − 100 mV
6. $V_{DDA}$ = 3.0 V, reference select set for $V_{DDA}$ (DACx_CO:DACRFS = 1), high power mode (DACx_C0:LPEN = 0), DAC set to 0x800, temperature range is across the full range of the device
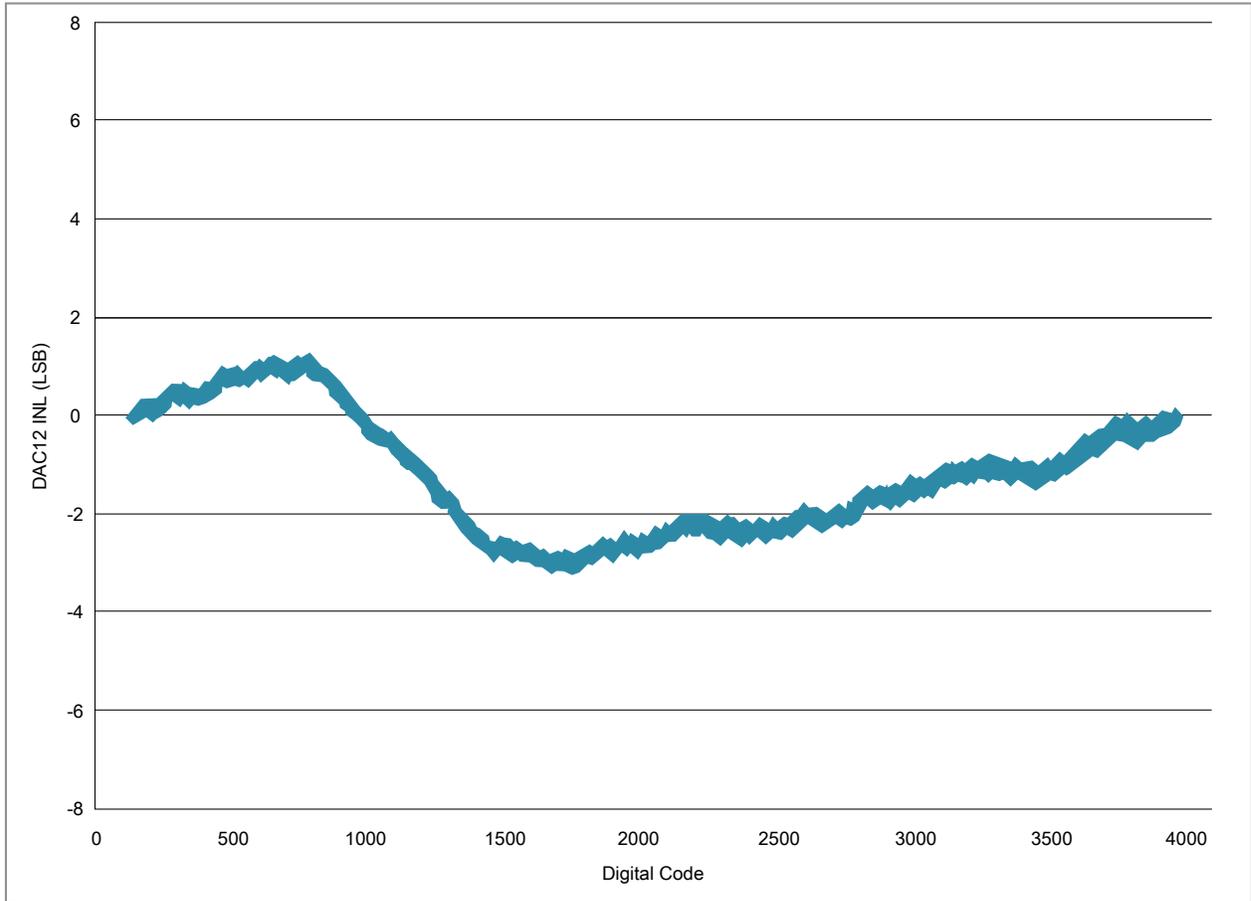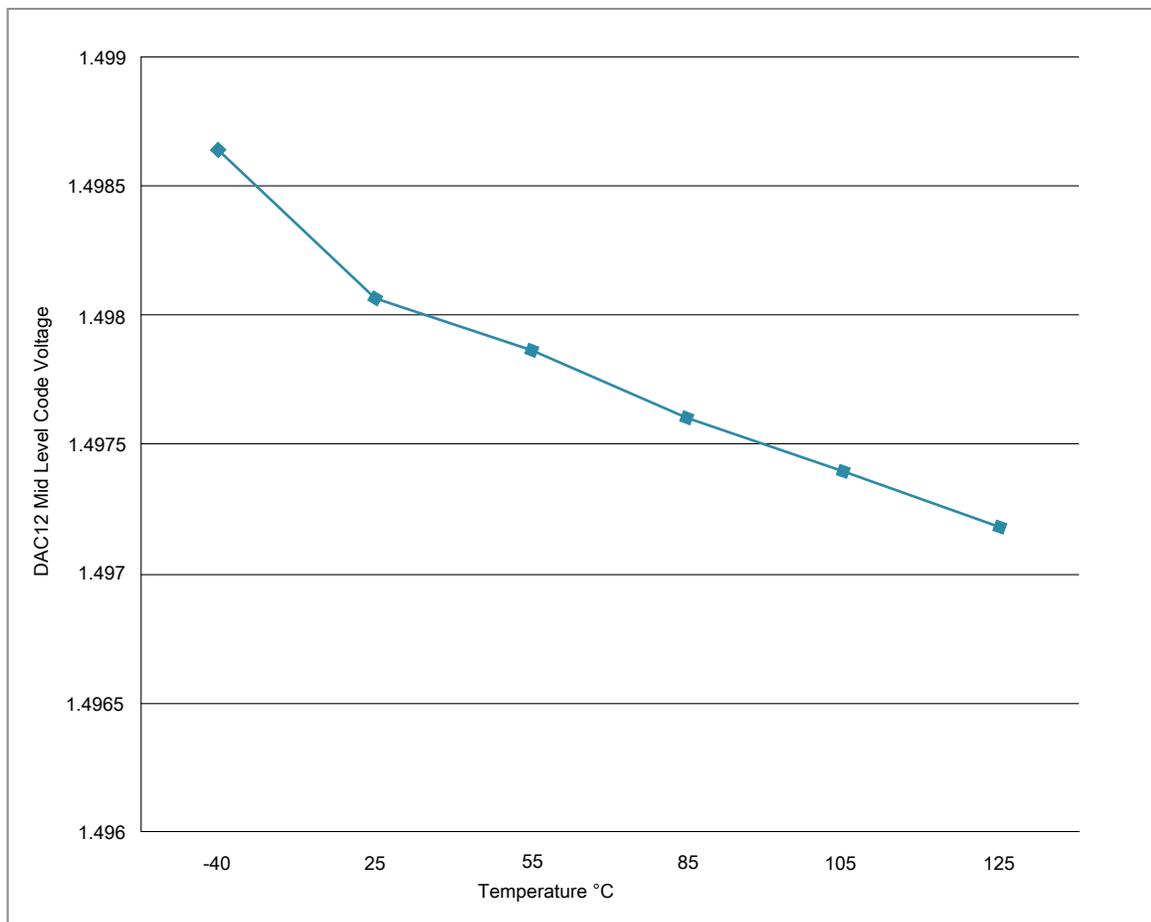
**Figure 16. Typical INL error vs. digital code**

**Figure 17. Offset at half scale vs. temperature**

## 3.6.4   Voltage reference electrical specifications

**Table 28.   VREF full-range operating requirements**

| Symbol | Description | Min. | Max. | Unit | Notes |
|--------|-------------|------|------|------|-------|
| $V_{DDA}$ | Supply voltage | 1.71 | 3.6 | V | |
| $T_A$ | Temperature | Operating temperature range of the device | | °C | |
| $C_L$ | Output load capacitance | 100 | | nF | 1, 2 |

1. $C_L$ must be connected to VREF_OUT if the VREF_OUT functionality is being used for either an internal or external reference.
2. The load capacitance should not exceed +/-25% of the nominal specified $C_L$ value over the operating temperature range of the device.

**Table 29. VREF full-range operating behaviors**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $V_{out}$ | Voltage reference output with factory trim at nominal $V_{DDA}$ and temperature=25°C | 1.1920 | 1.1950 | 1.1980 | V | 1 |
| $V_{out}$ | Voltage reference output with user trim at nominal $V_{DDA}$ and temperature=25°C | 1.1945 | 1.1950 | 1.1955 | V | 1 |
| $V_{step}$ | Voltage reference trim step | — | 0.5 | — | mV | 1 |
| $V_{tdrift}$ | Temperature drift (Vmax -Vmin across the full temperature range) | — | — | 15 | mV | 1 |
| $I_{bg}$ | Bandgap only current | — | — | 80 | µA | |
| $I_{lp}$ | Low-power buffer current | — | — | 360 | uA | 1 |
| $I_{hp}$ | High-power buffer current | — | — | 1 | mA | 1 |
| $\Delta V_{LOAD}$ | Load regulation<br>• current = ± 1.0 mA | <br>— | <br>200 | <br>— | µV | 1, 2 |
| $T_{stup}$ | Buffer startup time | — | — | 100 | µs | |
| $T_{chop\_osc\_stup}$ | Internal bandgap start-up delay with chop oscillator enabled | — | — | 35 | ms | |
| $V_{vdrift}$ | Voltage drift (Vmax -Vmin across the full voltage range) | — | 2 | — | mV | 1 |

1. See the chip's Reference Manual for the appropriate settings of the VREF Status and Control register.
2. Load regulation voltage is the difference between the VREF_OUT voltage with no load vs. voltage with defined load

**Table 30. VREF limited-range operating requirements**

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $T_A$ | Temperature | 0 | 70 | °C | |

**Table 31. VREF limited-range operating behaviors**

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $V_{tdrift}$ | Temperature drift ($V_{max}$ -$V_{min}$ across the limited temperature range) | — | 10 | mV | |

## 3.7 Timers

See General switching specifications.

## 3.8 Communication interfaces

## 3.8.1 DSPI switching specifications (limited voltage range)

The Deserial Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provide DSPI timing characteristics for classic SPI timing modes. Refer to the SPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

**Table 32.   Master mode DSPI timing (limited voltage range)**

| Num | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
|  | Operating voltage | 2.7 | 3.6 | V |  |
|  | Frequency of operation | — | 25 | MHz |  |
| DS1 | DSPI_SCK output cycle time | $2 \times t_{BUS}$ | — | ns |  |
| DS2 | DSPI_SCK output high/low time | $(t_{SCK}/2) - 2$ | $(t_{SCK}/2) + 2$ | ns |  |
| DS3 | DSPI_PCS*n* valid to DSPI_SCK delay | $(t_{BUS} \times 2) - 2$ | — | ns | 1 |
| DS4 | DSPI_SCK to DSPI_PCS*n* invalid delay | $(t_{BUS} \times 2) - 2$ | — | ns | 2 |
| DS5 | DSPI_SCK to DSPI_SOUT valid | — | 8.5 | ns |  |
| DS6 | DSPI_SCK to DSPI_SOUT invalid | -2 | — | ns |  |
| DS7 | DSPI_SIN to DSPI_SCK input setup | 16.2 | — | ns |  |
| DS8 | DSPI_SCK to DSPI_SIN input hold | 0 | — | ns |  |

1. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].
2. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].
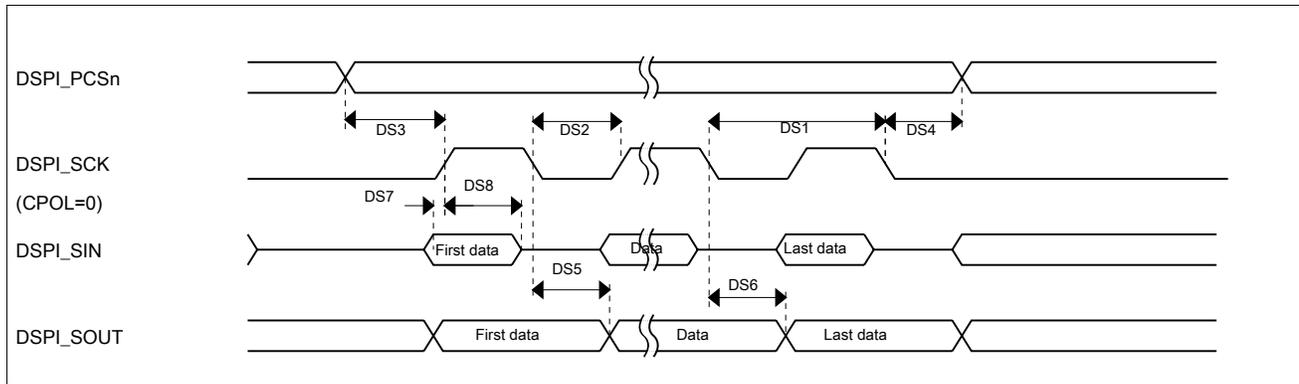


**Figure 18. DSPI classic SPI timing — master mode**

**Table 33.  Slave mode DSPI timing (limited voltage range)**

| Num | Description | Min. | Max. | Unit | Notes |
|------|-------------|------|------|------|-------|
|  | Operating voltage | 2.7 | 3.6 | V | |
|  | Frequency of operation | — | 12.5 | MHz | 1 |
| DS9 | DSPI_SCK input cycle time | 4 x $t_{BUS}$ | — | ns | |
| DS10 | DSPI_SCK input high/low time | $(t_{SCK}/2) - 2$ | $(t_{SCK}/2) + 2$ | ns | |
| DS11 | DSPI_SCK to DSPI_SOUT valid | — | 21.4 | ns | |
| DS12 | DSPI_SCK to DSPI_SOUT invalid | 0 | — | ns | |
| DS13 | DSPI_SIN to DSPI_SCK input setup | 2.6 | — | ns | |
| DS14 | DSPI_SCK to DSPI_SIN input hold | 7 | — | ns | |
| DS15 | $\overline{DSPI\_SS}$ active to DSPI_SOUT driven | — | 17 | ns | |
| DS16 | $\overline{DSPI\_SS}$ inactive to DSPI_SOUT not driven | — | 17 | ns | |

1. The maximum operating frequency is measured with noncontinuous CS and SCK. When DSPI is configured with continuous CS and SCK, the SPI clock must not be greater than 1/6 of the bus clock. For example, when the bus clock is 60 MHz, the SPI clock must not be greater than 10 MHz.
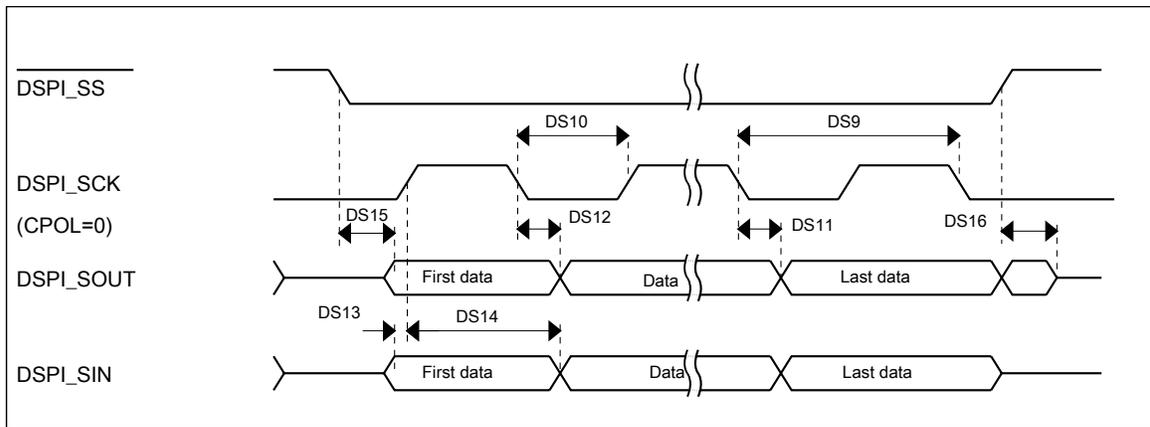


**Figure 19. DSPI classic SPI timing — slave mode**

## 3.8.2  DSPI switching specifications (full voltage range)

The Deserial Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provides DSPI timing characteristics for classic SPI timing modes. Refer to the SPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

**Table 34.  Master mode DSPI timing (full voltage range)**

| Num | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| | Operating voltage | 1.71 | 3.6 | V | 1 |
| | Frequency of operation | — | 12.5 | MHz | |
| DS1 | DSPI_SCK output cycle time | $4 \times t_{BUS}$ | — | ns | |
| DS2 | DSPI_SCK output high/low time | $(t_{SCK}/2) - 4$ | $(t_{SCK/2}) + 4$ | ns | |
| DS3 | DSPI_PCS$n$ valid to DSPI_SCK delay | $(t_{BUS} \times 2) - 4$ | — | ns | 2 |
| DS4 | DSPI_SCK to DSPI_PCS$n$ invalid delay | $(t_{BUS} \times 2) - 4$ | — | ns | 3 |
| DS5 | DSPI_SCK to DSPI_SOUT valid | — | 10 | ns | |
| DS6 | DSPI_SCK to DSPI_SOUT invalid | -4.5 | — | ns | |
| DS7 | DSPI_SIN to DSPI_SCK input setup | 24.6 | — | ns | |
| DS8 | DSPI_SCK to DSPI_SIN input hold | 0 | — | ns | |

1. The DSPI module can operate across the entire operating voltage for the processor, but to run across the full voltage range the maximum frequency of operation is reduced.
2. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].
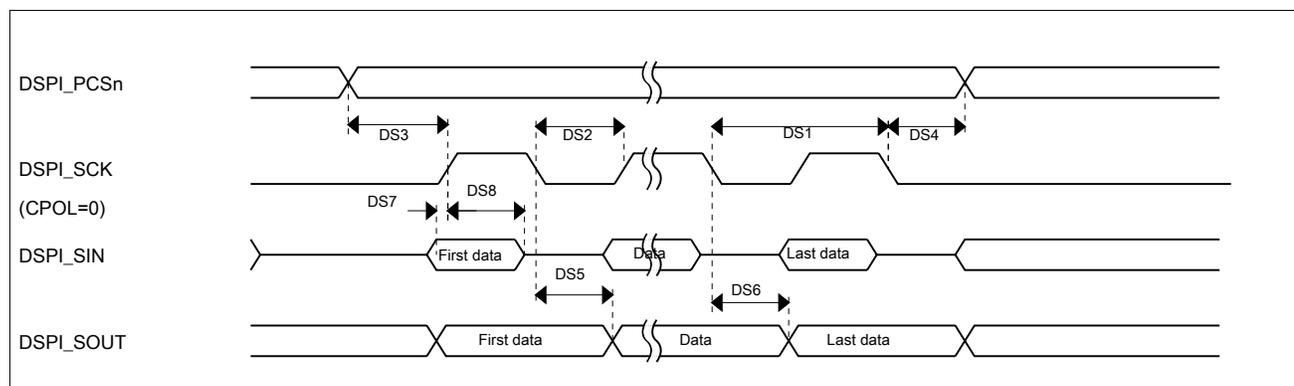3. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].



**Figure 20. DSPI classic SPI timing — master mode**

**Table 35. Slave mode DSPI timing (full voltage range)**

| Num | Description | Min. | Max. | Unit |
|-----|-------------|------|------|------|
| | Operating voltage | 1.71 | 3.6 | V |
| | Frequency of operation | — | 6.25 | MHz |
| DS9 | DSPI_SCK input cycle time | $8 \times t_{BUS}$ | — | ns |
| DS10 | DSPI_SCK input high/low time | $(t_{SCK}/2) - 4$ | $(t_{SCK/2}) + 4$ | ns |
| DS11 | DSPI_SCK to DSPI_SOUT valid | — | 29.5 | ns |
| DS12 | DSPI_SCK to DSPI_SOUT invalid | 0 | — | ns |
| DS13 | DSPI_SIN to DSPI_SCK input setup | 3.2 | — | ns |
| DS14 | DSPI_SCK to DSPI_SIN input hold | 7 | — | ns |
| DS15 | $\overline{DSPI\_SS}$ active to DSPI_SOUT driven | — | 25 | ns |
| DS16 | $\overline{DSPI\_SS}$ inactive to DSPI_SOUT not driven | — | 25 | ns |
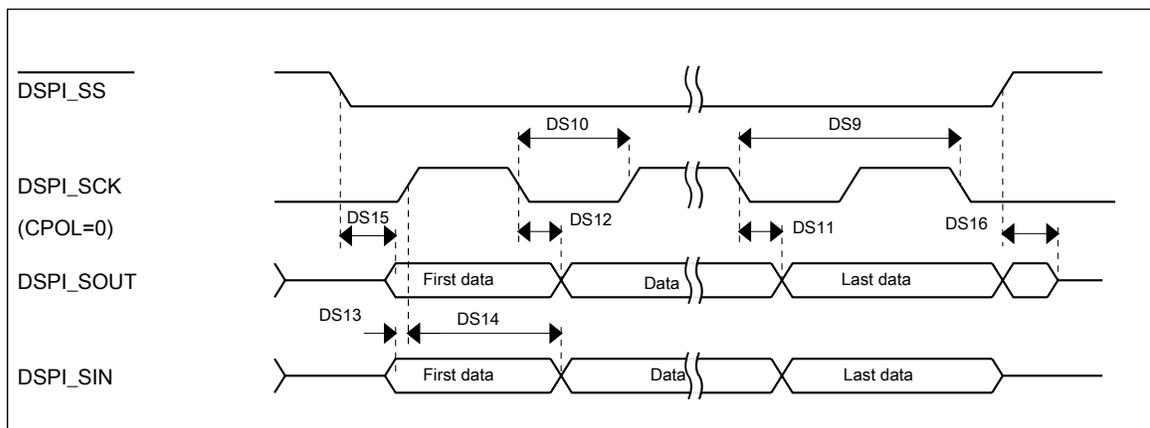


**Figure 21. DSPI classic SPI timing — slave mode**

## 3.8.3  Inter-Integrated Circuit Interface (I$^2$C) timing

**Table 36.  I $^2$C timing**

| Characteristic | Symbol | Standard Mode | | Fast Mode | | Unit |
|----------------|--------|---------------|---------|-----------|---------|------|
| | | Minimum | Maximum | Minimum | Maximum | |
| SCL Clock Frequency | $f_{SCL}$ | 0 | 100 | 0 | 400[1] | kHz |
| Hold time (repeated) START condition. After this period, the first clock pulse is generated. | $t_{HD}$; STA | 4 | — | 0.6 | — | µs |
| LOW period of the SCL clock | $t_{LOW}$ | 4.7 | — | 1.25 | — | µs |
| HIGH period of the SCL clock | $t_{HIGH}$ | 4 | — | 0.6 | — | µs |
| Set-up time for a repeated START condition | $t_{SU}$; STA | 4.7 | — | 0.6 | — | µs |

*Table continues on the next page...*

## Table 36.  I $^2$C timing (continued)

| Characteristic | Symbol | Standard Mode | | Fast Mode | | Unit |
|---|---|---|---|---|---|---|
| | | Minimum | Maximum | Minimum | Maximum | |
| Data hold time for I2C bus devices | $t_{HD}$; DAT | 0[2] | 3.45[3] | 0[4] | 0.9[2] | µs |
| Data set-up time | $t_{SU}$; DAT | 250[5] | — | 100[3, 6] | — | ns |
| Rise time of SDA and SCL signals | $t_r$ | — | 1000 | 20 +0.1$C_b$[7] | 300 | ns |
| Fall time of SDA and SCL signals | $t_f$ | — | 300 | 20 +0.1$C_b$[6] | 300 | ns |
| Set-up time for STOP condition | $t_{SU}$; STO | 4 | — | 0.6 | — | µs |
| Bus free time between STOP and START condition | $t_{BUF}$ | 4.7 | — | 1.3 | — | µs |
| Pulse width of spikes that must be suppressed by the input filter | $t_{SP}$ | N/A | N/A | 0 | 50 | ns |

1. The maximum SCL Clock Frequency in Fast mode with maximum bus loading can only be achieved when using the High drive pins across the full voltage range and when using the Normal drive pins and VDD ≥ 2.7 V.
2. The master mode I2C deasserts ACK of an address byte simultaneously with the falling edge of SCL. If no slaves acknowledge this address byte, then a negative hold time can result, depending on the edge rates of the SDA and SCL lines.
3. The maximum tHD; DAT must be met only if the device does not stretch the LOW period (tLOW) of the SCL signal.
4. Input signal Slew = 10 ns and Output Load = 50 pF
5. Set-up time in slave-transmitter mode is 1 IPBus clock period, if the TX FIFO is empty.
6. A Fast mode I2C bus device can be used in a Standard mode I2C bus system, but the requirement $t_{SU; DAT}$ ≥ 250 ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, then it must output the next data bit to the SDA line $t_{rmax}$ + $t_{SU; DAT}$ = 1000 + 250 = 1250 ns (according to the Standard mode I2C bus specification) before the SCL line is released.
7. $C_b$ = total capacitance of the one bus line in pF.

## Table 37.  I $^2$C 1 Mbps timing

| Characteristic | Symbol | Minimum | Maximum | Unit |
|---|---|---|---|---|
| SCL Clock Frequency | $f_{SCL}$ | 0 | 1[1] | MHz |
| Hold time (repeated) START condition. After this period, the first clock pulse is generated. | $t_{HD}$; STA | 0.26 | — | µs |
| LOW period of the SCL clock | $t_{LOW}$ | 0.5 | — | µs |
| HIGH period of the SCL clock | $t_{HIGH}$ | 0.26 | — | µs |
| Set-up time for a repeated START condition | $t_{SU}$; STA | 0.26 | — | µs |
| Data hold time for I2C bus devices | $t_{HD}$; DAT | 0 | — | µs |
| Data set-up time | $t_{SU}$; DAT | 50 | — | ns |
| Rise time of SDA and SCL signals | $t_r$ | 20 +0.1$C_b$, [2] | 120 | ns |
| Fall time of SDA and SCL signals | $t_f$ | 20 +0.1$C_b$[2] | 120 | ns |
| Set-up time for STOP condition | $t_{SU}$; STO | 0.26 | — | µs |
| Bus free time between STOP and START condition | $t_{BUF}$ | 0.5 | — | µs |
| Pulse width of spikes that must be suppressed by the input filter | $t_{SP}$ | 0 | 50 | ns |

1. The maximum SCL clock frequency of 1 Mbps can support maximum bus loading when using the High drive pins across the full voltage range.
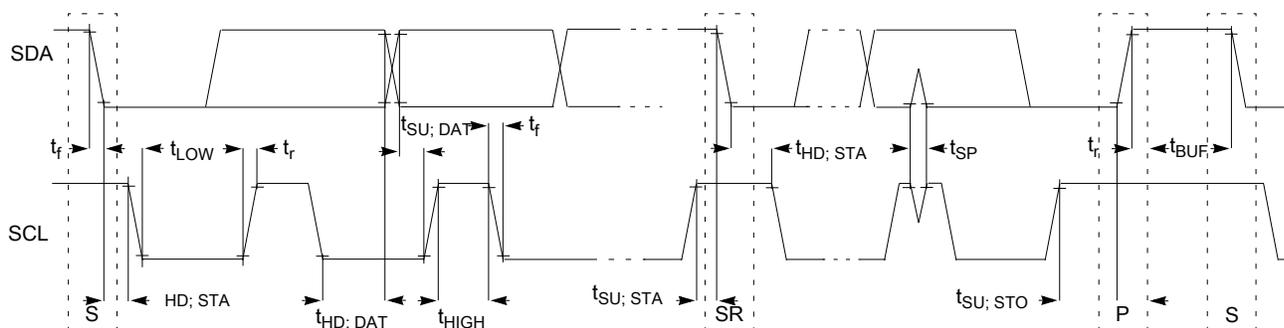2. $C_b$ = total capacitance of the one bus line in pF.

**Figure 22. Timing definition for devices on the I²C bus**

### 3.8.4   UART switching specifications

See General switching specifications.

## 3.9   Kinetis Motor Suite

Kinetis Motor Suite is a bundled software solution that enables the rapid configuration of motor drive systems, and accelerates development of the final motor drive application.

Several members of the KV3x family are enabled with Kinetis motor suite. The enabled devices can be identified within the orderable part numbers in this table. For more information refer to Kinetis Motor Suite User's Guide (KMS100UG) and Kinetis Motor Suite API Reference Manual (KMS100RM).

**NOTE**

To find the associated resource, go to freescale.com and perform a search using Document ID.

# 4   Dimensions

## 4.1   Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to freescale.com and perform a keyword search for the drawing's document number:

| If you want the drawing for this package | Then use this document number |
|---|---|
| 32-pin QFN | 98ARE10566D |
| 48-pin LQFP | 98ASH00962A |
| 64-pin LQFP | 98ASS23234W |

# 5 Pinout

## 5.1 KV30F Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

| 64 LQFP | 48 LQFP | 32 QFN | Pin Name | Default | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | — | — | PTE0/ CLKOUT32K | ADC1_SE4a | ADC1_SE4a | PTE0/ CLKOUT32K | | UART1_TX | | | | |
| 2 | — | — | PTE1/ LLWU_P0 | ADC1_SE5a | ADC1_SE5a | PTE1/ LLWU_P0 | | UART1_RX | | | | |
| 3 | 1 | 1 | VDD | VDD | VDD | | | | | | | |
| 4 | 2 | 2 | VSS | VSS | VSS | | | | | | | |
| 5 | 3 | 3 | PTE16 | ADC0_SE4a/ ADC0_DP1/ ADC1_DP2 | ADC0_SE4a/ ADC0_DP1/ ADC1_DP2 | PTE16 | SPI0_PCS0 | UART1_TX | FTM_CLKIN0 | | FTM0_FLT3 | |
| 6 | 4 | 4 | PTE17 | ADC0_SE5a/ ADC0_DM1/ ADC1_DM2 | ADC0_SE5a/ ADC0_DM1/ ADC1_DM2 | PTE17 | SPI0_SCK | UART1_RX | FTM_CLKIN1 | | LPTMR0_ ALT3 | |
| 7 | 5 | 5 | PTE18 | ADC0_SE6a/ ADC1_DP1/ ADC0_DP2 | ADC0_SE6a/ ADC1_DP1/ ADC0_DP2 | PTE18 | SPI0_SOUT | UART1_CTS_ b | I2C0_SDA | | | |
| 8 | 6 | 6 | PTE19 | ADC0_SE7a/ ADC1_DM1/ ADC0_DM2 | ADC0_SE7a/ ADC1_DM1/ ADC0_DM2 | PTE19 | SPI0_SIN | UART1_RTS_ b | I2C0_SCL | | | |
| 9 | 7 | — | ADC0_DP0/ ADC1_DP3 | ADC0_DP0/ ADC1_DP3 | ADC0_DP0/ ADC1_DP3 | | | | | | | |
| 10 | 8 | — | ADC0_DM0/ ADC1_DM3 | ADC0_DM0/ ADC1_DM3 | ADC0_DM0/ ADC1_DM3 | | | | | | | |
| 11 | — | — | ADC1_DP0/ ADC0_DP3 | ADC1_DP0/ ADC0_DP3 | ADC1_DP0/ ADC0_DP3 | | | | | | | |
| 12 | — | — | ADC1_DM0/ ADC0_DM3 | ADC1_DM0/ ADC0_DM3 | ADC1_DM0/ ADC0_DM3 | | | | | | | |
| 13 | 9 | 7 | VDDA | VDDA | VDDA | | | | | | | |

| 64 LQFP | 48 LQFP | 32 QFN | Pin Name | Default | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 14 | 10 | 7 | VREFH | VREFH | VREFH | | | | | | | |
| 15 | 11 | 8 | VREFL | VREFL | VREFL | | | | | | | |
| 16 | 12 | 8 | VSSA | VSSA | VSSA | | | | | | | |
| 17 | 13 | — | VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18 | VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18 | VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18 | | | | | | | |
| 18 | 14 | 9 | DAC0_OUT/ CMP1_IN3/ ADC0_SE23 | DAC0_OUT/ CMP1_IN3/ ADC0_SE23 | DAC0_OUT/ CMP1_IN3/ ADC0_SE23 | | | | | | | |
| 19 | — | — | CMP0_IN4/ ADC1_SE23 | CMP0_IN4/ ADC1_SE23 | CMP0_IN4/ ADC1_SE23 | | | | | | | |
| 20 | 15 | 10 | PTE24 | ADC0_SE17 | ADC0_SE17 | PTE24 | | FTM0_CH0 | | I2C0_SCL | EWM_OUT_b | |
| 21 | 16 | 11 | PTE25 | ADC0_SE18 | ADC0_SE18 | PTE25 | | FTM0_CH1 | | I2C0_SDA | EWM_IN | |
| 22 | 17 | 12 | PTA0 | JTAG_TCLK/ SWD_CLK | | PTA0 | UART0_CTS_b | FTM0_CH5 | | EWM_IN | | JTAG_TCLK/ SWD_CLK |
| 23 | 18 | 13 | PTA1 | JTAG_TDI | | PTA1 | UART0_RX | FTM2_CH0 | CMP0_OUT | FTM2_QD_PHA | FTM1_CH1 | JTAG_TDI |
| 24 | 19 | 14 | PTA2 | JTAG_TDO/ TRACE_SWO | | PTA2 | UART0_TX | FTM2_CH1 | CMP1_OUT | FTM2_QD_PHB | FTM1_CH0 | JTAG_TDO/ TRACE_SWO |
| 25 | 20 | 15 | PTA3 | JTAG_TMS/ SWD_DIO | | PTA3 | UART0_RTS_b | FTM0_CH0 | FTM2_FLT0 | EWM_OUT_b | | JTAG_TMS/ SWD_DIO |
| 26 | 21 | 16 | PTA4/ LLWU_P3 | NMI_b | | PTA4/ LLWU_P3 | | FTM0_CH1 | | FTM0_FLT3 | | NMI_b |
| 27 | — | — | PTA5 | DISABLED | | PTA5 | | FTM0_CH2 | | | | JTAG_TRST_b |
| 28 | — | — | PTA12 | DISABLED | | PTA12 | | FTM1_CH0 | | | | FTM1_QD_PHA |
| 29 | — | — | PTA13/ LLWU_P4 | DISABLED | | PTA13/ LLWU_P4 | | FTM1_CH1 | | | | FTM1_QD_PHB |
| 30 | 22 | — | VDD | VDD | VDD | | | | | | | |
| 31 | 23 | — | VSS | VSS | VSS | | | | | | | |
| 32 | 24 | 17 | PTA18 | EXTAL0 | EXTAL0 | PTA18 | | FTM0_FLT2 | FTM_CLKIN0 | | | |
| 33 | 25 | 18 | PTA19 | XTAL0 | XTAL0 | PTA19 | FTM0_FLT0 | FTM1_FLT0 | FTM_CLKIN1 | | LPTMR0_ALT1 | |
| 34 | 26 | 19 | RESET_b | RESET_b | RESET_b | | | | | | | |
| 35 | 27 | 20 | PTB0/ LLWU_P5 | ADC0_SE8/ ADC1_SE8 | ADC0_SE8/ ADC1_SE8 | PTB0/ LLWU_P5 | I2C0_SCL | FTM1_CH0 | | | FTM1_QD_PHA | UART0_RX |
| 36 | 28 | 21 | PTB1 | ADC0_SE9/ ADC1_SE9 | ADC0_SE9/ ADC1_SE9 | PTB1 | I2C0_SDA | FTM1_CH1 | FTM0_FLT2 | EWM_IN | FTM1_QD_PHB | UART0_TX |
| 37 | 29 | — | PTB2 | ADC0_SE12 | ADC0_SE12 | PTB2 | I2C0_SCL | UART0_RTS_b | FTM0_FLT1 | | FTM0_FLT3 | |
| 38 | 30 | — | PTB3 | ADC0_SE13 | ADC0_SE13 | PTB3 | I2C0_SDA | UART0_CTS_b | | | FTM0_FLT0 | |
| 39 | 31 | — | PTB16 | DISABLED | | PTB16 | | UART0_RX | FTM_CLKIN0 | | EWM_IN | |

**Pinout**

| 64 LQFP | 48 LQFP | 32 QFN | Pin Name | Default | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 40 | 32 | — | PTB17 | DISABLED | | PTB17 | | UART0_TX | FTM_CLKIN1 | | EWM_OUT_b | |
| 41 | — | — | PTB18 | DISABLED | | PTB18 | | FTM2_CH0 | | | FTM2_QD_PHA | |
| 42 | — | — | PTB19 | DISABLED | | PTB19 | | FTM2_CH1 | | | FTM2_QD_PHB | |
| 43 | 33 | — | PTC0 | ADC0_SE14 | ADC0_SE14 | PTC0 | SPI0_PCS4 | PDB0_EXTRG | | CMP0_OUT | FTM0_FLT1 | SPI0_PCS0 |
| 44 | 34 | 22 | PTC1/LLWU_P6 | ADC0_SE15 | ADC0_SE15 | PTC1/LLWU_P6 | SPI0_PCS3 | UART1_RTS_b | FTM0_CH0 | FTM2_CH0 | | |
| 45 | 35 | 23 | PTC2 | ADC0_SE4b/CMP1_IN0 | ADC0_SE4b/CMP1_IN0 | PTC2 | SPI0_PCS2 | UART1_CTS_b | FTM0_CH1 | FTM2_CH1 | | |
| 46 | 36 | 24 | PTC3/LLWU_P7 | CMP1_IN1 | CMP1_IN1 | PTC3/LLWU_P7 | SPI0_PCS1 | UART1_RX | FTM0_CH2 | CLKOUT | | |
| 47 | — | — | VSS | VSS | VSS | | | | | | | |
| 48 | — | — | VDD | VDD | VDD | | | | | | | |
| 49 | 37 | 25 | PTC4/LLWU_P8 | DISABLED | | PTC4/LLWU_P8 | SPI0_PCS0 | UART1_TX | FTM0_CH3 | | CMP1_OUT | |
| 50 | 38 | 26 | PTC5/LLWU_P9 | DISABLED | | PTC5/LLWU_P9 | SPI0_SCK | LPTMR0_ALT2 | | CMP0_OUT | FTM0_CH2 | |
| 51 | 39 | 27 | PTC6/LLWU_P10 | CMP0_IN0 | CMP0_IN0 | PTC6/LLWU_P10 | SPI0_SOUT | PDB0_EXTRG | | UART0_RX | | I2C0_SCL |
| 52 | 40 | 28 | PTC7 | CMP0_IN1 | CMP0_IN1 | PTC7 | SPI0_SIN | | | UART0_TX | | I2C0_SDA |
| 53 | — | — | PTC8 | ADC1_SE4b/CMP0_IN2 | ADC1_SE4b/CMP0_IN2 | PTC8 | | | | | | |
| 54 | — | — | PTC9 | ADC1_SE5b/CMP0_IN3 | ADC1_SE5b/CMP0_IN3 | PTC9 | | | | | FTM2_FLT0 | |
| 55 | — | — | PTC10 | ADC1_SE6b | ADC1_SE6b | PTC10 | | | | | | |
| 56 | — | — | PTC11/LLWU_P11 | ADC1_SE7b | ADC1_SE7b | PTC11/LLWU_P11 | | | | | | |
| 57 | 41 | — | PTD0/LLWU_P12 | DISABLED | | PTD0/LLWU_P12 | SPI0_PCS0 | UART0_RTS_b | FTM0_CH0 | UART1_RX | | |
| 58 | 42 | — | PTD1 | ADC0_SE5b | ADC0_SE5b | PTD1 | SPI0_SCK | UART0_CTS_b | FTM0_CH1 | UART1_TX | | |
| 59 | 43 | — | PTD2/LLWU_P13 | DISABLED | | PTD2/LLWU_P13 | SPI0_SOUT | UART0_RX | FTM0_CH2 | | | I2C0_SCL |
| 60 | 44 | — | PTD3 | DISABLED | | PTD3 | SPI0_SIN | UART0_TX | FTM0_CH3 | | | I2C0_SDA |
| 61 | 45 | 29 | PTD4/LLWU_P14 | DISABLED | | PTD4/LLWU_P14 | SPI0_PCS1 | UART0_RTS_b | FTM0_CH4 | FTM2_CH0 | EWM_IN | |
| 62 | 46 | 30 | PTD5 | ADC0_SE6b | ADC0_SE6b | PTD5 | SPI0_PCS2 | UART0_CTS_b | FTM0_CH5 | FTM2_CH1 | EWM_OUT_b | |
| 63 | 47 | 31 | PTD6/LLWU_P15 | ADC0_SE7b | ADC0_SE7b | PTD6/LLWU_P15 | SPI0_PCS3 | UART0_RX | FTM0_CH0 | FTM1_CH0 | FTM0_FLT0 | |
| 64 | 48 | 32 | PTD7 | DISABLED | | PTD7 | | UART0_TX | FTM0_CH1 | FTM1_CH1 | FTM0_FLT1 | |

## 5.2 Recommended connection for unused analog and digital pins

The following table shows the recommended connections for analog interface pins if those analog interfaces are not used in the customer's application.

**Table 38. Recommended connection for unused analog interfaces**

| Pin Type | | Short recommendation | Detailed recommendation |
|---|---|---|---|
| Analog/non GPIO | PGAx/ADCx | Float | Analog input - Float |
| Analog/non GPIO | ADCx/CMPx | Float | Analog input - Float |
| Analog/non GPIO | VREF_OUT | Float | Analog output - Float |
| Analog/non GPIO | DACx_OUT | Float | Analog output - Float |
| Analog/non GPIO | RTC_WAKEUP_B | Float | Analog output - Float |
| Analog/non GPIO | XTAL32 | Float | Analog output - Float |
| Analog/non GPIO | EXTAL32 | Float | Analog input - Float |
| GPIO/Analog | PTA18/EXTAL0 | Float | Analog input - Float |
| GPIO/Analog | PTA19/XTAL0 | Float | Analog output - Float |
| GPIO/Analog | PTx/ADCx | Float | Float (default is analog input) |
| GPIO/Analog | PTx/CMPx | Float | Float (default is analog input) |
| GPIO/Digital | PTA0/JTAG_TCLK | Float | Float (default is JTAG with pulldown) |
| GPIO/Digital | PTA1/JTAG_TDI | Float | Float (default is JTAG with pullup) |
| GPIO/Digital | PTA2/JTAG_TDO | Float | Float (default is JTAG with pullup) |
| GPIO/Digital | PTA3/JTAG_TMS | Float | Float (default is JTAG with pullup) |
| GPIO/Digital | PTA4/NMI_b | 10kΩ pullup or disable and float | Pull high or disable in PCR & FOPT and float |
| GPIO/Digital | PTx | Float | Float (default is disabled) |
| VDDA | VDDA | Always connect to VDD potential | Always connect to VDD potential |
| VREFH | VREFH | Always connect to VDD potential | Always connect to VDD potential |
| VREFL | VREFL | Always connect to VSS potential | Always connect to VSS potential |
| VSSA | VSSA | Always connect to VSS potential | Always connect to VSS potential |

## 5.3  KV30F Pinouts

The below figure shows the pinout diagram for the devices supported by this document. Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, see the previous section.
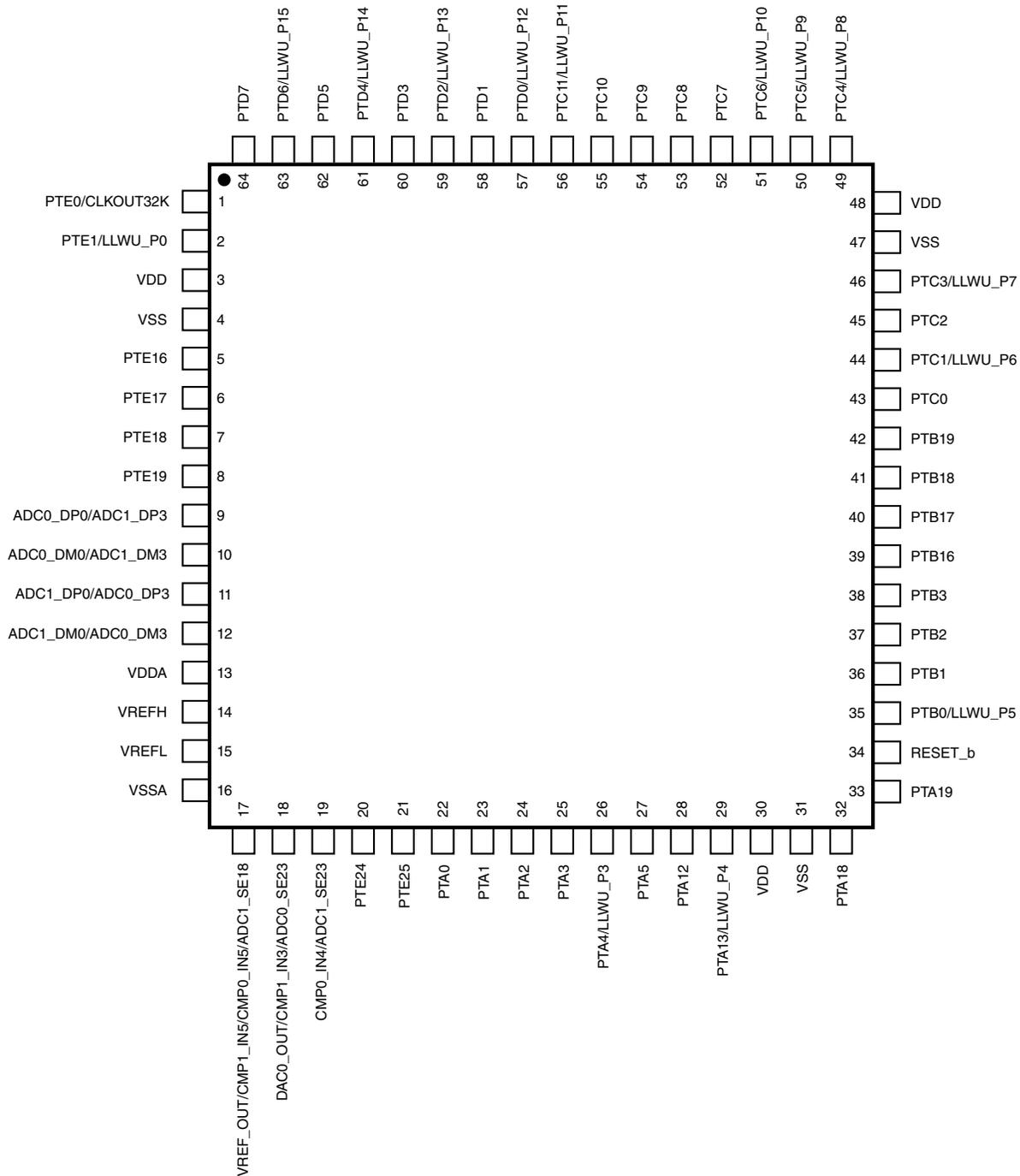


**Figure 23. KV30F 64 LQFP pinout diagram (top view)**
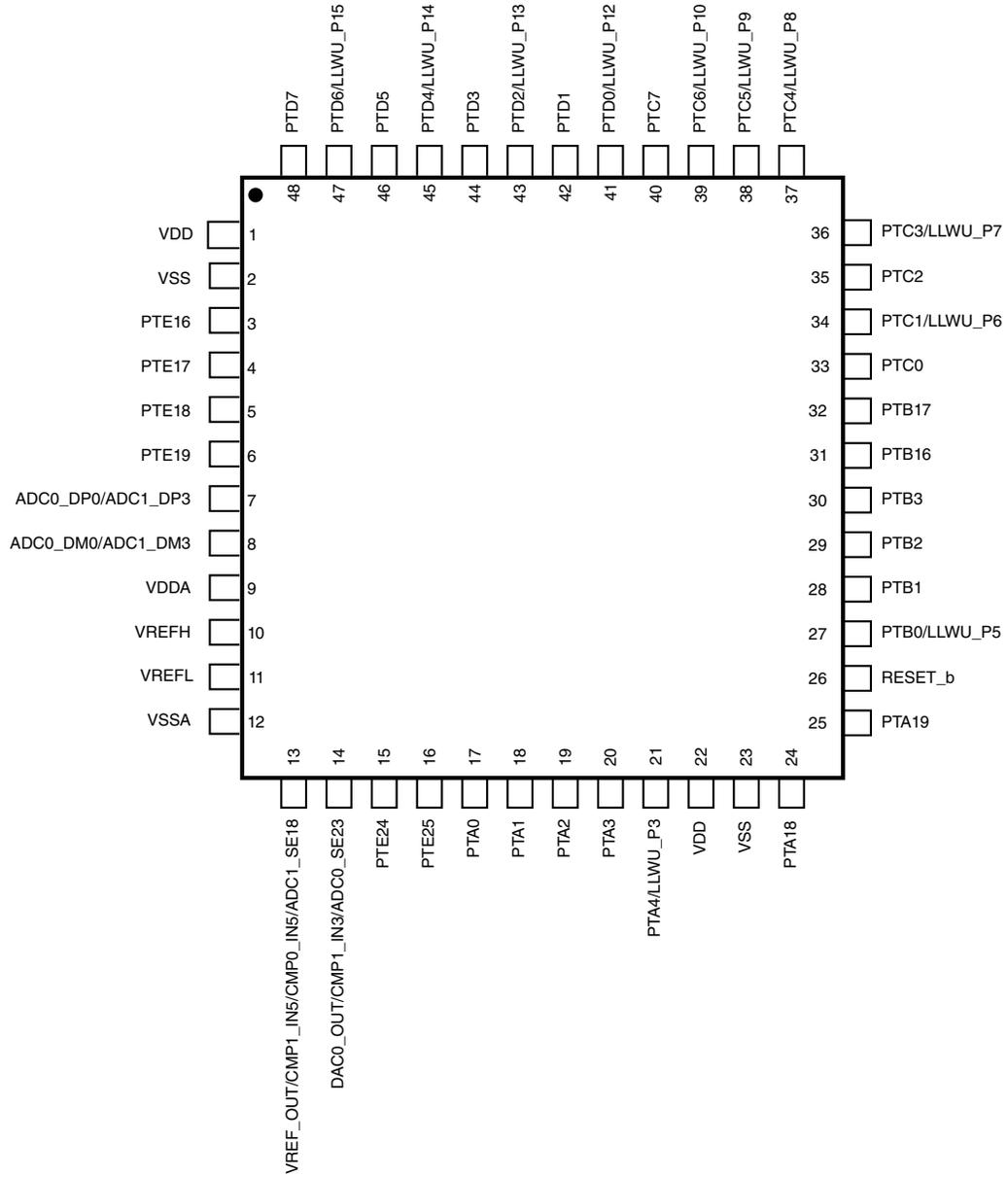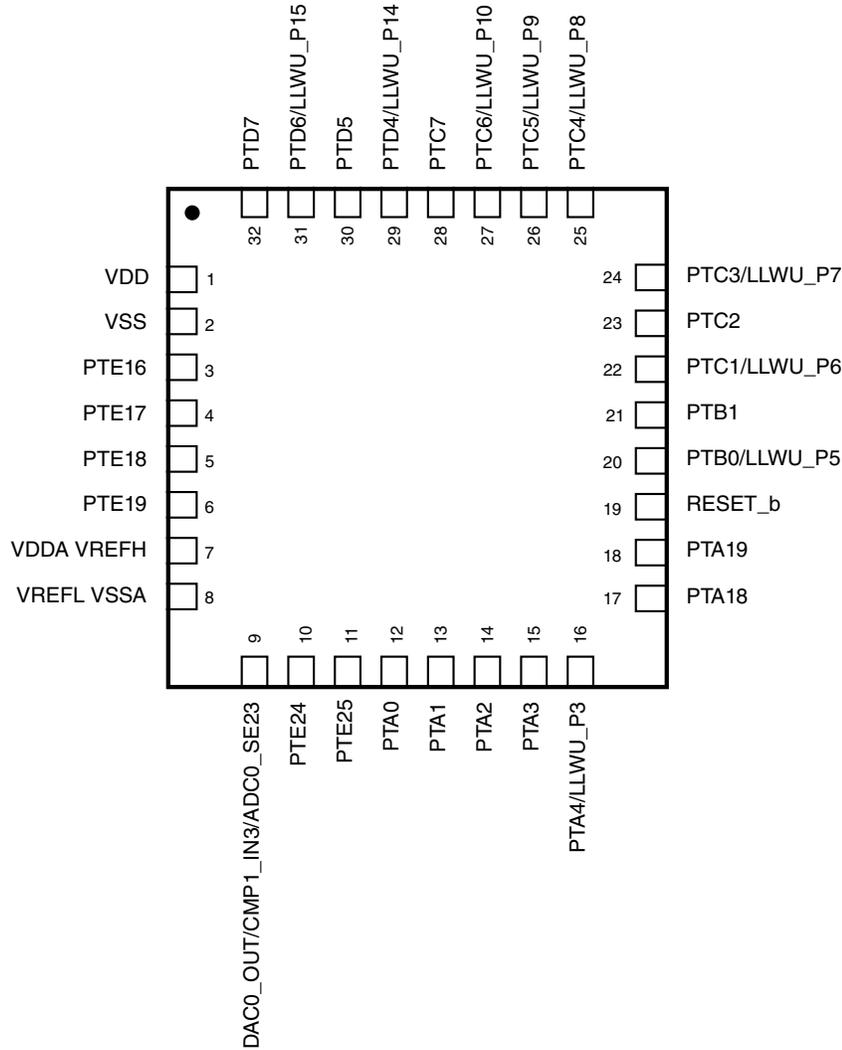
**Figure 24. KV30F 48 LQFP pinout diagram**

**Figure 25. KV30F 32 QFN pinout diagram (Transparent top view)**

# 6  Part identification

## 6.1  Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

## 6.2  Format

Part numbers for this device have the following format:

Q KV## A FFF R T PP CC S N


## 6.3  Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

| Field | Description | Values |
|-------|-------------|--------|
| Q | Qualification status | • M = Fully qualified, general market flow<br>• P = Prequalification |
| KV## | Kinetis V Series | • KV3x: Cortex-M4 based MCU |
| A | Key attribute | • D = Cortex-M4 w/ DSP<br>• F = Cortex-M4 w/ DSP and FPU |
| FFF | Program flash memory size | • 64 = 64 KB<br>• 128 = 128 KB<br>• 256 = 256 KB<br>• 512 = 512 KB |
| R | Silicon revision | • (Blank) = Main<br>• A = Revision after main |
| T | Temperature range (°C) | • V = −40 to 105<br>• C = −40 to 85 |
| PP | Package identifier | • FM = 32 QFN (5 mm x 5 mm)<br>• LF = 48 LQFP (7 mm x 7 mm)<br>• LH = 64 LQFP (10 mm x 10 mm)<br>• LL = 100 LQFP (14 mm x 14 mm)<br>• MC = 121 XFBGA (8 mm x 8 mm)<br>• DC = 121 XFBGA (8 mm x 8 mm x 0.5 mm) |
| CC | Maximum CPU frequency (MHz) | • 10 = 100 MHz<br>• 12 = 120 MHz |
| S | Software type | • P = KMS-PMSM and BLDC<br>• (Blank) = Not software enabled |
| N | Packaging type | • R = Tape and reel<br>• (Blank) = Trays |


## 6.4  Example

This is an example part number:

MKV30F128VLH10P

# 7 Terminology and guidelines

## 7.1 Definitions

Key terms are defined in the following table:

| Term | Definition |
|---|---|
| Rating | A minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:<br><br>• *Operating ratings* apply during operation of the chip.<br>• *Handling ratings* apply when the chip is not powered.<br><br>**NOTE:** The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings. |
| Operating requirement | A specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip |
| Operating behavior | A specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions |
| Typical value | A specified value for a technical characteristic that:<br><br>• Lies within the range of values specified by the operating behavior<br>• Is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions<br><br>**NOTE:** Typical values are provided as design guidelines and are neither tested nor guaranteed. |

## 7.2 Examples

*Operating rating*:

| Symbol | Description | Min. | Max. | Unit |
|--------|-------------|------|------|------|
| V$_{DD}$ | 1.0 V core supply voltage | −0.3 | 1.2 | V |

*Operating requirement*:

| Symbol | Description | Min. | Max. | Unit |
|--------|-------------|------|------|------|
| V$_{DD}$ | 1.0 V core supply voltage | 0.9 | 1.1 | V |

*Operating behavior* that includes a *typical value*:

| Symbol | Description | Min. | Typ. | Max. | Unit |
|--------|-------------|------|------|------|------|
| I$_{WP}$ | Digital I/O weak pullup/pulldown current | 10 | 70 | 130 | µA |

## 7.3 Typical-value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

| Symbol | Description | Value | Unit |
|--------|-------------|-------|------|
| T$_A$ | Ambient temperature | 25 | °C |
| V$_{DD}$ | Supply voltage | 3.3 | V |

## 7.4 Relationship between ratings and operating requirements

| Fatal range | Degraded operating range | Normal operating range | Degraded operating range | Fatal range |
|---|---|---|---|---|
| Expected permanent failure | - No permanent failure<br>- Possible decreased life<br>- Possible incorrect operation | - No permanent failure<br>- Correct operation | - No permanent failure<br>- Possible decreased life<br>- Possible incorrect operation | Expected permanent failure |

Operating rating (min.)    Operating requirement (min.)    Operating requirement (max.)    Operating rating (max.)

$-\infty$      $\infty$

Operating (power on)

| Fatal range | Handling range | Fatal range |
|---|---|---|
| Expected permanent failure | No permanent failure | Expected permanent failure |

Handling rating (min.)        Handling rating (max.)

$-\infty$      $\infty$

Handling (power off)

## 7.5 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

# 8 Revision History

The following table provides a revision history for this document.

**Table 39.  Revision History**

| Rev. No. | Date | Substantial Changes |
|---|---|---|
| 4 | 02/2016 | • In "Power consumption operating behaviors" table, added "Low power mode peripheral adders—typical value" table<br>• In "Thermal operating requirements" table, in footnote, corrected "$T_J = T_A + \Theta_{JA}$" to "$T_J = T_A + R_{\Theta JA}$" |

*Table continues on the next page...*

## Table 39.  Revision History (continued)

| Rev. No. | Date | Substantial Changes |
|---|---|---|
| | | • In "Slave mode DSPI timing (limited voltage range)" table, added footnote regarding maximum frequency of operation<br>• Added new section, "Recommended connections for unused analog and digital pins"<br>• Added Terminology and Guidelines section<br>• Updated Thermal Attributes value for 48LQFP<br>• Added KMS related information in front matter<br>• Added Kinetis Motor Suite section<br>• Added "S" in Format and Part Identification table<br>• Updated the Part Number Example<br>• Deleted Package Your Way footnote attached to 48 LQFP |
| 3 | 4/2015 | • Throughout: Modified notes related to 48-pin LQFP to say, "The 48-pin LQFP package for this product is not yet available; however, it is included in a Package Your Way program for Kinetis MCUs. Please visit www.Freescale.com/KPYW for more details."<br>• On page 1:<br>  • Under "Clocks," corrected second and third bullets—moved "with FLL" from "internal oscillators" to "multipurpose clock generator" bullet<br>  • Under "Communication interfaces," updated I$^2$C bullet to indicate support for up to 1 Mbps operation<br>  • Under "Operating characteristics," specified that voltage range includes flash writes<br>• In "Voltage and current operating requirements" table:<br>  • Removed content related to positive injection<br>  • Updated footnote 1 to say that all analog and I/O pins are internally clamped to $V_{SS}$ only (not $V_{SS}$ and $V_{DD}$)through ESD protection diodes.<br>• In "Power mode transition operating behaviors" table, removed rows for LLS2 and LLS3<br>• In "Power consumption operating behaviors" table:<br>  • Provided additional temperature data<br>  • Added Max IDD values based on characterization results equivalent to mean + 3 sigma<br>  • Removed rows for LLS2 and LLS3<br>• Updated "EMC radiated emissions operating behaviors" table<br>• In "Thermal operating requirements" table, added the following footnote for ambient temperature: "Maximum $T_A$ can be exceeded only if the user ensures that $T_J$ does not exceed maximum $T_J$. The simplest method to determine $T_J$ is: $T_J = T_A + \Theta_{JA}$ x chip power dissipation"<br>• Updated "IRC48M Specifications":<br>  • Updated maximum values for $\Delta_{firc48m\_lv}$ and $\Delta_{firc48m\_hv}$ (full temperature)<br>  • Added specifications for $\Delta_{firc48m\_hv}$ (-40°C to 85°C)<br>• In "I$^2$C timing" table,<br>  • Added the following footnote on maximum Fast mode value for SCL Clock Frequency: "The maximum SCL Clock Frequency in Fast mode with maximum bus loading can only be achieved when using the High drive pins across the full voltage range and when using the Normal drive pins and VDD ≥ 2.7 V."<br>  • Updated minimum Fast mode value for LOW period of the SCL clock to 1.25 µ<br>• Added "I$^2$C 1 Mbps timing" table<br>• Removed Section 6, "Ordering parts."<br>• Added "48-pin LQFP part marking" section<br>• Added "32-pin QFN part marking" section |
| 2 | 8/2014 | • On p. 1, under "Memories and memory interfaces," added bullet, "Preprogrammed Kinetis flashloader for one-time, in-system factory programming" |

*Table continues on the next page...*

## Table 39.   Revision History (continued)

| Rev. No. | Date | Substantial Changes |
|---|---|---|
|  |  | • On p. 1, added parenthetical element to the following bullet under "Analog modules":*Accurate internal voltage reference (not available for 32-pin QFN package)*<br>• In "Voltage and current operating ratings" section, updated digital supply current maximum value<br>• In "Voltage and current operating behaviors" section, updated input leakage information<br>• In "Power consumption operating behaviors table":<br>   • Updated existing typical and maximum power measurements<br>   • Added new typical power measurements for the following:<br>     • IDD_HSRUN (High Speed Run mode, all peripheral clocks disabled, current executing CoreMark code)<br>     • IDD_HSRUN (High Speed Run mode, all peripheral clocks disabled, current executing while(1) loop)<br>     • IDD_RUN (Run mode current in Compute operation, all peripheral clocks disabled, executing CoreMark code)<br>     • IDD_RUN (Run mode current in Compute operation, all peripheral clocks disabled, executing while(1) loop)<br>     • IDD_VLPR (Very Low Power mode current in Compute operation, all peripheral clocks disabled, executing CoreMark code)<br>     • IDD_VLPR (Very Low Power Run mode current in Compute operation, all peripheral clocks disabled, executing while(1) loop)<br>• Updated section, "EMC radiated emissions operating behaviors for 64 LQFP package"<br>• In "Thermal attributes" section, added 64-pin LQFP and 32-pin QFN package values<br>• Updated "MCG specifications" table<br>• Updated "VREF full-range operating behaviors" table<br>• In the "Part identification" section, added "Format" and "Fields" subsections |
| 1 | 3/2014 | Initial public release |

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