RLDRAM 3

IS49RL18320– 2 Meg x 18 x 16 Banks
IS49RL36160– 1 Meg x 36 x 16 Banks

Features

- 1066 MHz DDR operation (2133 Mb/s/ball data rate)
- 76.8 Gb/s peak bandwidth (x36 at 1066 MHz clock frequency)
- Organization
  - 32 Meg x 18, and 16 Meg x 36 common I/O (CIO)
  - 16 banks
- 1.2V center-terminated push/pull I/O
- 2.5V V_{EXT}, 1.35V V_{DD}, 1.2V V_{DDQ} I/O
- Reduced cycle time (^tRC (MIN) = 8 - 12ns)
- SDR addressing
- Programmable READ/WRITE latency (RL/WL) and burst length
- Data mask for WRITE commands
- Differential input clocks (CK, CK#)
- Free-running differential input data clocks (DKx, DKx#) and output data clocks (QKx, QKx#)
- On-die DLL generates CK edge-aligned data and differential output data clock signals
- 64ms refresh (128K refresh per 64ms)
- 168-ball FBGA package
- 40Ω or 60 Ω matched impedance outputs
- Integrated on-die termination (ODT)
- Single or multibank writes
- Extended operating range (200–1066 MHz)
- READ training register
- Multiplexed and non-multiplexed addressing capabilities
- Mirror function
- Output driver and ODT calibration
- JTAG interface (IEEE 1149.1-2001)

Options

- Clock cycle and ^tRC timing
  - 0.93ns and ^tRC (MIN) = 8ns (RL3-2133)
  - 0.93ns and ^tRC (MIN) = 10ns (RL3-2133)
  - 1.07ns and ^tRC (MIN) = 8ns (RL3-1866)
  - 1.07ns and ^tRC (MIN) = 10ns (RL3-1866)
  - 1.25ns and ^tRC (MIN) = 8ns (RL3-1600)
  - 1.25ns and ^tRC (MIN) = 10ns (RL3-1600)
  - 1.25ns and ^tRC (MIN) = 12ns (RL3-1600)
- Configuration
  - -32 Meg x 18
  - - 16 Meg x 36
- Operating Temperature
  - Commercial (T_C = 0° to +95°C)
  - Industrial (T_C = –40°C to +95°C)
- Package
  - 168-ball FBGA
  - 168-ball FBGA (Pb-free)
- Revision

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a.) the risk of injury or damage has been minimized;
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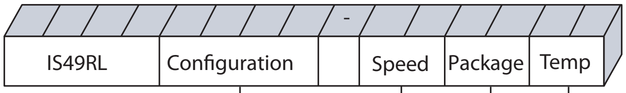
Figure 1: 576Mb RLDRAM® 3 Part Numbers

Example Part Number: IS49RL18320-093EBL



Configuration	
32 Meg x 18	18320
16 Meg x 36	36160

Temperature	
Commercial	None
Industrial	

Speed Grade	
-093E	^{t}CK = 0.93ns (8ns ^{t}RC)
-093	^{t}CK = 0.93ns (10ns ^{t}RC)
-107E	^{t}CK = 1.07ns (8ns ^{t}RC)
-107	^{t}CK = 1.07ns (10ns ^{t}RC)
-125F	^{t}CK = 1.25ns (8ns ^{t}RC)
-125E	^{t}CK = 1.25ns (10ns ^{t}RC)
-125	^{t}CK = 1.25ns (12ns ^{t}RC)

Package	
168-ball FBGA	B
168-ball FBGA (Pb-free)	BL

BGA Part Marking Decoder

Due to space limitations, BGA-packaged components have an abbreviated part marking that is different from the part number. ISSI'S BGA Part Marking Decoder is available on ISSI'S Web site at www.issi.com

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General Description

The ISSI® RLDRAM ® 3 is a high-speed memory device designed for high-bandwidth data storage—telecommunications, networking, cache applications, etc. The chip's 16-bank architecture is optimized for sustainable high-speed operation.

The DDR I/O interface transfers two data bits per clock cycle at the I/O balls. Output data is referenced to the READ strobes.

Commands, addresses, and control signals are also registered at every positive edge of the differential input clock, while input data is registered at both positive and negative edges of the input data strobes.

Read and write accesses to the RL3 device are burst-oriented. The burst length (BL) is programmable to 2, 4, or 8 by a setting in the mode register.

The device is supplied with 1.35V for the core and 1.2V for the output drivers. The 2.5V supply is used for an internal supply.

Bank-scheduled refresh is supported with the row address generated internally.

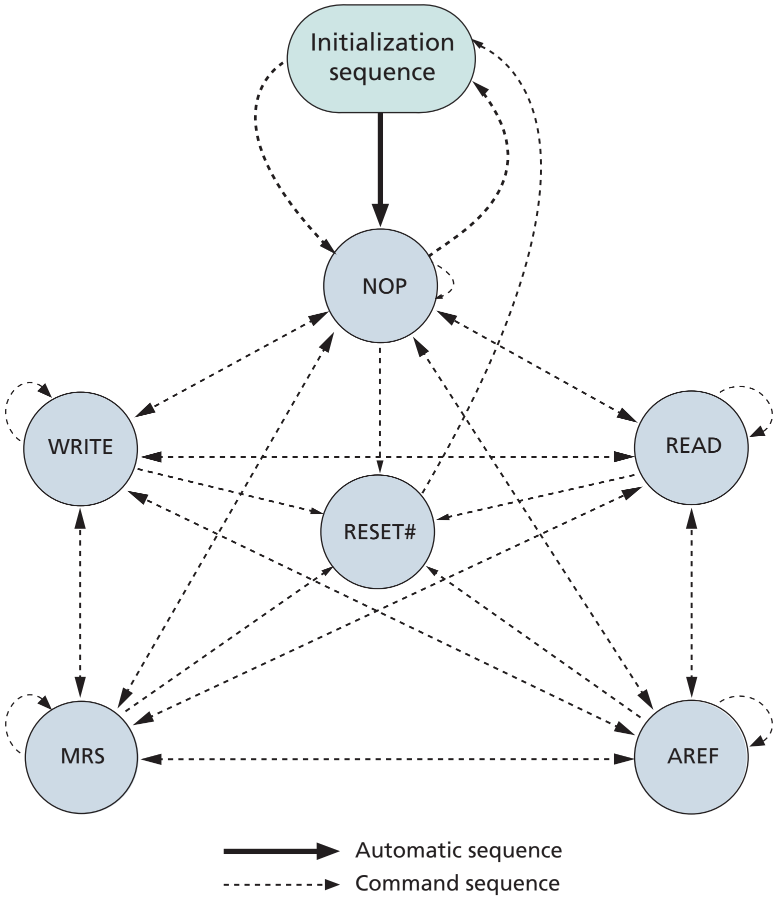
The 168-ball FBGA package is used to enable ultra-high-speed data transfer rates.

General Notes

- The functionality and the timing specifications discussed in this data sheet are for the DLL enable mode of operation.
- Any functionality not specifically stated is considered undefined, illegal, and not supported, and can result in unknown operation.
- Nominal conditions are assumed for specifications not defined within the figures shown in this data sheet.
- Throughout this data sheet, the terms "RLDRAM," "DRAM," and "RLDRAM 3" are all used interchangeably and refer to the RLDRAM 3 SDRAM device.
- References to DQ, DK, QK, DM, and QVLD are to be interpeted as each group collectively, unless specifically stated otherwise. This includes true and complement signals of differential signals.
- Non-multiplexed operation is assumed if not specified as multiplexed.
- A X36 Device supplies four QK/QK# sets. One per 9 DQs. If a user only wants to use two QK/QK# sets, this is allowed. The user needs to use QK0/QK0# and QK1/QK1#. QK0/QK0# will control DQ[8:0] & DQ[26:18]. QK1/QK1# will control DQ[17:9] & DQ[35:27]. The QK to DQ timing parameter to be used would be ^{t}QKQ02, ^{t}QKQ13. The unused QK/QK# pins should be left floating.

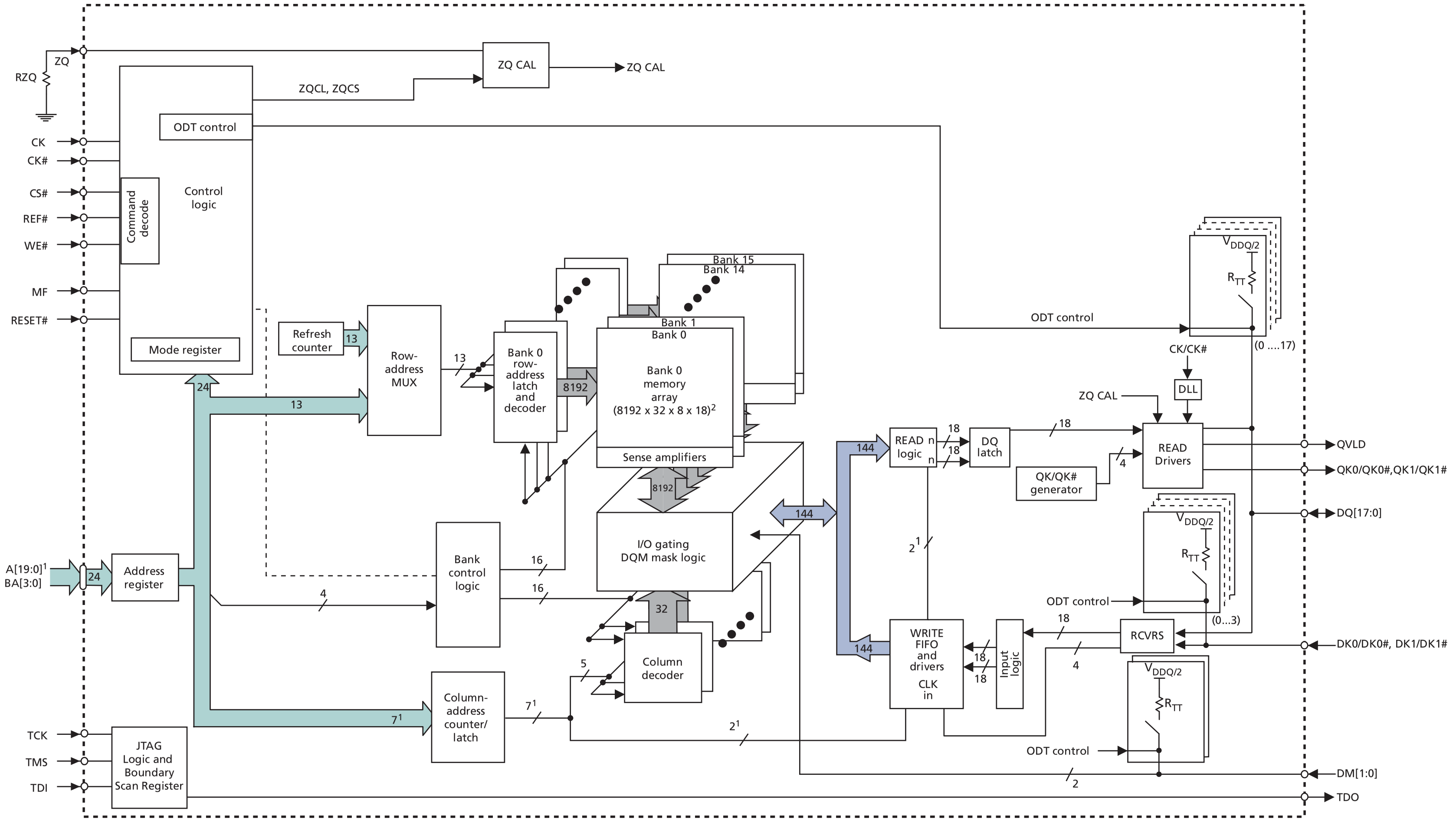
State Diagram

Figure 2: Simplified State Diagram


Initialization sequence
NOP
WRITE
READ
RESET#
MRS
AREF
Automatic sequence
Command sequence

Functional Block Diagrams

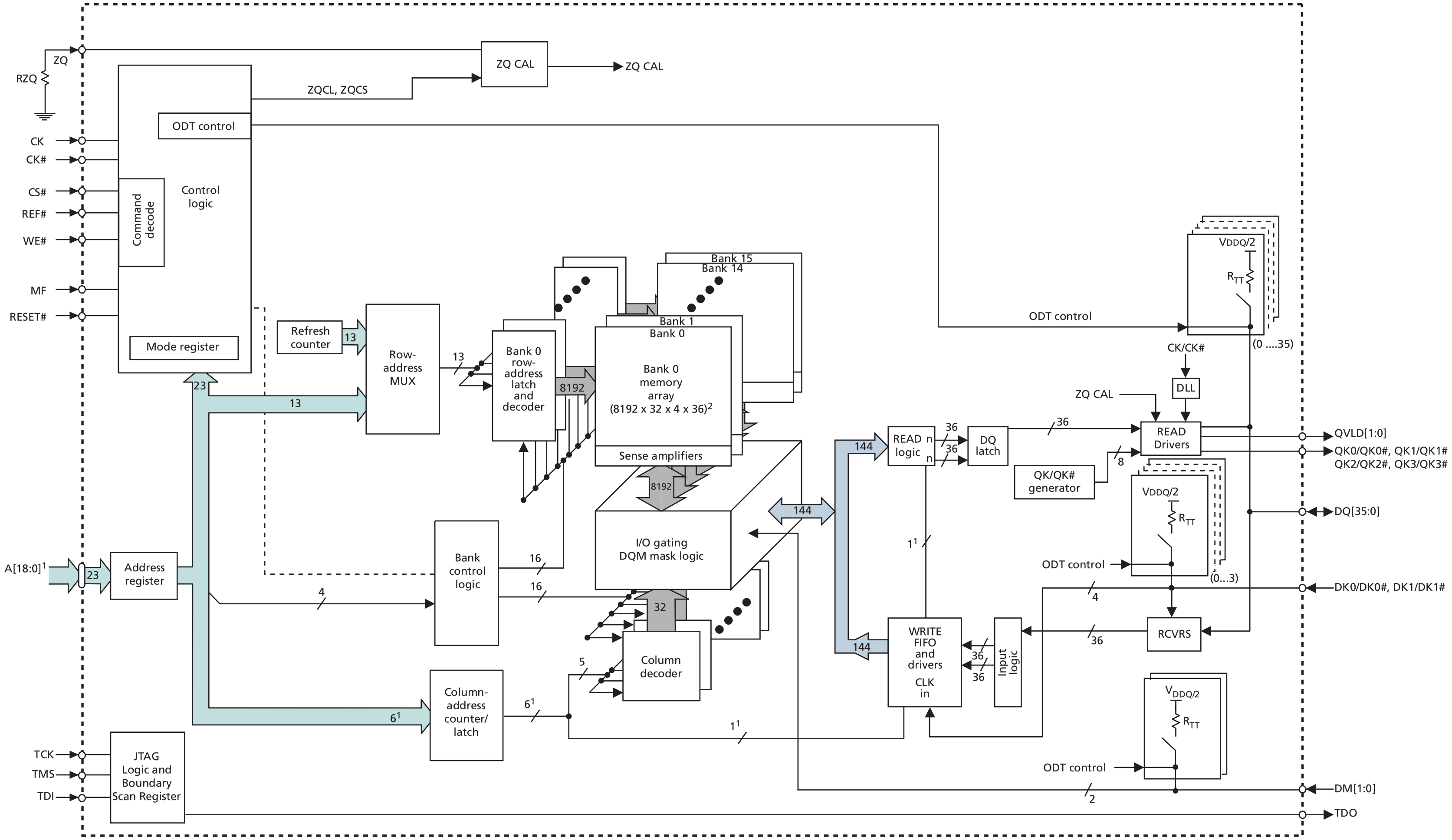
Figure 3: 32 Meg x 18 Functional Block Diagram


RZQ
ZQ
CK
CK#
CS#
REF#
WE#
MF
RESET#
A[19:0]1
BA[3:0]
TCK
TMS
TDI
ZQ CAL
ZQ CAL
ZQCL, ZQCS
ODT control
Control logic
Command decode
Mode register
24
Address register
24
13
Refresh counter
13
Row-address MUX
13
Bank 0 row-address latch and decoder
8192
Bank 0
Bank 1
Bank 14
Bank 15
Bank 0 memory array (8192 x 32 x 8 x 18)2
Sense amplifiers
8192
I/O gating DQM mask logic
32
Column decoder
5
Bank control logic
16
16
4
Column-address counter/ latch
71
71
21
144
144
144
READ logic
n
n
18
18
DQ latch
18
QK/QK# generator
4
READ Drivers
ZQ CAL
DLL
CK/CK#
ODT control
VDDQ/2
RTT
(0 ....17)
VDDQ/2
RTT
(0...3)
ODT control
RCVRS
18
4
Input logic
18
18
WRITE FIFO and drivers
CLK in
21
VDDQ/2
RTT
ODT control
2
QVLD
QK0/QK0#,QK1/QK1#
DQ[17:0]
DK0/DK0#, DK1/DK1#
DM[1:0]
TDO
JTAG Logic and Boundary Scan Register

Notes:
1. Example for BL = 2; column address will be reduced with an increase in burst length.
2. 8 = (length of burst) x 2^ (number of column addresses to WRITE FIFO and READ logic).

Functional Block Diagrams

Figure 4: 16 Meg x 36 Functional Block Diagram


ZQ
RZQ
ZQ CAL
ZQ CAL
ZQCL, ZQCS
ODT control
Control logic
Command decode
Mode register
CK
CK#
CS#
REF#
WE#
MF
RESET#
A[18:0]1
23
Address register
23
13
Refresh counter
13
Row-address MUX
13
Bank 0 row-address latch and decoder
8192
Bank 15
Bank 14
Bank 1
Bank 0
Bank 0 memory array (8192 x 32 x 4 x 36)2
Sense amplifiers
8192
I/O gating DQM mask logic
144
32
Column decoder
5
Bank control logic
16
16
4
Column-address counter/latch
61
61
11
11
JTAG Logic and Boundary Scan Register
TCK
TMS
TDI
TDO
144
144
READ n logic n
36
36
DQ latch
36
READ Drivers
ZQ CAL
CK/CK#
DLL
QK/QK# generator
8
VDDQ/2
RTT
(0 ....35)
(0...3)
ODT control
ODT control
ODT control
WRITE FIFO and drivers CLK in
36
36
Input logic
36
RCVRS
4
2
QVLD[1:0]
QK0/QK0#, QK1/QK1#
QK2/QK2#, QK3/QK3#
DQ[35:0]
DK0/DK0#, DK1/DK1#
DM[1:0]

Notes:
1. Example for BL = 2; column address will be reduced with an increase in burst length.
2. 4 = (length of burst) x 2^ (number of column addresses to WRITE FIFO and READ logic).

Ball Assignments and Descriptions

Table 1: 32 Meg x 18 Ball Assignments – 168-Ball FBGA (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13
A		V_{SS}	V_{DD}	NF	V_{DDQ}	NF	V_{REF}	DQ7	V_{DDQ}	DQ8	V_{DD}	V_{SS}	RESET#
B	V_{EXT}	V_{SS}	NF	V_{SSQ}	NF	V_{DDQ}	DM0	V_{DDQ}	DQ5	V_{SSQ}	DQ6	V_{SS}	V_{EXT}
C	V_{DD}	NF	V_{DDQ}	NF	V_{SSQ}	NF	DK0#	DQ2	V_{SSQ}	DQ3	V_{DDQ}	DQ4	V_{DD}
D	A11	V_{SSQ}	NF	V_{DDQ}	NF	V_{SSQ}	DK0	V_{SSQ}	QK0	V_{DDQ}	DQ0	V_{SSQ}	A13
E	V_{SS}	A0	V_{SSQ}	NF	V_{DDQ}	NF	MF	QK0#	V_{DDQ}	DQ1	V_{SSQ}	CS#	V_{SS}
F	A7	NF$_{(CS1)}$[1]	V_{DD}	A2	A1	WE#	ZQ	REF#	A3	A4	V_{DD}	A5	A9
G	$V_{SS(A20)}$[1]	A15	A6	V_{SS}	BA1	V_{SS}	CK#	V_{SS}	BA0	V_{SS}	A8	A18	$V_{SS(A21)}$[1]
H	A19	V_{DD}	A14	A16	V_{DD}	BA3	CK	BA2	V_{DD}	A17	A12	V_{DD}	A10
J	V_{DDQ}	NF	V_{SSQ}	NF	V_{DDQ}	NF	V_{SS}	QK1#	V_{DDQ}	DQ9	V_{SSQ}	QVLD	V_{DDQ}
K	NF	V_{SSQ}	NF	V_{DDQ}	NF	V_{SSQ}	DK1	V_{SSQ}	QK1	V_{DDQ}	DQ10	V_{SSQ}	DQ11
L	V_{DD}	NF	V_{DDQ}	NF	V_{SSQ}	NF	DK1#	DQ12	V_{SSQ}	DQ13	V_{DDQ}	DQ14	V_{DD}
M	V_{EXT}	V_{SS}	NF	V_{SSQ}	NF	V_{DDQ}	DM1	V_{DDQ}	DQ15	V_{SSQ}	DQ16	V_{SS}	V_{EXT}
N	V_{SS}	TCK	V_{DD}	TDO	V_{DDQ}	NF	V_{REF}	DQ17	V_{DDQ}	TDI	V_{DD}	TMS	V_{SS}

Notes:

1. F2 is the Location of the extra CS (CS1) needed to support the x18 DDP device. G1 & G13 are the locations of the additional address signals (A20 & A21 respectfully) needed to support the 2Gb monolithic device. F2 is Internally connected and will mirror the A5 address signal when MF is asserted HIGH and has parasitic characteristics of an address pin. G1 & G13 are VSS pins for this device, but have been designated as the location of A20 & A21 for the future 2Gb device.
2. NF balls for the x18 configuration are internally connected and have parasitic characteristics of an I/O. Balls may be connected to V_{SSQ}.
3. MF is assumed to be tied LOW for this ball assignment.

Table 2: 16 Meg x 36 Ball Assignments – 168-Ball FBGA (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13
A		V_{SS}	V_{DD}	DQ26	V_{DDQ}	DQ25	V_{REF}	DQ7	V_{DDQ}	DQ8	V_{DD}	V_{SS}	RESET#
B	V_{EXT}	V_{SS}	DQ24	V_{SSQ}	DQ23	V_{DDQ}	DM0	V_{DDQ}	DQ5	V_{SSQ}	DQ6	V_{SS}	V_{EXT}
C	V_{DD}	DQ22	V_{DDQ}	DQ21	V_{SSQ}	DQ20	DK0#	DQ2	V_{SSQ}	DQ3	V_{DDQ}	DQ4	V_{DD}
D	A11	V_{SSQ}	DQ18	V_{DDQ}	QK2	V_{SSQ}	DK0	V_{SSQ}	QK0	V_{DDQ}	DQ0	V_{SSQ}	A13
E	V_{SS}	A0	V_{SSQ}	DQ19	V_{DDQ}	QK2#	MF	QK0#	V_{DDQ}	DQ1	V_{SSQ}	CS#	V_{SS}
F	A7	$NF_{(CS1)}$[1]	V_{DD}	A2	A1	WE#	ZQ	REF#	A3	A4	V_{DD}	A5	A9
G	$V_{SS(A20)}$[1]	A15	A6	V_{SS}	BA1	V_{SS}	CK#	V_{SS}	BA0	V_{SS}	A8	A18	$V_{SS(A21)}$[1]
H	$NF_{(A19)}$[2]	V_{DD}	A14	A16	V_{DD}	BA3	CK	BA2	V_{DD}	A17	A12	V_{DD}	A10
J	V_{DDQ}	QVLD1	V_{SSQ}	DQ27	V_{DDQ}	QK3#	V_{SS}	QK1#	V_{DDQ}	DQ9	V_{SSQ}	QVLD0	V_{DDQ}
K	DQ29	V_{SSQ}	DQ28	V_{DDQ}	QK3	V_{SSQ}	DK1	V_{SSQ}	QK1	V_{DDQ}	DQ10	V_{SSQ}	DQ11
L	V_{DD}	DQ32	V_{DDQ}	DQ31	V_{SSQ}	DQ30	DK1#	DQ12	V_{SSQ}	DQ13	V_{DDQ}	DQ14	V_{DD}
M	V_{EXT}	V_{SS}	DQ34	V_{SSQ}	DQ33	V_{DDQ}	DM1	V_{DDQ}	DQ15	V_{SSQ}	DQ16	V_{SS}	V_{EXT}
N	V_{SS}	TCK	V_{DD}	TDO	V_{DDQ}	DQ35	V_{REF}	DQ17	V_{DDQ}	TDI	V_{DD}	TMS	V_{SS}

Notes:

1. F2 is the Location of the extra CS (CS1) needed to support the x18 DDP device. G1 & G13 are the locations of the additional address signals (A20 & A21 respectfully) needed to support the 2Gb monolithic device. F2 is Internally connected so it can mirror the A5 address signal when MF is asserted HIGH and has parasitic characteristics of an address pin. G1 & G13 are just place holders for the future device.
2. NF ball for x36 configuration is internally connected and has parasitic characteristics of an address (A19 for x18 configuration). Ball may be connected to V_{SSQ}.
3. MF is assumed to be tied LOW for this ball assignment.

Table 3: Ball Descriptions

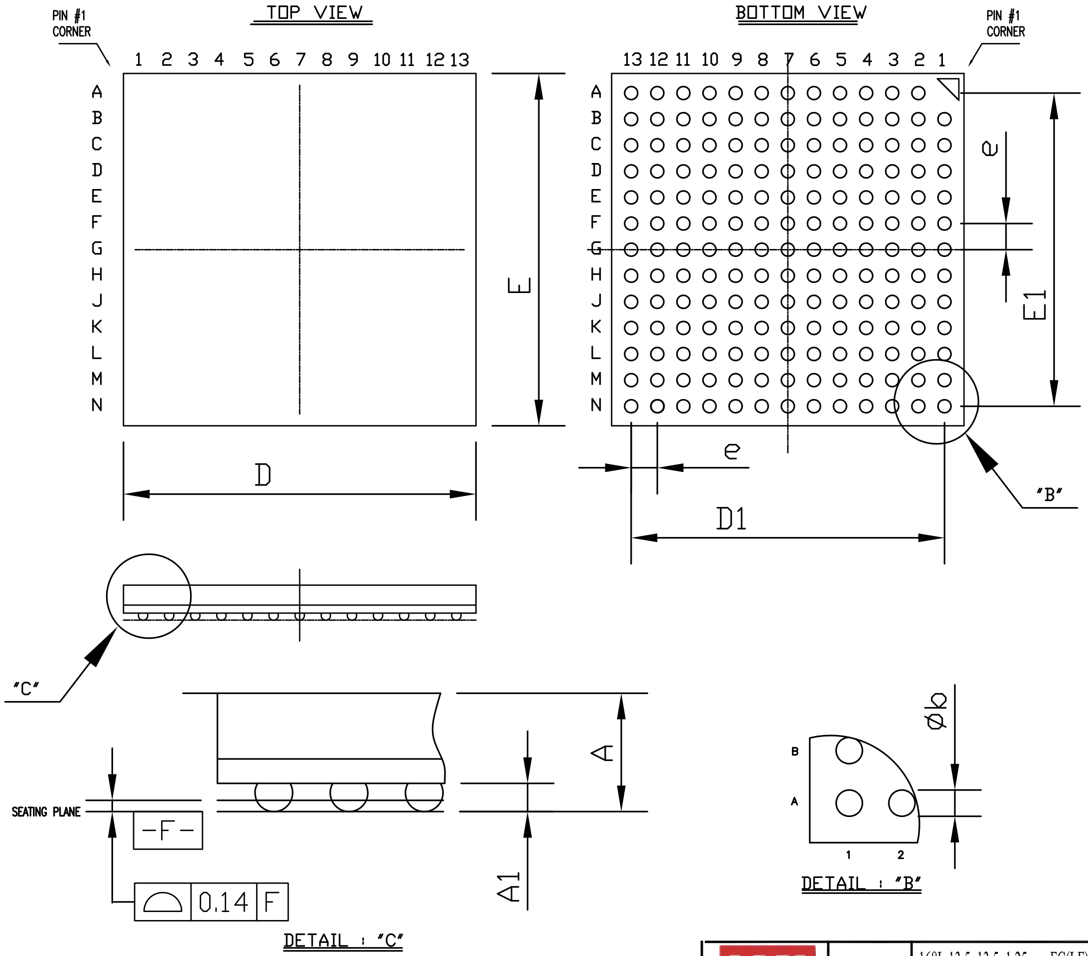
Symbol	Type	Description
A[19:0]	Input	**Address inputs:** A[19:0] define the row and column addresses for READ and WRITE operations. During a MODE REGISTER SET, the address inputs define the register settings along with BA[3:0]. They are sampled at the rising edge of CK.
BA[3:0]	Input	**Bank address inputs:** Select the internal bank to which a command is being applied.
CK/CK#	Input	**Input clock:** CK and CK# are differential input clocks. Addresses and commands are latched on the rising edge of CK.
CS#	Input	**Chip select:** CS# enables the command decoder when LOW and disables it when HIGH. When the command decoder is disabled, new commands are ignored, but internal operations continue.
DQ[35:0]	I/O	**Data input:** The DQ signals form the 36-bit data bus. During READ commands, the data is referenced to both edges of QK. During WRITE commands, the data is sampled at both edges of DK.
DK*x*, DK*x*#	Input	**Input data clock:** DK*x* and DK*x*# are differential input data clocks. All input data is referenced to both edges of DK*x*. For the x36 device, DQ[8:0] and DQ[26:18] are referenced to DK0 and DK0#, and DQ[17:9] and DQ[35:27] are referenced to DK1 and DK1#. For the x18 device, DQ[8:0] are referenced to DK0 and DK0#, and DQ[17:9] are referenced to DK1 and DK1#. DK*x* and DK*x*# are free-running signals and must always be supplied to the device.
DM[1:0]	Input	**Input data mask:** DM is the input mask signal for WRITE data. Input data is masked when DM is sampled HIGH. DM0 is used to mask the lower byte for the x18 device and DQ[8:0] and DQ[26:18] for the x36 device. DM1 is used to mask the upper byte for the x18 device and DQ[17:9] and DQ[35:27] for the x36 device. Tie DM[1:0] to V_{SS} if not used.
TCK	Input	**IEEE 1149.1 clock input:** This ball must be tied to V_{SS} if the JTAG function is not used.
TMS, TDI	Input	**IEEE 1149.1 test inputs:** These balls may be left as no connects if the JTAG function is not used.
WE#, REF#	Input	**Command inputs:** Sampled at the positive edge of CK, WE# and REF# (together with CS#) define the command to be executed.
RESET#	Input	**Reset:** RESET# is an active LOW CMOS input referenced to V_{SS}. RESET# assertion and deassertion are asynchronous. RESET# is a CMOS input defined with DC HIGH ≥ 0.8 x V_{DD} and DC LOW ≤ 0.2 x V_{DDQ}.
ZQ	Input	**External impedance:** This signal is used to tune the device's output impedance and ODT. RZQ needs to be 240Ω, where RZQ is a resistor from this signal to ground.
QK*x*, QK*x*#	Output	**Output data clocks:** QK and QK# are opposite-polarity output data clocks. They are free-running signals and during READ commands are edge-aligned with the DQs. For the x36 device, QK0, QK0# align with DQ[8:0]; QK1, QK1# align with DQ[17:9]; QK2, QK2# align with DQ[26:18]; QK3, QK3# align with DQ[35:27]. For the x18 device, QK0, QK0# align with DQ[8:0]; QK1, QK1# align with DQ[17:9].
QVLD*x*	Output	**Data valid:** The QVLD ball indicates that valid output data will be available on the subsequent rising clock edge. There is a single QVLD ball for the x18 device and two, QVLD0 and QVLD1, for the x36 device. QVLD0 aligns with DQ[17:0]; QVLD1 aligns with DQ[35:18].
MF	Input	**Mirror function:** The mirror function ball is a DC input used to create mirrored ballouts for simple dual-loaded clamshell mounting. If the ball is tied to V_{SS}, the address and command balls are in their true layout. If the ball is tied to V_{DDQ}, they are in the complement location. MF must be tied HIGH or LOW and cannot be left floating. MF is a CMOS input defined with DC HIGH ≥ 0.8 x V_{DD} and DC LOW ≤ 0.2 x V_{DDQ}.

Table 3: Ball Descriptions (Continued)

Symbol	Type	Description
TDO	Output	**IEEE 1149.1 test output:** JTAG output. This ball may be left as no connect if the JTAG function is not used.
V_{DD}	Supply	**Power supply:** 1.35V nominal. See Table 7 (page 22) for range.
V_{DDQ}	Supply	**DQ power supply:** 1.2V nominal. Isolated on the device for improved noise immunity. See Table 7 (page 22) for range.
V_{EXT}	Supply	**Power supply:** 2.5V nominal. See Table 7 (page 22) for range.
V_{REF}	Supply	**Input reference voltage:** $V_{DDQ}/2$ nominal. Provides a reference voltage for the input buffers.
V_{SS}	Supply	Ground.
V_{SSQ}	Supply	**DQ ground:** Isolated on the device for improved noise immunity.
NC	–	**No connect:** These balls are not connected to the DRAM.
NF	–	**No function:** These balls are connected to the DRAM, but provide no functionality.

Package Dimensions

Figure 5: 168-Ball FBGA


PIN #1 CORNER
TOP VIEW
1 2 3 4 5 6 7 8 9 10 11 12 13
A B C D E F G H J K L M N
E
D
BOTTOM VIEW
PIN #1 CORNER
13 12 11 10 9 8 7 6 5 4 3 2 1
A B C D E F G H J K L M N
e
E1
e
D1
"B"
"C"
SEATING PLANE
-F-
0.14 F
A1
A
DETAIL : "C"
B
A
1
2
øb
DETAIL : "B"

Symbol	Dimension in mm		
	Min	Nom	Max
A	—	—	1.25
A1	0.325	—	0.50
D	13.40	13.50	13.60
D1	—	12.00	—
E	13.40	13.50	13.60
E1	—	12.00	—
e	—	1.00	—
øb	0.45	0.55	0.60

NOTE :

1. CONTROLLING DIMENSION : MM .
2. Reference document : JEDEC MS-034B

TITLE	168L 13.5x13.5x1.25mm FC(LF)-BGA Package Outline	REV.	D	DATE	2/5/2014

Electrical Characteristics – I_{DD} Specifications

Table 4: I_{DD} Operating Conditions and Maximum Limits

Notes 1–6 apply to the entire table

Description	Condition	Symbol	-093E	-093	-107E	-107	-125F	-125E	-125	Units	Notes
Standby current	^tCK = idle; All banks idle; No inputs toggling	I_{SB1} (V_{DD}) x18	125	125	125	125	125	125	125	mA	7
		I_{SB1} (V_{DD}) x36	125	125	125	125	125	125	125		
		I_{SB1} (V_{EXT})	30	30	30	30	30	30	30		
Clock active standby current	CS# = 1; No commands; Bank address incremented and half address/ data change once every four clock cycles	I_{SB2} (V_{DD}) x18	870	870	815	815	725	725	725	mA	
		I_{SB2} (V_{DD}) x36	895	895	835	835	740	740	740		
		I_{SB2} (V_{EXT})	30	30	30	30	30	30	30		
Operational current: BL2	BL = 2; Sequential bank access; Bank transitions once every ^tRC; Half address transitions once every ^tRC; Read followed by write sequence; Continuous data during WRITE commands	I_{DD1} (V_{DD}) x18	1175	1115	1100	1045	990	940	915	mA	
		I_{DD1} (V_{DD}) x36	1185	1125	1110	1055	1000	950	925		
		I_{DD1} (V_{EXT})	35	35	35	35	35	35	35		
Operational current: BL4	BL = 4; Sequential bank access; Bank transitions once every ^tRC; Half address transitions once every ^tRC; Read followed by write sequence; Continuous data during WRITE commands	I_{DD2} (V_{DD}) x18	1205	1145	1130	1075	1020	970	945	mA	
		I_{DD2} (V_{DD}) x36	1215	1155	1140	1080	1030	980	950		
		I_{DD2} (V_{EXT})	35	35	35	35	35	35	35		
Operational current: BL8	BL = 8; Sequential bank access; Bank transitions once every ^tRC; Half address transitions once every ^tRC; Read followed by write sequence; Continuous data during WRITE commands	I_{DD3} (V_{DD}) x18	1300	1220	1200	1130	1085	1030	1000	mA	
		I_{DD3} (V_{DD}) x36	NA	NA	NA	NA	N/A	NA	NA		
		I_{DD3} (V_{EXT})	35	35	35	35	35	35	35		
Burst refresh current	Sixteen bank cyclic refresh using Bank Address Control AREF protocol; Command bus remains in refresh for all sixteen banks; DQs are High-Z and at V_{DDQ}/2; Addresses are at V_{DDQ}/2	I_{REF1} (V_{DD}) x18	1550	1550	1400	1400	1230	1230	1230	mA	
		I_{REF1} (V_{DD}) x36	1570	1570	1420	1420	1245	1245	1245		
		I_{REF1} (V_{EXT})	80	80	75	75	70	70	70		

Table 4: I_{DD} Operating Conditions and Maximum Limits (Continued)

Notes 1–6 apply to the entire table

Description	Condition	Symbol	-093E	-093	-107E	-107	-125F	-125E	-125	Units	Notes
Distributed refresh current	Single bank refresh using Bank Address Control AREF protocol; Sequential bank access every 0.489µs; DQs are High-Z and at $V_{DDQ}/2$; Addresses are at $V_{DDQ}/2$	I_{REF2} (V_{DD}) x18	875	875	820	820	730	730	730	mA	
		I_{REF2} (V_{DD}) x36	900	900	840	840	745	745	745		
		I_{REF2} (V_{EXT})	30	30	30	30	30	30	30		
Multibank refresh current: 4 bank refresh	Quad bank refresh using Multibank AREF protocol; BL = 4; Cyclic bank access; Subject to ^tSAW and ^tMMD specifications; DQs are High-Z and at $V_{DDQ}/2$; Bank addresses are at $V_{DDQ}/2$	I_{MBREF4} (V_{DD}) x18	2130	1925	2030	1810	1885	1885	1645	mA	
		I_{MBREF4} (V_{DD}) x36	2155	1950	2050	1830	1900	1900	1660		
		I_{MBREF4} (V_{EXT})	130	130	115	115	105	105	105		
Operating burst write current : BL2	BL = 2; Cyclic bank access; Half of address bits change every clock cycle; Continuous data; Measurement is taken during continuous WRITE	I_{DD2W} (V_{DD}) x18	2110	2110	1910	1910	1665	1665	1665	mA	
		I_{DD2W} (V_{DD}) x36	2290	2290	2070	2070	1805	1805	1805		
		I_{DD2W} (V_{EXT})	80	80	75	75	70	70	70		
Operating burst write current : BL4	BL = 4; Cyclic bank access; Half of address bits change every two clock cycles; Continuous data; Measurement is taken during continuous WRITE	I_{DD4W} (V_{DD}) x18	1730	1730	1590	1590	1395	1395	1395	mA	
		I_{DD4W} (V_{DD}) x36	1815	1815	1665	1665	1460	1460	1460		
		I_{DD4W} (V_{EXT})	55	55	55	55	50	50	50		
Operating burst write current :BL8	BL = 8; Cyclic bank access; Half of address bits change every four clock cycles; Continuous data; Measurement is taken during continuous WRITE	I_{DD8W} (V_{DD}) x18	1475	1475	1335	1335	1190	1190	1190	mA	
		I_{DD8W} (V_{DD}) x36	NA	NA	NA	NA	NA	NA	NA		
		I_{DD8W} (V_{EXT})	45	45	40	40	40	40	40		
Multibank write current: Dual bank write	BL = 4; Cyclic bank access using Dual Bank WRITE; Half of address bits change every two clock cycles; Continuous data; Measurement is taken during continuous WRITE	I_{DBWR} (V_{DD}) x18	2305	2305	2170	2170	1885	1885	1885	mA	
		I_{DBWR} (V_{DD}) x36	2400	2400	2250	2250	1960	1960	1960		
		I_{DBWR} (V_{EXT})	80	80	75	75	70	70	70		
Multibank write current: Quad bank write	BL = 4; Cyclic bank access using Quad Bank WRITE; Half of address bits change every two clock cycles; Continuous data; Measurement is taken during continuous WRITE; Subject to ^tSAW specification	I_{QBWR} (V_{DD}) x18	2965	2965	2890	2890	2525	2525	2525	mA	
		I_{QBWR} (V_{DD}) x36	3195	3195	3000	3000	2615	2615	2615		
		I_{QBWR} (V_{EXT})	130	130	115	115	100	100	100		

Table 4: I_{DD} Operating Conditions and Maximum Limits (Continued)

Notes 1–6 apply to the entire table

Description	Condition	Symbol	-093E	-093	-107E	-107	-125F	-125E	-125	Units	Notes
Operating burst read current example	BL = 2; Cyclic bank access; Half of address bits change every clock cycle; Continuous data; Measurement is taken during continuous READ	I_{DD2R} (V_{DD}) x18	2250	2250	2045	2045	1785	1785	1785	mA	
		I_{DD2R} (V_{DD}) x36	2395	2395	2180	2180	1895	1895	1895		
		I_{DD2R} (V_{EXT})	80	80	75	75	70	70	70		
Operating burst read current example	BL = 4; Cyclic bank access; Half of address bits change every two clock cycles; Continuous data; Measurement is taken during continuous READ	I_{DD4R} (V_{DD}) x18	1740	1740	1595	1595	1400	1400	1400	mA	
		I_{DD4R} (V_{DD}) x36	1835	1835	1685	1685	1475	1475	1475		
		I_{DD4R} (V_{EXT})	55	55	55	55	50	50	50		
Operating burst read current example	BL = 8; Cyclic bank access; Half of address bits change every four clock cycles; Continuous data; Measurement is taken during continuous READ	I_{DD8R} (V_{DD}) x18	1450	1450	1315	1315	1175	1175	1175	mA	
		I_{DD8R} (V_{DD}) x36	NA	NA	NA	NA	NA	NA	NA		
		I_{DD8R} (V_{EXT})	45	45	40	40	40	40	40		

Notes:

1. I_{DD} specifications are tested after the device is properly initialized. $0°C \le T_C \le +95°C$; $+1.28V \le V_{DD} \le +1.42V$, $+1.14V \le V_{DDQ} \le +1.26V$, $+2.38V \le V_{EXT} \le +2.63V$, $V_{REF} = V_{DDQ}/2$.
2. I_{DD} mesurements use ^tCK (MIN), ^tRC (MIN), and minimum data latency (RL and WL).
3. Input slew rate is 1V/ns for single ended signals and 2V/ns for differential signals.
4. Definitions for I_{DD} conditions:
    - LOW is defined as $V_{IN} \le V_{IL(AC)MAX}$.
    - HIGH is defined as $V_{IN} \ge V_{IH(AC)MIN}$.
    - Continuous data is defined as half the DQ signals changing between HIGH and LOW every half clock cycle (twice per clock).
    - Continuous address is defined as half the address signals changing between HIGH and LOW every clock cycle (once per clock).
    - Sequential bank access is defined as the bank address incrementing by one every ^tRC.
    - Cyclic bank access is defined as the bank address incrementing by one for each command access. For BL = 2 this is every clock, for BL = 4 this is every other clock, and for BL = 8 this is every fourth clock.
5. CS# is HIGH unless a READ, WRITE, AREF, or MRS command is registered. CS# never transitions more than once per clock cycle.
6. I_{DD} parameters are specified with ODT disabled.
7. Upon exiting standby current conditions, at least one NOP command must be issued with stable clock prior to issuing any other valid command.

Electrical Specifications – Absolute Ratings and I/O Capacitance

Absolute Maximum Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

Table 5: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units
V_{DD}	V_{DD} supply voltage relative to V_{SS}	–0.4	1.975	V
V_{DDQ}	Voltage on V_{DDQ} supply relative to V_{SS}	–0.4	1.66	V
V_{IN},V_{OUT}	Voltage on any ball relative to V_{SS}	–0.4	1.66	V
V_{EXT}	Voltage on V_{EXT} supply relative to V_{SS}	–0.4	2.8	V

Input/Output Capacitance

Table 6: Input/Output Capacitance

Notes 1 and 2 apply to entire table

Capacitance Parameters	Symbol	RL3-2133		RL3-1866		RL3-1600		Units	Notes
		Min	Max	Min	Max	Min	Max		
CK/CK#	C_{CK}	1.3	2.1	1.3	2.1	1.3	2.2	pF	
ΔC: CK to CK#	C_{DCK}	0	0.15	0	0.15	0	0.15	pF	
Single-ended I/O: DQ, DM	C_{IO}	1.9	2.9	1.9	3.0	2.0	3.1	pF	3
Input strobe: DK/DK#	C_{IO}	1.9	2.9	1.9	3.0	2.0	3.1	pF	
Output strobe: QK/QK#, QVLD	C_{IO}	1.9	2.9	1.9	3.0	2.0	3.1	pF	
ΔC: DK to DK#	C_{DDK}	0	0.15	0	0.15	0	0.15	pF	
ΔC: QK to QK#	C_{DQK}	0	0.15	0	0.15	0	0.15	pF	
ΔC: DQ to QK or DQ to DK	C_{DIO}	–0.5	0.3	–0.5	0.3	–0.5	0.3	pF	4
Inputs (CMD, ADDR)	C_I	1.25	2.25	1.25	2.25	1.25	2.25	pF	5
ΔC: CMD_ADDR to CK	$C_{DI\_CMD\_ADDR}$	–0.5	0.3	–0.5	0.3	–0.4	0.4	pF	6
JTAG balls	C_{JTAG}	1.5	4.5	1.5	4.5	1.5	4.5	pF	7
RESET#, MF balls	C_I	–	3.0	–	3.0	–	3.0	pF	

Notes:
1. $+1.28V \leq V_{DD} \leq +1.42V$, $+1.14V \leq V_{DDQ} \leq 1.26V$, $+2.38V \leq V_{EXT} \leq +2.63V$, $V_{REF} = V_{SS}$, $f = 100$ MHz, $T_C = 25°C$, $V_{OUT(DC)} = 0.5 \times V_{DDQ}$, V_{OUT} (peak-to-peak) = 0.1V.
2. Capacitance is not tested on ZQ ball.
3. DM input is grouped with the I/O balls, because they are matched in loading.
4. $C_{DIO} = C_{IO(DQ)} - 0.5 \times (C_{IO}\ [QK] + C_{IO}\ [QK\#])$.
5. Includes CS#, REF#, WE#, A[19:0], and BA[3:0].
6. $C_{DI\_CMD\_ADDR} = C_I\ (CMD\_ADDR) - 0.5 \times (C_{CK}\ [CK] + C_{CK}\ [CK\#])$.
7. JTAG balls are tested at 50 MHz.

AC and DC Operating Conditions

Table 7: DC Electrical Characteristics and Operating Conditions

Note 1 applies to the entire table; Unless otherwise noted: 0°C ≤ T_C ≤ +95°C; +1.28V ≤ V_{DD} ≤ +1.42V

Description	Symbol	Min	Max	Units	Notes
Supply voltage	V_{EXT}	2.38	2.63	V	
Supply voltage	V_{DD}	1.28	1.42	V	
Isolated output buffer supply	V_{DDQ}	1.14	1.26	V	
Reference voltage	V_{REF}	0.49 × V_{DDQ}	0.51 × V_{DDQ}	V	2, 3
Input HIGH (logic 1) voltage	$V_{IH(DC)}$	V_{REF} + 0.10	V_{DDQ}	V	
Input LOW (logic 0) voltage	$V_{IL(DC)}$	V_{SS}	V_{REF} - 0.10	V	
Input leakage current: Any input 0V ≤ V_{IN} ≤ V_{DD}, V_{REF} ball 0V ≤ V_{IN} ≤ 1.1V (All other balls not under test = 0V)	I_{LI}	–2	2	µA	
Reference voltage current (All other balls not under test = 0V)	I_{REF}	–5	5	µA	

Notes:
1. All voltages referenced to V_{SS} (GND).
2. The nominal value of V_{REF} is expected to be 0.5 × V_{DDQ} of the transmitting device. V_{REF} is expected to track variations in V_{DDQ}.
3. Peak-to-peak noise (non-common mode) on V_{REF} may not exceed ±2% of the DC value. DC values are determined to be less than 20 MHz. Peak-to-peak AC noise on V_{REF} should not exceed ±2% of $V_{REF(DC)}$. Thus, from V_{DDQ}/2, V_{REF} is allowed ±2% V_{DDQ}/2 for DC error and an additional ±2% V_{DDQ}/2 for AC noise. The measurement is to be taken at the nearest V_{REF} bypass capacitor.

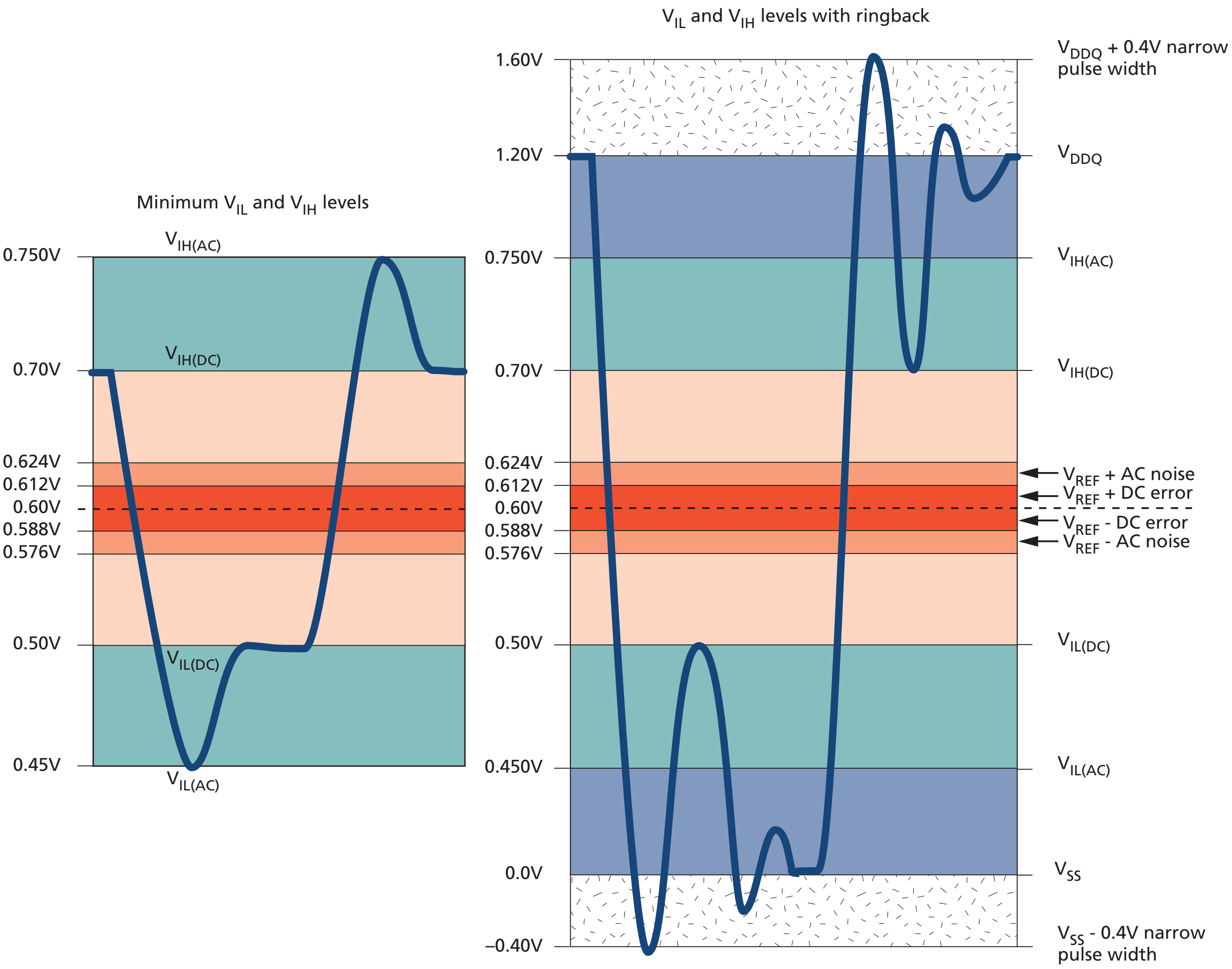
Table 8: Input AC Logic Levels

Notes 1-3 apply to entire table; Unless otherwise noted: 0°C ≤ T_C ≤ +95°C; +1.28V ≤ V_{DD} ≤ +1.42V

Description	Symbol	Min	Max	Units
Input HIGH (logic 1) voltage	$V_{IH(AC)}$	V_{REF} + 0.15	–	V
Input LOW (logic 0) voltage	$V_{IL(AC)}$	–	V_{REF} - 0.15	V

Notes:
1. All voltages referenced to V_{SS} (GND).
2. The receiver will effectively switch as a result of the signal crossing the AC input level, and will remain in that state as long as the signal does not ring back above/below the DC input LOW/HIGH level.
3. Single-ended input slew rate = 1 V/ns; maximum input voltage swing under test is 900mV (peak-to-peak).

Figure 6: Single-Ended Input Signal



AC Overshoot/Undershoot Specifications

Table 9: Control and Address Balls

Parameter	RL3-2133	RL3-1866	RL3-1600
Maximum peak amplitude allowed for overshoot area	0.4V	0.4V	0.4V
Maximum peak amplitude allowed for undershoot area	0.4V	0.4V	0.4V
Maximum overshoot area above V_{DDQ}	0.25 Vns	0.28 Vns	0.33 Vns
Maximum undershoot area below V_{SS}/V_{SSQ}	0.25 Vns	0.28 Vns	0.33 Vns

Table 10: Clock, Data, Strobe, and Mask Balls

Parameter	RL3-2133	RL3-1866	RL3-1600
Maximum peak amplitude allowed for overshoot area	0.4V	0.4V	0.4V
Maximum peak amplitude allowed for undershoot area	0.4V	0.4V	0.4V
Maximum overshoot area above V_{DDQ}	0.10 Vns	0.11 Vns	0.13 Vns
Maximum undershoot area below V_{SS}/V_{SSQ}	0.10 Vns	0.11 Vns	0.13 Vns

Figure 7: Overshoot

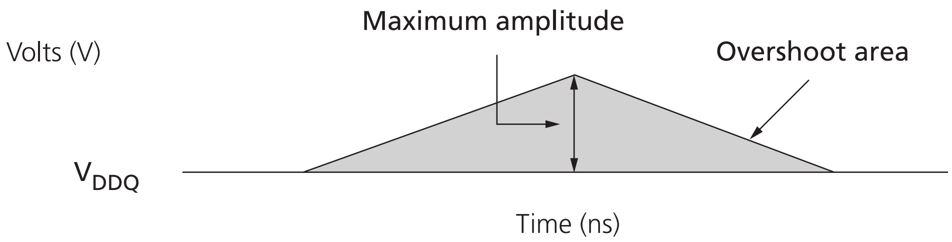

Maximum amplitude
Volts (V)
Overshoot area
V_{DDQ}
Time (ns)

Figure 8: Undershoot

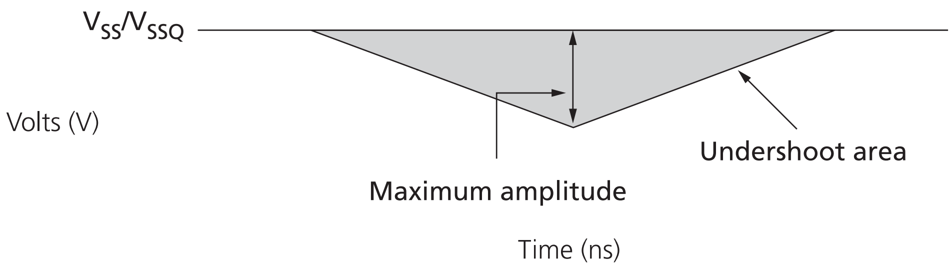

V_{SS}/V_{SSQ}
Volts (V)
Undershoot area
Maximum amplitude
Time (ns)

Table 11: Differential Input Operating Conditions (CK, CK# and DK*x*, DK*x*#)

Notes 1 and 2 apply to entire table

Parameter/Condition	Symbol	Min	Max	Units	Notes
Differential input voltage logic HIGH – slew	$V_{IH,diff\_slew}$	+200	n/a	mV	3
Differential input voltage logic LOW – slew	$V_{IL,diff\_slew}$	n/a	-200	mV	3
Differential input voltage logic HIGH	$V_{IH,diff(AC)}$	2 × ($V_{IH(AC)}$ - V_{REF})	V_{DDQ}	mV	4
Differential input voltage logic LOW	$V_{IL,diff(AC)}$	V_{SSQ}	2 × ($V_{IL(AC)}$ - V_{REF})	mV	5
Differential input crossing voltage relative to $V_{DD}/2$	V_{IX}	$V_{REF(DC)}$ - 150	$V_{REF(DC)}$ + 150	mV	6
Single-ended HIGH level	V_{SEH}	$V_{IH(AC)}$	V_{DDQ}	mV	4
Single-ended LOW level	V_{SEL}	V_{SSQ}	$V_{IL(AC)}$	mV	5

Notes:
1. CK/CK# and DK*x*/DK*x*# are referenced to V_{DDQ} and V_{SSQ}.
2. Differential input slew rate = 2 V/ns.
3. Defines slew rate reference points, relative to input crossing voltages.
4. Maximum limit is relative to single-ended signals; overshoot specifications are applicable.
5. Minimum limit is relative to single-ended signals; undershoot specifications are applicable.
6. The typical value of V_{IX} is expected to be about 0.5 × V_{DDQ} of the transmitting device and V_{IX} is expected to track variations in V_{DDQ}. V_{IX} indicates the voltage at which differential input signals must cross.

Figure 9: V_{IX} for Differential Signals

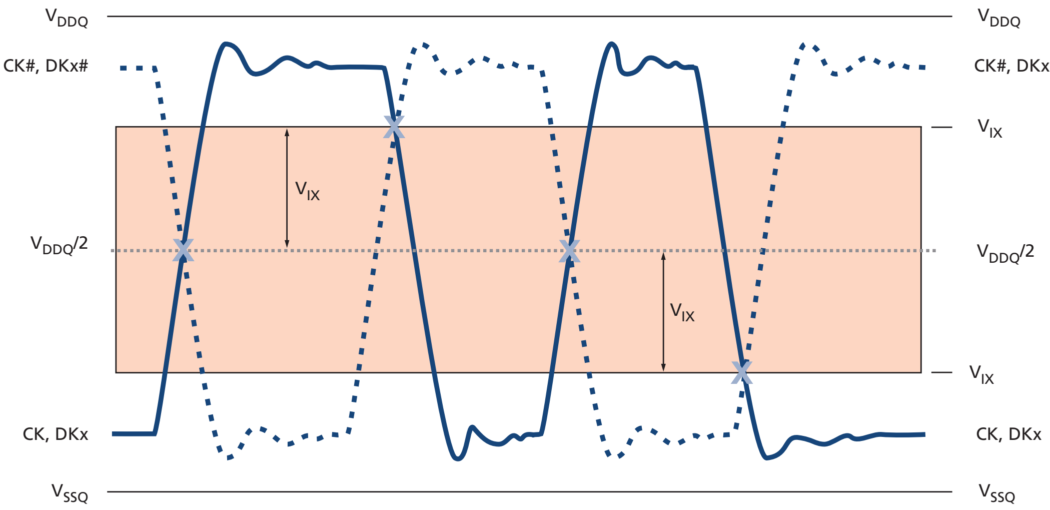


Figure 10: Single-Ended Requirements for Differential Signals

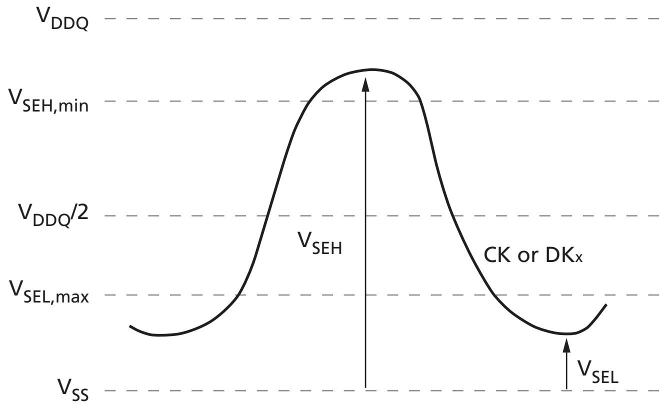

VDDQ
VSEH,min
VDDQ/2
VSEL,max
VSS
VSEH
CK or DKx
VSEL

Figure 11: Definition of Differential AC Swing and ^{t}DVAC

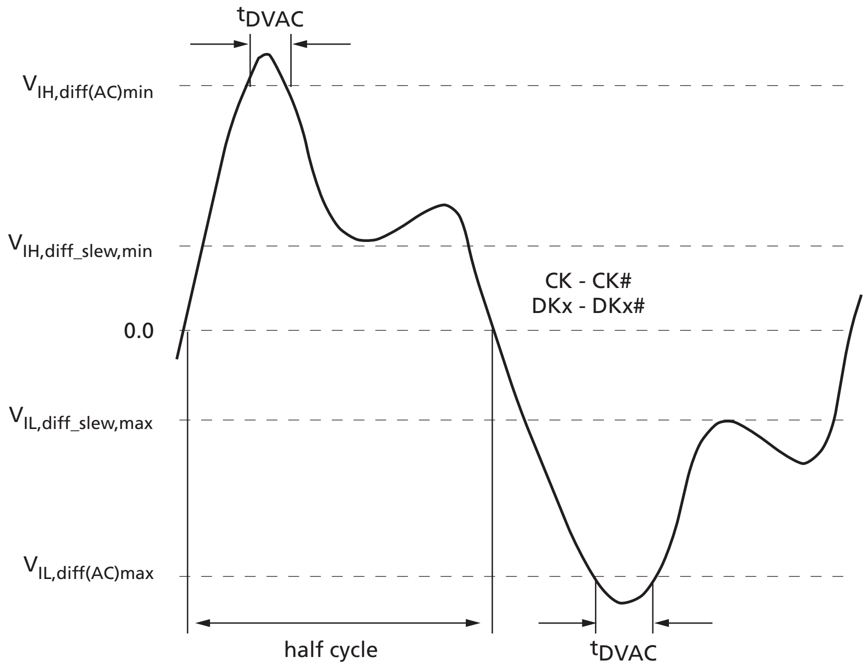

tDVAC
VIH,diff(AC)min
VIH,diff_slew,min
0.0
VIL,diff_slew,max
VIL,diff(AC)max
CK - CK#
DKx - DKx#
half cycle
tDVAC

Table 12: Allowed Time Before Ringback (^{t}DVAC) for CK, CK#, DK*x*, and DK*x*#

Slew Rate (V/ns)	MIN ^{t}DVAC (ps) at $\vert V_{IH}/V_{IL,diff(AC)}\vert$
>4.0	175
4.0	170
3.0	167
2.0	163
1.9	162
1.6	161
1.4	159
1.2	155
1.0	150
<1.0	150

Slew Rate Definitions for Single-Ended Input Signals

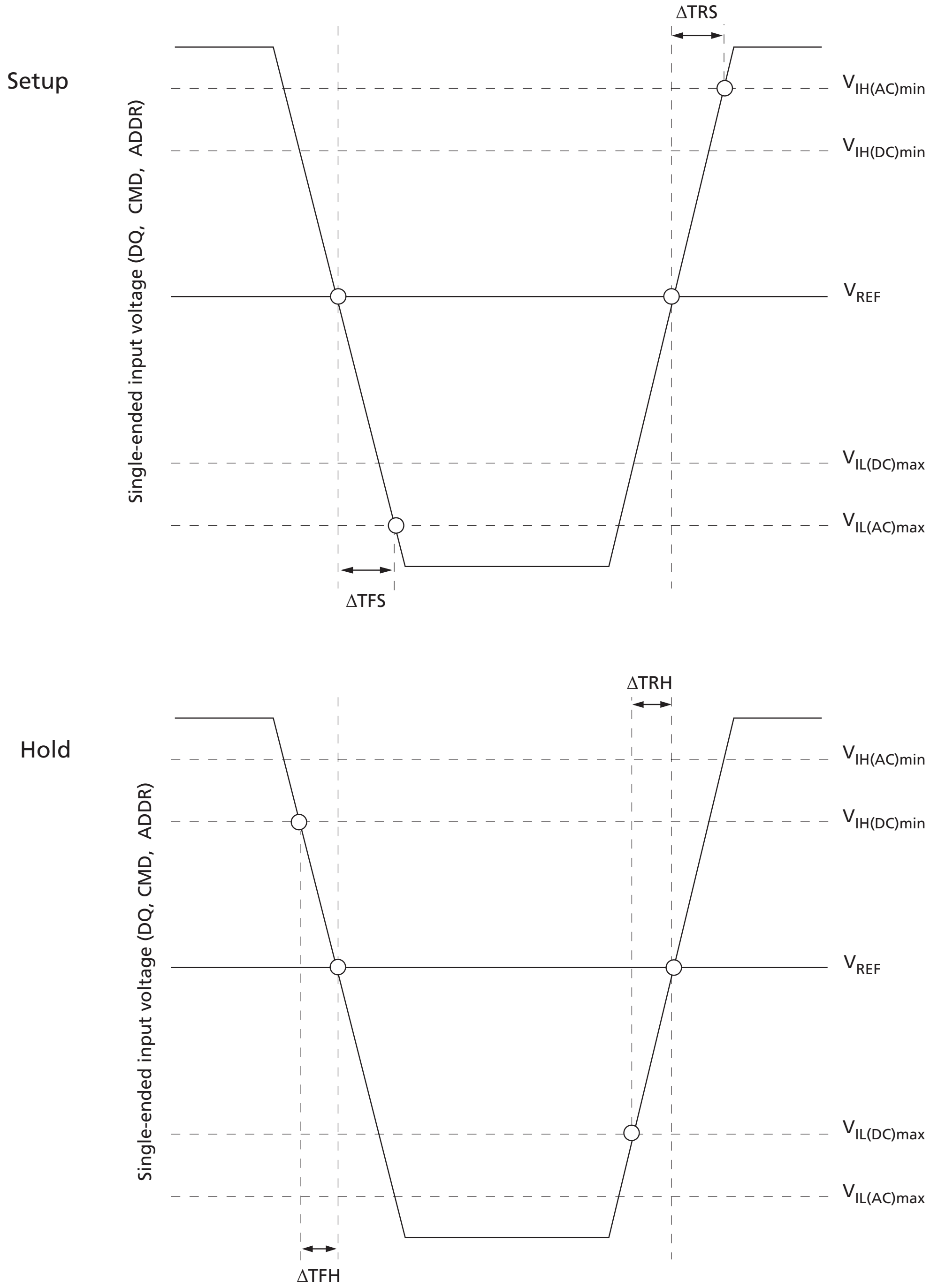
Setup (^{t}IS and ^{t}DS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of V_{REF} and the first crossing of $V_{IH(AC)min}$. Setup (^{t}IS and ^{t}DS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of V_{REF} and the first crossing of $V_{IL(AC)max}$.

Hold (^{t}IH and ^{t}DH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{IL(DC)max}$ and the first crossing of V_{REF}. Hold (^{t}IH and ^{t}DH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{IH(DC)min}$ and the first crossing of V_{REF} (see Figure 12 (page 28)).

Table 13: Single-Ended Input Slew Rate Definition

Input Slew Rates (Linear Signals)		Measured		Calculation
Input	Edge	From	To	
Setup	Rising	V_{REF}	$V_{IH(AC)min}$	$[V_{IH(AC)min} - V_{REF}]/\Delta TRS$
	Falling	V_{REF}	$V_{IL(AC)max}$	$[V_{REF} - V_{IL(AC)max}]/\Delta TFS$
Hold	Rising	$V_{IL(DC)max}$	V_{REF}	$[V_{REF} - V_{IL(DC)max}]/\Delta TRH$
	Falling	$V_{IH(DC)min}$	V_{REF}	$[V_{IH(DC)min} - V_{REF}]/\Delta TFH$

Figure 12: Nominal Slew Rate Definition for Single-Ended Input Signals


ΔTRS
Setup
$V_{IH(AC)min}$
$V_{IH(DC)min}$
Single-ended input voltage (DQ, CMD, ADDR)
V_{REF}
$V_{IL(DC)max}$
$V_{IL(AC)max}$
ΔTFS
ΔTRH
Hold
$V_{IH(AC)min}$
$V_{IH(DC)min}$
Single-ended input voltage (DQ, CMD, ADDR)
V_{REF}
$V_{IL(DC)max}$
$V_{IL(AC)max}$
ΔTFH

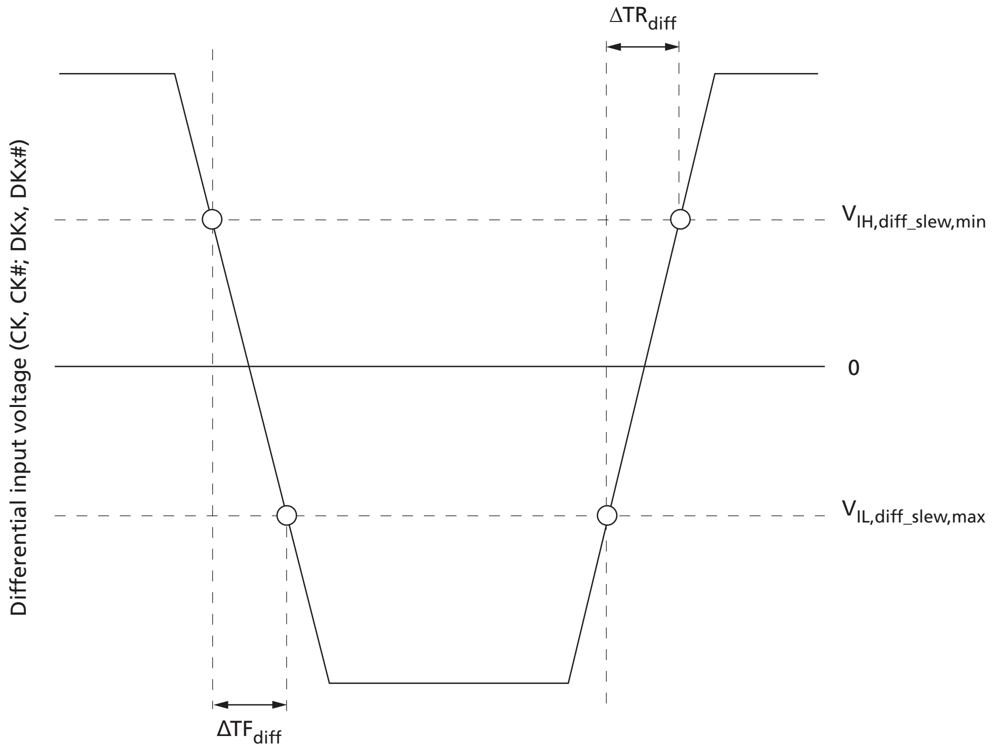
Slew Rate Definitions for Differential Input Signals

Input slew rate for differential signals (CK, CK# and DK*x*, DK*x*#) are defined and measured as shown in the following two tables. The nominal slew rate for a rising signal is defined as the slew rate between $V_{IL,diff,max}$ and $V_{IH,diff,min}$. The nominal slew rate for a falling signal is defined as the slew rate between $V_{IH,diff,min}$ and $V_{IL,diff,max}$.

Table 14: Differential Input Slew Rate Definition

Differential Input Slew Rates (Linear Signals)		Measured		
Input	**Edge**	**From**	**To**	**Calculation**
CK and DK reference	Rising	$V_{IL,diff\_slew,max}$	$V_{IH,diff\_slew,min}$	$[V_{IH,diff\_slew,min} - V_{IL,diff\_slew,max}]/\Delta TR_{diff}$
	Falling	$V_{IH,diff\_slew,min}$	$V_{IL,diff\_slew,max}$	$[V_{IH,diff\_slew,min} - V_{IL,diff\_slew,max}]/\Delta TF_{diff}$

Figure 13: Nominal Differential Input Slew Rate Definition for CK, CK#, DK*x*, and DK*x*#


ΔTR_{diff}
Differential input voltage (CK, CK#; DKx, DKx#)
$V_{IH,diff\_slew,min}$
0
$V_{IL,diff\_slew,max}$
ΔTF_{diff}

ODT Characteristics

ODT effective resistance, R_{TT}, is defined by MR1[4:2]. ODT is applied to the DQ, DM, and DK*x*, DK*x*# balls. The individual pull-up and pull-down resistors (R_{TTPU} and R_{TTPD}) are defined as follows:

$R_{TTPU} = (V_{DDQ} - V_{OUT}) / |I_{OUT}|$, under the condition that R_{TTPD} is turned off

$R_{TTPD} = (V_{OUT}) / |I_{OUT}|$, under the condition that R_{TTPU} is turned off

Figure 14: ODT Levels and I-V Characteristics

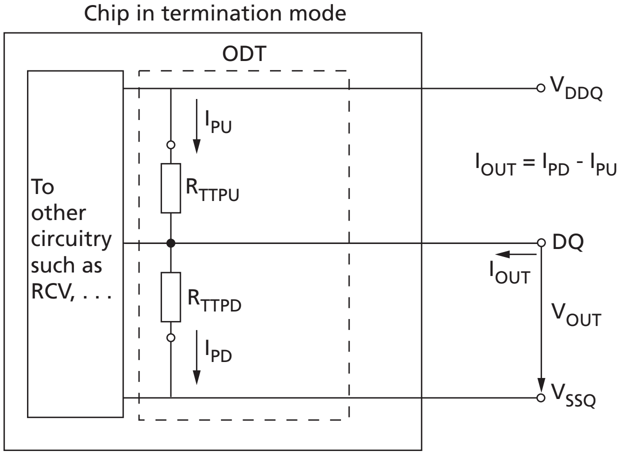


Table 15: ODT DC Electrical Characteristics

Parameter/Condition	Symbol	Min	Nom	Max	Units	Notes
R_{TT} effective impedance from $V_{IL(AC)}$ to $V_{IH(AC)}$	R_{TT_EFF}	*See Table 16 (page 31).*				1, 2
Deviation of V_M with respect to $V_{DDQ}/2$	ΔVm	-5	-	+5	%	3

Notes:
1. Tolerance limits are applicable after proper ZQ calibration has been performed at a stable temperature and voltage. Refer to ODT Sensitivity (page 32) if either the temperature or voltage changes after calibration.
2. Measurement definition for R_{TT}: Apply $V_{IH(AC)}$ to ball under test and measure current $I[V_{IH(AC)}]$, then apply $V_{IL(AC)}$ to ball under test and measure current $I[V_{IL(AC)}]$:

$$R_{TT} = \frac{V_{IH(AC)} - V_{IL(AC)}}{\left| I[V_{IH(AC)}] - I[V_{IL(AC)}] \right|}$$

3. Measure voltage (V_M) at the tested ball with no load:

$$\Delta VM = \left(\frac{2 \times VM}{V_{DDQ}} - 1 \right) \times 100$$

ODT Resistors

The on-die termination resistance is selected by MR1[4:2]. The following table provides an overview of the ODT DC electrical characteristics. The values provided are not specification requirements; however, they can be used as design guidelines to indicate what R_{TT} is targeted to provide:

- R_{TT} 120Ω is made up of $R_{TT120(PD240)}$ and $R_{TT120(PU240)}$.
- R_{TT} 60Ω is made up of $R_{TT60(PD120)}$ and $R_{TT60(PU120)}$.
- R_{TT} 40Ω is made up of $R_{TT40(PD80)}$ and $R_{TT40(PU80)}$.

Table 16: R_{TT} Effective Impedances

R_{TT}	Resistor	V_{OUT}	Min	Nom	Max	Units
120Ω	$R_{TT120(PD240)}$	0.2 x V_{DDQ}	0.6	1.0	1.1	RZQ/1
		0.5 x V_{DDQ}	0.9	1.0	1.1	RZQ/1
		0.8 x V_{DDQ}	0.9	1.0	1.4	RZQ/1
	$R_{TT120(PU240)}$	0.2 x V_{DDQ}	0.9	1.0	1.4	RZQ/1
		0.5 x V_{DDQ}	0.9	1.0	1.1	RZQ/1
		0.8 x V_{DDQ}	0.6	1.0	1.1	RZQ/1
120Ω		$V_{IL(AC)}$ to $V_{IH(AC)}$	0.9	1.0	1.6	RZQ/2
60Ω	$R_{TT60(PD120)}$	0.2 x V_{DDQ}	0.6	1.0	1.1	RZQ/2
		0.5 x V_{DDQ}	0.9	1.0	1.1	RZQ/2
		0.8 x V_{DDQ}	0.9	1.0	1.4	RZQ/2
	$R_{TT60(PU120)}$	0.2 x V_{DDQ}	0.9	1.0	1.4	RZQ/2
		0.5 x V_{DDQ}	0.9	1.0	1.1	RZQ/2
		0.8 x V_{DDQ}	0.6	1.0	1.1	RZQ/2
60Ω		$V_{IL(AC)}$ to $V_{IH(AC)}$	0.9	1.0	1.6	RZQ/4
40Ω	$R_{TT40(PD80)}$	0.2 x V_{DDQ}	0.6	1.0	1.1	RZQ/3
		0.5 x V_{DDQ}	0.9	1.0	1.1	RZQ/3
		0.8 x V_{DDQ}	0.9	1.0	1.4	RZQ/3
	$R_{TT40(PU80)}$	0.2 x V_{DDQ}	0.9	1.0	1.4	RZQ/3
		0.5 x V_{DDQ}	0.9	1.0	1.1	RZQ/3
		0.8 x V_{DDQ}	0.6	1.0	1.1	RZQ/3
40Ω		$V_{IL(AC)}$ to $V_{IH(AC)}$	0.9	1.0	1.6	RZQ/6

ODT Sensitivity

If either temperature or voltage changes after I/O calibration, then the tolerance limits listed in Table 15 (page 30) and Table 16 (page 31) can be expected to widen according to Table 17 (page 32) and Table 18 (page 32).

Table 17: ODT Sensitivity Definition

Symbol	Min	Max	Units
R_{TT}	0.9 - $dR_{TT}dT$ × |DT| - $dR_{TT}dV$ × |DV|	1.6 + $dR_{TT}dT$ × |DT| + $dR_{TT}dV$ × |DV|	RZQ/(2,4,6)

Note: 1. DT = T - T(@ calibration), DV = V_{DDQ} - V_{DDQ}(@ calibration) or V_{DD} - V_{DD}(@ calibration).

Table 18: ODT Temperature and Voltage Sensitivity

Change	Min	Max	Units
$dR_{TT}dT$	0	1.5	%/°C
$dR_{TT}dV$	0	0.15	%/mV

Output Driver Impedance

The output driver impedance is selected by MR1[1:0] during initialization. The selected value is able to maintain the tight tolerances specified if proper ZQ calibration is performed.

Output specifications refer to the default output driver unless specifically stated otherwise. A functional representation of the output buffer is shown below. The output driver impedance R_{ON} is defined by the value of the external reference resistor RZQ as follows:

- $R_{ON,x} = RZQ/y$ (with RZQ = 240Ω ±1%; $x = 40\Omega$ or 60Ω with $y = 6$ or 4, respectively)

The individual pull-up and pull-down resistors ($R_{ON(PU)}$ and $R_{ON(PD)}$) are defined as follows:

- $R_{ON(PU)} = (V_{DDQ} - V_{OUT})/|I_{OUT}|$, when $R_{ON(PD)}$ is turned off
- $R_{ON(PD)} = (V_{OUT})/|I_{OUT}|$, when $R_{ON(PU)}$ is turned off

Figure 15: Output Driver

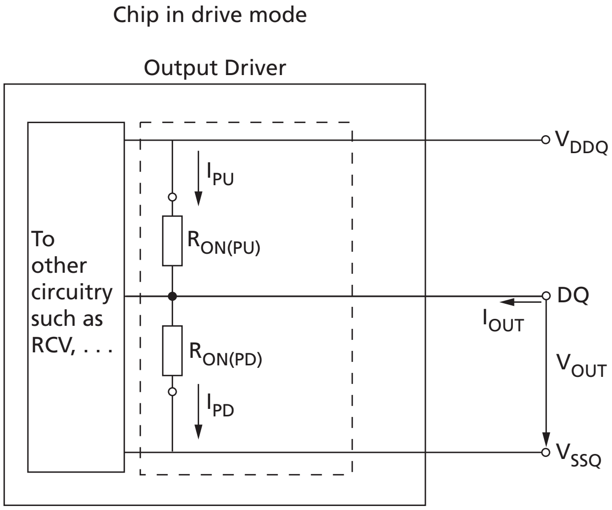

Chip in drive mode
Output Driver
To other circuitry such as RCV, . . .
V_{DDQ}
I_{PU}
$R_{ON(PU)}$
DQ
I_{OUT}
$R_{ON(PD)}$
V_{OUT}
I_{PD}
V_{SSQ}

Table 19: Driver Pull-Up and Pull-Down Impedance Calculations

R_{ON}		Min	Nom	Max	Units
RZQ/6 = (240Ω ±1%)/6		39.6	40	40.4	Ω
RZQ/4 = (240Ω ±1%)/4		59.4	60	60.6	Ω
Driver	**V_{OUT}**	**Min**	**Nom**	**Max**	**Units**
40Ω pull-down	0.2 × V_{DDQ}	24	40	44	Ω
	0.5 × V_{DDQ}	36	40	44	Ω
	0.8 × V_{DDQ}	36	40	56	Ω
40Ω pull-up	0.2 × V_{DDQ}	36	40	56	Ω
	0.5 × V_{DDQ}	36	40	44	Ω
	0.8 × V_{DDQ}	24	40	44	Ω
60Ω pull-down	0.2 × V_{DDQ}	36	60	66	Ω
	0.5 × V_{DDQ}	54	60	66	Ω
	0.8 × V_{DDQ}	54	60	84	Ω
60Ω pull-up	0.2 × V_{DDQ}	54	60	84	Ω
	0.5 × V_{DDQ}	54	60	66	Ω
	0.8 × V_{DDQ}	36	60	66	Ω

Output Driver Sensitivity

If either the temperature or the voltage changes after ZQ calibration, then the tolerance limits listed in Table 19 (page 34) can be expected to widen according to Table 20 (page 35) and Table 21 (page 35).

Table 20: Output Driver Sensitivity Definition

Symbol	Min	Max	Units
$R_{ON(PD)}$ @ 0.2 × V_{DDQ}	0.6 - $dR_{ON}dTH$ × DT - $dR_{ON}dVH$ × DV	1.1 + $dR_{ON}dTH$ × DT + $dR_{ON}dVH$ × DV	RZQ/(6, 4)
$R_{ON(PD)}$ @ 0.5 × V_{DDQ}	0.9 - $dR_{ON}dTM$ × DT - $dR_{ON}dVM$ × DV	1.1 + $dR_{ON}dTM$ × DT + $dR_{ON}dVM$ × DV	RZQ/(6, 4)
$R_{ON(PD)}$ @ 0.8 × V_{DDQ}	0.9 - $dR_{ON}dTL$ × DT - $dR_{ON}dVL$ × DV	1.4 + $dR_{ON}dTL$ × DT + $dR_{ON}dVL$ × D	RZQ/(6, 4)
$R_{ON(PU)}$ @ 0.2 × V_{DDQ}	0.9 - $dR_{ON}dTH$ × DT - $dR_{ON}dVH$ × DV	1.4 + $dR_{ON}dTH$ × DT + $dR_{ON}dVH$ × DV	RZQ/(6, 4)
$R_{ON(PU)}$ @ 0.5 × V_{DDQ}	0.9 - $dR_{ON}dTM$ × DT - $dR_{ON}dVM$ × DV	1.1 + $dR_{ON}dTM$ × DT + $dR_{ON}dVM$ × DV	RZQ/(6, 4)
$R_{ON(PU)}$ @ 0.8 × V_{DDQ}	0.6 - $dR_{ON}dTL$ × DT - $dR_{ON}dVL$ × DV	1.1 + $dR_{ON}dTL$ × DT + $dR_{ON}dVL$ × DV	RZQ/(6, 4)

Note: 1. DT = T - T(@ calibration), DV = V_{DDQ} - V_{DDQ}(@ calibration) or V_{DD} - V_{DD}(@ calibration).

Table 21: Output Driver Voltage and Temperature Sensitivity

Change	Min	Max	Unit
$dR_{ON}dTM$	0	1.5	%/°C
$dR_{ON}dVM$	0	0.15	%/mV
$dR_{ON}dTL$	0	1.5	%/°C
$dR_{ON}dVL$	0	0.15	%/mV
$dR_{ON}dTH$	0	1.5	%/°C
$dR_{ON}dVH$	0	0.15	%/mV

Output Characteristics and Operating Conditions

Table 22: Single-Ended Output Driver Characteristics

Note 1 and 2 apply to entire table

Parameter/Condition	Symbol	Min	Max	Units	Notes
Output leakage current; DQ are disabled; Any output ball $0V \leq V_{OUT} \leq V_{DDQ}$; ODT is disabled; All other balls not under test = 0V	I_{OZ}	–5	5	µA	
Output slew rate: Single-ended; For rising and falling edges, measures between $V_{OL(AC)} = V_{REF} - 0.1 \times V_{DDQ}$ and $V_{OH(AC)} = V_{REF} + 0.1 \times V_{DDQ}$	SRQ_{SE}	2.5	6	V/ns	4, 5
Single-ended DC high-level output voltage	$V_{OH(DC)}$	$0.8 \times V_{DDQ}$		V	6
Single-ended DC mid-point level output voltage	$V_{OM(DC)}$	$0.5 \times V_{DDQ}$		V	6
Single-ended DC low-level output voltage	$V_{OL(DC)}$	$0.2 \times V_{DDQ}$		V	6
Single-ended AC high-level output voltage	$V_{OH(AC)}$	$V_{TT} + 0.1 \times V_{DDQ}$		V	7, 8, 9
Single-ended AC low-level output voltage	$V_{OL(AC)}$	$V_{TT} - 0.1 \times V_{DDQ}$		V	7, 8, 9
Impedance delta between pull-up and pull-down for DQ and QVLD	MM_{PUPD}	–10	10	%	3
Test load for AC timing and output slew rates	Output to V_{TT} ($V_{DDQ}/2$) via 25Ω resistor				9

Notes:

1. All voltages are referenced to V_{SS}.
2. RZQ is 240Ω (±1%) and is applicable after proper ZQ calibration has been performed at a stable temperature and voltage.
3. Measurement definition for mismatch between pull-up and pull-down (MM_{PUPD}). Measure both $R_{ON(PU)}$ and $R_{ON(PD)}$ at $0.5 \times V_{DDQ}$:

$$MM_{PUPD} = \frac{Ron_{PU} - Ron_{PD}}{Ron_{NOM}} \times 100$$

4. The 6 V/ns maximum is applicable for a single DQ signal when it is switching either from HIGH to LOW or LOW to HIGH while the remaining DQ signals in the same byte lane are either all static or switching the opposite direction. For all other DQ signal switching combinations, the maximum limit of 6 V/ns is reduced to 5 V/ns.
5. See Table 24 (page 40) for output slew rate.
6. See the Driver Pull-Up and Pull-Down Impedance Calculations table for IV curve linearity. Do not use AC test load.
7. $V_{TT} = V_{DDQ}/2$
8. See Figure 16 (page 38) for an example of a single-ended output signal.
9. See Figure 18 (page 39) for the test load configuration.

Table 23: Differential Output Driver Characteristics

Notes 1 and 2 apply to entire table

Parameter/Condition	Symbol	Min	Max	Units	Notes
Output leakage current; DQ are disabled; Any output ball 0V ≤ V_{OUT} ≤ V_{DDQ}; ODT is disabled; All other balls not under test = 0V	I_{OZ}	–5	5	µA	
Output slew rate: Differential; For rising and falling edges, measures between $V_{OL,diff(AC)} = -0.2 \times V_{DDQ}$ and $V_{OH,diff(AC)} = +0.2 \times V_{DDQ}$	SRQ_{diff}	5	12	V/ns	5
Output differential cross-point voltage	$V_{OX(AC)}$	V_{REF} - 150	V_{REF} + 150	mV	6
Differential high-level output voltage	$V_{OH,diff(AC)}$	+0.2 × V_{DDQ}		V	6
Differential low-level output voltage	$V_{OL,diff(AC)}$	–0.2 × V_{DDQ}		V	6
Delta resistance between pull-up and pull-down for QK/QK#	MM_{PUPD}	–10	10	%	3
Test load for AC timing and output slew rates	Output to V_{TT} (V_{DDQ}/2) via 25Ω resistor				4

Notes:
1. All voltages are referenced to V_{SS}.
2. RZQ is 240Ω (±1%) and is applicable after proper ZQ calibration has been performed at a stable temperature and voltage.
3. Measurement definition for mismatch between pull-up and pull-down (MM_{PUPD}). Measure both $R_{ON(PU)}$ and $R_{ON(PD)}$ at 0.5 x V_{DDQ}:

$$MM_{PUPD} = \frac{Ron_{PU} - Ron_{PD}}{Ron_{NOM}} \times 100$$

4. See Figure 18 (page 39) for the test load configuration.
5. See Table 25 (page 41) for the output slew rate.
6. See Figure 17 (page 39) for an example of a differential output signal.

Figure 16: DQ Output Signal

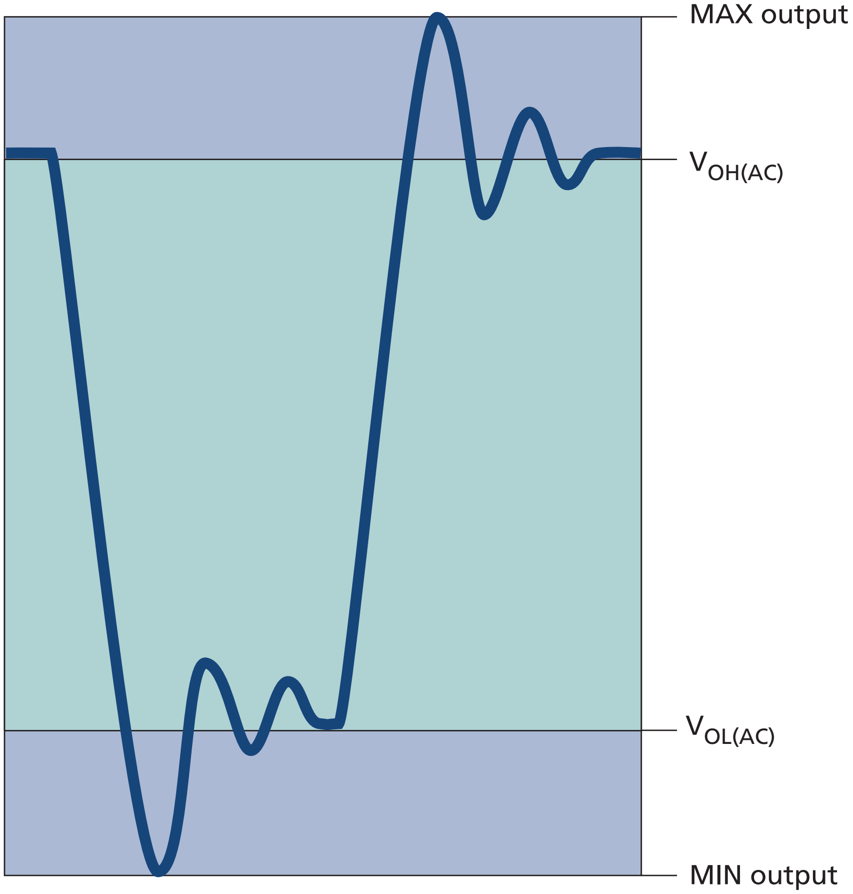
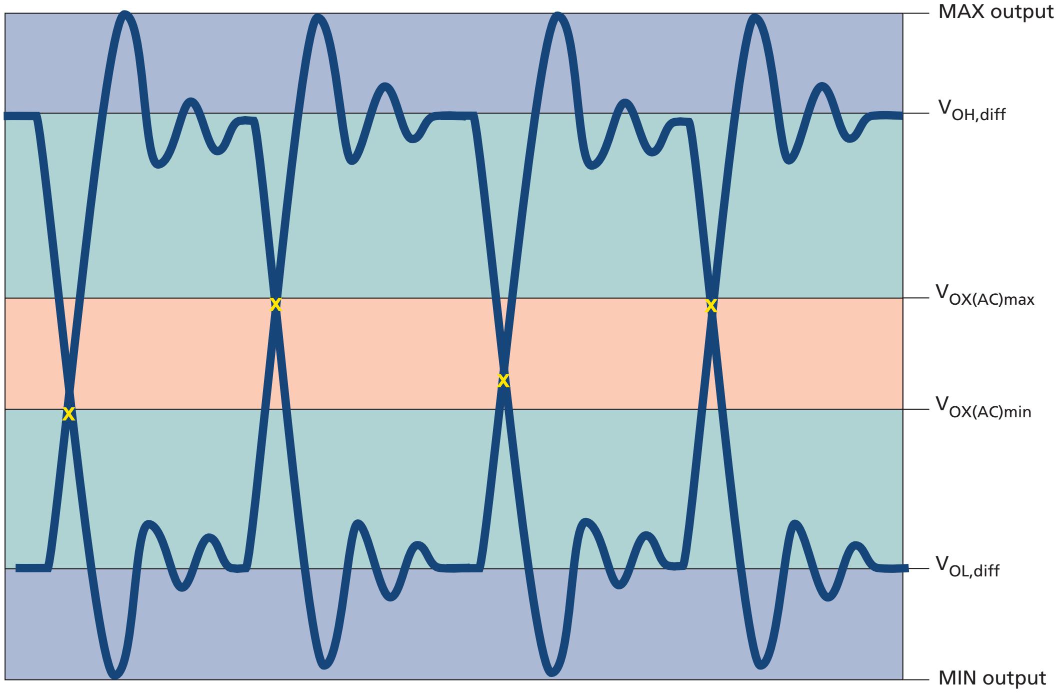

MAX output
$V_{OH(AC)}$
$V_{OL(AC)}$
MIN output

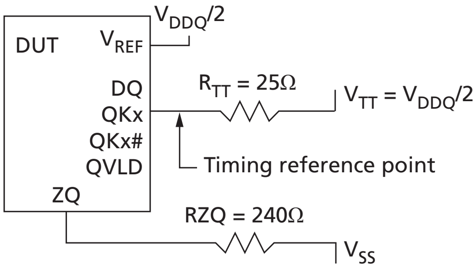
Figure 17: Differential Output Signal


MAX output
$V_{OH,diff}$
$V_{OX(AC)max}$
$V_{OX(AC)min}$
$V_{OL,diff}$
MIN output

Reference Output Load

The following figure represents the effective reference load of 25Ω used in defining the relevant device AC timing parameters as well as the output slew rate measurements. It is not intended to be a precise representation of a particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment.

Figure 18: Reference Output Load for AC Timing and Output Slew Rate


DUT
V_{REF}
$V_{DDQ}/2$
DQ
QKx
QKx#
QVLD
ZQ
R_{TT} = 25Ω
$V_{TT} = V_{DDQ}/2$
Timing reference point
RZQ = 240Ω
V_{SS}

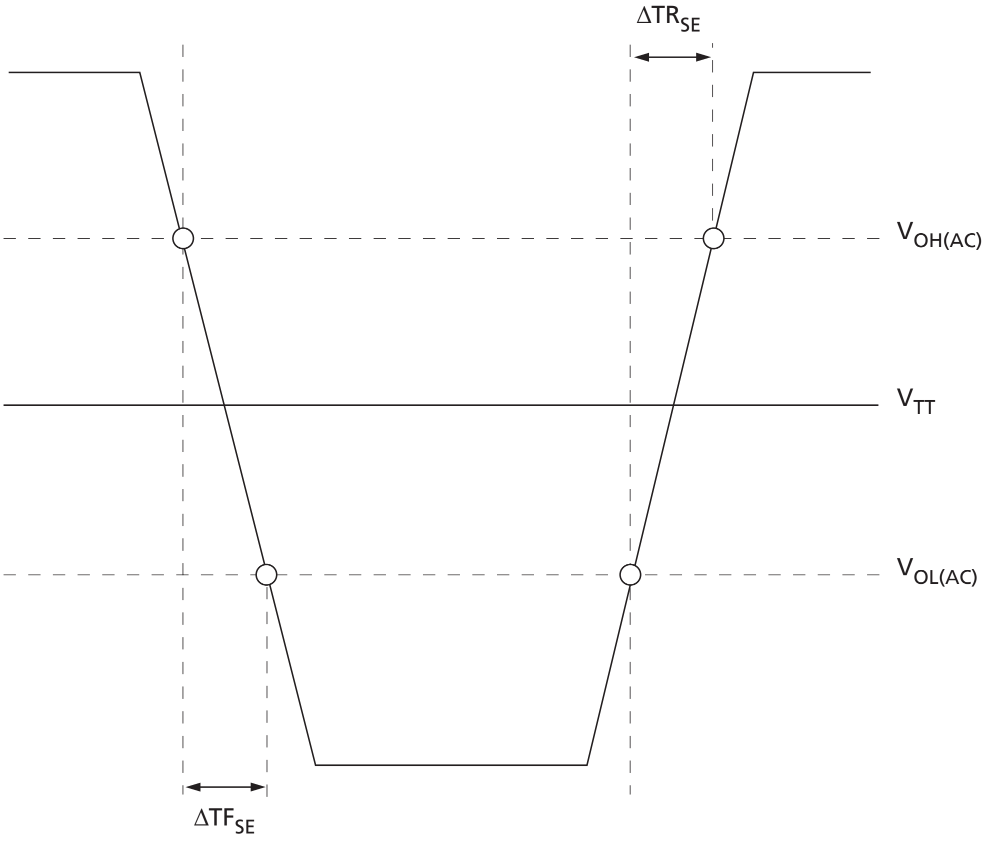
Slew Rate Definitions for Single-Ended Output Signals

The single-ended output driver is summarized in the following table. With the reference load for timing measurements, the output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)}$ and $V_{OH(AC)}$ for single-ended signals.

Table 24: Single-Ended Output Slew Rate Definition

Single-Ended Output Slew Rates (Linear Signals)		Measured		
Output	**Edge**	**From**	**To**	**Calculation**
DQ and QVLD	Rising	$V_{OL(AC)}$	$V_{OH(AC)}$	$\frac{V_{OH(AC)} - V_{OL(AC)}}{\Delta TR_{SE}}$
	Falling	$V_{OH(AC)}$	$V_{OL(AC)}$	$\frac{V_{OH(AC)} - V_{OL(AC)}}{\Delta TF_{SE}}$

Figure 19: Nominal Slew Rate Definition for Single-Ended Output Signals



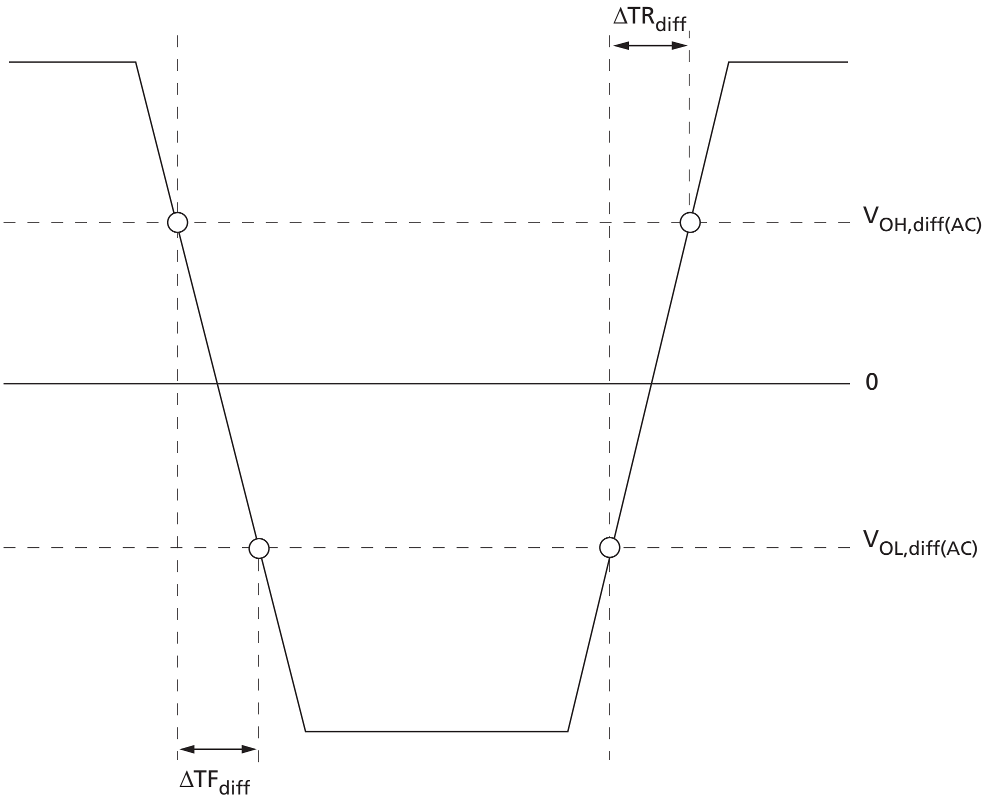
Slew Rate Definitions for Differential Output Signals

The differential output driver is summarized in the following table. With the reference load for timing measurements, the output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)}$ and $V_{OH(AC)}$ for differential signals.

Table 25: Differential Output Slew Rate Definition

Differential Output Slew Rates (Linear Signals)		Measured		Calculation
Output	**Edge**	**From**	**To**	
QK*x*, QK*x*#	Rising	$V_{OL,diff(AC)}$	$V_{OH,diff(AC)}$	$\frac{V_{OH,diff(AC)max} - V_{OL,diff(AC)}}{\Delta TR_{diff}}$
	Falling	$V_{OH,diff(AC)}$	$V_{OL,diff(AC)}$	$\frac{V_{OH,diff(AC)} - V_{OL,diff(AC)}}{\Delta TF_{diff}}$

Figure 20: Nominal Differential Output Slew Rate Definition for QKx, QKx#



Speed Bin Tables

Table 26: RL3 2133/1866 Speed Bins

The MIN ^{t}CK value for a given RL/WL parameter must be used to determine the ^{t}RC mode register setting.

Parameter	Symbol	-093E		-093		-107E		-107		Units
		Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
Clock Timing										
RL = 3 ; WL = 4	^{t}CK (avg)	5	5	5	5	Reserved		Reserved		ns
RL = 4 ; WL = 5	^{t}CK (avg)	4	5	4	5	4	5	4	5	ns
RL = 5 ; WL = 6	^{t}CK (avg)	3	4.3	3	4.3	3.5	4.3	4	4.3	ns
RL = 6 ; WL = 7	^{t}CK (avg)	2.5	3.5	2.5	4	3	3.5	3	4.3	ns
RL = 7 ; WL = 8	^{t}CK (avg)	2.5	3	2.5	3	2.5	3	2.5	3	ns
RL = 8 ; WL = 9	^{t}CK (avg)	1.875	2.5	1.875	3	2	2.5	2	3	ns
RL = 9 ; WL = 10	^{t}CK (avg)	1.875	2	1.875	2	1.875	2	1.875	2	ns
RL = 10 ; WL = 11	^{t}CK (avg)	1.5	2	1.5	2	1.875	2	1.875	2	ns
RL = 11 ; WL = 12	^{t}CK (avg)	1.5	1.875	1.5	2	1.5	1.875	1.5	2	ns
RL = 12 ; WL = 13	^{t}CK (avg)	1.25	1.5	1.25	1.875	1.5	1.66	1.5	1.875	ns
RL = 13 ; WL = 14	^{t}CK (avg)	1.25	1.5	1.25	1.5	1.25	1.5	1.25	1.5	ns
RL = 14 ; WL = 15	^{t}CK (avg)	1.07	1.25	1.07	1.5	1.25	1.33	1.25	1.5	ns
RL = 15 ; WL = 16	^{t}CK (avg)	1.0	1.25	1.0	1.25	1.07	1.33	1.07	1.25	ns
RL = 16 ; WL = 17	^{t}CK (avg)	0.9375	1.25	0.9375	1.25	Reserved		Reserved		ns
Row Cycle Timing										
Row cycle time	^{t}RC	8	–	10	–	8	–	10	–	ns

Table 27: RL3 1600 Speed Bins

The MIN ^{t}CK value for a given RL/WL parameter must be used to determine the ^{t}RC mode register setting.

Parameter	Symbol	-125F		125E		-125		Units
		Min	Max	Min	Max	Min	Max	
Clock Timing								
RL = 3 ; WL = 4	^{t}CK (avg)	Reserved		Reserved		Reserved		ns
RL = 4 ; WL = 5	^{t}CK (avg)	Reserved		4	5	5	5	ns
RL = 5 ; WL = 6	^{t}CK (avg)	Reserved		4	4.3	4	5	ns
RL = 6 ; WL = 7	^{t}CK (avg)	Reserved		3	4.3	3.5	4.3	ns
RL = 7 ; WL = 8	^{t}CK (avg)	Reserved		2.5	3	3	3.5	ns
RL = 8 ; WL = 9	^{t}CK (avg)	Reserved		2	3	2.5	3	ns
RL = 9 ; WL = 10	^{t}CK (avg)	Reserved		1.875	2	2.33	2.66	ns
RL = 10 ; WL = 11	^{t}CK (avg)	Reserved		1.875	2	2	2.33	ns
RL = 11 ; WL = 12	^{t}CK (avg)	Reserved		1.5	2	1.875	2.33	ns
RL = 12 ; WL = 13	^{t}CK (avg)	1.33	1.66	1.5	1.875	1.875	2	ns
RL = 13 ; WL = 14	^{t}CK (avg)	1.25	1.5	1.25	1.5	1.5	1.875	ns
RL = 14 ; WL = 15	^{t}CK (avg)	Reserved		Reserved		1.4	1.66	ns
RL = 15 ; WL = 16	^{t}CK (avg)	Reserved		Reserved		1.33	1.66	ns
RL = 16 ; WL = 17	^{t}CK (avg)	Reserved		Reserved		1.25	1.33	ns
Row Cycle Timing								
Row cycle time	^{t}RC	8	–	10	–	12	–	ns

AC Electrical Characteristics

Table 28: AC Electrical Characteristics

Notes 1–7 apply to entire table

Parameter		Symbol	RL3–2133		RL3–1866		RL3–1600		Units	Notes
			Min	Max	Min	Max	Min	Max		
Clock Timing										
Clock period average: DLL disable mode		^{t}CK(DLL_DIS)	8	488	8	488	8	488	ns	8
Clock period average: DLL enable mode		^{t}CK(avg)	See ^{t}CK values in the RL3 Speed Bins table.						ns	9, 10
High pulse width average		^{t}CH(avg)	0.47	0.53	0.47	0.53	0.47	0.53	CK	11
Low pulse width average		^{t}CL(avg)	0.47	0.53	0.47	0.53	0.47	0.53	CK	11
Clock period jitter	DLL locked	^{t}JIT(per)	–50	50	–60	60	–70	70	ps	12
	DLL locking	^{t}JIT(per),lck	–40	40	–50	50	–60	60	ps	12
Clock absolute period		^{t}CK(abs)	MIN = ^{t}CK(avg),min + ^{t}JIT(per),min; MAX = ^{t}CK(avg),max + ^{t}JIT(per),max						ps	
Clock absolute high pulse width		^{t}CH(abs)	0.43	–	0.43	–	0.43	–	^{t}CK(avg)	13
Clock absolute low pulse width		^{t}CL(abs)	0.43	–	0.43	–	0.43	–	^{t}CK(avg)	14
Cycle-to-cycle jitter	DLL locked	^{t}JIT(cc)	100		120		140		ps	15
	DLL locking	^{t}JIT(cc),lck	80		100		120		ps	15
Cumulative error across	2 cycles	^{t}ERR(2per)	–74	74	–88	88	–103	103	ps	16
	3 cycles	^{t}ERR(3per)	–87	87	–105	105	–122	122	ps	16
	4 cycles	^{t}ERR(4per)	–97	97	–117	117	–136	136	ps	16
	5 cycles	^{t}ERR(5per)	–105	105	–126	126	–147	147	ps	16
	6 cycles	^{t}ERR(6per)	–111	111	–133	133	–155	155	ps	16
	7 cycles	^{t}ERR(7per)	–116	116	–139	139	–163	163	ps	16
	8 cycles	^{t}ERR(8per)	–121	121	–145	145	–169	169	ps	16
	9 cycles	^{t}ERR(9per)	–125	125	–150	150	–175	175	ps	16
	10 cycles	^{t}ERR(10per)	–128	128	–154	154	–180	180	ps	16
	11 cycles	^{t}ERR(11per)	–132	132	–158	158	–184	184	ps	16
	12 cycles	^{t}ERR(12per)	–134	134	–161	161	–188	188	ps	16
	n = 13, 14 ... 49, 50 cycles	^{t}ERR(nper)	^{t}ERR(nper),min = [1 + 0.68LN(n)] × ^{t}JIT(per),min ^{t}ERR(nper),max = [1 + 0.68LN(n)] × ^{t}JIT(per),max						ps	16
DQ Input Timing										
Data setup time to DK, DK#	Base (specification)	^{t}DS(AC150)	–30	–	–15	–	10	–	ps	17, 18
	V_{REF} @ 1 V/ns		120	–	135	–	160	–	ps	18, 19

Table 28: AC Electrical Characteristics (Continued)

Notes 1–7 apply to entire table

Parameter		Symbol	RL3–2133		RL3–1866		RL3–1600		Units	Notes
			Min	Max	Min	Max	Min	Max		
Data hold time from DK, DK#	Base (specification)	^{t}DH(DC100)	5	–	20	–	45	–	ps	17, 18
	V$_{REF}$ @ 1 V/ns		105	–	120	–	145	–	ps	
Minimum data pulse width		^{t}DIPW	280	–	320	–	360	–	ps	20
DQ Output Timing										
QK, QK# edge to output data edge within byte group		^{t}QKQ$_x$	–	75	–	85	–	100	ps	
QK, QK# edge to any output data edge within specific data word grouping (only for x36)		^{t}QKQ02, ^{t}QKQ13	–	125	–	135	–	150	ps	22
DQ output hold time from QK, QK#		^{t}QH	0.38	–	0.38	–	0.38	–	^{t}CK(avg)	23
DQ Low-Z time from CK, CK#		^{t}LZ	–360	180	–390	195	–450	225	ps	24, 26
DQ High-Z time from CK, CK#		^{t}HZ	–	180	–	195	–	225	ps	24, 26
Input and Output Strobe Timing										
DK (rising), DK# (falling) edge to/from CK (rising), CK# (falling) edge		^{t}CKDK	–0.27	0.27	–0.27	0.27	–0.27	0.27	CK	29
DK, DK# differential input HIGH width		^{t}DKH	0.45	0.55	0.45	0.55	0.45	0.55	CK	
DK, DK# differential input LOW width		^{t}DKL	0.45	0.55	0.45	0.55	0.45	0.55	CK	
QK (rising), QK# (falling) edge to CK (rising), CK# (falling) edge		^{t}CKQK	–135 - 5% tCK	135 + 5% tCK	–140 - 5% tCK	140 + 5% tCK	–160 - 5% tCK	160 + 5% tCK	ps	26
QK (rising), QK# (falling) edge to CK (rising), CK# (falling) edge with DLL disabled		^{t}CKQK DLL_DIS	1	10	1	10	1	10	ns	27
QK, QK# differential output HIGH time		^{t}QKH	0.4	–	0.4	–	0.4	–	CK	23
QK, QK# differential output LOW time		^{t}QKL	0.4	–	0.4	–	0.4	–	CK	23
QK (falling), QK# (rising) edge to QVLD edge		^{t}QKVLD	–	125	–	135	–	150	ps	25
Command and Address Timing										
CTRL, CMD, ADDR, setup to CK,CK#	Base (specification)	^{t}IS(AC150)	85	–	120	–	170	–	ps	28, 30
	V$_{REF}$ @ 1 V/ns		235	–	270	–	320	–	ps	19, 30

Table 28: AC Electrical Characteristics (Continued)

Notes 1–7 apply to entire table

Parameter		Symbol	RL3–2133		RL3–1866		RL3–1600		Units	Notes
			Min	Max	Min	Max	Min	Max		
CTRL, CMD, ADDR, hold from CK,CK#	Base (specification)	^{t}IH(DC100)	65	–	100	–	120	–	ps	28, 30
	V_{REF} @ 1 V/ns		165	–	200	–	220	–	ps	19, 30
Minimum CTRL, CMD, ADDR pulse width		^{t}IPW	470	–	535	–	560	–	ps	20
Row cycle time		^{t}RC	See minimum ^{t}RC values in the RL3 Speed Bins table.						ns	21
Refresh rate		^{t}REF	64	–	64	–	64	–	ms	
Sixteen-bank access window		^{t}SAW	8	–	8	–	8	–	ns	
Multibank access delay		^{t}MMD	2	–	2	–	2	–	CK	33
WRITE-to-READ to same address		^{t}WTR	WL + BL/2	–	WL + BL/2	–	WL + BL/2	–	CK	32
Mode register set cycle time to any command		^{t}MRSC	12	–	12	–	12	–	CK	
READ training register minimum READ time		^{t}RTRS	2	–	2	–	2	–	CK	
READ training register burst end to mode register set for training register exit		^{t}RTRE	1	–	1	–	1	–	CK	
Calibration Timing										
ZQCL: Long calibration time	POWER-UP and RESET operation	^{t}ZQinit	512	–	512	–	512	–	CK	
	Normal operation	^{t}ZQoper	256	–	256	–	256	–	CK	
ZQCS: Short calibration time		^{t}ZQcs	64	–	64	–	64	–	CK	
Initialization and Reset Timing										
Begin power-supply ramp to power supplies stable		$^{t}V_{DDPR}$	–	200	–	200	–	200	ms	
RESET# LOW to power supplies stable		^{t}RPS	–	200	–	200	–	200	ms	
RESET# LOW to I/O and R_{TT} High-Z		^{t}IOz	–	20	–	20	–	20	ns	31

Notes:

1. Parameters are applicable with $0°C \le T_C \le +95°C$; $+1.28V \le V_{DD} \le +1.42V$, $+2.38V \le V_{EXT} \le +2.63V$, $+1.14V \le V_{DDQ} \le 1.26V$.
2. All voltages are referenced to V_{SS}.
3. The unit ^{t}CK(avg) represents the actual ^{t}CK(avg) of the input clock under operation. The unit CK represents one clock cycle of the input clock, counting the actual clock edges.
4. AC timing and I_{DD} tests may use a V_{IL}-to-V_{IH} swing of up to 900mV in the test environment, but input timing is still referenced to V_{REF} (except ^{t}IS, ^{t}IH, ^{t}DS, and ^{t}DH use the AC/DC trip points and CK,CK# and DKx, DKx# use their crossing points). The minimum slew rate for the input signals used to test the device is 1 V/ns for single-ended inputs and 2 V/ns for differential inputs in the range between $V_{IL(AC)}$ and $V_{IH(AC)}$.

5. All timings that use time-based values (ns, µs, ms) should use ^{t}CK(avg) to determine the correct number of clocks. In the case of noninteger results, all minimum limits should be rounded up to the nearest whole integer, and all maximum limits should be rounded down to the nearest whole integer.
6. The term “strobe” refers to the DK and DK# or QK and QK# differential crossing point when DK and QK, respectively, is the rising edge. Clock, or CK, refers to the CK and CK# differential crossing point when CK is the rising edge.
7. The output load defined in Figure 18 (page 39) is used for all AC timing and slew rates. The actual test load may be different. The output signal voltage reference point is V_{DDQ}/2 for single-ended signals and the crossing point for differential signals.
8. When operating in DLL disable mode, ISSI does not warrant compliance with normal mode timings or functionality.
9. The clock’s ^{t}CK(avg) is the average clock over any 200 consecutive clocks and ^{t}CK(avg),min is the smallest clock rate allowed, with the exception of a deviation due to clock jitter. Input clock jitter is allowed provided it does not exceed values specified and must be of a random Gaussian distribution in nature.
10. Spread spectrum is not included in the jitter specification values. However, the input clock can accommodate spread spectrum at a sweep rate in the range of 20–60 kHz with an additional 1% of ^{t}CK(avg) as a long-term jitter component; however, the spread spectrum may not use a clock rate below ^{t}CK(avg),min.
11. The clock’s ^{t}CH(avg) and ^{t}CL(avg) are the average half-clock period over any 200 consecutive clocks and is the smallest clock half-period allowed, with the exception of a deviation due to clock jitter. Input clock jitter is allowed provided it does not exceed values specified and must be of a random Gaussian distribution in nature.
12. The period jitter, ^{t}JIT(per), is the maximum deviation in the clock period from the average or nominal clock. It is allowed in either the positive or negative direction.
13. ^{t}CH(abs) is the absolute instantaneous clock high pulse width as measured from one rising edge to the following falling edge.
14. ^{t}CL(abs) is the absolute instantaneous clock low pulse width as measured from one falling edge to the following rising edge.
15. The cycle-to-cyle jitter, ^{t}JIT(cc), is the amount the clock period can deviate from one cycle to the next. It is important to keep cycle-to-cycle jitter at a minimum during the DLL locking time.
16. The cumulative jitter error, ^{t}ERR(nper), where n is the number of clocks between 2 and 50, is the amount of clock time allowed to accumulate consecutively away from the average clock over n number of clock cycles.
17. ^{t}DS(base) and ^{t}DH(base) values are for a single-ended 1 V/ns DQ slew rate and 2 V/ns differential DK, DK# slew rate.
18. These parameters are measured from a data signal (DM, DQ0, DQ1, and so forth) transition edge to its respective data strobe signal (DK, DK#) crossing.
19. The setup and hold times are listed converting the base specification values (to which derating tables apply) to V_{REF} when the slew rate is 1 V/ns. These values, with a slew rate of 1 V/ns, are for reference only.
20. Pulse width of an input signal is defined as the width between the first crossing of $V_{REF(DC)}$ and the consecutive crossing of $V_{REF(DC)}$
21. Bits MR0[3:0] select the number of clock cycles required to satisfy the minimum ^{t}RC value. Minimum ^{t}RC value must be divided by the clock period and rounded up to the next whole number to determine the earliest clock edge that the subsequent command can be issued to the bank.
22. ^{t}QKQ02 defines the skew between QK0 and DQ[26:18] and between QK2 and DQ[8:0]. ^{t}QKQ13 defines the skew between QK1 and DQ[35:27] and between QK3 and DQ[17:9].
23. When the device is operated with input clock jitter, this parameter needs to be derated by the actual ^{t}JIT(per) (the larger of ^{t}JIT(per),min or ^{t}JIT(per),max of the input clock; output deratings are relative to the SDRAM input clock).

24. Single-ended signal parameter.
25. For x36 device this specification references the skew between the falling edge of QK0 and QK1 to QVLD0 and the falling edge of QK2 and QK3 to QVLD1.
26. The DRAM output timing is aligned to the nominal or average clock. The following output parameters must be derated by the actual jitter error when input clock jitter is present, even when within specification. This results in each parameter becoming larger. The following parameters are required to be derated by subtracting ^{t}ERR(10per),max: ^{t}CKQK (MIN), and ^{t}LZ (MIN). The following parameters are required to be derated by subtracting ^{t}ERR(10per),min: ^{t}CKQK (MAX), ^{t}HZ (MAX), and ^{t}LZ (MAX).
27. The ^{t}DQSCKdll_dis parameter begins RL - 1 cycles after the READ command.
28. ^{t}IS(base) and ^{t}IH(base) values are for a single-ended 1 V/ns control/command/address slew rate and 2 V/ns CK, CK# differential slew rate.
29. These parameters are measured from the input data strobe signal (DK/DK#) crossing to its respective clock signal crossing (CK/CK#). The specification values are not affected by the amount of clock jitter applied as they are relative to the clock signal crossing. These parameters should be met whether or not clock jitter is present.
30. These parameters are measured from a command/address signal transition edge to its respective clock (CK, CK#) signal crossing. The specification values are not affected by the amount of clock jitter applied as the setup and hold times are relative to the clock signal crossing that latches the command/address. These parameters should be met whether or not clock jitter is present.
31. RESET# should be LOW as soon as power starts to ramp to ensure the outputs are in High-Z. Until RESET# is LOW, the outputs are at risk of driving and could result in excessive current, depending on bus activity.
32. If ^{t}WTR is violated, the data just written will not be read out when a READ command is issued to the same address. Whatever data was previously written to the address will be output with the READ command.
33. This specification is defined as any bank command (READ, WRITE, AREF) to a multi-bank command or a multi-bank command to any bank command. This specification only applies to quad bank WRITE, 3-bank AREF and 4-bank AREF commands. Dual bank WRITE, 2-bank AREF, and all single bank access commands are not bound by this specification.

Temperature and Thermal Impedance Characteristics

It is imperative that the device's temperature specifications be maintained in order to ensure that the junction temperature is in the proper operating range to meet data sheet specifications. An important way to maintain the proper junction temperature is to use the device's thermal impedances correctly. Thermal impedances are listed for the available packages.

Incorrectly using thermal impedances can produce significant errors.

The device's safe junction temperature range can be maintained when the T_C specification is not exceeded. In applications where the device's ambient temperature is too high, use of forced air and/or heat sinks may be required in order to meet the case temperature specifications.

Table 29: Temperature Limits

Parameter		Symbol	Min	Max	Units	Notes
Storage temperature		T_{STG}	-55	150	°C	1
Reliability junction temperature	Commercial	$T_{J(REL)}$	-	110	°C	2
	Industrial		-	110	°C	2
Operating junction temperature	Commercial	$T_{J(OP)}$	0	100	°C	3
	Industrial		-40	100	°C	3
Operating case temperature	Commercial	T_C	0	95	°C	4, 5
	Industrial		-40	95	°C	4, 5

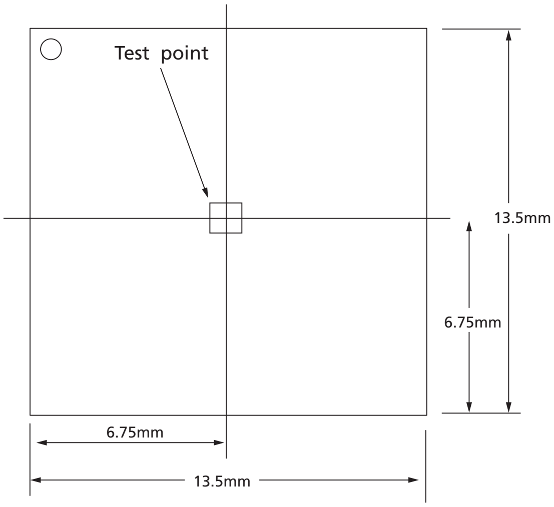
Notes:
1. MAX storage case temperature; T_{STG} is measured in the center of the package (see Figure 21 (page 50)). This case temperature limit is allowed to be exceeded briefly during package reflow.
2. Temperatures greater than 110°C may cause permanent damage to the device. This is a stress rating only and functional operation of the device at or above this is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect the reliability of the part.
3. Junction temperature depends upon package type, cycle time, loading, ambient temperature, and airflow.
4. MAX operating case temperature; T_C is measured in the center of the package (see Figure 21 (page 50)).
5. Device functionality is not guaranteed if the device exceeds maximum T_C during operation.

Table 30: Thermal Impedance

Package	Substrate	θ JA (°C/W) Airflow = 0m/s	θ JA (°C/W) Airflow = 1m/s	θ JA (°C/W) Airflow = 2m/s	θ JB (°C/W)	θ JC (°C/W)
FBGA	2-layer	39.3	28.8	25.2	16.3	2.0
	4-layer	22.0	17.2	15.9	10.3	

Note:
1. Thermal impedance data is based on a number of samples from multiple lots, and should be viewed as a typical number.

Figure 21: Example Temperature Test Point Location


Test point
13.5mm
6.75mm
6.75mm
13.5mm

Command and Address Setup, Hold, and Derating

The total ^tIS (setup time) and ^tIH (hold time) required is calculated by adding the data sheet ^tIS (base) and ^tIH (base) values (see Table 31 (page 51); values come from Table 28 (page 44)) to the Δ^tIS and Δ^tIH derating values (see Table 32 (page 52)), respectively. Example: ^tIS (total setup time) = ^tIS (base) + Δ^tIS. For a valid transition, the input signal must remain above/below $V_{IH(AC)}/V_{IL(AC)}$ for some time ^tVAC (see Table 33 (page 52)).

Although the total setup time for slow slew rates might be negative (for example, a valid input signal will not have reached $V_{IH(AC)}/V_{IL(AC)}$ at the time of the rising clock transition), a valid input signal is still required to complete the transition and to reach $V_{IH(AC)}/V_{IL(AC)}$. For slew rates which fall between the values listed in Table 32 (page 52) and Table 33 (page 52) for Valid Transition, the derating values may be obtained by linear interpolation.

Setup (^tIS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{REF(DC)}$ and the first crossing of $V_{IH(AC)min}$. Setup (^tIS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{REF(DC)}$ and the first crossing of $V_{IL(AC)max}$. If the actual signal is always earlier than the nominal slew rate line between the shaded $V_{REF(DC)}$-to-AC region, use the nominal slew rate for derating value (see Figure 22 (page 53)). If the actual signal is later than the nominal slew rate line anywhere between the shaded $V_{REF(DC)}$-to-AC region, the slew rate of a tangent line to the actual signal from the AC level to the DC level is used for derating value (see Figure 24 (page 55)).

Hold (^tIH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{IL(DC)max}$ and the first crossing of $V_{REF(DC)}$. Hold (^tIH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{IH(DC)min}$ and the first crossing of $V_{REF(DC)}$. If the actual signal is always later than the nominal slew rate line between the shaded DC-to-$V_{REF(DC)}$ region, use the nominal slew rate for derating value (see Figure 23 (page 54)). If the actual signal is earlier than the nominal slew rate line anywhere between the shaded DC-to-$V_{REF(DC)}$ region, the slew rate of a tangent line to the actual signal from the DC level to the $V_{REF(DC)}$ level is used for derating value (see Figure 25 (page 56)).

Table 31: Command and Address Setup and Hold Values Referenced at 1 V/ns – AC/DC-Based

Symbol	RL3-2133	RL3-1866	RL3-1600	Units	Reference
^tIS(base),AC150	85	120	170	ps	$V_{IH(AC)}/V_{IL(AC)}$
^tIH(base),DC100	65	100	120	ps	$V_{IH(DC)}/V_{IL(DC)}$

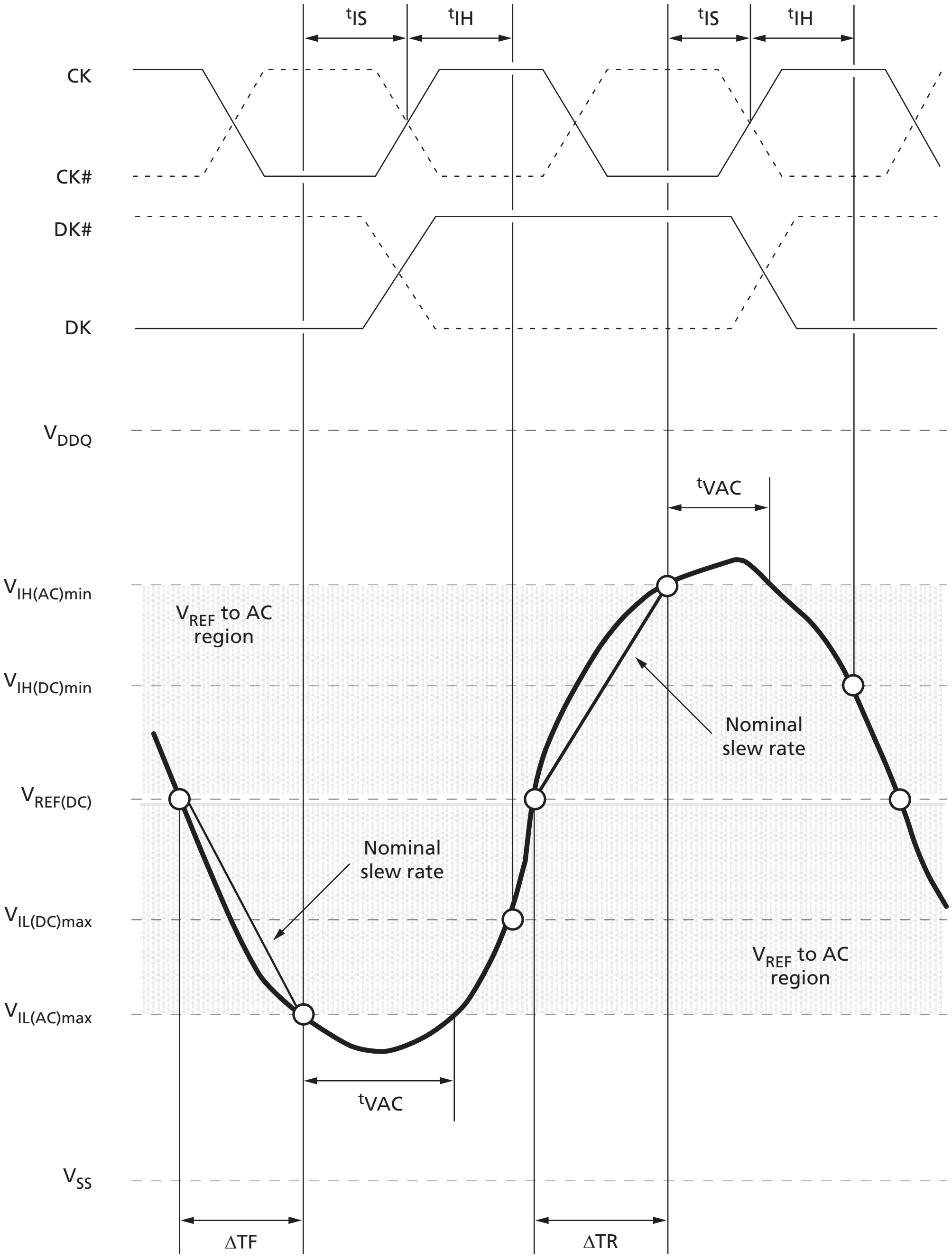
Table 32: Derating Values for ^{t}IS/^{t}IH – AC150/DC100-Based

Δ^tIS, Δ^tIH Derating (ps) - AC/DC-Based AC 150 Threshold: $V_{IH(AC)} = V_{REF(DC)}$ + 150mV, $V_{IL(AC)} = V_{REF(DC)}$ - 150mV																
CMD/ADDR Slew Rate (V/ns)	**CK, CK# Differential Slew Rate**															
	4.0 V/ns		**3.0 V/ns**		**2.0 V/ns**		**1.8 V/ns**		**1.6 V/ns**		**1.4 V/ns**		**1.2 V/ns**		**1.0 V/ns**	
	Δ^tIS	**Δ^tIH**	**Δ^tIS**	**Δ^tIH**	**Δ^tIS**	**Δ^tIH**	**Δ^tIS**	**Δ^tIH**	**Δ^tIS**	**Δ^tIH**	**Δ^tIS**	**Δ^tIH**	**Δ^tIS**	**Δ^tIH**	**Δ^tIS**	**Δ^tIH**
2.0	75	50	75	50	75	50	83	58	91	66	99	74	107	84	115	100
1.5	50	34	50	34	50	34	58	42	66	50	74	58	82	68	90	84
1.0	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
0.9	0	–4	0	–4	0	–4	8	4	16	12	24	20	32	30	40	46
0.8	0	–10	0	–10	0	–10	8	–2	16	6	24	14	32	24	40	40
0.7	0	–16	0	–16	0	–16	8	–8	16	0	24	8	32	18	40	34
0.6	–1	–26	–1	–26	–1	–26	7	–18	15	–10	23	–2	31	8	39	24
0.5	–10	–40	–10	–40	–10	–40	–2	–32	6	–24	14	–16	22	–6	30	10
0.4	–25	–60	–25	–60	–25	–60	–17	–52	–9	–44	–1	–36	7	–26	15	–10

Table 33: Minimum Required Time ^{t}VAC Above $V_{IH(AC)}$ (or Below $V_{IL(AC)}$) for Valid Transition

Slew Rate (V/ns)	^{t}VAC (ps)
>2.0	175
2.0	170
1.5	167
1.0	163
0.9	162
0.8	161
0.7	159
0.6	155
0.5	150
<0.5	150

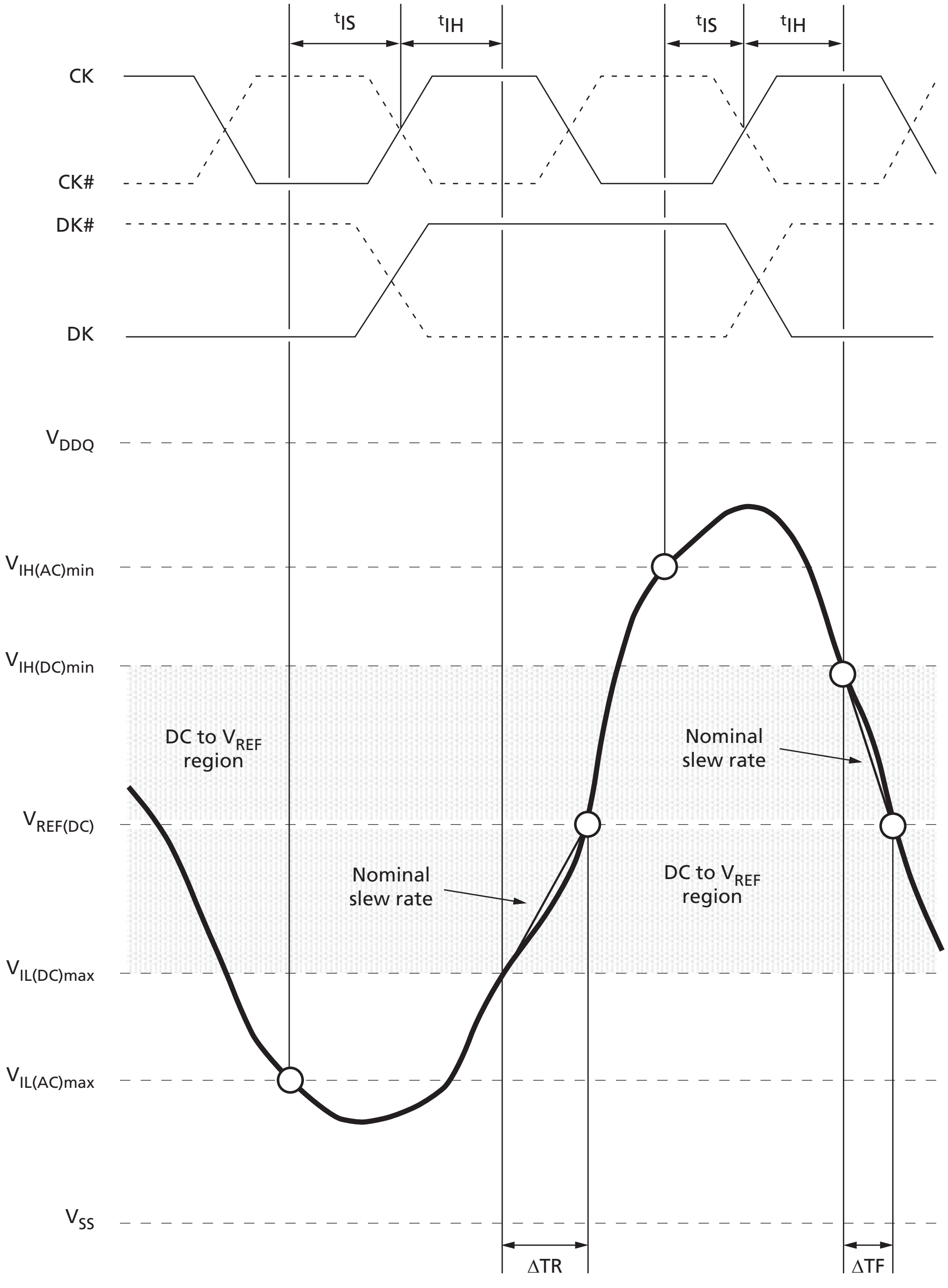
Figure 22: Nominal Slew Rate and ^{t}VAC for ^{t}IS (Command and Address - Clock)


tIS
tIH
tIS
tIH
CK
CK#
DK#
DK
VDDQ
tVAC
VIH(AC)min
VREF to AC region
VIH(DC)min
Nominal slew rate
VREF(DC)
Nominal slew rate
VIL(DC)max
VREF to AC region
VIL(AC)max
tVAC
VSS
ΔTF
ΔTR

$$\text{Setup slew rate falling signal} = \frac{V_{REF(DC)} - V_{IL(AC)max}}{\Delta TF} \qquad \text{Setup slew rate rising signal} = \frac{V_{IH(AC)min} - V_{REF(DC)}}{\Delta TR}$$

Note: 1. Both the clock and the data strobe are drawn on different time scales.

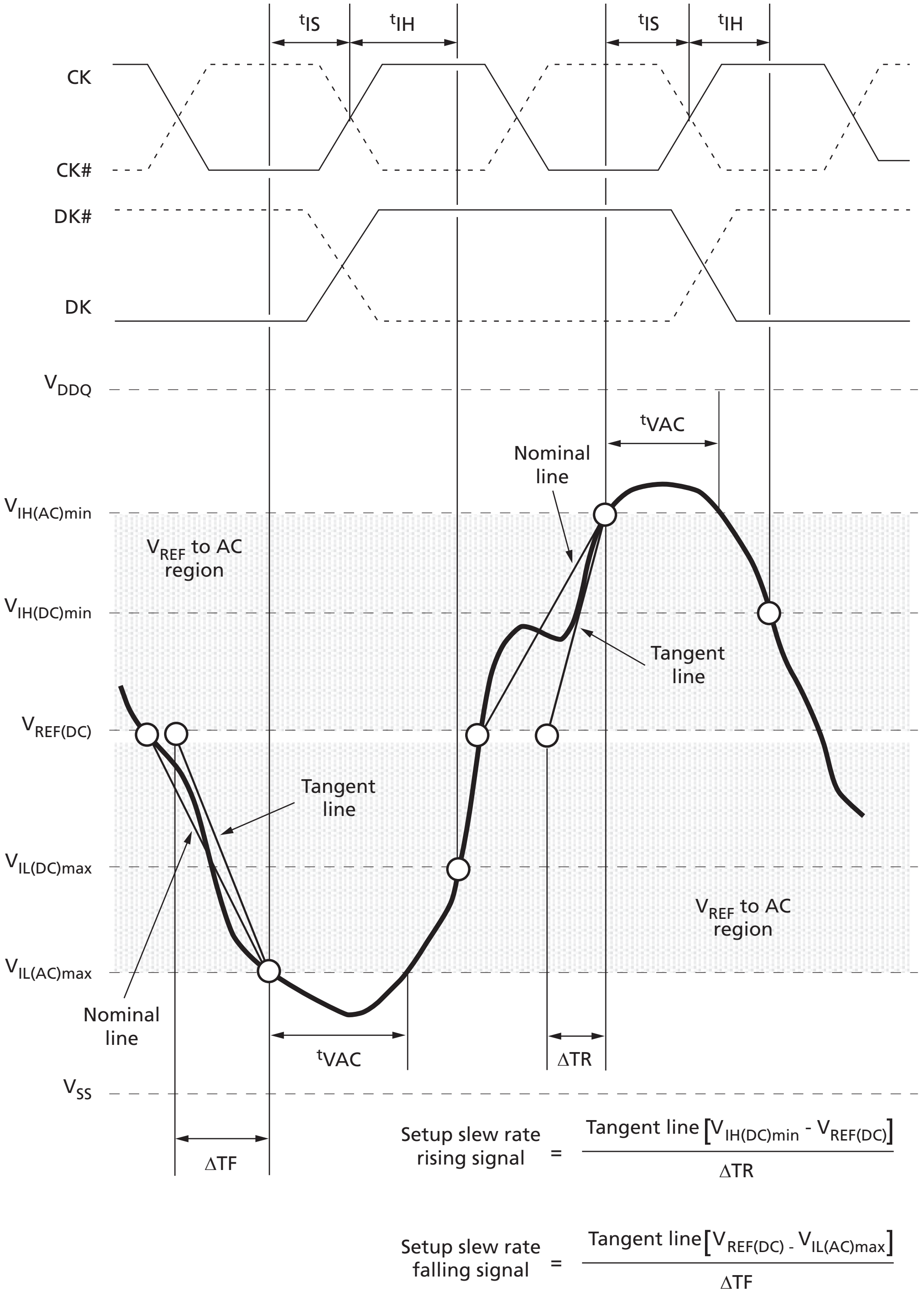
Figure 23: Nominal Slew Rate for ^{t}IH (Command and Address - Clock)


^{t}IS
^{t}IH
^{t}IS
^{t}IH
CK
CK#
DK#
DK
V_{DDQ}
$V_{IH(AC)min}$
$V_{IH(DC)min}$
DC to V_{REF} region
Nominal slew rate
$V_{REF(DC)}$
Nominal slew rate
DC to V_{REF} region
$V_{IL(DC)max}$
$V_{IL(AC)max}$
V_{SS}
ΔTR
ΔTF

$$\text{Hold slew rate rising signal} = \frac{V_{REF(DC)} - V_{IL(DC)max}}{\Delta TR} \qquad \text{Hold slew rate falling signal} = \frac{V_{IH(DC)min} - V_{REF(DC)}}{\Delta TF}$$

Note: 1. Both the clock and the data strobe are drawn on different time scales.

Figure 24: Tangent Line for ^{t}IS (Command and Address - Clock)

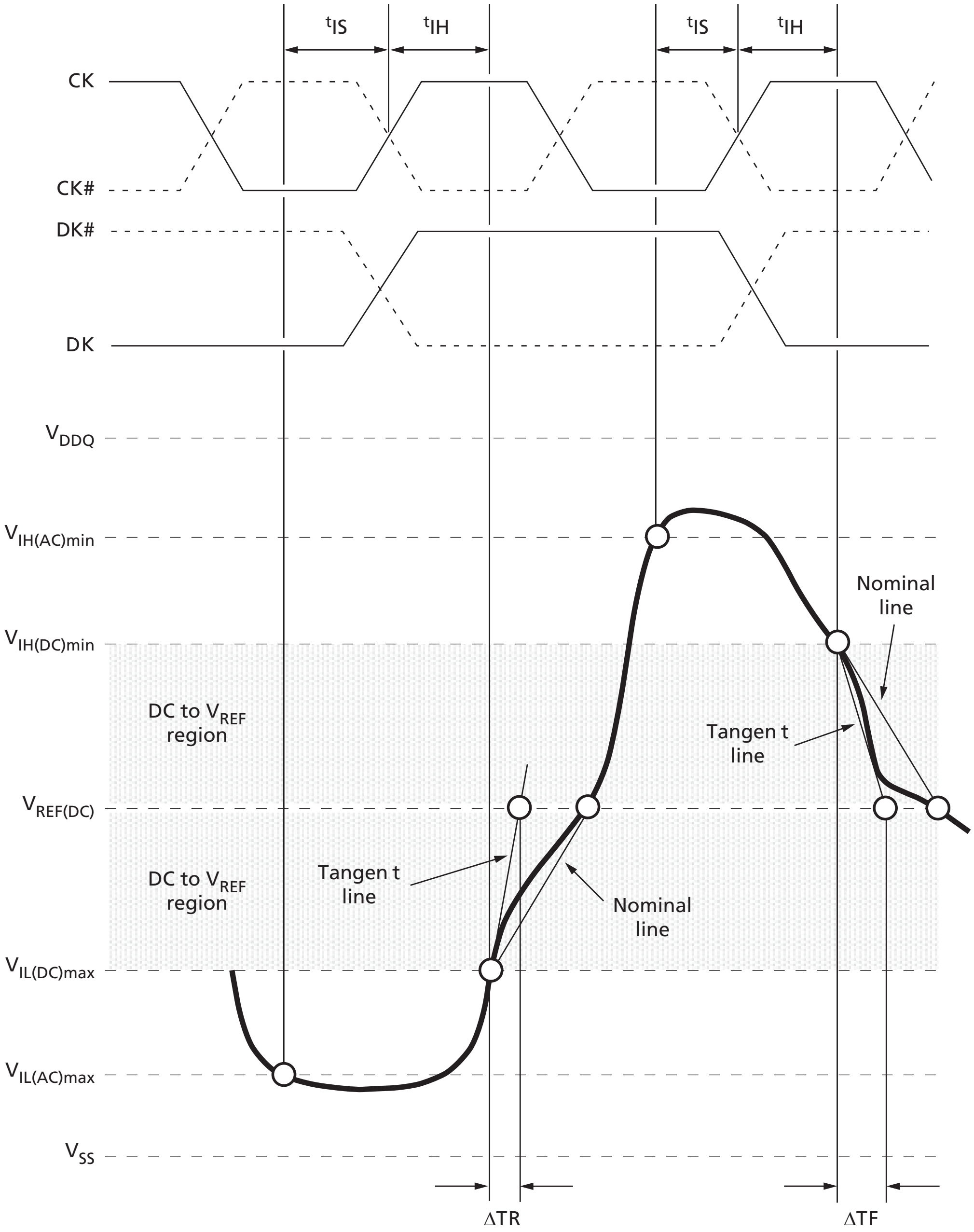

^{t}IS
^{t}IH
^{t}IS
^{t}IH
CK
CK#
DK#
DK
V_{DDQ}
^{t}VAC
Nominal line
$V_{IH(AC)min}$
V_{REF} to AC region
$V_{IH(DC)min}$
Tangent line
$V_{REF(DC)}$
Tangent line
$V_{IL(DC)max}$
V_{REF} to AC region
$V_{IL(AC)max}$
Nominal line
^{t}VAC
ΔTR
V_{SS}
ΔTF

$$\text{Setup slew rate rising signal} = \frac{\text{Tangent line}\left[V_{IH(DC)min} - V_{REF(DC)}\right]}{\Delta TR}$$

$$\text{Setup slew rate falling signal} = \frac{\text{Tangent line}\left[V_{REF(DC)} - V_{IL(AC)max}\right]}{\Delta TF}$$

Note: 1. Both the clock and the data strobe are drawn on different time scales.

Figure 25: Tangent Line for ^{t}IH (Command and Address - Clock)


tIS
tIH
tIS
tIH
CK
CK#
DK#
DK
VDDQ
VIH(AC)min
VIH(DC)min
DC to VREF region
VREF(DC)
DC to VREF region
VIL(DC)max
VIL(AC)max
VSS
Nominal line
Tangent line
Tangent line
Nominal line
ΔTR
ΔTF

$$\text{Hold slew rate rising signal} = \frac{\text{Tangent line }[V_{REF(DC)} - V_{IL(DC)max}]}{\Delta TR}$$

$$\text{Hold slew rate falling signal} = \frac{\text{Tangent line }[V_{IH(DC)min} - V_{REF(DC)}]}{\Delta TF}$$

Note: 1. Both the clock and the data strobe are drawn on different time scales.

Data Setup, Hold, and Derating

The total ^{t}DS (setup time) and ^{t}DH (hold time) required is calculated by adding the data sheet ^{t}DS (base) and ^{t}DH (base) values (see the table below; values come from Table 28 (page 44)) to the Δ^tDS and Δ^tDH derating values (see Table 35 (page 58)), respectively. Example: ^{t}DS (total setup time) = ^{t}DS (base) + Δ^tDS. For a valid transition, the input signal has to remain above/below $V_{IH(AC)}/V_{IL(AC)}$ for some time ^{t}VAC (see Table 36 (page 58)).

Although the total setup time for slow slew rates might be negative (for example, a valid input signal will not have reached $V_{IH(AC)}/V_{IL(AC)}$) at the time of the rising clock transition), a valid input signal is still required to complete the transition and to reach $V_{IH}/V_{IL(AC)}$. For slew rates which fall between the values listed in Table 35 (page 58) and Table 36 (page 58), the derating values may obtained by linear interpolation.

Setup (^{t}DS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{REF(DC)}$ and the first crossing of $V_{IH(AC)min}$. Setup (^{t}DS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{REF(DC)}$ and the first crossing of $V_{IL(AC)max}$. If the actual signal is always earlier than the nominal slew rate line between the shaded $V_{REF(DC)}$-to-AC region, use the nominal slew rate for derating value (see Figure 26 (page 59)). If the actual signal is later than the nominal slew rate line anywhere between the shaded $V_{REF(DC)}$-to-AC region, the slew rate of a tangent line to the actual signal from the AC level to the DC level is used for derating value (see Figure 28 (page 61)).

Hold (^{t}DH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{IL(DC)max}$ and the first crossing of $V_{REF(DC)}$. Hold (^{t}DH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{IH(DC)min}$ and the first crossing of $V_{REF(DC)}$. If the actual signal is always later than the nominal slew rate line between the shaded DC-to-$V_{REF(DC)}$ region, use the nominal slew rate for derating value (see Figure 27 (page 60)). If the actual signal is earlier than the nominal slew rate line anywhere between the shaded DC-to-$V_{REF(DC)}$ region, the slew rate of a tangent line to the actual signal from the DC-to-$V_{REF(DC)}$ region is used for derating value (see Figure 29 (page 62)).

Table 34: Data Setup and Hold Values at 1 V/ns (DKx, DKx# at 2V/ns) – AC/DC-Based

Symbol	RL3-2133	RL3-1866	RL3-1600	Units	Reference
^{t}DS(base),AC150	–30	-15	10	ps	$V_{IH(AC)}/V_{IL(AC)}$
^{t}DH(base),DC100	5	20	45	ps	$V_{IH(DC)}/V_{IL(DC)}$

Table 35: Derating Values for ^{t}DS/^{t}DH – AC150/DC100-Based

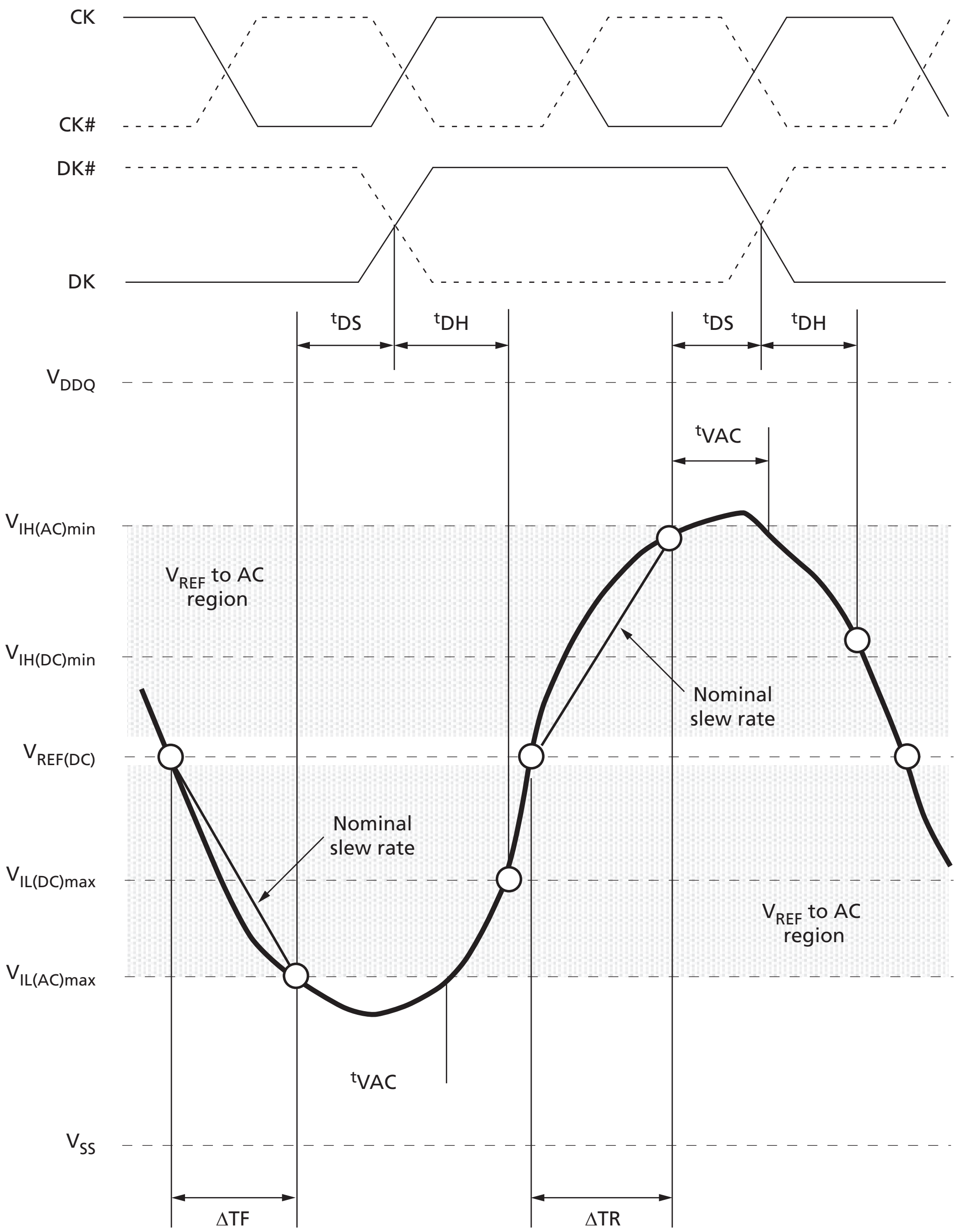
Empty cells indicate slew rate combinations not supported

Δ^{t}DS, Δ^{t}DH Derating (ps) - AC/DC-Based																
DQ Slew Rate (V/ns)	DKx, DKx# Differential Slew Rate															
	4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
	Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH
2.0	75	50	75	50	75	50										
1.5	50	34	50	34	50	34	58	42								
1.0	0	0	0	0	0	0	8	8	16	16						
0.9			0	–4	0	–4	8	4	16	12	24	20				
0.8					0	–10	8	–2	16	6	24	14	32	24		
0.7							8	–8	16	0	24	8	32	18	40	34
0.6									15	–10	23	–2	31	8	39	24
0.5											14	–16	22	–6	30	10
0.4													7	–26	15	–10

Table 36: Minimum Required Time ^{t}VAC Above $V_{IH(AC)}$ (or Below $V_{IL(AC)}$) for Valid Transition

Slew Rate (V/ns)	^{t}VAC (ps)
>2.0	175
2.0	170
1.5	167
1.0	163
0.9	162
0.8	161
0.7	159
0.6	155
0.5	150
<0.5	150

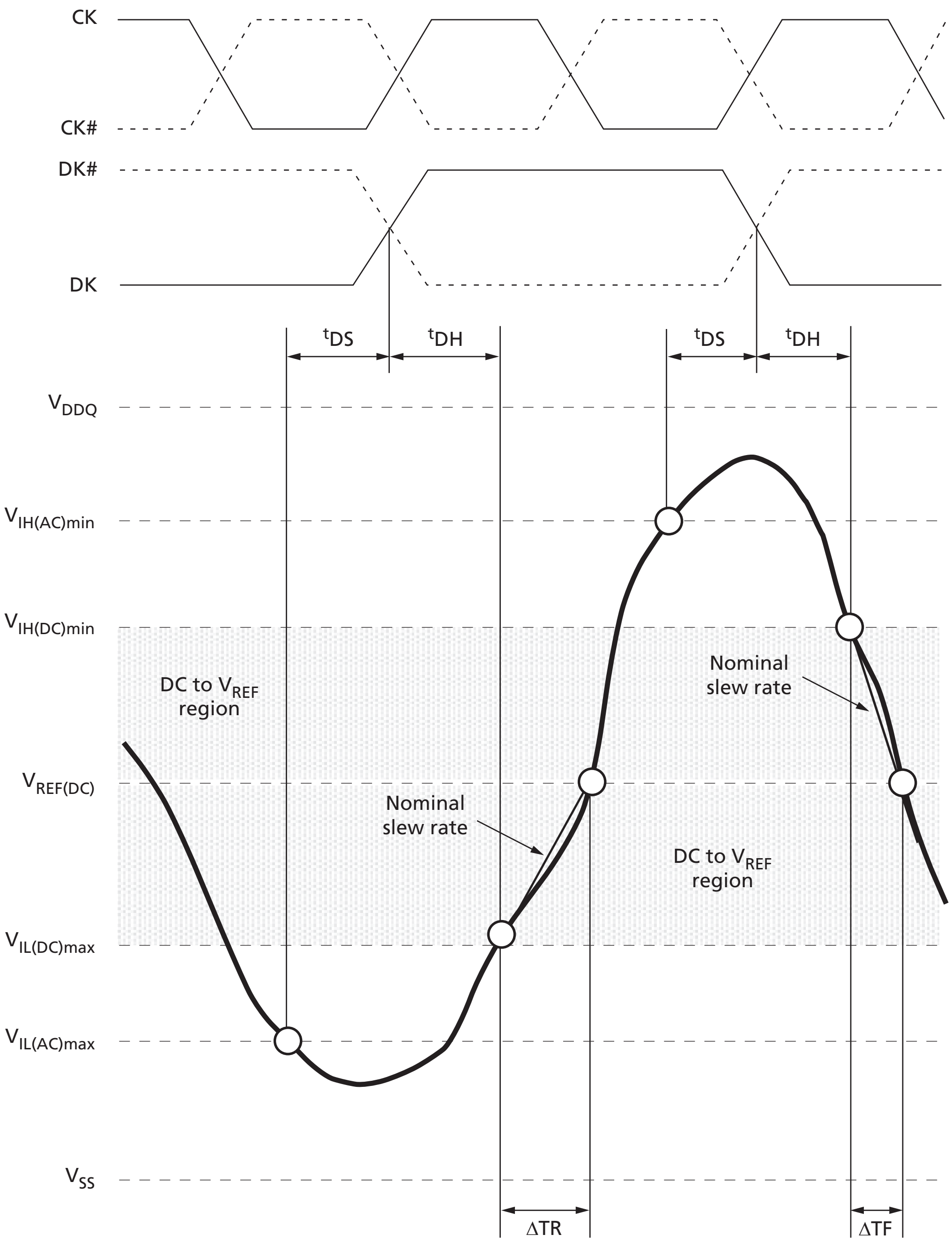
Figure 26: Nominal Slew Rate and ^tVAC for ^tDS (DQ - Strobe)


CK
CK#
DK#
DK
^tDS
^tDH
^tDS
^tDH
V_{DDQ}
^tVAC
$V_{IH(AC)min}$
V_{REF} to AC region
$V_{IH(DC)min}$
Nominal slew rate
$V_{REF(DC)}$
Nominal slew rate
$V_{IL(DC)max}$
V_{REF} to AC region
$V_{IL(AC)max}$
^tVAC
V_{SS}
ΔTF
ΔTR

$$\text{Setup slew rate falling signal} = \frac{V_{REF(DC)} - V_{IL(AC)max}}{\Delta TF} \qquad \text{Setup slew rate rising signal} = \frac{V_{IH(AC)min} - V_{REF(DC)}}{\Delta TR}$$

Note: 1. Both the clock and the strobe are drawn on different time scales.

Figure 27: Nominal Slew Rate for ^{t}DH (DQ - Strobe)

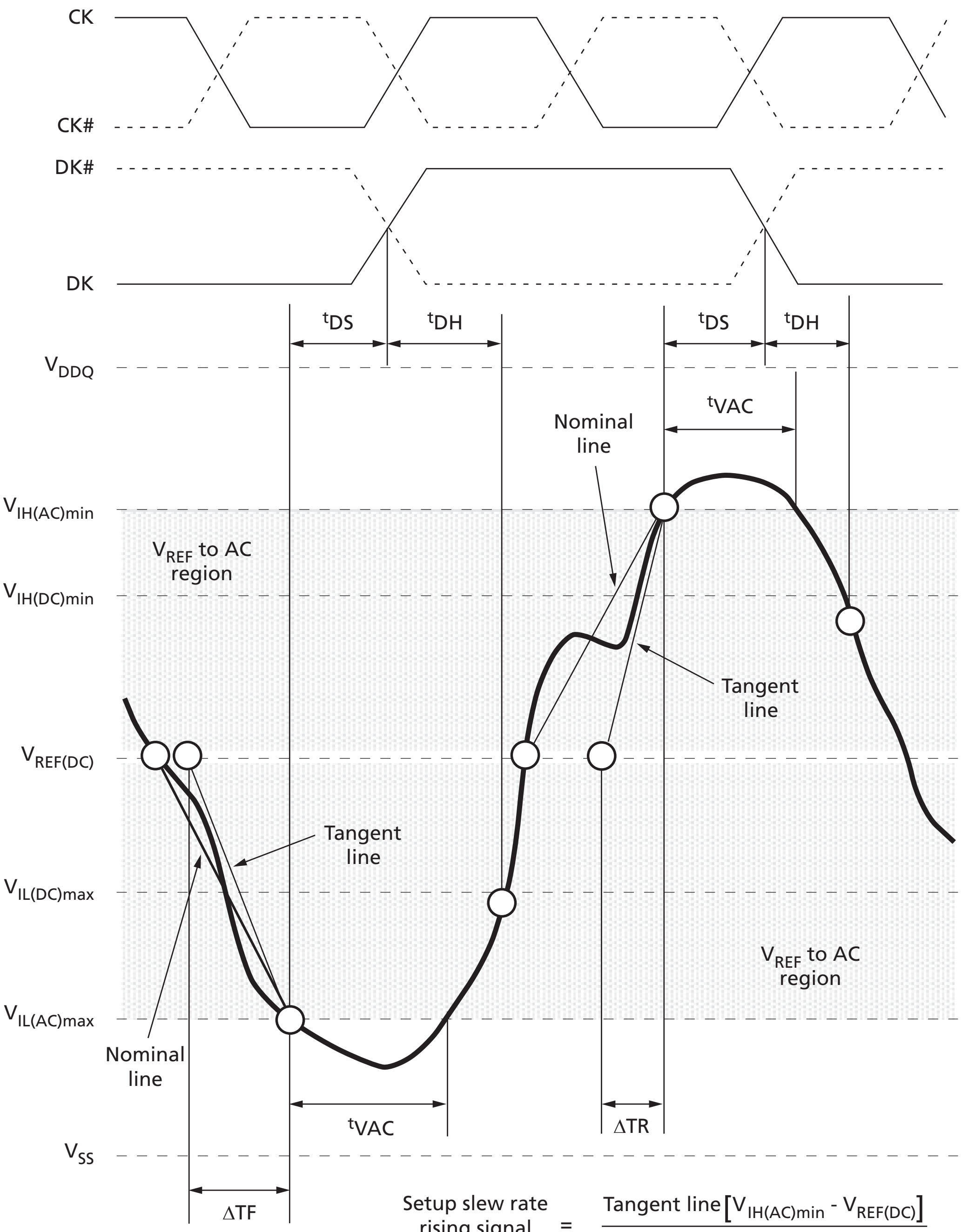

CK
CK#
DK#
DK
tDS
tDH
tDS
tDH
VDDQ
VIH(AC)min
VIH(DC)min
DC to VREF region
Nominal slew rate
VREF(DC)
Nominal slew rate
DC to VREF region
VIL(DC)max
VIL(AC)max
VSS
ΔTR
ΔTF

Hold slew rate rising signal $= \frac{V_{REF(DC)} - V_{IL(DC)max}}{\Delta TR}$

Hold slew rate falling signal $= \frac{V_{IH(DC)min} - V_{REF(DC)}}{\Delta TF}$

Note: 1. Both the clock and the strobe are drawn on different time scales.

Figure 28: Tangent Line for ^{t}DS (DQ - Strobe)

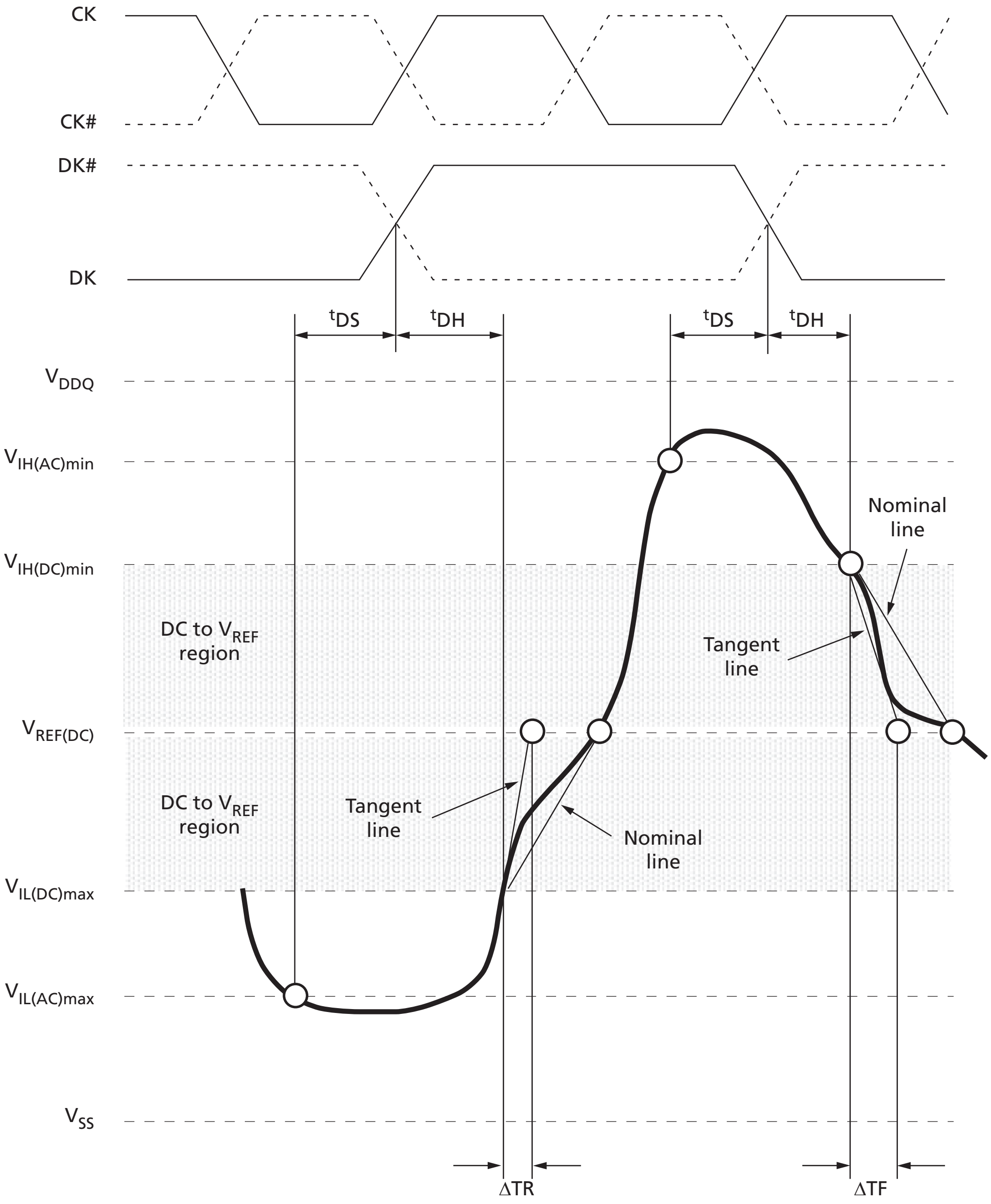

CK
CK#
DK#
DK
tDS
tDH
tDS
tDH
VDDQ
tVAC
Nominal line
VIH(AC)min
VREF to AC region
VIH(DC)min
Tangent line
VREF(DC)
Tangent line
VIL(DC)max
VREF to AC region
VIL(AC)max
Nominal line
tVAC
ΔTR
VSS
ΔTF

$$\text{Setup slew rate rising signal} = \frac{\text{Tangent line}\left[V_{IH(AC)min} - V_{REF(DC)}\right]}{\Delta TR}$$

$$\text{Setup slew rate falling signal} = \frac{\text{Tangent line}\left[V_{REF(DC)} - V_{IL(AC)max}\right]}{\Delta TF}$$

Note: 1. Both the clock and the strobe are drawn on different time scales.

Figure 29: Tangent Line for ^{t}DH (DQ - Strobe)


CK
CK#
DK#
DK
tDS
tDH
tDS
tDH
VDDQ
VIH(AC)min
VIH(DC)min
VREF(DC)
VIL(DC)max
VIL(AC)max
VSS
DC to VREF region
DC to VREF region
Tangent line
Nominal line
Tangent line
Nominal line
ΔTR
ΔTF

$$\text{Hold slew rate rising signal} = \frac{\text{Tangent line}\left[V_{REF(DC)} - V_{IL(DC)max}\right]}{\Delta TR}$$

$$\text{Hold slew rate falling signal} = \frac{\text{Tangent line}\left[V_{IH(DC)min} - V_{REF(DC)}\right]}{\Delta TF}$$

Note: 1. Both the clock and the strobe are drawn on different time scales.

Commands

The following table provides descriptions of the valid commands of the RLDRAM 3 device. All command and address inputs must meet setup and hold times with respect to the rising edge of CK.

Table 37: Command Descriptions

Command	Description
NOP	The NOP command prevents new commands from being executed by the DRAM. Operations already in progress are not affected by NOP commands. Output values depend on command history.
MRS	Mode registers MR0, MR1, and MR2 are used to define various modes of programmable operations of the DRAM. A mode register is programmed via the MODE REGISTER SET (MRS) command during initialization and retains the stored information until it is reprogrammed, RESET# goes LOW, or until the device loses power. The MRS command can be issued only when all banks are idle, and no bursts are in progress.
READ	The READ command is used to initiate a burst read access to a bank. The BA[3:0] inputs select a bank, and the address provided on inputs A[19:0] select a specific location within a bank.
WRITE	The WRITE command is used to initiate a burst write access to a bank (or banks). MRS bits MR2[4:3] select single, dual, or quad bank WRITE protocol. The BA[*x*:0] inputs select the bank(s) (x = 3, 2, or 1 for single, dual, or quad bank WRITE, respectively). The address provided on inputs A[19:0] select a specific location within the bank. Input data appearing on the DQ is written to the memory array subject to the DM input logic level appearing coincident with the data. If the DM signal is registered LOW, the corresponding data will be written to memory. If the DM signal is registered HIGH, the corresponding data inputs will be ignored (that is, this part of the data word will not be written).
AREF	The AREF command is used during normal operation of the RLDRAM 3 to refresh the memory content of a bank. There are two methods by which the RLDRAM 3 can be refreshed, both of which are selected within the mode register. The first method, bank address-controlled AREF, is identical to the method used in RLDRAM2. The second method, multibank AREF, enables refreshing of up to four banks simultaneously. More info is available in the Auto Refresh section. For both methods, the command is nonpersistent, so it must be issued each time a refresh is required.

Table 38: Command Table

Note 1 applies to the entire table

Operation	Code	CS#	WE#	REF#	A[19:0]	BA[3:0]	Notes
NOP	NOP	H	H	H	X	X	
MRS	MRS	L	L	L	OPCODE	OPCODE	
READ	READ	L	H	H	A	BA	2
WRITE	WRITE	L	L	H	A	BA	2
AUTO REFRESH	AREF	L	H	L	A	BA	3

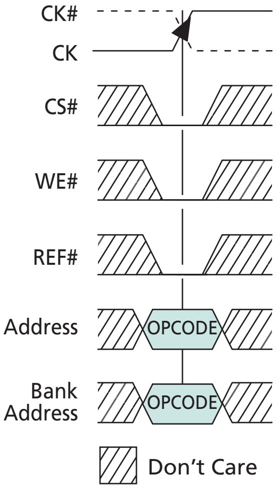
Notes:
1. X = "Don't Care;" H = logic HIGH; L = logic LOW; A = valid address; BA = valid bank address; OPCODE = mode register bits
2. Address width varies with burst length and configuration; see the Address Widths of Different Burst Lengths table for more information.
3. Bank address signals (BA) are used only during bank address-controlled AREF; Address signals (A) are used only during multibank AREF.

MODE REGISTER SET (MRS) Command

The mode registers, MR0, MR1, and MR2, store the data for controlling the operating modes of the memory. The MODE REGISTER SET (MRS) command programs the RLDRAM 3 operating modes and I/O options. During an MRS command, the address inputs are sampled and stored in the mode registers. The BA[1:0] signals select between mode registers 0–2 (MR0–MR2). After the MRS command is issued, each mode register retains the stored information until it is reprogrammed, until RESET# goes LOW, or until the device loses power.

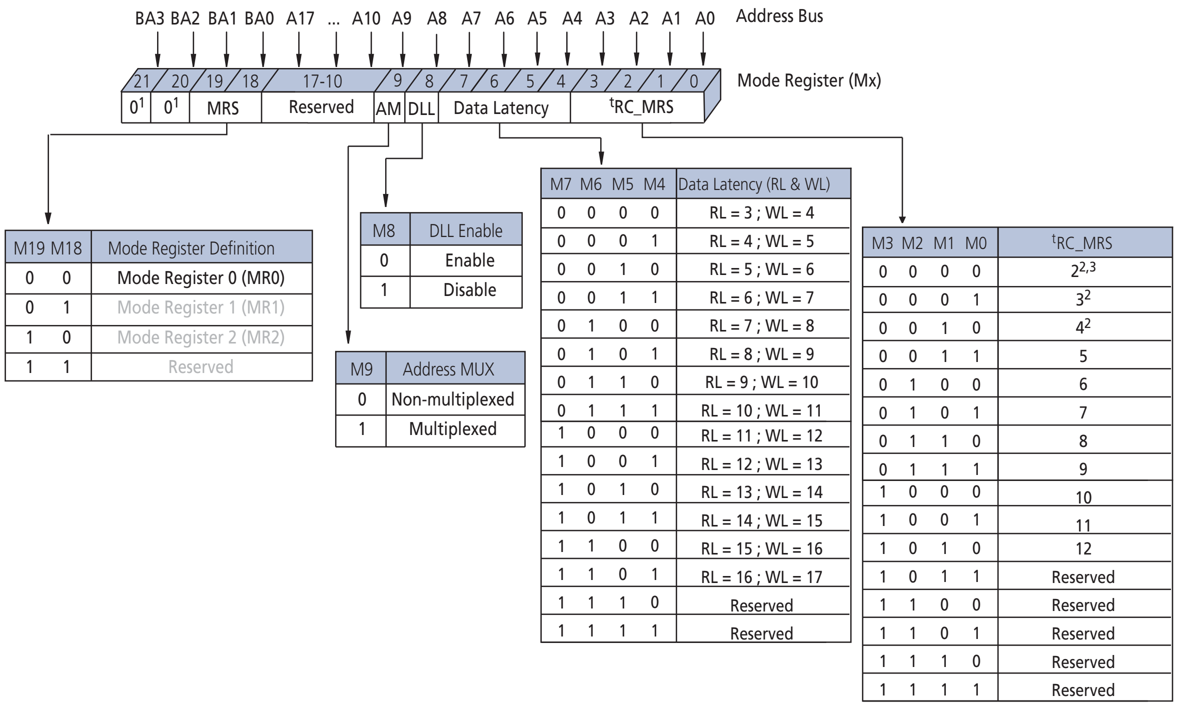
After issuing a valid MRS command, ^{t}MRSC must be met before any command can be issued to the RLDRAM 3. The MRS command can be issued only when all banks are idle, and no bursts are in progress.

Figure 30: MRS Command Protocol



Mode Register 0 (MR0)

Figure 31: MR0 Definition for Non-Multiplexed Address Mode


BA3 BA2 BA1 BA0 A17 ... A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0
Address Bus
21 20 19 18 17-10 9 8 7 6 5 4 3 2 1 0
Mode Register (Mx)
0[1] 0[1] MRS Reserved AM DLL Data Latency tRC_MRS

M19	M18	Mode Register Definition
0	0	Mode Register 0 (MR0)
0	1	Mode Register 1 (MR1)
1	0	Mode Register 2 (MR2)
1	1	Reserved

M9	Address MUX
0	Non-multiplexed
1	Multiplexed

M8	DLL Enable
0	Enable
1	Disable

M7	M6	M5	M4	Data Latency (RL & WL)
0	0	0	0	RL = 3 ; WL = 4
0	0	0	1	RL = 4 ; WL = 5
0	0	1	0	RL = 5 ; WL = 6
0	0	1	1	RL = 6 ; WL = 7
0	1	0	0	RL = 7 ; WL = 8
0	1	0	1	RL = 8 ; WL = 9
0	1	1	0	RL = 9 ; WL = 10
0	1	1	1	RL = 10 ; WL = 11
1	0	0	0	RL = 11 ; WL = 12
1	0	0	1	RL = 12 ; WL = 13
1	0	1	0	RL = 13 ; WL = 14
1	0	1	1	RL = 14 ; WL = 15
1	1	0	0	RL = 15 ; WL = 16
1	1	0	1	RL = 16 ; WL = 17
1	1	1	0	Reserved
1	1	1	1	Reserved

M3	M2	M1	M0	tRC_MRS
0	0	0	0	2[2,3]
0	0	0	1	3[2]
0	0	1	0	4[2]
0	0	1	1	5
0	1	0	0	6
0	1	0	1	7
0	1	1	0	8
0	1	1	1	9
1	0	0	0	10
1	0	0	1	11
1	0	1	0	12
1	0	1	1	Reserved
1	1	0	0	Reserved
1	1	0	1	Reserved
1	1	1	0	Reserved
1	1	1	1	Reserved

Notes:
1. BA2, BA3, and all address balls corresponding to reserved bits must be held LOW during the MRS command.
2. BL8 not allowed.
3. BL4 not allowed.

^{t}RC

Bits MR0[3:0] select the number of clock cycles required to satisfy the ^{t}RC specifications.

After a READ, WRITE, or AREF command is issued to a bank, a subsequent READ, WRITE, or AREF cannot be issued to the same bank until ^{t}RC has been satisfied. The correct value (^{t}RC_MRS) to program into MR0[3:0] is shown in the table below.

Table 39: ^{t}RC_MRS MR0[3:0] values

Parameter	-093E	-093	-107E	-107	-125F	-125E	-125
RL = 3; WL = 4	2	2	Reserved	Reserved	Reserved	Reserved	Reserved
RL = 4; WL = 5	2	3	2	3	Reserved	3	3
RL = 5; WL = 6	3	4	3	3	Reserved	3	3
RL = 6; WL = 7	4	4	3	4	Reserved	4	4
RL = 7; WL = 8	4	4	4	4	Reserved	4	4
RL = 8; WL = 9	5	6	4	5	Reserved	5	5
RL = 9; WL = 10	5	6	5	6	Reserved	6	6
RL = 10; WL = 11	6	7	5	6	Reserved	6	6
RL = 11; WL = 12	6	7	6	7	Reserved	7	7
RL = 12; WL = 13	7	8	6	7	6	7	7
RL = 13; WL = 14	7	8	7	8	7	8	8
RL = 14; WL = 15	8	10	7	8	Reserved	Reserved	9
RL = 15; WL = 16	8	10	8	10	Reserved	Reserved	10
RL = 16; WL = 17	9	11	Reserved	Reserved	Reserved	Reserved	10

Data Latency

The data latency register uses MR0[7:4] to set both the READ and WRITE latency (RL and WL). The valid operating frequencies for each data latency register setting can be found in Table 28 (page 44).

DLL Enable/Disable

Through the programming of MR0[8], the DLL can be enabled or disabled.

The DLL must be enabled for normal operation. The DLL must be enabled during the initialization routine and upon returning to normal operation after having been disabled for the purpose of debugging or evaluation. To operate the RLDRAM with the DLL disabled, the ^{t}RC MRS setting must equal the read latency (RL) setting. Enabling the DLL should always be followed by resetting the DLL using the appropriate MR1 command.

Address Multiplexing

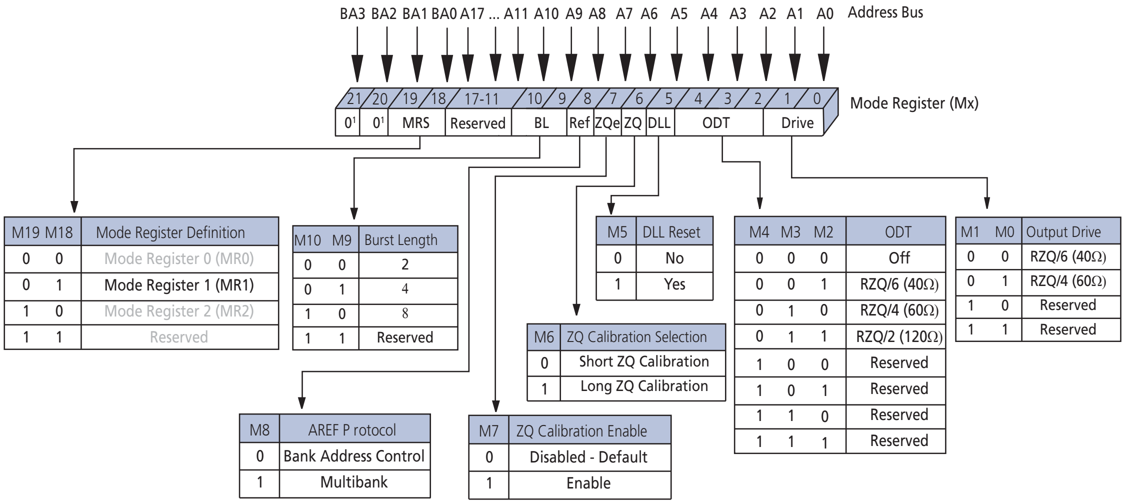
Although the RLDRAM has the ability to operate similar to an SRAM interface by accepting the entire address in one clock (non-multiplexed, or broadside addressing), MR0[9] can be set to 1 so that it functions with multiplexed addressing, similar to a traditional DRAM. In multiplexed address mode, the address is provided to the RLDRAM in two parts that are latched into the memory with two consecutive rising edges of CK.

When in multiplexed address mode, only 11 address balls are required to control the RLDRAM, as opposed to 20 address balls when in non-multiplexed address mode. The data bus efficiency in continuous burst mode is only affected when using the BL = 2 setting because the device requires two clocks to read and write data. During multiplexed mode, the bank addresses as well as WRITE and READ commands are issued during the first address part, A*x*. The Address Mapping in Multiplexed Address Mode table shows the addresses needed for both the first and second rising clock edges (A*x* and A*y*, respectively).

After MR0[9] is set HIGH, READ, WRITE, and MRS commands follow the format described in the Command Description in Multiplexed Address Mode figure. Refer to Multiplexed Address Mode for further information on operation with multiplexed addressing.

Mode Register 1 (MR1)

Figure 32: MR1 Definition for Non-Multiplexed Address Mode


BA3 BA2 BA1 BA0 A17 ... A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0
Address Bus
21 20 19 18 17-11 10 9 8 7 6 5 4 3 2 1 0
0¹ 0¹ MRS Reserved BL Ref ZQe ZQ DLL ODT Drive
Mode Register (Mx)

M19	M18	Mode Register Definition
0	0	Mode Register 0 (MR0)
0	1	Mode Register 1 (MR1)
1	0	Mode Register 2 (MR2)
1	1	Reserved

M10	M9	Burst Length
0	0	2
0	1	4
1	0	8
1	1	Reserved

M8	AREF P rotocol
0	Bank Address Control
1	Multibank

M7	ZQ Calibration Enable
0	Disabled - Default
1	Enable

M6	ZQ Calibration Selection
0	Short ZQ Calibration
1	Long ZQ Calibration

M5	DLL Reset
0	No
1	Yes

M4	M3	M2	ODT
0	0	0	Off
0	0	1	RZQ/6 (40Ω)
0	1	0	RZQ/4 (60Ω)
0	1	1	RZQ/2 (120Ω)
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

M1	M0	Output Drive
0	0	RZQ/6 (40Ω)
0	1	RZQ/4 (60Ω)
1	0	Reserved
1	1	Reserved

Notes:
1. BA2, BA3, and all address balls corresponding to reserved bits must be held LOW during the MRS command.
2. BL8 not available in x36.

Output Drive Impedance

The RLDRAM 3 uses programmable impedance output buffers, which enable the user to match the driver impedance to the system. MR1[0] and MR1[1] are used to select 40Ω or 60Ω output impedance, but the device powers up with an output impedance of 40Ω. The drivers have symmetrical output impedance. To calibrate the impedance a 240Ω ±1% external precision resistor (RZQ) is connected between the ZQ ball and V_{SSQ}.

The output impedance is calibrated during initialization through the ZQCL mode register setting. Subsequent periodic calibrations (ZQCS) may be performed to compensate for shifts in output impedance due to changes in temperature and voltage. More detailed information on calibration can be found in the ZQ Calibration section.

DQ On-Die Termination (ODT)

MR1[4:2] are used to select the value of the on-die termination (ODT) for the DQ, DK*x* and DM balls. When enabled, ODT terminates these balls to $V_{DDQ}/2$. The RLDRAM 3 device supports 40Ω, 60Ω, or 120Ω ODT. The ODT function is dynamically switched off when a DQ begins to drive after a READ command has been issued. Similarly, ODT is designed to switch on at the DQs after the RLDRAM has issued the last piece of data. The DM and DK*x* balls are always terminated after ODT is enabled.

DLL Reset

Programming MR1[5] to 1 activates the DLL RESET function. MR1[5] is self-clearing, meaning it returns to a value of 0 after the DLL RESET function has been initiated.

Whenever the DLL RESET function is initiated, CK/CK# must be held stable for 512 clock cycles before a READ command can be issued. This is to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may cause output timing specifications, such as ^{t}CKQK, to be invalid .

ZQ Calibration

The ZQ CALIBRATION mode register command is used to calibrate the DRAM output drivers (R_{ON}) and ODT values (R_{TT}) over process, voltage, and temperature, provided a dedicated 240Ω (±1%) external resistor is connected from the DRAM's RZQ ball to V_{SSQ}. Bit MR1[6] selects between ZQ calibration long (ZQCL) and ZQ calibration short (ZQCS), each of which are described in detail below. When bit MR1[7] is set HIGH, it enables the calibration sequence. Upon completion of the ZQ calibration sequence, MR1[7] automatically resets LOW.

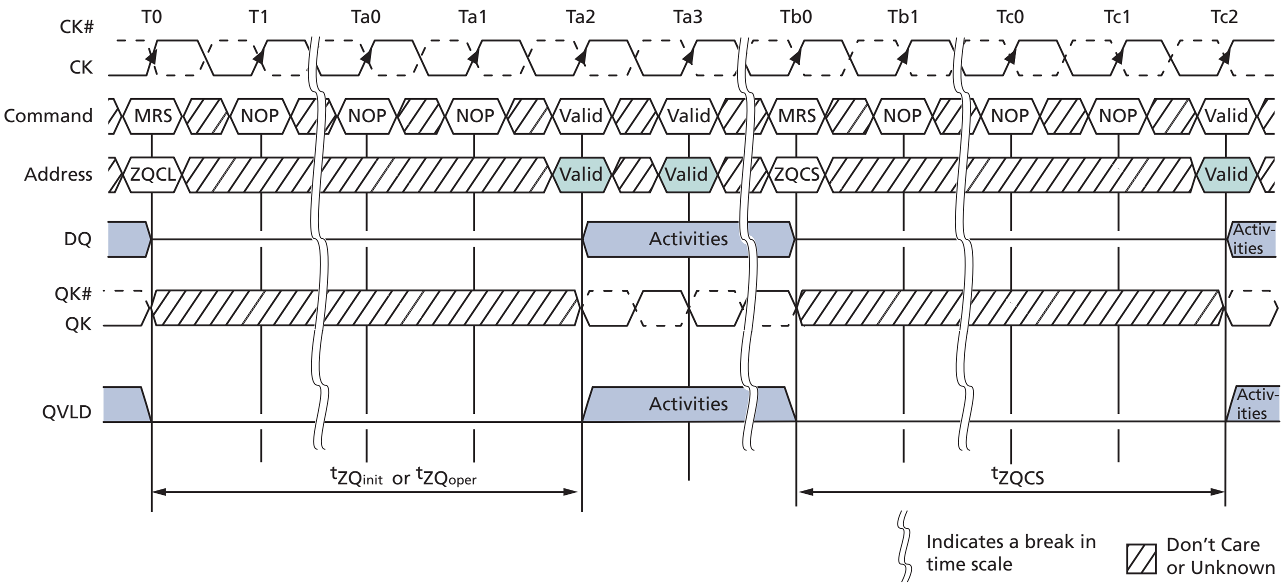
The RLDRAM 3 needs a longer time to calibrate R_{ON} and ODT at power-up initialization and a relatively shorter time to perform periodic calibrations. An example of ZQ calibration timing is shown below.

All banks must have ^{t}RC met before ZQCL or ZQCS mode register settings can be issued to the DRAM. No other activities (other than loading another ZQCL or ZQCS mode register setting may be issued to another DRAM) can be performed on the DRAM channel by the controller for the duration of ^{t}ZQinit or ^{t}ZQoper. The quiet time on the DRAM channel helps accurately calibrate R_{ON} and ODT. After DRAM calibration is achieved, the DRAM will disable the ZQ ball's current consumption path to reduce power.

ZQ CALIBRATION mode register settings can be loaded in parallel to DLL reset and locking time.

In systems that share the ZQ resistor between devices, the controller must not allow overlap of ^{t}ZQinit, ^{t}ZQoper, or ^{t}ZQcs between devices.

Figure 33: ZQ Calibration Timing (ZQCL and ZQCS)


CK#
CK
T0
T1
Ta0
Ta1
Ta2
Ta3
Tb0
Tb1
Tc0
Tc1
Tc2
Command
MRS
NOP
NOP
NOP
Valid
Valid
MRS
NOP
NOP
NOP
Valid
Address
ZQCL
Valid
Valid
ZQCS
Valid
DQ
Activities
Activ-ities
QK#
QK
QVLD
Activities
Activ-ities
tZQinit or tZQoper
tZQCS
Indicates a break in time scale
Don't Care or Unknown

Notes:
1. All devices connected to the DQ bus should be held High-Z during calibration.
2. The state of QK and QK# are unknown during ZQ calibration.
3. tMRSC after loading the MR1 settings, QVLD output drive strength will be at the value selected or higher (lower resistance) until ZQ calibration is complete.

ZQ Calibration Long

The ZQ calibration long (ZQCL) mode register setting is used to perform the initial calibration during a power-up initialization and reset sequence. It may be loaded at any time by the controller depending on the system environment. ZQCL triggers the calibration engine inside the DRAM. After calibration is achieved, the calibrated values are transferred from the calibration engine to the DRAM I/O, which are reflected as updated R_{ON} and ODT values.

The DRAM is allowed a timing window defined by either tZQinit or tZQoper to perform the full calibration and transfer of values. When ZQCL is issued during the initialization sequence, the timing parameter tZQinit must be satisfied. When initialization is complete, subsequent loading of the ZQCL mode register setting requires the timing parameter tZQoper to be satisfied.

ZQ Calibration Short

The ZQ calibration short (ZQCS) mode register setting is used to perform periodic calibrations to account for small voltage and temperature variations. The shorter timing window is provided to perform the reduced calibration and transfer of values as defined by timing parameter tZQCS. ZQCS can effectively correct a minimum of 0.5% R_{ON} and R_{TT} impedance error within 64 clock cycles, assuming the maximum sensitivities specified in the ODT Temperature and Voltage Sensitivity and the Output Driver Voltage and Temperature Sensitivity tables.

AUTO REFRESH Protocol

The AUTO REFRESH (AREF) protocol is selected with bit MR1[8]. There are two ways in which AREF commands can be issued to the RLDRAM. Depending upon how bit MR1[8] is programmed, the memory controller can issue either bank address-controlled or multibank AREF commands. Bank address-controlled AREF uses the BA[3:0] inputs to refresh a single bank per command. Multibank AREF is enabled by setting bit MR1[8] HIGH during an MRS command. This refresh protocol enables the simultaneous refreshing of a row in up to four banks. In this method, the address pins A[15:0] represent banks 0–15, respectively. More information on both AREF protocols can be found in AUTO REFRESH Command (page 78).

Burst Length (BL)

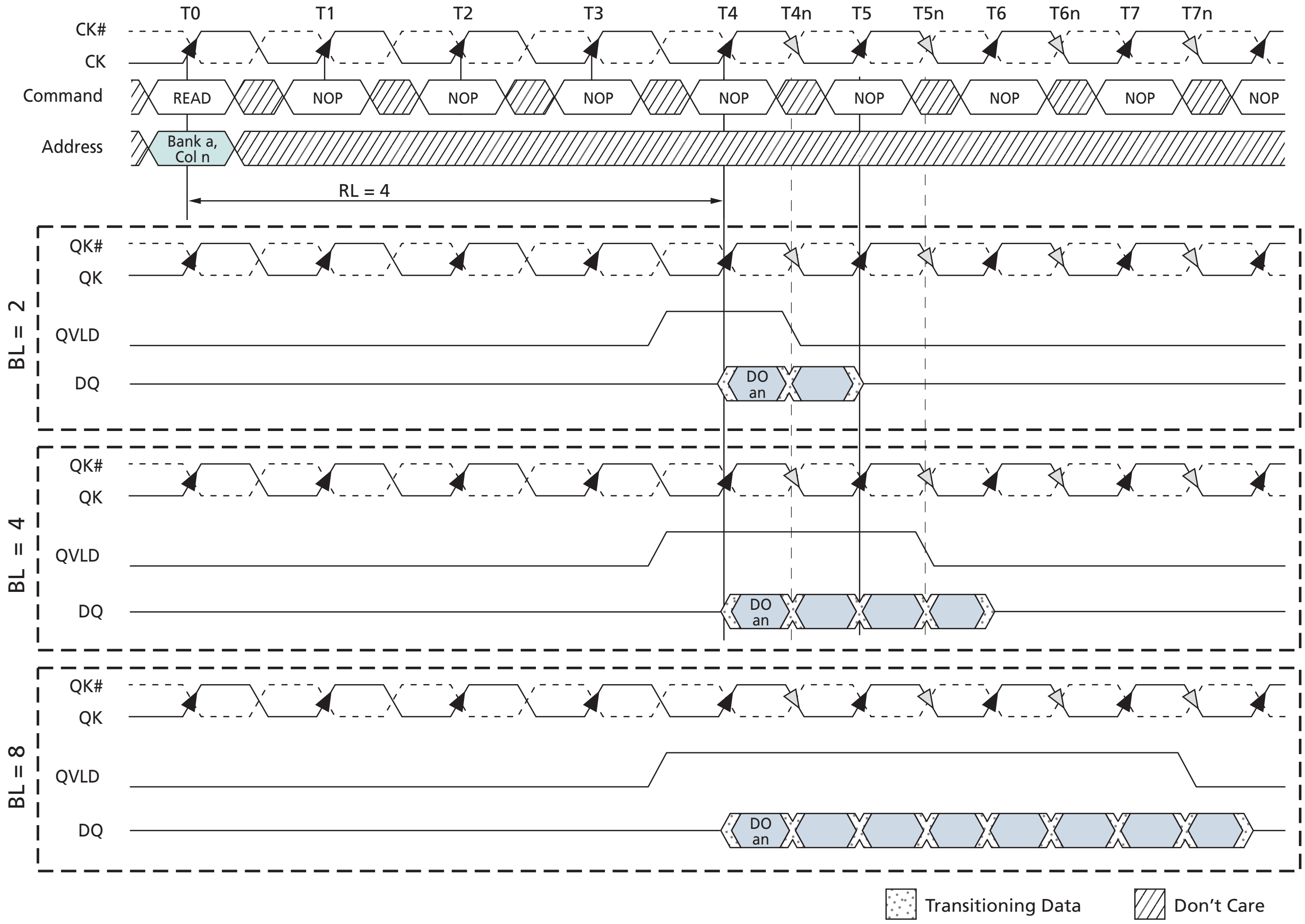
Burst length is defined by MR1[9] and MR1[10]. Read and write accesses to the RLDRAM are burst-oriented, with the burst length being programmable to 2, 4, or 8. Figure 34 (page 72) shows the different burst lengths with respect to a READ command. Changes in the burst length affect the width of the address bus (see the following table for details).

The data written by the prior burst length is not guaranteed to be accurate when the burst length of the device is changed.

Table 40: Address Widths of Different Burst Lengths

Burst Length	Configuration	
	x18	x36
2	A[19:0]	A[18:0]
4	A[18:0]	A[17:0]
8	A[17:0]	NA

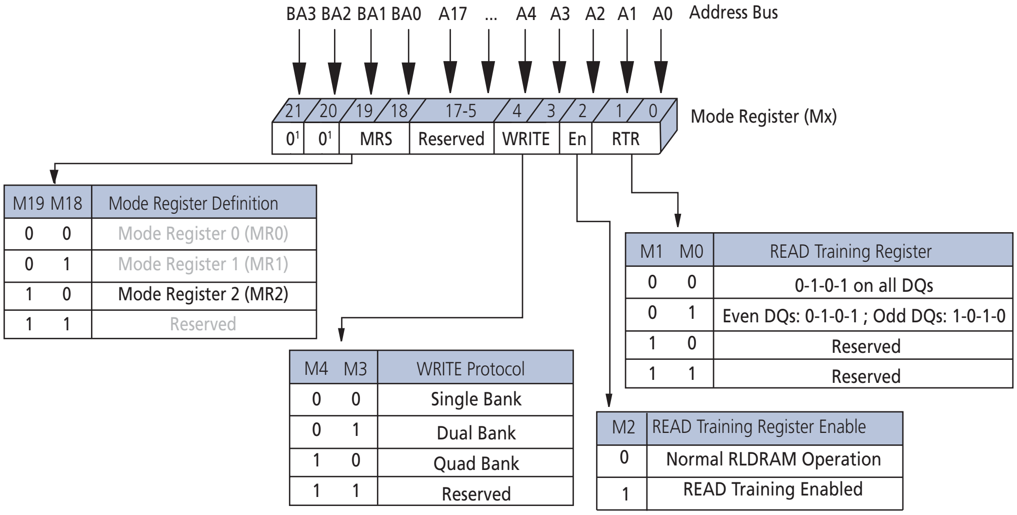
Figure 34: Read Burst Lengths


T0
T1
T2
T3
T4
T4n
T5
T5n
T6
T6n
T7
T7n
CK#
CK
Command
READ
NOP
Address
Bank a, Col n
RL = 4
BL = 2
BL = 4
BL = 8
QK#
QK
QVLD
DQ
DO an
Transitioning Data
Don't Care

Note: 1. DO *an* = data-out from bank *a* and address *an*.

Mode Register 2 (MR2)

Figure 35: MR2 Definition for Non-Multiplexed Address Mode


BA3 BA2 BA1 BA0 A17 ... A4 A3 A2 A1 A0
Address Bus
21 20 19 18 17-5 4 3 2 1 0
0[1] 0[1] MRS Reserved WRITE En RTR
Mode Register (Mx)

M19	M18	Mode Register Definition
0	0	Mode Register 0 (MR0)
0	1	Mode Register 1 (MR1)
1	0	Mode Register 2 (MR2)
1	1	Reserved

M4	M3	WRITE Protocol
0	0	Single Bank
0	1	Dual Bank
1	0	Quad Bank
1	1	Reserved

M1	M0	READ Training Register
0	0	0-1-0-1 on all DQs
0	1	Even DQs: 0-1-0-1 ; Odd DQs: 1-0-1-0
1	0	Reserved
1	1	Reserved

M2	READ Training Register Enable
0	Normal RLDRAM Operation
1	READ Training Enabled

Note: 1. BA2, BA3, and all address balls corresponding to reserved bits must be held LOW during the MRS command.

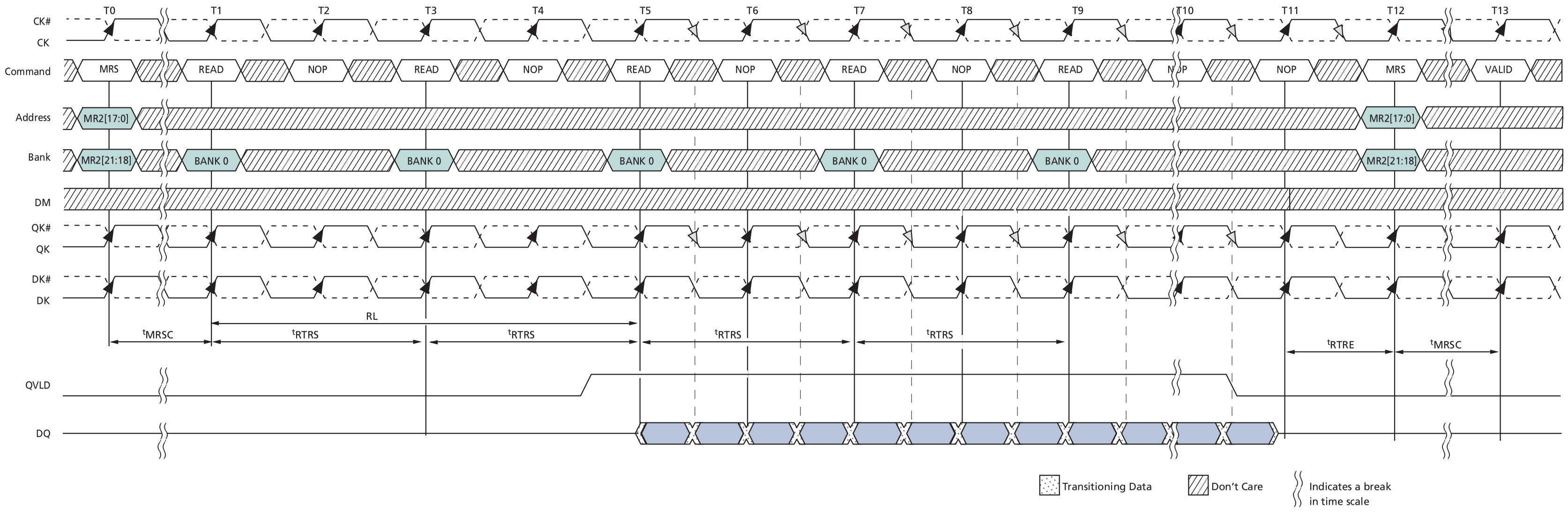
READ Training Register (RTR)

The READ training register (RTR) is controlled through MR2[2:0]. It is used to output a predefined bit sequence on the output balls to aid in system timing calibration. MR2[2] is the master bit that enables or disables access to the READ training register, and MR2[1:0] determine which predefined pattern for system calibration is selected. If MR2[2] is set to 0, the RTR is disabled, and the DRAM operates in normal mode. When MR2[2] is set to 1, the DRAM no longer outputs normal read data, but a predefined pattern that is defined by MR2[1:0].

Prior to enabling the RTR, all banks must be in the idle state (^{t}RC met). When the RTR is enabled, all subsequent READ commands will output four bits of a predefined sequence from the RTR on all DQs. The READ latency during RTR is defined with the Data Latency bits in MR0. To loop on the predefined pattern when the RTR is enabled, successive READ commands must be issued and satisfy ^{t}RTRS. Address balls A[19:0] are considered "Don't Care" during RTR READ commands. Bank address bits BA[3:0] must access Bank 0 with each RTR READ command. ^{t}RC does not need to be met in between RTR READ commands to Bank 0. When the RTR is enabled, only READ commands are allowed. When the last RTR READ burst has completed and ^{t}RTRE has been satisfied, an MRS command can be issued to exit the RTR. Standard RLDRAM 3 operation may then start after ^{t}MRSC has been met. The RESET function is supported when the RTR is enabled.

If MR2[1:0] is set to 00 a 0-1-0-1 pattern will be output on all DQs with each RTR READ command. If MR2[1:0] is set to 01, a 0-1-0-1 pattern will output on all even DQs and the opposite pattern, a 1-0-1-0, will output on all odd DQs with each RTR READ command. **Note:** Enabling RTR may corrupt previously written data.

Figure 36: READ Training Function - Back-to-Back Readout


T0
T1
T2
T3
T4
T5
T6
T7
T8
T9
T10
T11
T12
T13
CK#
CK
Command
MRS
READ
NOP
READ
NOP
READ
NOP
READ
NOP
READ
NOP
NOP
MRS
VALID
Address
MR2[17:0]
MR2[17:0]
Bank
MR2[21:18]
BANK 0
BANK 0
BANK 0
BANK 0
BANK 0
MR2[21:18]
DM
QK#
QK
DK#
DK
RL
^tMRSC
^tRTRS
^tRTRS
^tRTRS
^tRTRS
^tRTRE
^tMRSC
QVLD
DQ
Transitioning Data
Don't Care
Indicates a break in time scale

Note: 1. RL = READ latency defined with data latency MR0 setting.

WRITE Protocol

Single or multibank WRITE operation is programmed with bits MR2[4:3]. The purpose of multibank WRITE operation is to reduce the effective ^{t}RC during READ commands. When dual- or quad-bank WRITE protocol is selected, identical data is written to two or four banks, respectively. With the same data stored in multiple banks on the RLDRAM, the memory controller can select the appropriate bank to READ the data from and minimize ^{t}RC delay. Detailed information on the multibank WRITE protocol can be found in Multibank WRITE (page 76).

WRITE Command

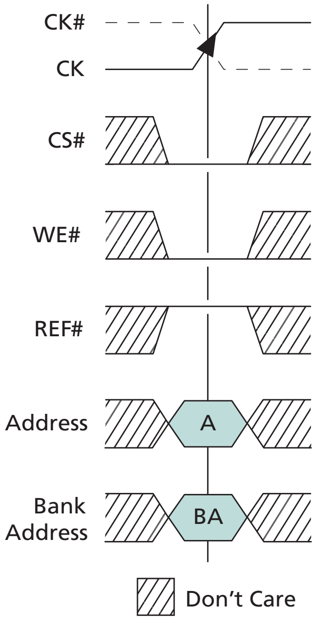
Write accesses are initiated with a WRITE command. The address needs to be provided concurrent with the WRITE command.

During WRITE commands, data will be registered at both edges of DK, according to the programmed burst length (BL). The RLDRAM operates with a WRITE latency (WL) determined by the data latency bits within MR0. The first valid data is registered at the first rising DK edge WL cycles after the WRITE command.

Any WRITE burst may be followed by a subsequent READ command (assuming ^{t}RC is met). Depending on the amount of input timing skew, an additional NOP command might be necessary between WRITE and READ commands to avoid external data bus contention (see Figure 44 (page 84)).

Setup and hold times for incoming DQ relative to the DK edges are specified as ^{t}DS and ^{t}DH. The input data is masked if the corresponding DM signal is HIGH.

Figure 37: WRITE Command



Multibank WRITE

All the information provided above in the WRITE section is applicable to a multibank WRITE operation as well. Either two or four banks can be simultaneously written to when the appropriate MR2[4:3] mode register bits are selected.

If a dual-bank WRITE has been selected through the mode register, both banks *x* and *x* +8 will be written to simultaneously with identical data provided during the WRITE command. For example, when a dual-bank WRITE has been loaded and the bank address for Bank 1 has been provided during the WRITE command, Bank 9 will also be written to at the same time. When a dual-bank WRITE command is issued, only bank address bits BA[2:0] are valid and BA3 is considered a “Don’t Care.”

The same methodology is used if the quad-bank WRITE has been selected through the mode register. Under these conditions, when a WRITE command is issued to Bank *x*, the data provided on the DQs will be issued to banks *x*, *x*+4, *x*+8, and *x*+12. When a quad-bank WRITE command is issued, only bank address bits BA[1:0] are valid and BA[3:2] are considered “Don’t Care.”

The timing parameter ^{t}SAW must be adhered to when operating with multibank WRITE commands. This parameter limits the number of active banks at 16 within an 8ns window. The ^{t}MMD specification must also be followed if the quad-bank WRITE is being used. This specification requires two clock cycles between any bank command (READ, WRITE, or AREF) to a quad-bank WRITE or a quad-bank WRITE to any bank command. The data bus efficiency is not compromised if BL4 or BL8 is being utilized.

READ Command

Read accesses are initiated with a READ command (see the figure below). Addresses are provided with the READ command.

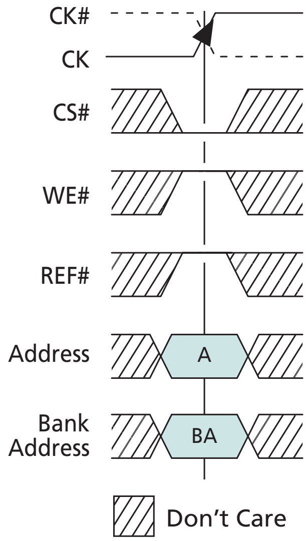
During READ bursts, the memory device drives the read data so it is edge-aligned with the QK signals. After a programmable READ latency, data is available at the outputs. One half clock cycle prior to valid data on the read bus, the data valid signal(s), QVLD, transitions from LOW to HIGH. QVLD is also edge-aligned with the QK signals.

The skew between QK and the crossing point of CK is specified as ^{t}CKQK. ^{t}QKQ*x* is the skew between a QK pair and the last valid data edge generated at the DQ signals in the associated byte group, such as DQ[7:0] and QK0. ^{t}QKQ*x* is derived at each QK clock edge and is not cumulative over time. For the x36 device, the ^{t}QKQ02 and ^{t}QKQ13 specifications define the relationship between the DQs and QK signals within specific data word groupings. ^{t}QKQ02 defines the skew between QK0 and DQ[26:18] and between QK2 and DQ[8:0]. ^{t}QKQ13 defines the skew between QK1 and DQ[35:17] and between QK3 and DQ[17:9].

After completion of a burst, assuming no other commands have been initiated, output data (DQ) will go High-Z. The QVLD signal transitions LOW on the last bit of the READ burst. The QK clocks are free-running and will continue to cycle after the read burst is complete. Back-to-back READ commands are possible, producing a continuous flow of output data.

Any READ burst may be followed by a subsequent WRITE command. Some systems having long line lengths or severe skews may need an additional idle cycle inserted between READ and WRITE commands to prevent data bus contention.

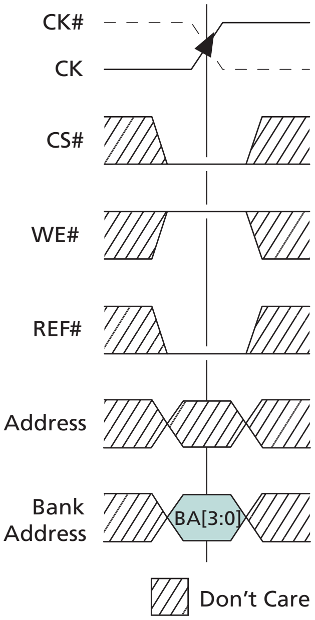
Figure 38: READ Command


CK#
CK
CS#
WE#
REF#
Address
A
Bank Address
BA
Don’t Care

AUTO REFRESH Command

The RLDRAM 3 device uses two unique AUTO REFRESH (AREF) command protocols, bank address-controlled AREF and multibank AREF. The desired protocol is selected by setting MR1[8] LOW (for bank address-controlled AREF) or HIGH (for multibank AREF) during an MRS command. Bank address-controlled AREF is identical to the method used in RLDRAM2 devices, whereby banks are refreshed independently. The value on bank addresses BA[3:0], issued concurrently with the AREF command, define which bank is to be refreshed. The array address is generated by an internal refresh counter, effectively making each address bit a "Don't Care" during the AREF command. The delay between the AREF command and a subsequent command to the same bank must be at least ^{t}RC.

Figure 39: Bank Address-Controlled AUTO REFRESH Command

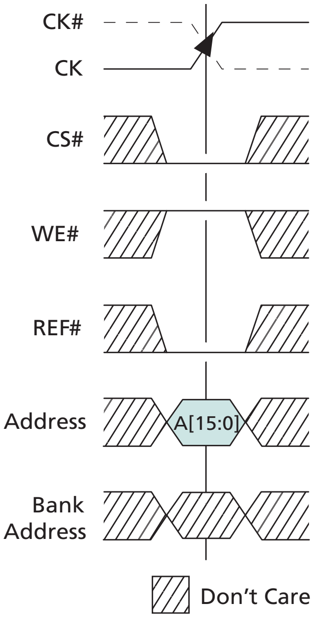


The multibank AREF protocol, enabled by setting bit MR1[8] HIGH during an MRS command, enables the simultaneous refresh of a row in up to four banks. In this method, address balls A[15:0] represent banks [15:0], respectively. The row addresses are generated by an internal refresh counter for each bank; therefore, the purpose of the address balls during an AREF command is only to identify the banks to be refreshed. The bank address balls BA[3:0] are considered "Don't Care" during a multibank AREF command.

A multibank AUTO REFRESH is performed for a given bank when its corresponding address ball is asserted HIGH during an AREF command. Any combination of up to four address balls can be asserted HIGH during the rising clock edge of an AREF command to simultaneously refresh a row in each corresponding bank. The delay between an AREF command and subsequent commands to the banks refreshed must be at least ^{t}RC. Adherence to ^{t}SAW must be followed when simultaneously refreshing multiple banks. If refreshing three or four banks with the multibank AREF command, ^{t}MMD must be followed. This specification requires two clock cycles between any bank command (READ, WRITE, AREF) to the multibank AREF or the multibank AREF to any bank command. Note that refreshing one or two banks with the multibank AREF command is not subject to the ^{t}MMD specification.

The entire device must be refreshed every 64ms (^{t}REF). The RLDRAM device requires 128K cycles at an average periodic interval of 0.489µs MAX (64ms/[8K rows x 16 banks]).

Figure 40: Multibank AUTO REFRESH Command


CK#
CK
CS#
WE#
REF#
Address
A[15:0]
Bank Address
Don't Care

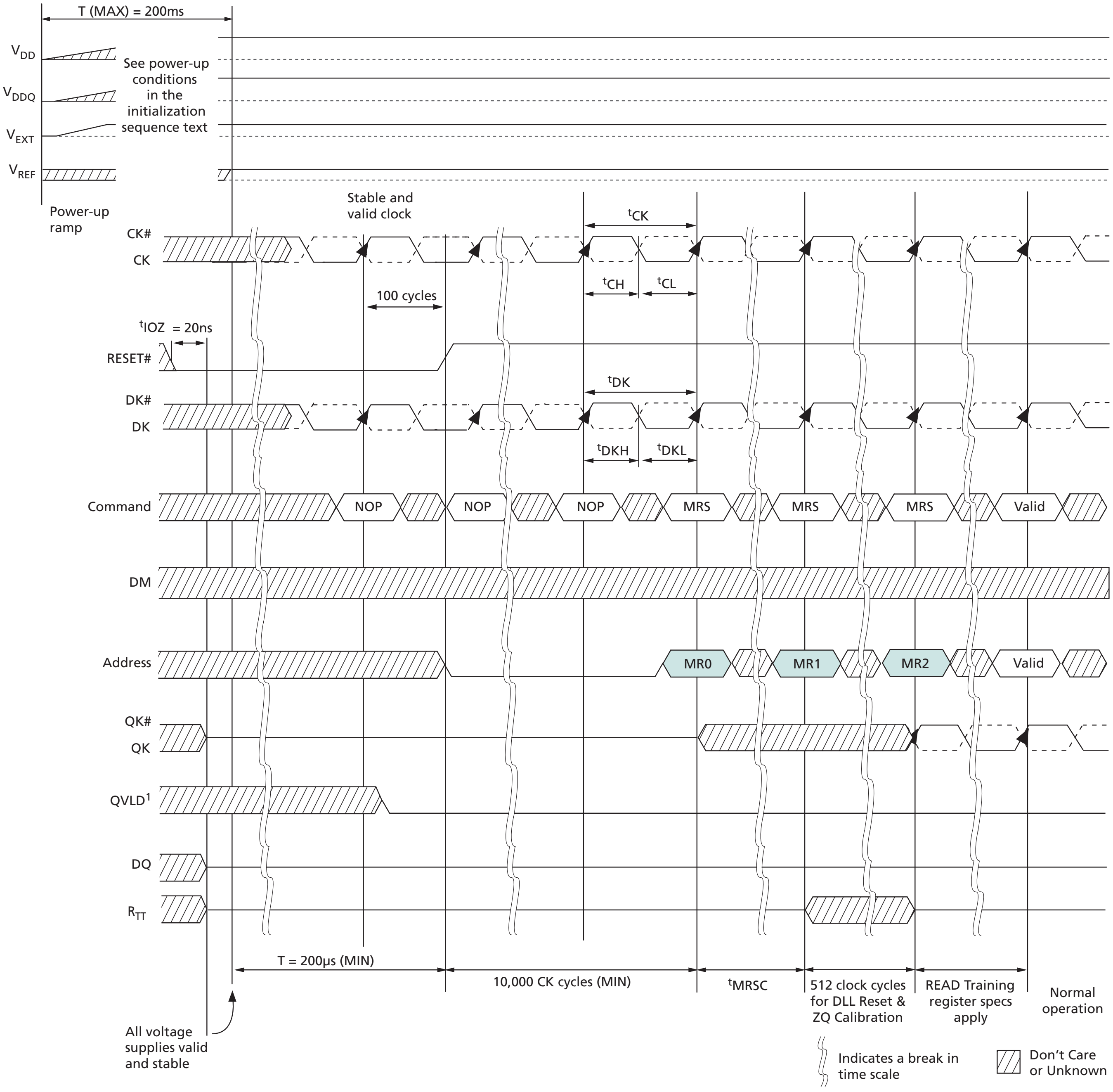
INITIALIZATION Operation

The RLDRAM 3 device must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operations or permanent damage to the device.

The following sequence is used for power-up:

1. Apply power (V_{EXT}, V_{DD}, V_{DDQ}). Apply V_{DD} and V_{EXT} before, or at the same time as, V_{DDQ}. V_{DD} must not exceed V_{EXT} during power supply ramp. V_{EXT}, V_{DD}, V_{DDQ} must all ramp to their respective minimum DC levels within 200ms.
2. Ensure that RESET# is below $0.2 \times V_{DDQ}$ during power ramp to ensure the outputs remain disabled (High-Z) and ODT is off (R_{TT} is also High-Z). DQs, and QK signals will remain High-Z until MR0 command. All other inputs may be undefined during the power ramp.
3. After the power is stable, RESET# must be LOW for at least 200µs to begin the initialization process.
4. After 100 or more stable input clock cycles with NOP commands, bring RESET# HIGH.
5. After RESET# goes HIGH, a stable clock must be applied in conjunction with NOP commands and all Address pins (A[19:0] & BA[3:0]) to be held low for 10,000 cycles.
6. Load desired settings into MR0.
7. ^{t}MRSC after loading the MR0 settings, load operating parameters in MR1, including DLL Reset and Long ZQ Calibration.
8. After the DLL is reset and Long ZQ Calibration is enabled, the input clock must be stable for 512 clock cycles while NOPs are issued.
9. Load desired settings into MR2. If using the RTR, follow the procedure outlined in the READ Training Function – Back-to-Back Readout figure prior to entering normal operation.
10. The RLDRAM 3 is ready for normal operation.

Figure 41: Power-Up/Initialization Sequence

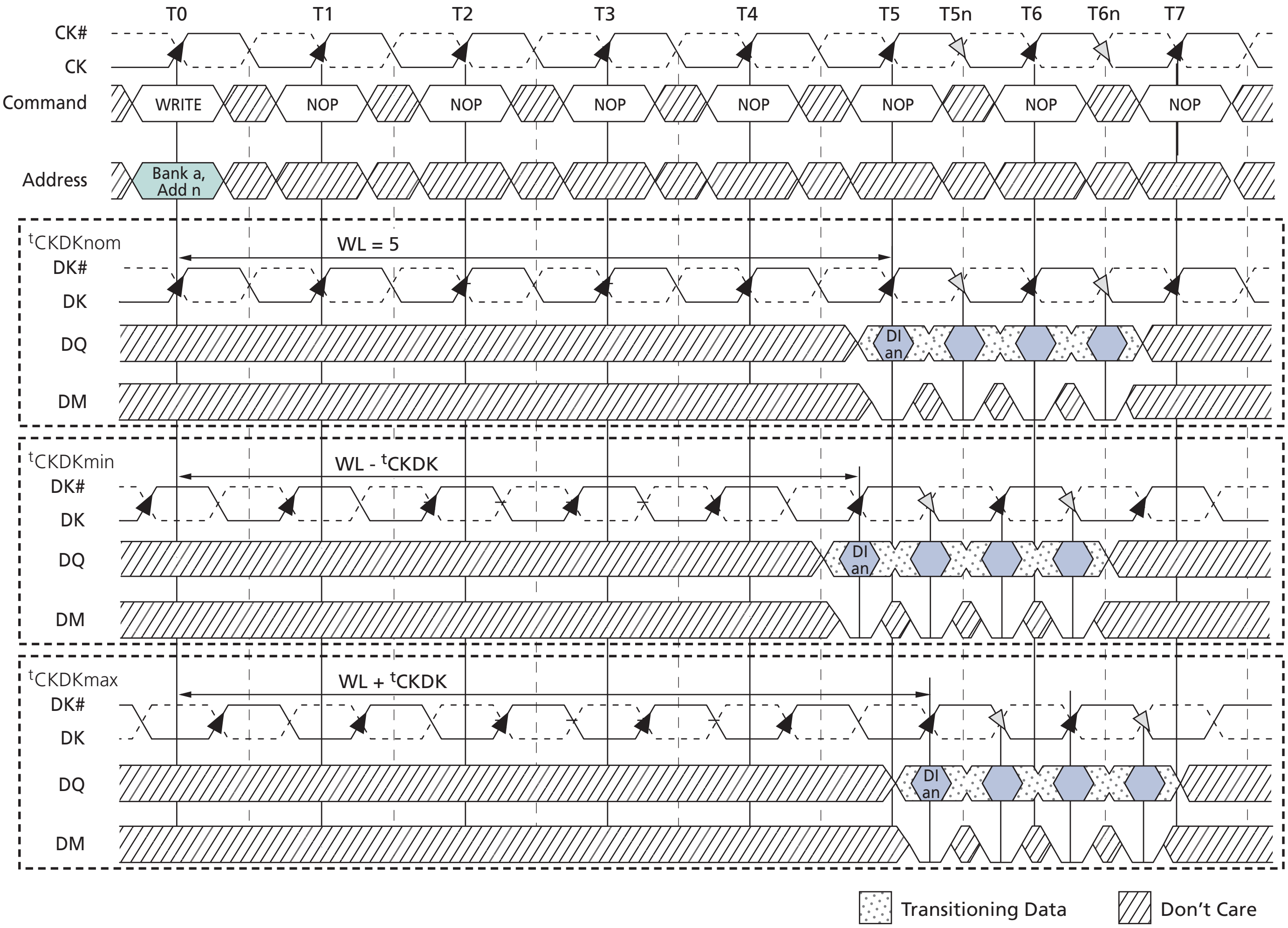

T (MAX) = 200ms
V_{DD}
V_{DDQ}
V_{EXT}
V_{REF}
See power-up conditions in the initialization sequence text
Power-up ramp
Stable and valid clock
^tCK
CK#
CK
^tCH
^tCL
100 cycles
^tIOZ = 20ns
RESET#
^tDK
DK#
DK
^tDKH
^tDKL
Command
NOP
NOP
NOP
MRS
MRS
MRS
Valid
DM
Address
MR0
MR1
MR2
Valid
QK#
QK
QVLD[1]
DQ
R_{TT}
T = 200µs (MIN)
10,000 CK cycles (MIN)
^tMRSC
512 clock cycles for DLL Reset & ZQ Calibration
READ Training register specs apply
Normal operation
All voltage supplies valid and stable
Indicates a break in time scale
Don't Care or Unknown

Notes: 1. QVLD output drive status during power-up and initialization:
   a. QVLD remains High-Z until 20ns after power supplies are stable and TCK or CK have cycled 4 times.
   b. QVLD will then drive LOW with 40Ω or lower until the output drive value selected in MR1 is enabled.

  c. ^{t}MRSC after loading the MR1 settings, QVLD output drive strength will be at the value selected or lower until ZQ calibration is complete.
  d. QVLD will meet the output drive strength specifications upon completion of the ZQ calibration timing.
2. After MR2 has been issued, Rtt is either High-Z or enabled to the ODT value selected in MR1.

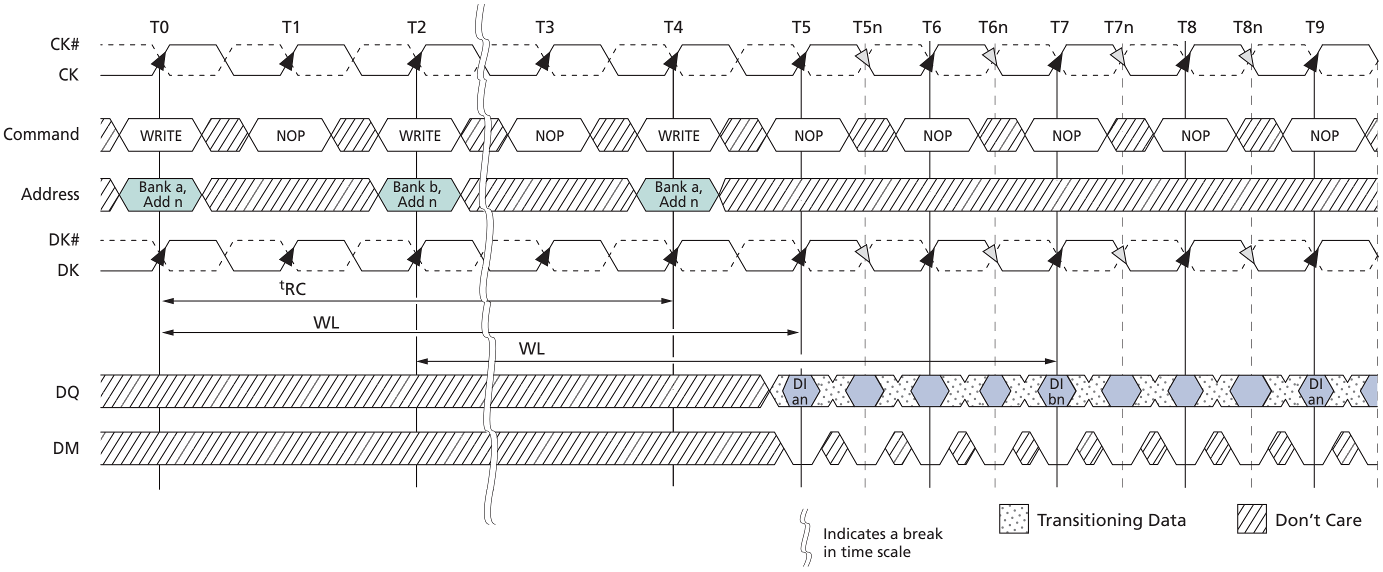
WRITE Operation

Figure 42: WRITE Burst


T0
T1
T2
T3
T4
T5
T5n
T6
T6n
T7
CK#
CK
Command
WRITE
NOP
NOP
NOP
NOP
NOP
NOP
NOP
Address
Bank a, Add n
tCKDKnom
WL = 5
DK#
DK
DQ
DI an
DM
tCKDKmin
WL - tCKDK
DK#
DK
DQ
DI an
DM
tCKDKmax
WL + tCKDK
DK#
DK
DQ
DI an
DM
Transitioning Data
Don't Care

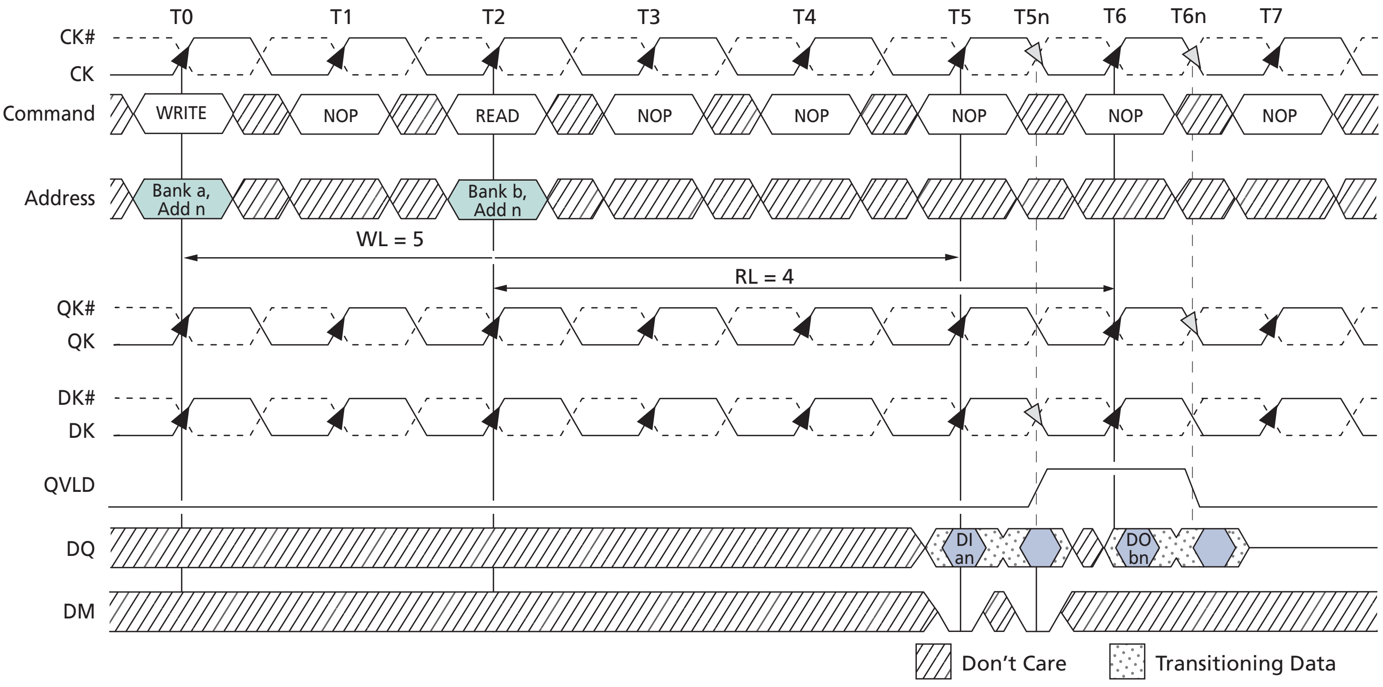
Note: 1. DI *an* = data-in for bank *a* and address *n*.

Figure 43: Consecutive WRITE Bursts


T0
T1
T2
T3
T4
T5
T5n
T6
T6n
T7
T7n
T8
T8n
T9
CK#
CK
Command
WRITE
NOP
WRITE
NOP
WRITE
NOP
NOP
NOP
NOP
NOP
Address
Bank a, Add n
Bank b, Add n
Bank a, Add n
DK#
DK
tRC
WL
WL
DQ
DI an
DI bn
DI an
DM
Indicates a break in time scale
Transitioning Data
Don't Care

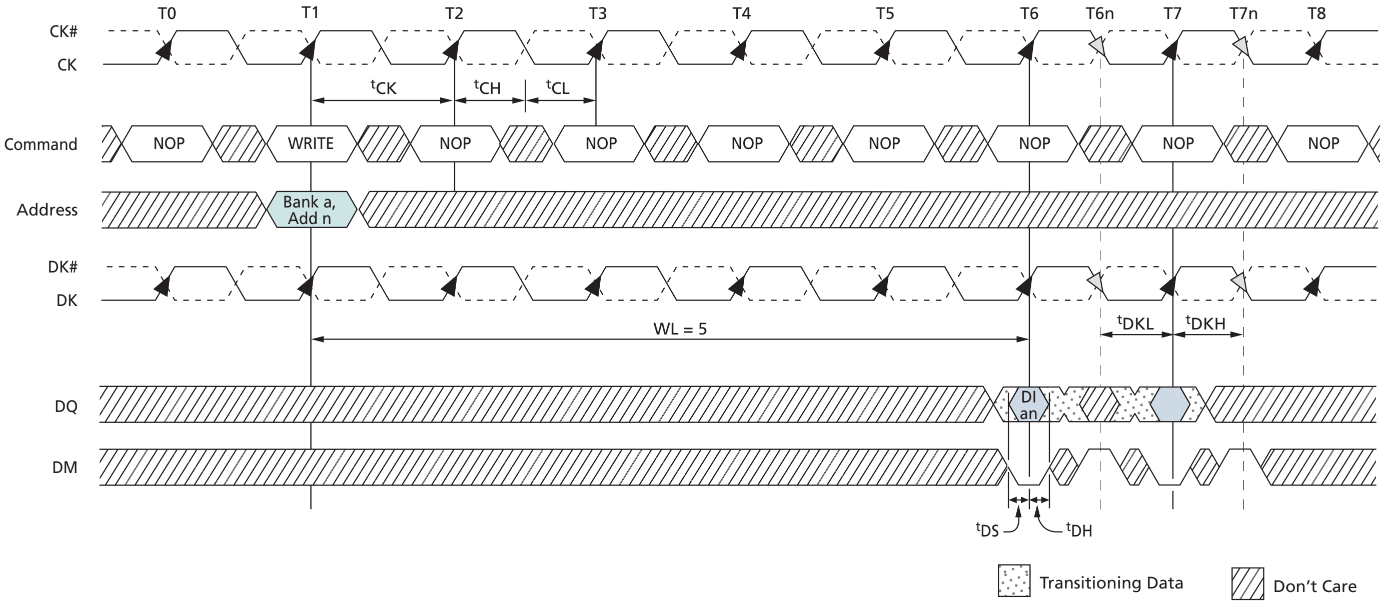
Note: 1. DI *an* (or *bn or cn)* = data-in for bank *a (or b or c)* and address *n*.

Figure 44: WRITE-to-READ


T0
T1
T2
T3
T4
T5
T5n
T6
T6n
T7
CK#
CK
Command
WRITE
NOP
READ
NOP
NOP
NOP
NOP
NOP
Address
Bank a, Add n
Bank b, Add n
WL = 5
RL = 4
QK#
QK
DK#
DK
QVLD
DQ
DI an
DO bn
DM
Don't Care
Transitioning Data

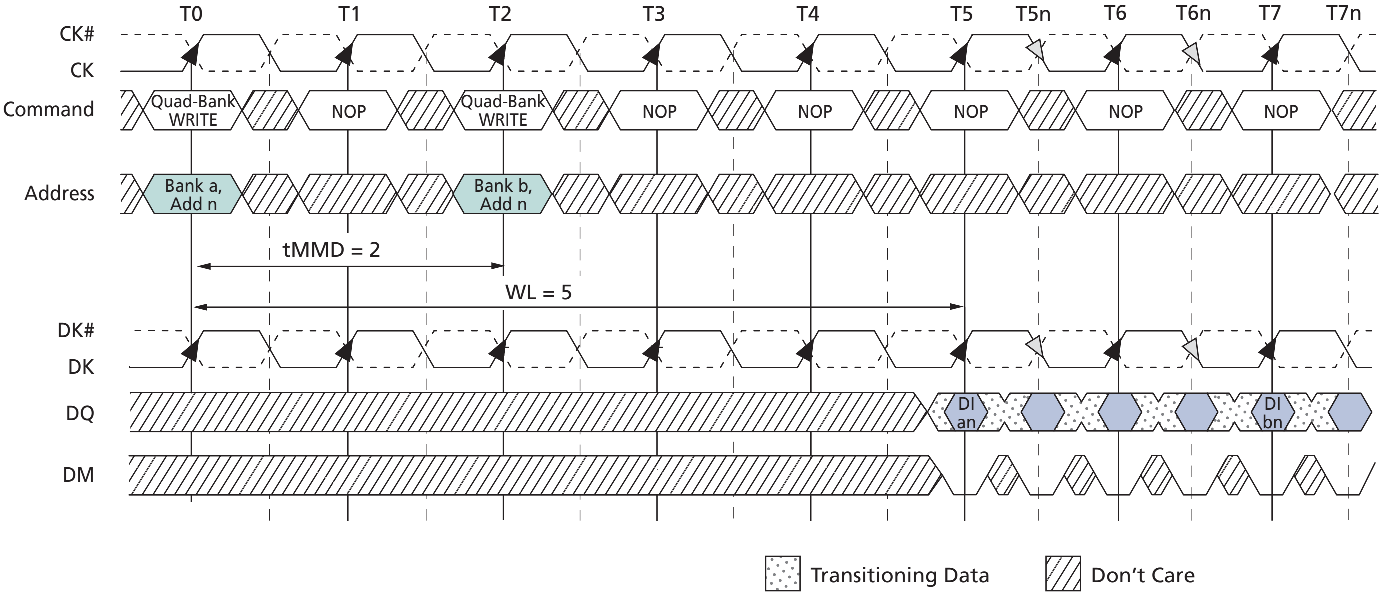
Notes:
1. DI *an* = data-in for bank *a* and address *n*.
2. DO *bn* = data-out from bank *b* and address *n*.

Figure 45: WRITE - DM Operation


T0
T1
T2
T3
T4
T5
T6
T6n
T7
T7n
T8
CK#
CK
tCK
tCH
tCL
Command
NOP
WRITE
NOP
NOP
NOP
NOP
NOP
NOP
NOP
Address
Bank a, Add n
DK#
DK
WL = 5
tDKL
tDKH
DQ
DI an
DM
tDS
tDH
Transitioning Data
Don't Care

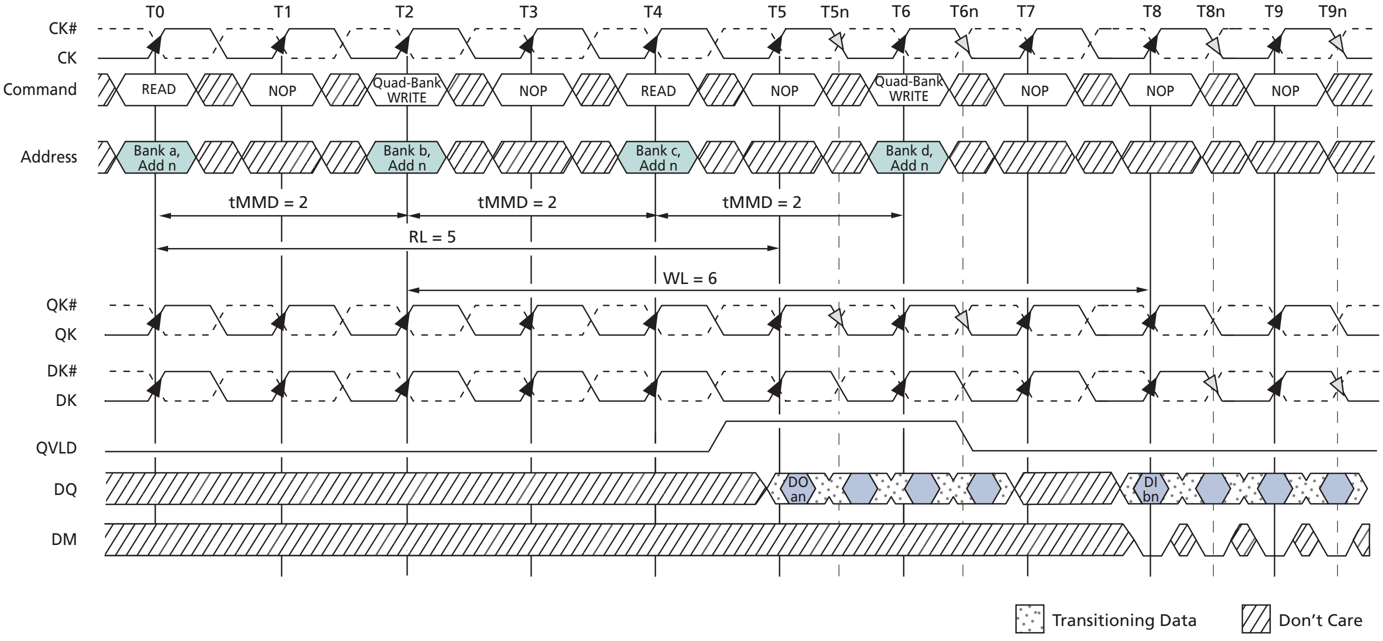
Note: 1. DI *an* = data-in for bank *a* and address *n*.

Figure 46: Consecutive Quad Bank WRITE Bursts


T0
T1
T2
T3
T4
T5
T5n
T6
T6n
T7
T7n
CK#
CK
Command
Quad-Bank WRITE
NOP
Quad-Bank WRITE
NOP
NOP
NOP
NOP
NOP
Address
Bank a, Add n
Bank b, Add n
tMMD = 2
WL = 5
DK#
DK
DQ
DI an
DI bn
DM
Transitioning Data
Don't Care

Notes:
1. DI *an* = data-in for bank *a, a+4, a+8, and a+12* and address *n*.
2. DI *bn* = data-in for bank *b, b+4, b+8, and b+12* and address *n*.

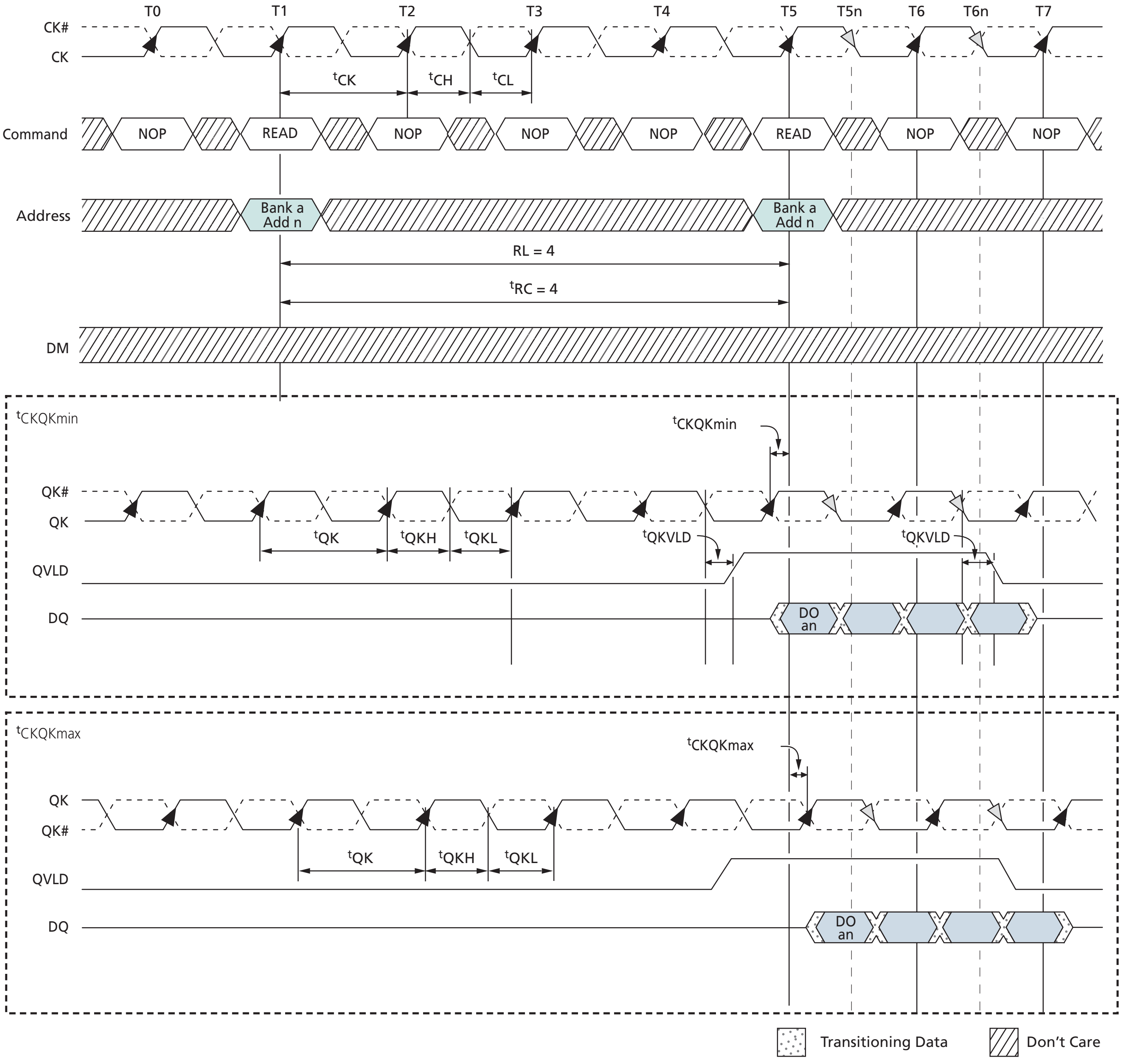
Figure 47: Interleaved READ and Quad Bank WRITE Bursts


T0
T1
T2
T3
T4
T5
T5n
T6
T6n
T7
T8
T8n
T9
T9n
CK#
CK
Command
READ
NOP
Quad-Bank WRITE
NOP
READ
NOP
Quad-Bank WRITE
NOP
NOP
NOP
Address
Bank a, Add n
Bank b, Add n
Bank c, Add n
Bank d, Add n
tMMD = 2
tMMD = 2
tMMD = 2
RL = 5
WL = 6
QK#
QK
DK#
DK
QVLD
DQ
DO an
DI bn
DM
Transitioning Data
Don't Care

Notes:
1. DO *an* = data-out for bank *a* and address *n*.
2. DI *bn* = data-in for bank *b, b+4, b+8, and b+12* and address *n*.

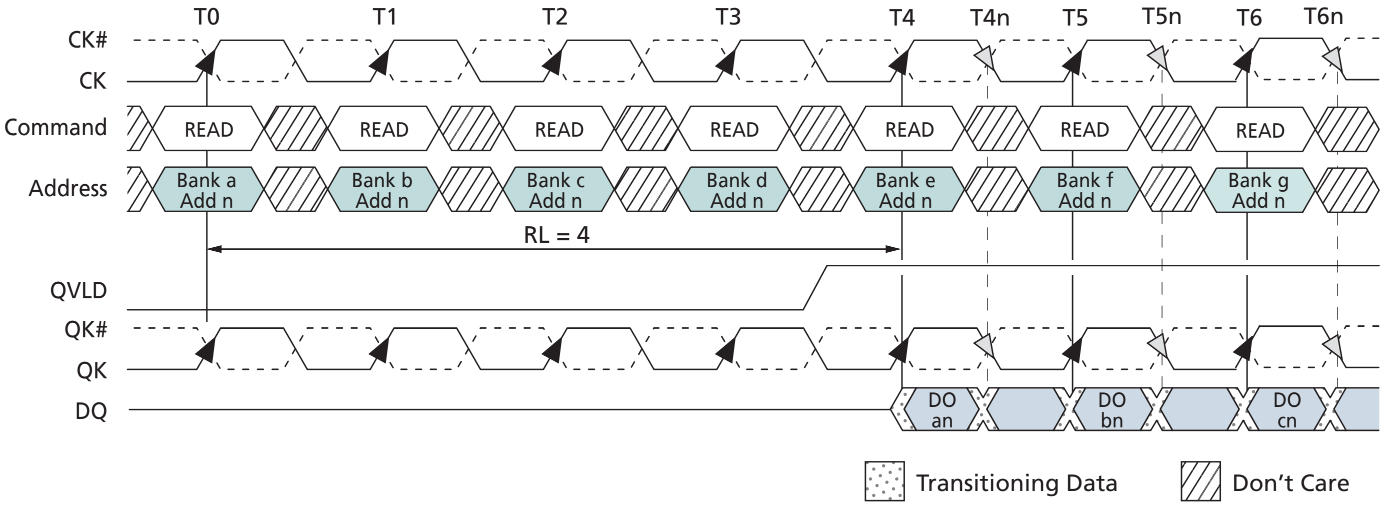
READ Operation

Figure 48: Basic READ Burst


T0
T1
T2
T3
T4
T5
T5n
T6
T6n
T7
CK#
CK
tCK
tCH
tCL
Command
NOP
READ
NOP
NOP
NOP
READ
NOP
NOP
Address
Bank a
Add n
Bank a
Add n
RL = 4
tRC = 4
DM
tCKQKmin
tCKQKmin
QK#
QK
tQK
tQKH
tQKL
tQKVLD
tQKVLD
QVLD
DQ
DO
an
tCKQKmax
tCKQKmax
QK
QK#
tQK
tQKH
tQKL
QVLD
DQ
DO
an
Transitioning Data
Don't Care

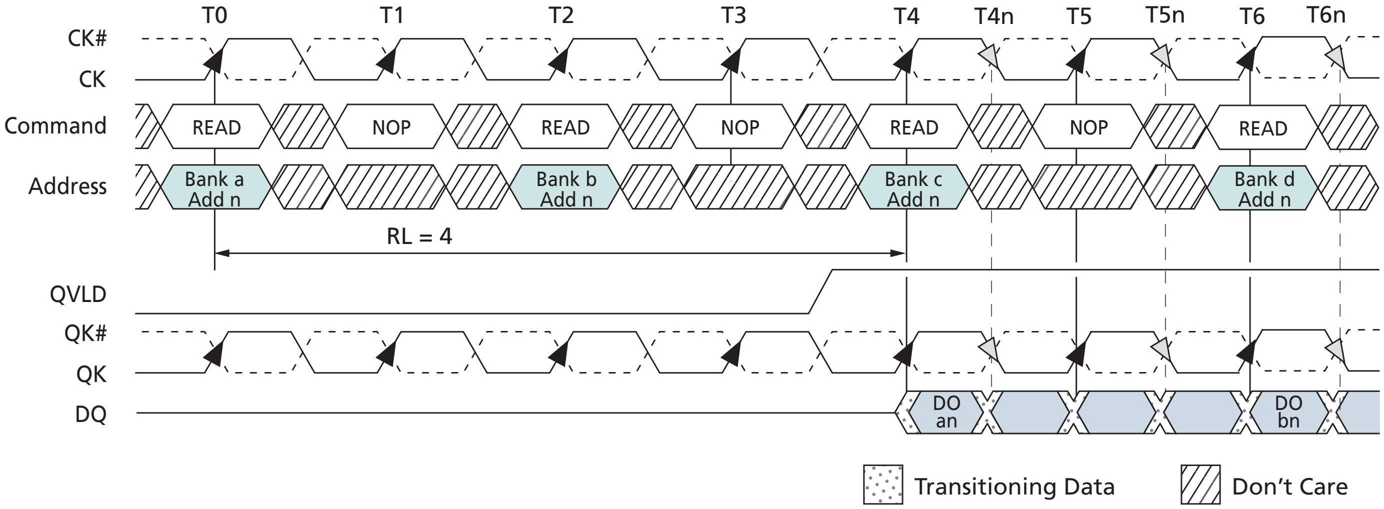
Note: 1. DO *an* = data-out from bank *a* and address *an*.

Figure 49: Consecutive READ Bursts (BL = 2)


T0
T1
T2
T3
T4
T4n
T5
T5n
T6
T6n
CK#
CK
Command
READ
READ
READ
READ
READ
READ
READ
Address
Bank a Add n
Bank b Add n
Bank c Add n
Bank d Add n
Bank e Add n
Bank f Add n
Bank g Add n
RL = 4
QVLD
QK#
QK
DQ
DO an
DO bn
DO cn
Transitioning Data
Don’t Care

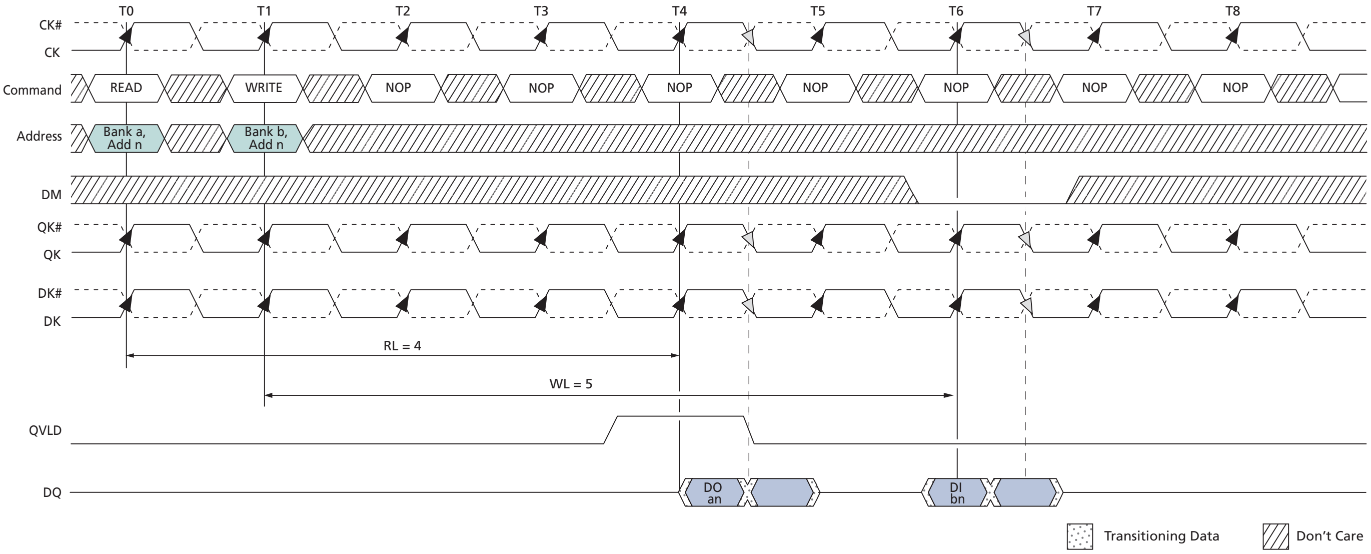
Note: 1. DO *an* (or *bn, cn*) = data-out from bank *a* (or bank *b, c*) and address *n*.

Figure 50: Consecutive READ Bursts (BL = 4)


T0
T1
T2
T3
T4
T4n
T5
T5n
T6
T6n
CK#
CK
Command
READ
NOP
READ
NOP
READ
NOP
READ
Address
Bank a Add n
Bank b Add n
Bank c Add n
Bank d Add n
RL = 4
QVLD
QK#
QK
DQ
DO an
DO bn
Transitioning Data
Don’t Care

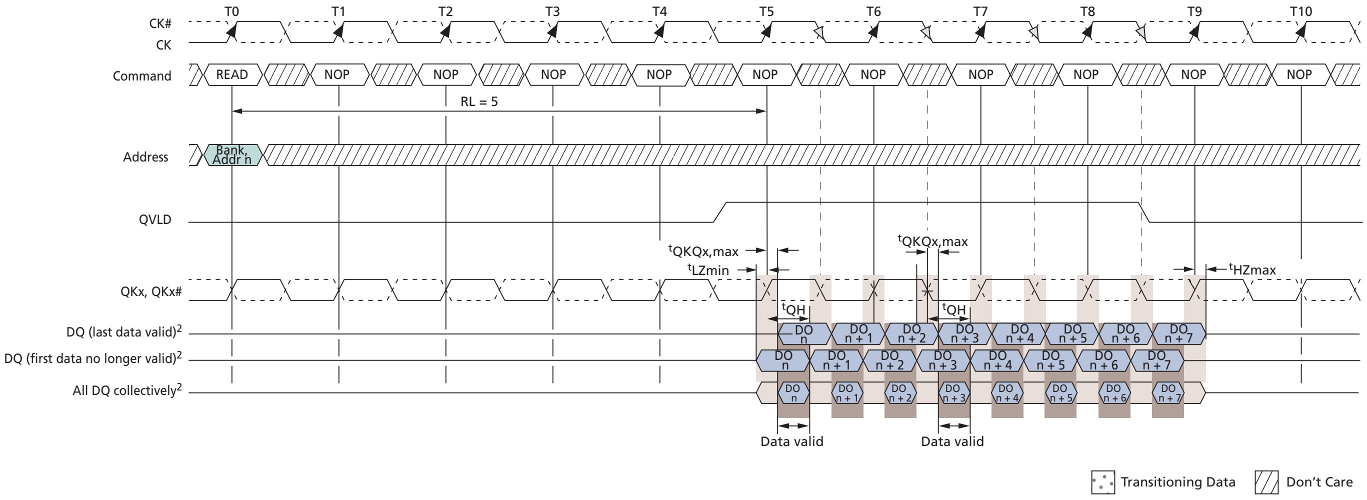
Note: 1. DO *an* (or *bn*) = data-out from bank *a* (or bank *b*) and address *n*.

Figure 51: READ-to-WRITE (BL = 2)


T0
T1
T2
T3
T4
T5
T6
T7
T8
CK#
CK
Command
READ
WRITE
NOP
Address
Bank a, Add n
Bank b, Add n
DM
QK#
QK
DK#
DK
RL = 4
WL = 5
QVLD
DQ
DO an
DI bn
Transitioning Data
Don't Care

Notes:
1. DO *an* = data-out from bank *a* and address *n*.
2. DI *bn* = data-in for bank *b* and address *n*.

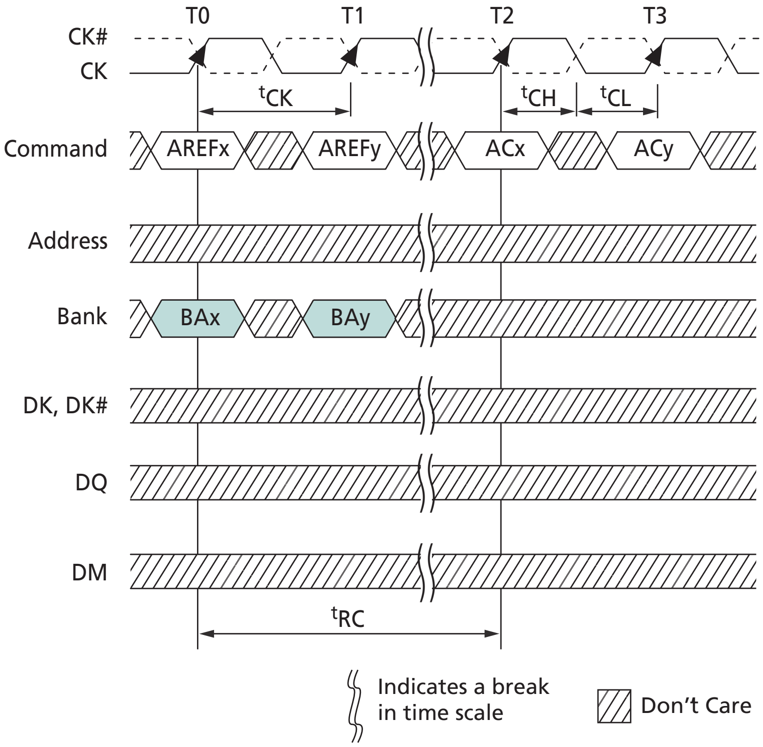
Figure 52: Read Data Valid Window


T0
T1
T2
T3
T4
T5
T6
T7
T8
T9
T10
CK#
CK
Command
READ
NOP
RL = 5
Address
Bank, Addr n
QVLD
tQKQx,max
tLZmin
tQKQx,max
tHZmax
QKx, QKx#
tQH
tQH
DQ (last data valid)2
DQ (first data no longer valid)2
All DQ collectively2
DO n
DO n + 1
DO n + 2
DO n + 3
DO n + 4
DO n + 5
DO n + 6
DO n + 7
Data valid
Data valid
Transitioning Data
Don't Care

Notes:
1. DO *n* = data-out from bank *a* and address *n*.
2. Represents DQs associated with a specific QK, QK# pair.
3. Output timings are referenced to $V_{DDQ}/2$ and DLL on and locked.
4. ^{t}QKQ*x* defines the skew between the QK0, QK0# pair to its respective DQs. ^{t}QKQ*x* does not define the skew between QK and CK.
5. Early data transitions may not always happen at the same DQ. Data transitions of a DQ can vary (either early or late) within a burst.

AUTO REFRESH Operation

Figure 53: Bank Address-Controlled AUTO REFRESH Cycle


T0
T1
T2
T3
CK#
CK
tCK
tCH
tCL
Command
AREFx
AREFy
ACx
ACy
Address
Bank
BAx
BAy
DK, DK#
DQ
DM
tRC
Indicates a break in time scale
Don't Care

Notes:
1. AREF*x* (or AREF*y*)= AUTO REFRESH command to bank *x (or bank y)*.
2. AC*x* = any command to bank *x*; AC*y* = any command to bank *y*.
3. BA*x* = bank address to bank *x*; BA*y* = bank address to bank *y*.

Figure 54: Multibank AUTO REFRESH Cycle

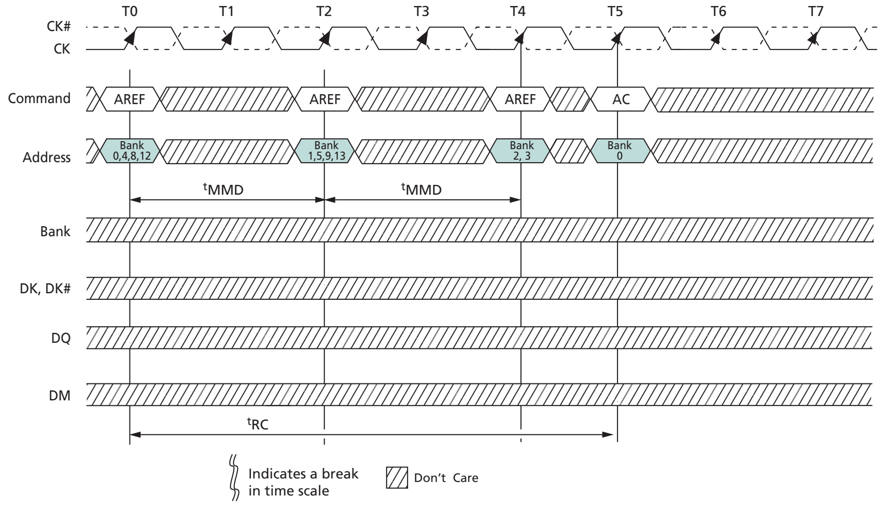
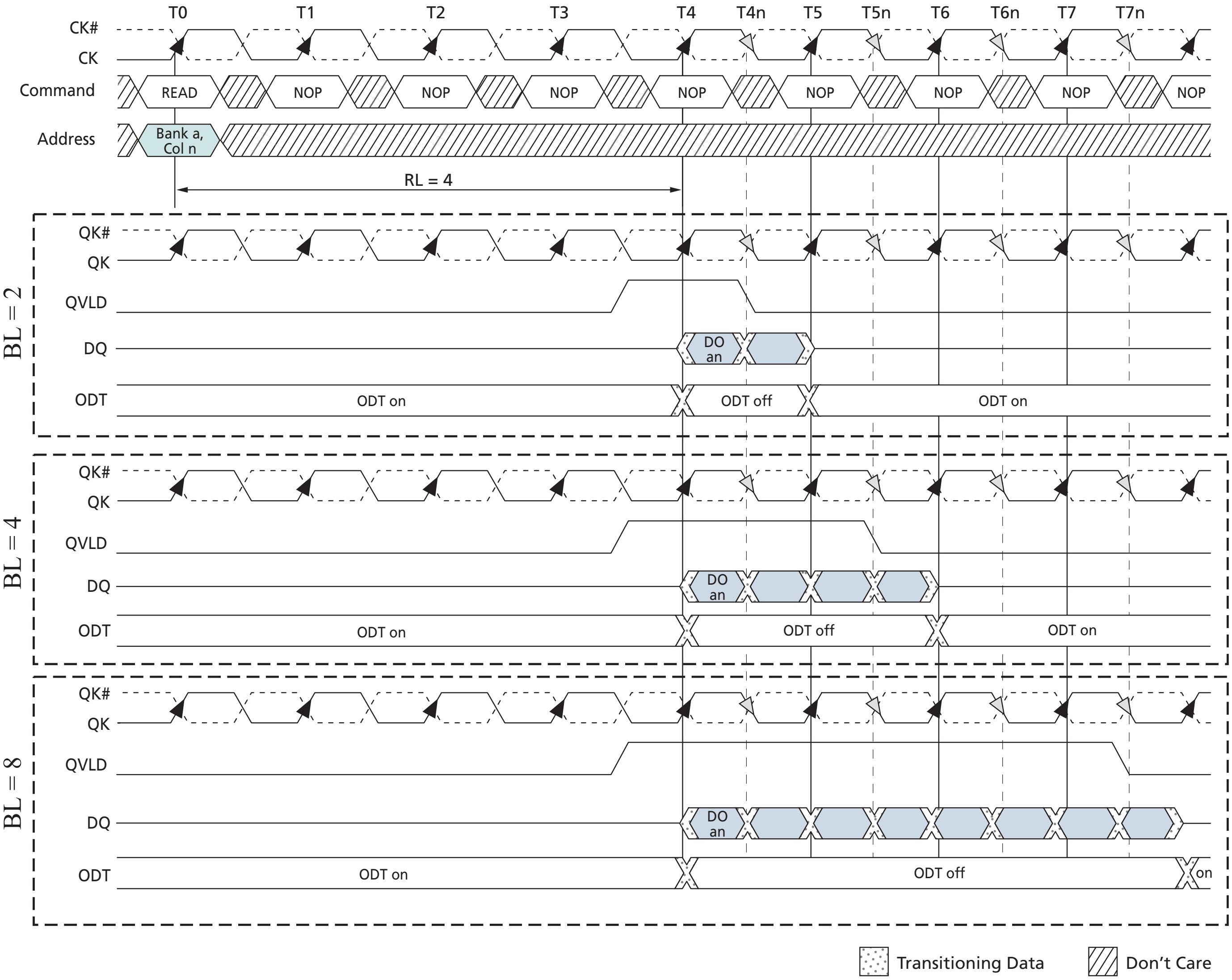
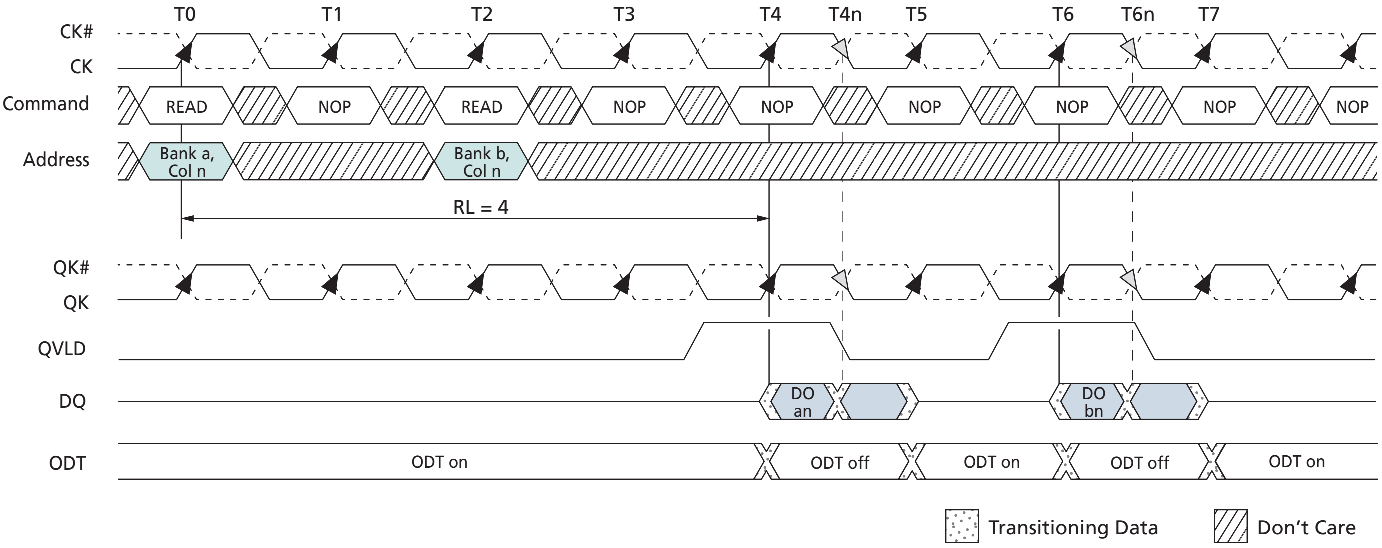

T0
T1
T2
T3
T4
T5
T6
T7
CK#
CK
Command
AREF
AREF
AREF
AC
Address
Bank 0,4,8,12
Bank 1,5,9,13
Bank 2, 3
Bank 0
tMMD
tMMD
Bank
DK, DK#
DQ
DM
tRC
Indicates a break in time scale
Don't Care

Figure 55: READ Burst with ODT


T0
T1
T2
T3
T4
T4n
T5
T5n
T6
T6n
T7
T7n
CK#
CK
Command
READ
NOP
Address
Bank a, Col n
RL = 4
BL = 2
BL = 4
BL = 8
QK#
QK
QVLD
DQ
DO an
ODT
ODT on
ODT off
on
Transitioning Data
Don't Care

Note: 1. DO *an* = data out from bank *a* and address *n*.

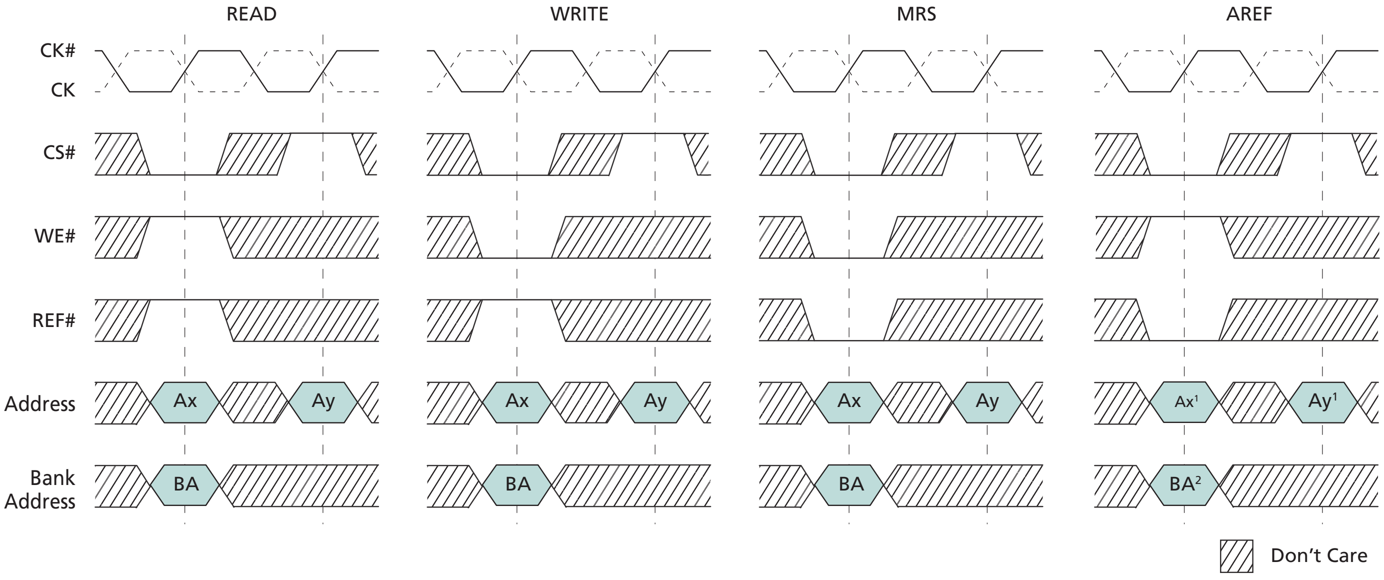
Figure 56: READ-NOP-READ with ODT


T0
T1
T2
T3
T4
T4n
T5
T6
T6n
T7
CK#
CK
Command
READ
NOP
READ
NOP
NOP
NOP
NOP
NOP
NOP
Address
Bank a, Col n
Bank b, Col n
RL = 4
QK#
QK
QVLD
DQ
DO an
DO bn
ODT
ODT on
ODT off
ODT on
ODT off
ODT on
Transitioning Data
Don't Care

Note: 1. DO *an* (or *bn*) = data-out from bank *a* (or bank *b*) and address *n*.

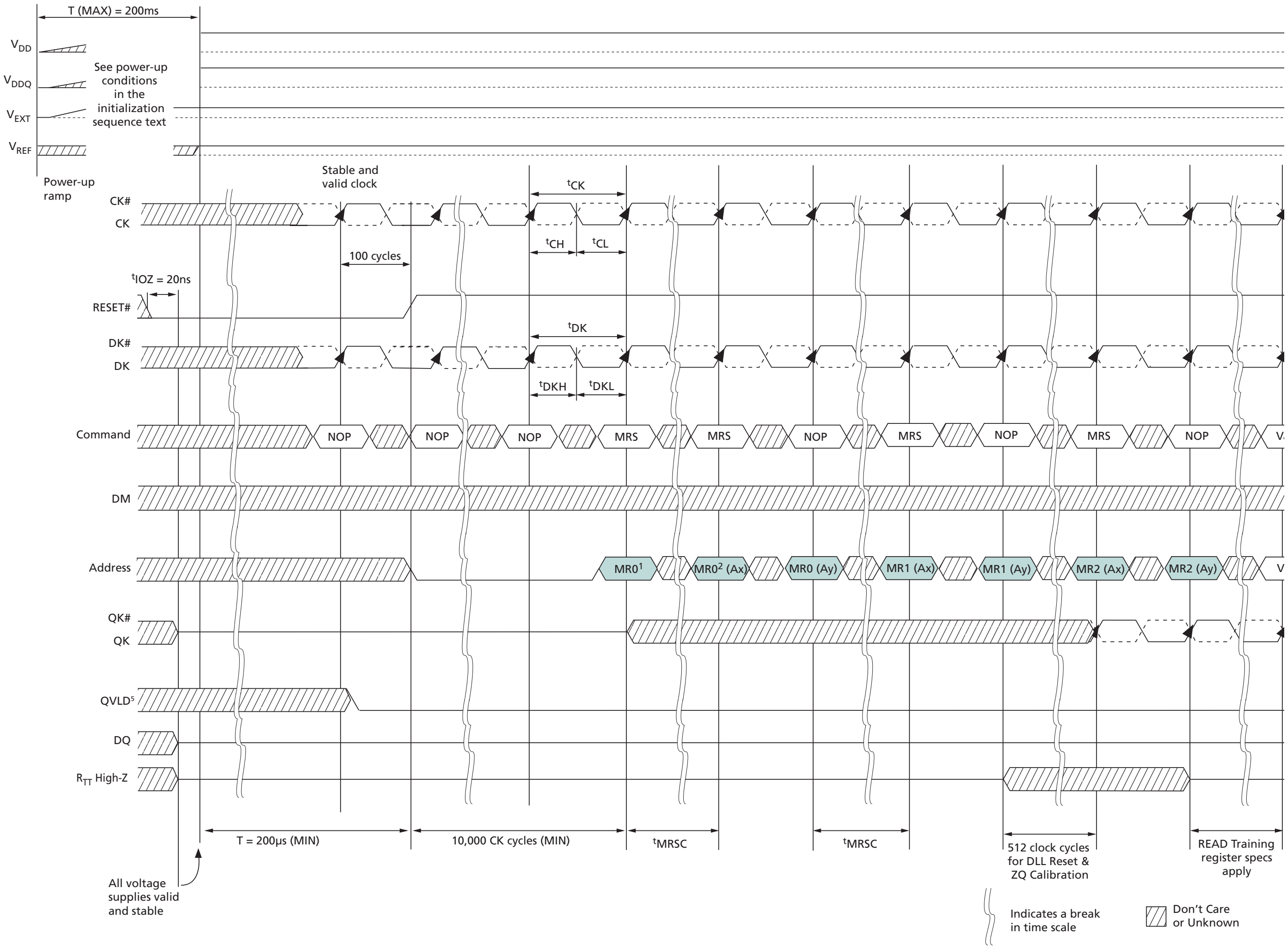
Multiplexed Address Mode

Figure 57: Command Description in Multiplexed Address Mode


READ
WRITE
MRS
AREF
CK#
CK
CS#
WE#
REF#
Address
Bank Address
Ax
Ay
BA
Ax¹
Ay¹
BA²
Don't Care

Notes:
1. Addresses valid only during a multibank AUTO REFRESH command.
2. Bank addresses valid only during a bank address-controlled AUTO REFRESH command.
3. The minimum setup and hold times of the two address parts are defined as ^{t}IS and ^{t}IH.

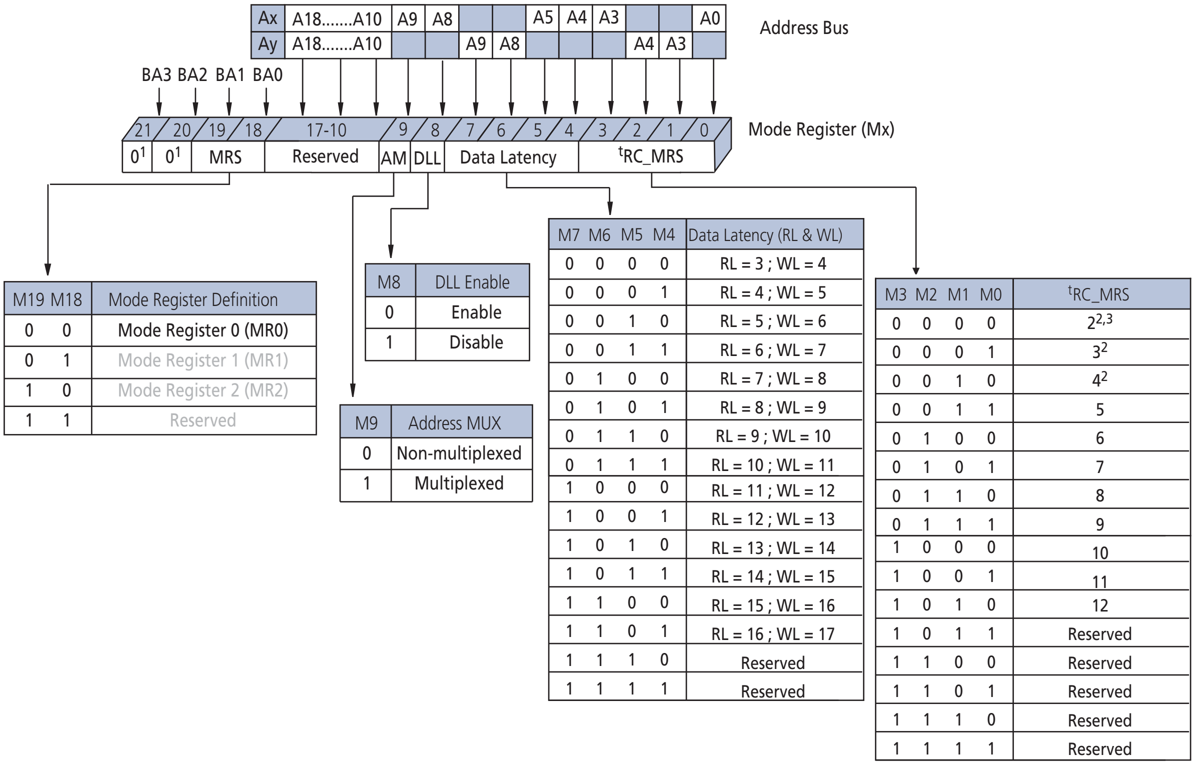
Figure 58: Power-Up/Initialization Sequence in Multiplexed Address Mode


T (MAX) = 200ms
VDD
VDDQ
VEXT
VREF
See power-up conditions in the initialization sequence text
Power-up ramp
Stable and valid clock
tCK
CK#
CK
tCH
tCL
100 cycles
tIOZ = 20ns
RESET#
tDK
DK#
DK
tDKH
tDKL
Command
NOP
NOP
NOP
MRS
MRS
NOP
MRS
NOP
MRS
NOP
DM
Address
MR0¹
MR0² (Ax)
MR0 (Ay)
MR1 (Ax)
MR1 (Ay)
MR2 (Ax)
MR2 (Ay)
QK#
QK
QVLD⁵
DQ
RTT High-Z
T = 200µs (MIN)
10,000 CK cycles (MIN)
tMRSC
tMRSC
512 clock cycles for DLL Reset & ZQ Calibration
READ Training register specs apply
All voltage supplies valid and stable
Indicates a break in time scale
Don't Care or Unknown

Notes:

1. Set address bit MR0[9] HIGH. This enables the device to enter multiplexed address mode when in non-multiplexed mode operation. Multiplexed address mode can also be entered at a later time by issuing an MRS command with MR0[9] HIGH. After address bit MR0[9] is set HIGH, tMRSC must be satisfied before the two-cycle multiplexed mode MRS command is issued.
2. Address MR0[9] must be set HIGH. This and the following step set the desired MR0 setting after the RLDRAM device is in multiplexed address mode.
3. MR1 (A*x*), MR1 (A*y*), MR2 (A*x*), and MR2 (A*y*) represent MR1 and MR2 settings in multiplexed address mode.
4. The above sequence must be followed in order to power up the RLDRAM device in the multiplexed address mode.
5. See QVLD output drive strength status during power up and initialization in non-multiplexed initialization operation section.
6. After MR2 has been issued, R_{TT} is either High-Z or enabled to the ODT value selected in MR1.

Figure 59: MR0 Definition for Multiplexed Address Mode


Ax A18.......A10 A9 A8 A5 A4 A3 A0
Ay A18.......A10 A9 A8 A4 A3
Address Bus
BA3 BA2 BA1 BA0
21 20 19 18 17-10 9 8 7 6 5 4 3 2 1 0
Mode Register (Mx)
0¹ 0¹ MRS Reserved AM DLL Data Latency tRC_MRS

M19	M18	Mode Register Definition
0	0	Mode Register 0 (MR0)
0	1	Mode Register 1 (MR1)
1	0	Mode Register 2 (MR2)
1	1	Reserved

M9	Address MUX
0	Non-multiplexed
1	Multiplexed

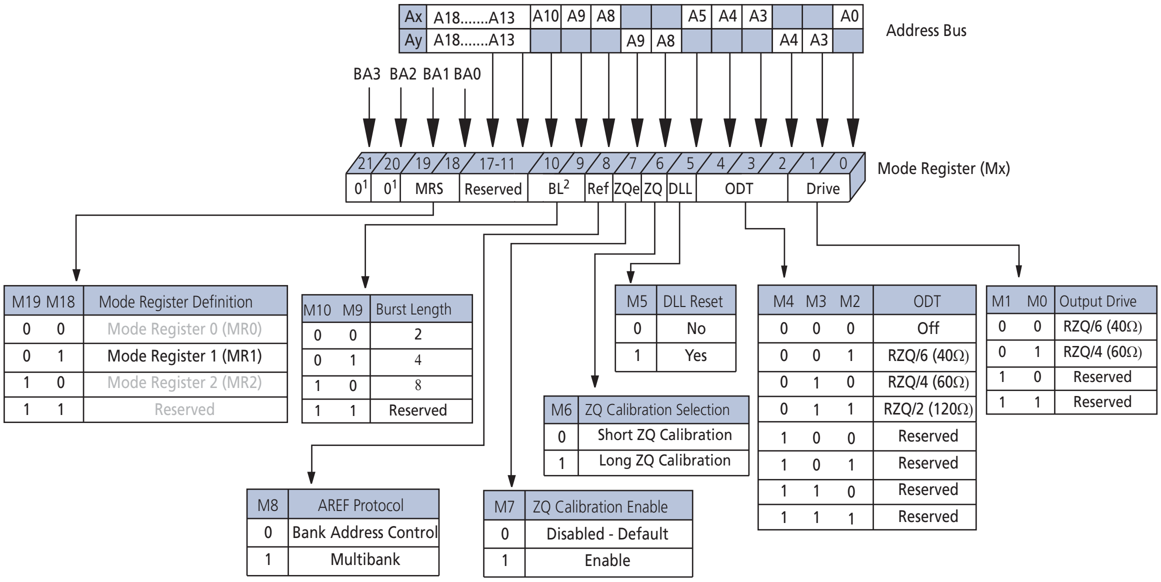
M8	DLL Enable
0	Enable
1	Disable

M7	M6	M5	M4	Data Latency (RL & WL)
0	0	0	0	RL = 3 ; WL = 4
0	0	0	1	RL = 4 ; WL = 5
0	0	1	0	RL = 5 ; WL = 6
0	0	1	1	RL = 6 ; WL = 7
0	1	0	0	RL = 7 ; WL = 8
0	1	0	1	RL = 8 ; WL = 9
0	1	1	0	RL = 9 ; WL = 10
0	1	1	1	RL = 10 ; WL = 11
1	0	0	0	RL = 11 ; WL = 12
1	0	0	1	RL = 12 ; WL = 13
1	0	1	0	RL = 13 ; WL = 14
1	0	1	1	RL = 14 ; WL = 15
1	1	0	0	RL = 15 ; WL = 16
1	1	0	1	RL = 16 ; WL = 17
1	1	1	0	Reserved
1	1	1	1	Reserved

M3	M2	M1	M0	^{t}RC_MRS
0	0	0	0	2[2,3]
0	0	0	1	3[2]
0	0	1	0	4[2]
0	0	1	1	5
0	1	0	0	6
0	1	0	1	7
0	1	1	0	8
0	1	1	1	9
1	0	0	0	10
1	0	0	1	11
1	0	1	0	12
1	0	1	1	Reserved
1	1	0	0	Reserved
1	1	0	1	Reserved
1	1	1	0	Reserved
1	1	1	1	Reserved

Notes:
1. BA2, BA3, and all address balls corresponding to reserved bits must be held LOW during the MRS command.
2. BL8 not allowed.
3. BL4 not allowed.

Figure 60: MR1 Definition for Multiplexed Address Mode


Ax A18.......A13 A10 A9 A8 A5 A4 A3 A0
Ay A18.......A13 A9 A8 A4 A3
Address Bus
BA3 BA2 BA1 BA0
21 20 19 18 17-11 10 9 8 7 6 5 4 3 2 1 0
0[1] 0[1] MRS Reserved BL[2] Ref ZQe ZQ DLL ODT Drive
Mode Register (Mx)

M19	M18	Mode Register Definition
0	0	Mode Register 0 (MR0)
0	1	Mode Register 1 (MR1)
1	0	Mode Register 2 (MR2)
1	1	Reserved

M10	M9	Burst Length
0	0	2
0	1	4
1	0	8
1	1	Reserved

M5	DLL Reset
0	No
1	Yes

M4	M3	M2	ODT
0	0	0	Off
0	0	1	RZQ/6 (40Ω)
0	1	0	RZQ/4 (60Ω)
0	1	1	RZQ/2 (120Ω)
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

M1	M0	Output Drive
0	0	RZQ/6 (40Ω)
0	1	RZQ/4 (60Ω)
1	0	Reserved
1	1	Reserved

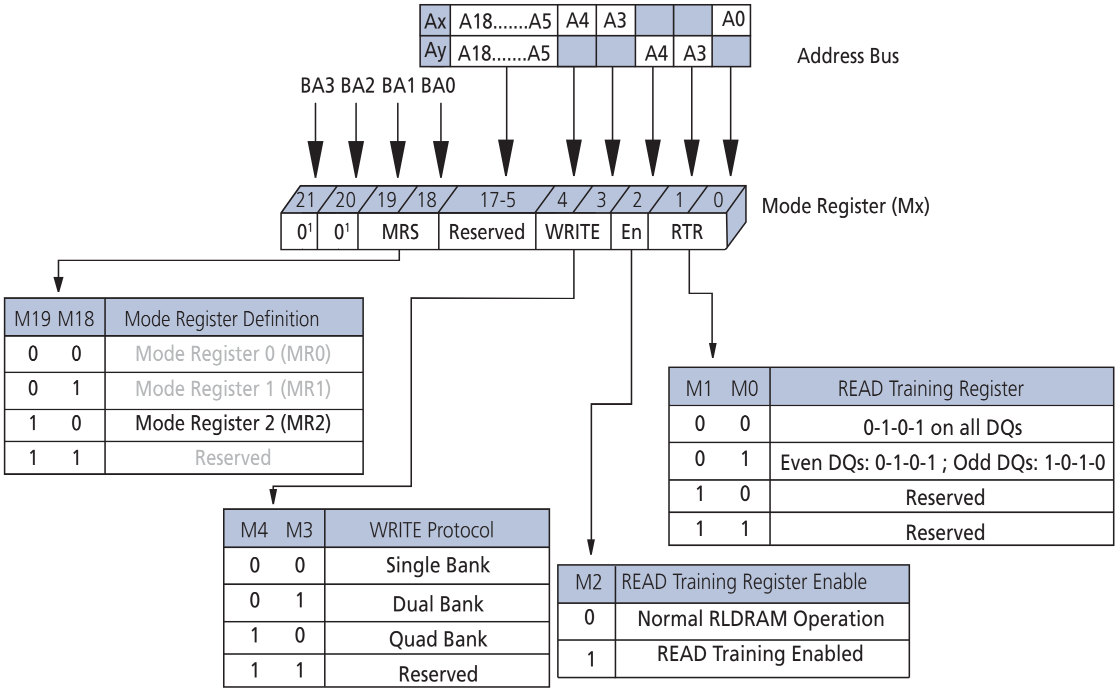
M6	ZQ Calibration Selection
0	Short ZQ Calibration
1	Long ZQ Calibration

M8	AREF Protocol
0	Bank Address Control
1	Multibank

M7	ZQ Calibration Enable
0	Disabled - Default
1	Enable

Notes:
1. BA2, BA3, and all address balls corresponding to reserved bits must be held LOW during the MRS command.
2. BL8 not available in x36.

Figure 61: MR2 Definition for Multiplexed Address Mode



M19	M18	Mode Register Definition
0	0	Mode Register 0 (MR0)
0	1	Mode Register 1 (MR1)
1	0	Mode Register 2 (MR2)
1	1	Reserved

M4	M3	WRITE Protocol
0	0	Single Bank
0	1	Dual Bank
1	0	Quad Bank
1	1	Reserved

M2	READ Training Register Enable
0	Normal RLDRAM Operation
1	READ Training Enabled

M1	M0	READ Training Register
0	0	0-1-0-1 on all DQs
0	1	Even DQs: 0-1-0-1 ; Odd DQs: 1-0-1-0
1	0	Reserved
1	1	Reserved

Note: 1. BA2, BA3, and all address balls corresponding to reserved bits must be held LOW during the MRS command.

Table 41: Address Mapping in Multiplexed Address Mode

Data Width	Burst Length	Ball	Address										
			A0	**A3**	**A4**	**A5**	**A8**	**A9**	**A10**	**A13**	**A14**	**A17**	**A18**
x36	2	Ax	A0	A3	A4	A5	A8	A9	A10	A13	A14	A17	A18
		Ay	X	A1	A2	X	A6	A7	X	A11	A12	A16	A15
	4	Ax	A0	A3	A4	A5	A8	A9	A10	A13	A14	A17	X
		Ay	X	A1	A2	X	A6	A7	X	A11	A12	A16	A15
x18	2	Ax	A0	A3	A4	A5	A8	A9	A10	A13	A14	A17	A18
		Ay	X	A1	A2	X	A6	A7	A19	A11	A12	A16	A15
	4	Ax	A0	A3	A4	A5	A8	A9	A10	A13	A14	A17	A18
		Ay	X	A1	A2	X	A6	A7	X	A11	A12	A16	A15
	8	Ax	A0	A3	A4	A5	A8	A9	A10	A13	A14	A17	X
		Ay	X	A1	A2	X	A6	A7	X	A11	A12	A16	A15

Note: 1. X = "Don't Care"

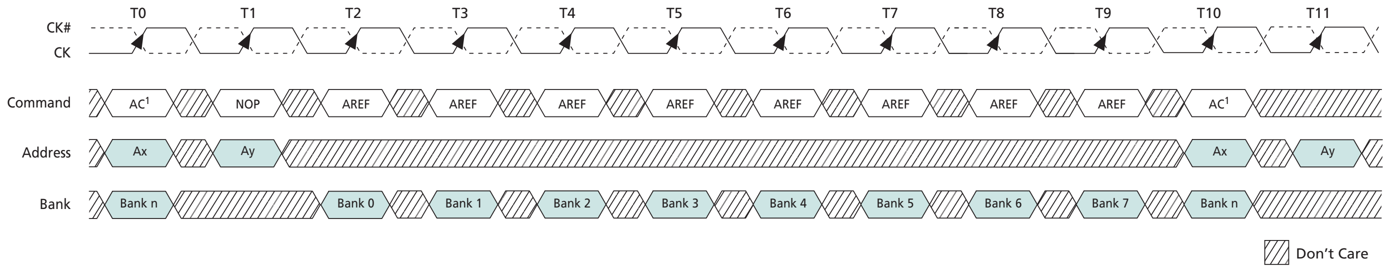
Data Latency in Multiplexed Address Mode

When in multiplexed address mode, data latency (READ and WRITE) begins when the A*y* part of the address is issued with any READ or WRITE command. ^{t}RC is measured from the clock edge in which the command and A*x* part of the address is issued in both multiplexed and non-multiplexed address mode.

REFRESH Command in Multiplexed Address Mode

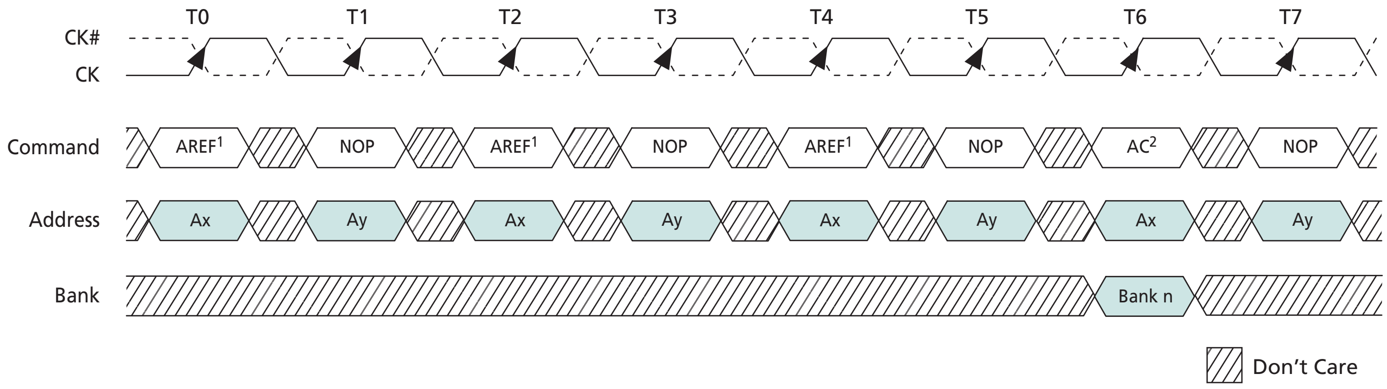
Similar to other commands when in multiplexed address mode, both modes of AREF (single and multibank) are executed on the rising clock edge, following the one on which the command is issued. However, when in bank address-controlled AREF, as only the bank address is required, the next command can be applied on the following clock. When using multibank AREF, the bank addresses are mapped across A*x* and A*y* so a subsequent command cannot be issued until two clock cycles later.

Figure 62: Bank Address-Controlled AUTO REFRESH Operation with Multiplexed Addressing


T0
T1
T2
T3
T4
T5
T6
T7
T8
T9
T10
T11
CK#
CK
Command
AC[1]
NOP
AREF
AREF
AREF
AREF
AREF
AREF
AREF
AREF
AC[1]
Address
Ax
Ay
Ax
Ay
Bank
Bank n
Bank 0
Bank 1
Bank 2
Bank 3
Bank 4
Bank 5
Bank 6
Bank 7
Bank n
Don't Care

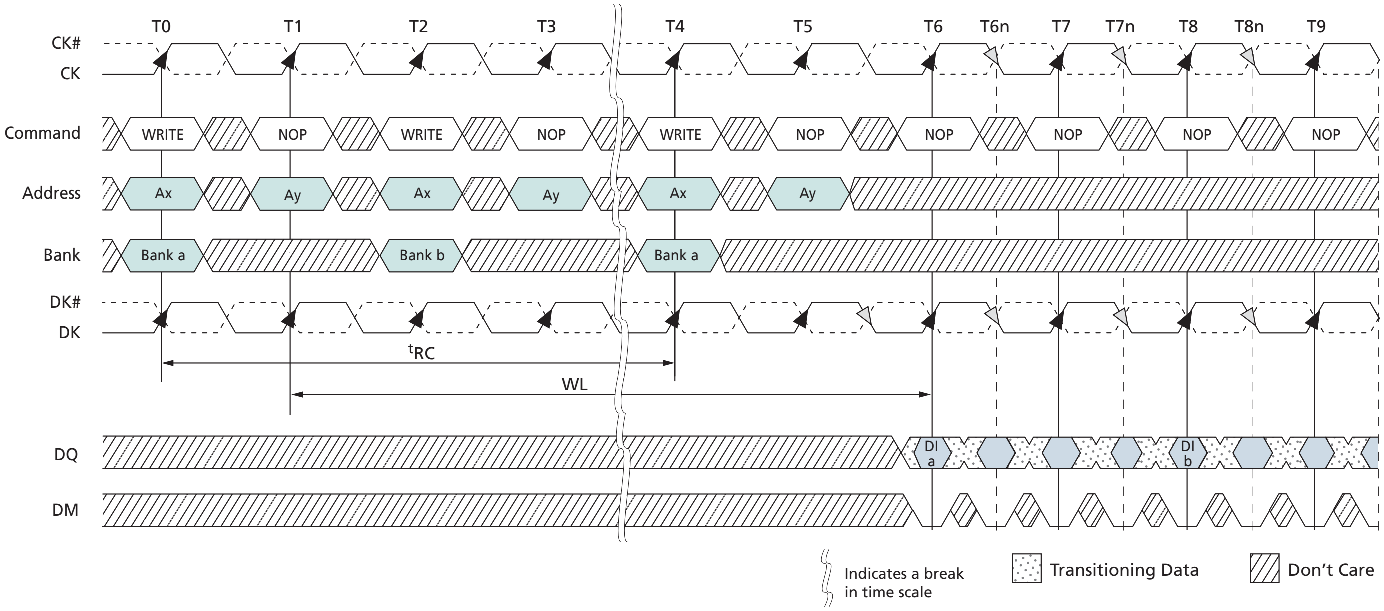
Note: 1. Any command subject to ^{t}RC specification.

Figure 63: Multibank AUTO REFRESH Operation with Multiplexed Addressing


T0
T1
T2
T3
T4
T5
T6
T7
CK#
CK
Command
AREF[1]
NOP
AREF[1]
NOP
AREF[1]
NOP
AC[2]
NOP
Address
Ax
Ay
Ax
Ay
Ax
Ay
Ax
Ay
Bank
Bank n
Don't Care

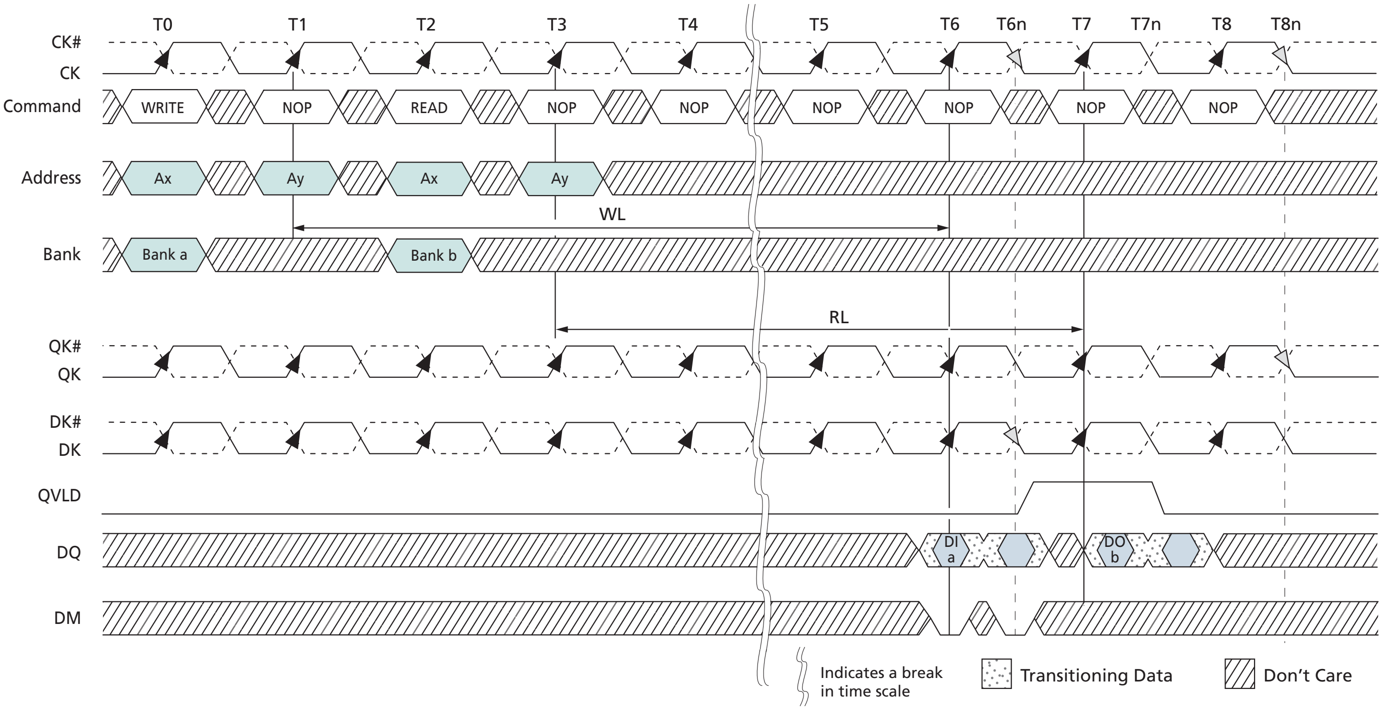
Notes:
1. Usage of multibank AREF subject to ^{t}SAW and ^{t}MMD specifications.
2. Any command subject to ^{t}RC specification.

Figure 64: Consecutive WRITE Bursts with Multiplexed Addressing


T0
T1
T2
T3
T4
T5
T6
T6n
T7
T7n
T8
T8n
T9
CK#
CK
Command
WRITE
NOP
WRITE
NOP
WRITE
NOP
NOP
NOP
NOP
NOP
Address
Ax
Ay
Ax
Ay
Ax
Ay
Bank
Bank a
Bank b
Bank a
DK#
DK
tRC
WL
DQ
DI a
DI b
DM
Indicates a break in time scale
Transitioning Data
Don't Care

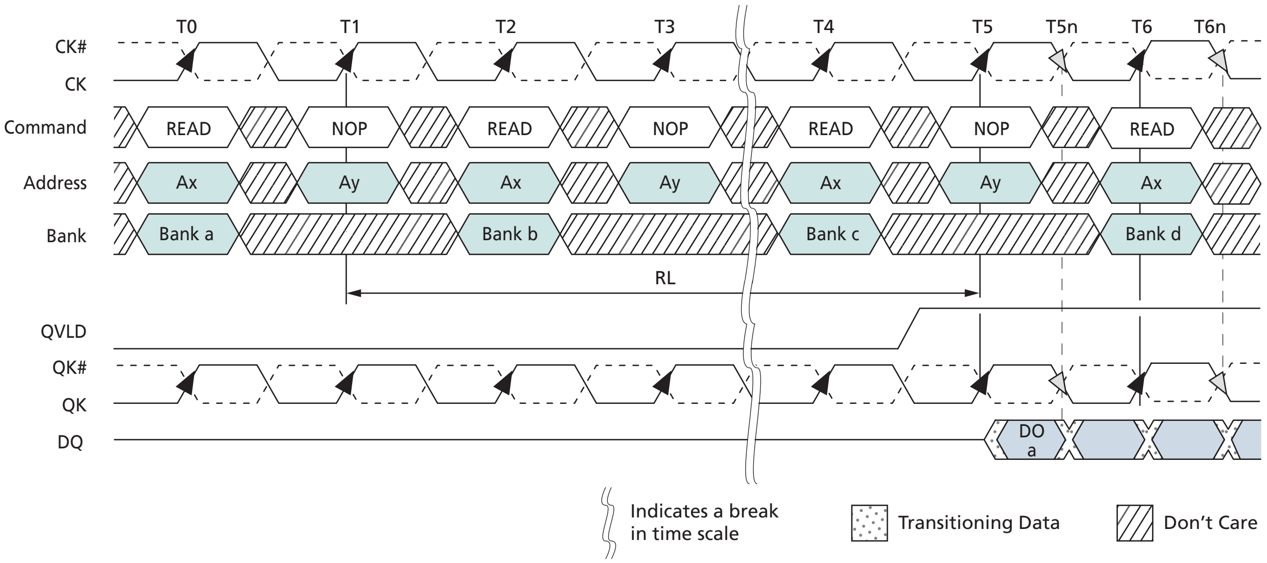
Note: 1. DI *a* = data-in for bank *a*; DI *b* = data-in for bank *b*.

Figure 65: WRITE-to-READ with Multiplexed Addressing


T0
T1
T2
T3
T4
T5
T6
T6n
T7
T7n
T8
T8n
CK#
CK
Command
WRITE
NOP
READ
NOP
NOP
NOP
NOP
NOP
NOP
Address
Ax
Ay
Ax
Ay
WL
Bank
Bank a
Bank b
RL
QK#
QK
DK#
DK
QVLD
DQ
DI a
DO b
DM
Indicates a break in time scale
Transitioning Data
Don't Care

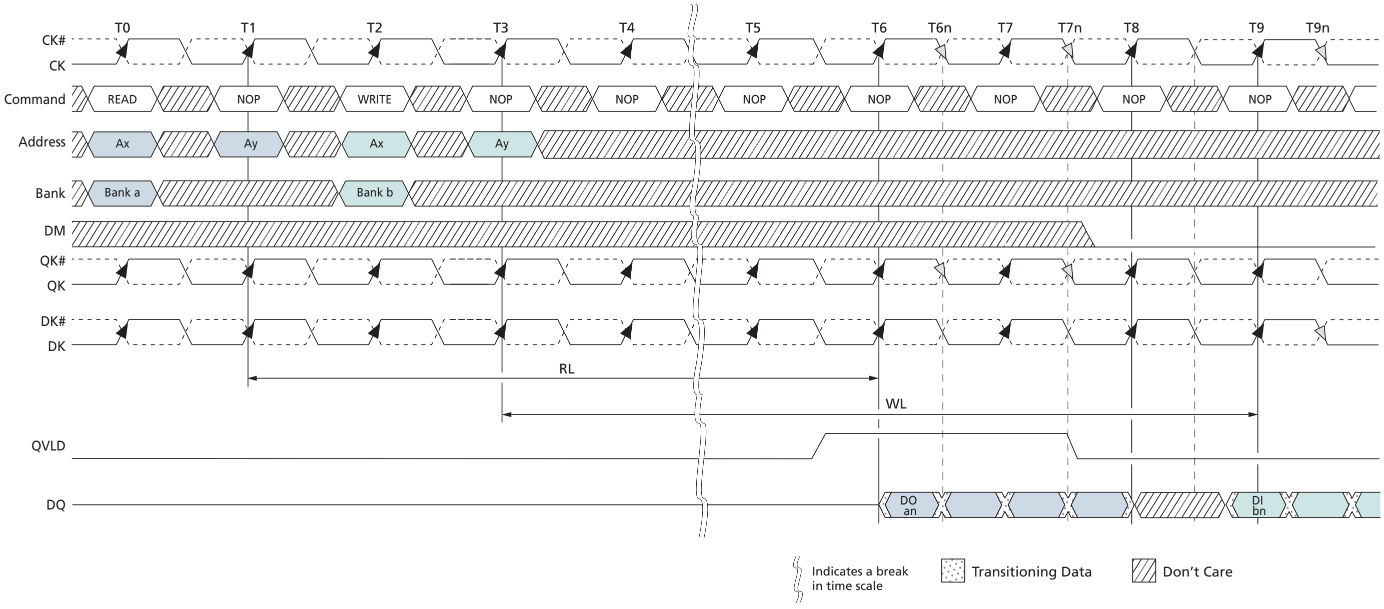
Note: 1. DI *a* = data-in for bank *a*; DI *b* = data-in for bank *b*.

Figure 66: Consecutive READ Bursts with Multiplexed Addressing


T0
T1
T2
T3
T4
T5
T5n
T6
T6n
CK#
CK
Command
READ
NOP
READ
NOP
READ
NOP
READ
Address
Ax
Ay
Ax
Ay
Ax
Ay
Ax
Bank
Bank a
Bank b
Bank c
Bank d
RL
QVLD
QK#
QK
DQ
DO a
Indicates a break in time scale
Transitioning Data
Don't Care

Note: 1. DO *a* = data-out for bank *a.*

Figure 67: READ-to-WRITE with Multiplexed Addressing


T0
T1
T2
T3
T4
T5
T6
T6n
T7
T7n
T8
T9
T9n
CK#
CK
Command
READ
NOP
WRITE
NOP
NOP
NOP
NOP
NOP
NOP
NOP
Address
Ax
Ay
Ax
Ay
Bank
Bank a
Bank b
DM
QK#
QK
DK#
DK
RL
WL
QVLD
DQ
DO an
DI bn
Indicates a break in time scale
Transitioning Data
Don't Care

Note: 1. DO *a* = data-out for bank *a;* DI *b* = data-in for bank *b.*

Mirror Function

The mirror function ball (MF) is a DC input used to create mirrored ballouts for simple dual-loaded clamshell mounting. If the MF ball is tied LOW, the address and command balls are in their true layout. If the MF ball is tied HIGH, the address and command balls are mirrored around the central y-axis (column 7). The following table shows the ball assignments when the MF ball is tied HIGH for a x18 device. Compare that table to Table 1 (page 12) to see how the address and command balls are mirrored. The same balls are mirrored on the x36 device.

Table 42: 32 Meg x 18 Ball Assignments with MF Ball Tied HIGH

	1	2	3	4	5	6	7	8	9	10	11	12	13
A		V_{SS}	V_{DD}	NF	V_{DDQ}	NF	V_{REF}	DQ7	V_{DDQ}	DQ8	V_{DD}	V_{SS}	RESET#
B	V_{EXT}	V_{SS}	NF	V_{SSQ}	NF	V_{DDQ}	DM0	V_{DDQ}	DQ5	V_{SSQ}	DQ6	V_{SS}	V_{EXT}
C	V_{DD}	NF	V_{DDQ}	NF	V_{SSQ}	NF	DK0#	DQ2	V_{SSQ}	DQ3	V_{DDQ}	DQ4	V_{DD}
D	A13	V_{SSQ}	NF	V_{DDQ}	NF	V_{SSQ}	DK0	V_{SSQ}	QK0	V_{DDQ}	DQ0	V_{SSQ}	A11
E	V_{SS}	CS#	V_{SSQ}	NF	V_{DDQ}	NF	MF	QK0#	V_{DDQ}	DQ1	V_{SSQ}	A0	V_{SS}
F	A9	A5	V_{DD}	A4	A3	REF#	ZQ	WE#	A1	A2	V_{DD}	NC[1]	A7
G	V_{SS}	A18	A8	V_{SS}	BA0	V_{SS}	CK#	V_{SS}	BA1	V_{SS}	A6	A15	V_{SS}
H	A10	V_{DD}	A12	A17	V_{DD}	BA2	CK	BA3	V_{DD}	A16	A14	V_{DD}	A19
J	V_{DDQ}	NF	V_{SSQ}	NF	V_{DDQ}	NF	V_{SS}	QK1#	V_{DDQ}	DQ9	V_{SSQ}	QVLD	V_{DDQ}
K	NF	V_{SSQ}	NF	V_{DDQ}	NF	V_{SSQ}	DK1	V_{SSQ}	QK1	V_{DDQ}	DQ10	V_{SSQ}	DQ11
L	V_{DD}	NF	V_{DDQ}	NF	V_{SSQ}	NF	DK1#	DQ12	V_{SSQ}	DQ13	V_{DDQ}	DQ14	V_{DD}
M	V_{EXT}	V_{SS}	NF	V_{SSQ}	NF	V_{DDQ}	DM1	V_{DDQ}	DQ15	V_{SSQ}	DQ16	V_{SS}	V_{EXT}
N	V_{SS}	TCK	V_{DD}	TDO	V_{DDQ}	NF	V_{REF}	DQ17	V_{DDQ}	TDI	V_{DD}	TMS	V_{SS}

RESET Operation

The RESET signal (RESET#) is an asynchronous signal that triggers any time it drops LOW. There are no restrictions for when it can go LOW. After RESET# goes LOW, it must remain LOW for 100ns. During this time, the outputs are disabled, ODT (R_{TT}) turns off (High-Z), and the DRAM resets itself. Prior to RESET# going HIGH, at least 100 stable CK cycles with NOP commands must be given to the RLDRAM. After RESET# goes HIGH, the DRAM must be reinitialized as though a normal power-up was executed. All refresh counters on the DRAM are reset, and data stored in the DRAM is assumed unknown after RESET# has gone LOW.

IEEE 1149.1 Serial Boundary Scan (JTAG)

The RLDRAM 3 device incorporates a serial boundary-scan test access port (TAP) for the purpose of testing the connectivity of the device after it has been mounted on a printed circuit board (PCB). As the complexity of PCB high-density surface mounting techniques increases, the boundary-scan architecture is a valuable resource for interconnectivity debug. This port operates in accordance with IEEE Standard 1149.1-2001 (JTAG) with the exception of the ZQ pin. To ensure proper boundary-scan testing of the ZQ pin, MR1[7] needs to be set to 0 until the JTAG testing of the pin is complete. Note that upon power up, the default state of the MRS bit M1[7] is low.

The JTAG test access port utilizes the TAP controller on the device, from which the instruction register, boundary-scan register, bypass register, and ID register can be selected. Each of these functions of the TAP controller is described in detail below.

Disabling the JTAG Feature

It is possible to operate an RLDRAM 3 device without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW (V_{SS}) to prevent clocking of the device. TDI and TMS are internally pulled up and may be unconnected. They may alternately be connected to V_{DDQ} through a pull-up resistor. TDO should be left unconnected. Upon power-up, the device will come up in a reset state, which will not interfere with the operation of the device.

Test Access Port (TAP)

Test Clock (TCK)

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

Test Mode Select (TMS)

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK.

All the states in Figure 68 (page 105) are entered through the serial input of the TMS ball. A 0 in the diagram represents a LOW on the TMS ball during the rising edge of TCK, while a 1 represents a HIGH on TMS.

Test Data-In (TDI)

The TDI ball is used to serially input test instructions and data into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. For information on loading the instruction register, see Figure 68 (page 105). TDI is connected to the most significant bit (MSB) of any register (see Figure 69 (page 105)).

Test Data-Out (TDO)

The TDO output ball is used to serially clock test instructions and data out from the registers. The TDO output driver is only active during the Shift-IR and Shift-DR TAP controller states. In all other states, the TDO ball is in a High-Z state. The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register (see Figure 69 (page 105)).

TAP Controller

The TAP controller is a finite state machine that uses the state of the TMS ball at the rising edge of TCK to navigate through its various modes of operation (see Figure 68 (page 105)). Each state is described in detail below.

Test-Logic-Reset

The test-logic-reset controller state is entered when TMS is held HIGH for at least five consecutive rising edges of TCK. As long as TMS remains HIGH, the TAP controller will remain in the test-logic-reset state. The test logic is inactive during this state.

Run-Test/Idle

The run-test/idle is a controller state in between scan operations. This state can be maintained by holding TMS LOW. From there, either the data register scan, or subsequently, the instruction register scan, can be selected.

Select-DR-Scan

Select-DR-scan is a temporary controller state. All test data registers retain their previous state while here.

Capture-DR

The capture-DR state is where the data is parallel-loaded into the test data registers. If the boundary-scan register is the currently selected register, then the data currently on the balls is latched into the test data registers.

Shift-DR

Data is shifted serially through the data register while in this state. As new data is input through the TDI ball, data is shifted out of the TDO ball.

Exit1-DR, Pause-DR, and Exit2-DR

The purpose of exit1-DR is used to provide a path to return back to the run-test/idle state (through the update-DR state). The pause-DR state is entered when the shifting of data through the test registers needs to be suspended. When shifting is to reconvene, the controller enters the exit2-DR state and then can re-enter the shift-DR state.

Update-DR

When the EXTEST instruction is selected, there are latched parallel outputs of the boundary-scan shift register that only change state during the update-DR controller state.

Instruction Register States

The instruction register states of the TAP controller are similar to the data register states. The desired instruction is serially shifted into the instruction register during the shift-IR state and is loaded during the update-IR state.

Figure 68: TAP Controller State Diagram

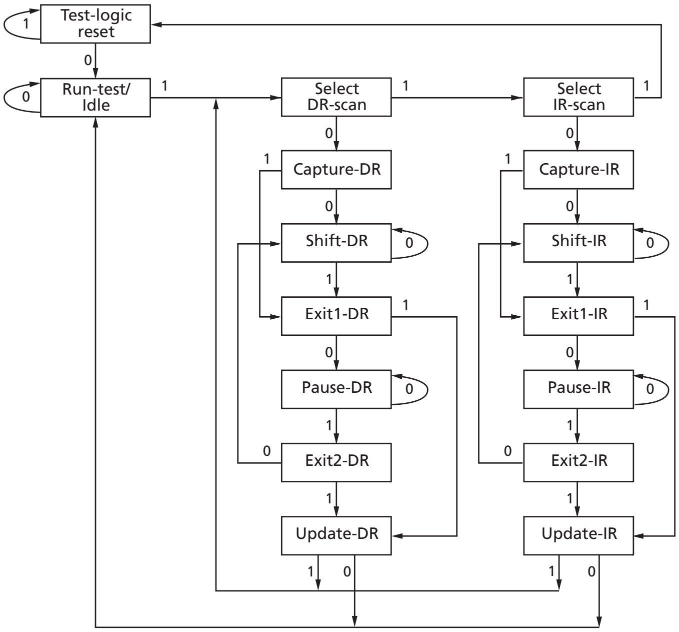
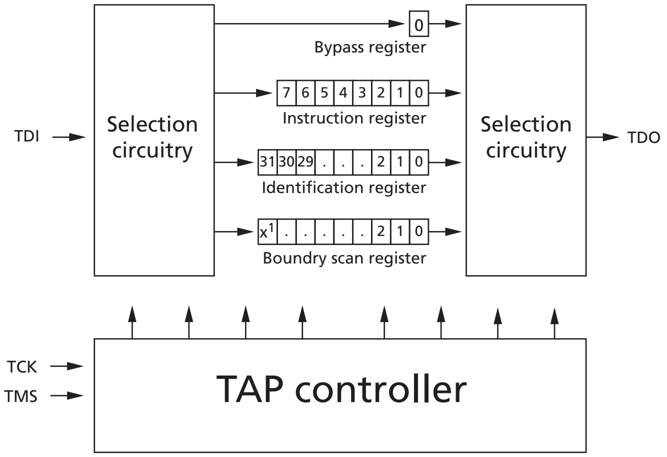

Test-logic reset
Run-test/ Idle
Select DR-scan
Select IR-scan
Capture-DR
Shift-DR
Exit1-DR
Pause-DR
Exit2-DR
Update-DR
Capture-IR
Shift-IR
Exit1-IR
Pause-IR
Exit2-IR
Update-IR
0
1

Figure 69: TAP Controller Functional Block Diagram


Bypass register
Instruction register
Identification register
Boundry scan register
Selection circuitry
Selection circuitry
TDI
TDO
TCK
TMS
TAP controller
7 6 5 4 3 2 1 0
31 30 29 . . . 2 1 0
x1 . . . . . . 2 1 0

Note: 1. x = 121 for all configurations.

Performing a TAP RESET

A reset is performed by forcing TMS HIGH (V_{DDQ}) for five rising edges of ^{t}CK. This RESET does not affect the operation of the device and may be performed while the device is operating.

At power-up, the TAP is reset internally to ensure that TDO comes up in a High-Z state. If JTAG inputs cannot be guaranteed to be stable during power-up it is recommended that TMS be held HIGH for at least 5 consecutive TCK cycles prior to boundary scan testing.

TAP Registers

Registers are connected between the TDI and TDO balls and allow data to be scanned into and out of the RLDRAM 3 device test circuitry. Only one register can be selected at a time through the instruction register. Data is serially loaded into the TDI ball on the rising edge of TCK. Data is output on the TDO ball on the falling edge of TCK.

Instruction Register

Eight-bit instructions can be serially loaded into the instruction register. This register is loaded during the update-IR state of the TAP controller. Upon power-up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as described in the previous section.

When the TAP controller is in the capture-IR state, the two LSBs are loaded with a binary 01 pattern to allow for fault isolation of the board-level serial test data path.

Bypass Register

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain chips. The bypass register is a single-bit register that can be placed between the TDI and TDO balls. This enables data to be shifted through the device with minimal delay. The bypass register is set LOW (V_{SS}) when the BYPASS instruction is executed.

Boundary-Scan Register

The boundary-scan register is connected to all the input and bidirectional balls on the device. Several balls are also included in the scan register to reserved balls. The device has a 121-bit register.

The boundary-scan register is loaded with the contents of the RAM I/O ring when the TAP controller is in the capture-DR state and is then placed between the TDI and TDO balls when the controller is moved to the shift-DR state.

The order in which the bits are connected is shown in Table 49 (page 111). Each bit corresponds to one of the balls on the RLDRAM package. The MSB of the register is connected to TDI, and the LSB is connected to TDO.

Identification (ID) Register

The ID register is loaded with a vendor-specific, 32-bit code during the capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the RLDRAM 3 and can be shifted out when the TAP controller is in the shift-DR state. The ID register has a vendor code and other information described in Table 46 (page 110).

TAP Instruction Set

Overview

There are 2^8 different instructions possible with the 8-bit instruction register. All combinations used are listed in Table 48 (page 111). These six instructions are described in detail below. The remaining instructions are reserved and should not be used.

The TAP controller used in this RLDRAM 3 device is fully compliant to the IEEE 1149.1 convention.

Instructions are loaded into the TAP controller during the shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register through the TDI and TDO balls. To execute the instruction after it is shifted in, the TAP controller needs to be moved into the update-IR state.

EXTEST

The EXTEST instruction enables circuitry external to the component package to be tested. Boundary-scan register cells at output balls are used to apply a test vector, while those at input balls capture test results. Typically, the first test vector to be applied using the EXTEST instruction will be shifted into the boundary-scan register using the PRELOAD instruction. Thus, during the update-IR state of EXTEST, the output driver is turned on, and the PRELOAD data is driven onto the output balls.

IDCODE

The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the instruction register. It also places the instruction register between the TDI and TDO balls and enables the IDCODE to be shifted out of the device when the TAP controller enters the shift-DR state. The IDCODE instruction is loaded into the instruction register upon power-up or whenever the TAP controller is given a test logic reset state.

High-Z

The High-Z instruction causes the bypass register to be connected between the TDI and TDO. This places all RLDRAM outputs into a High-Z state.

CLAMP

When the CLAMP instruction is loaded into the instruction register, the data driven by the output balls are determined from the values held in the boundary-scan register.

SAMPLE/PRELOAD

When the SAMPLE/PRELOAD instruction is loaded into the instruction register and the TAP controller is in the capture-DR state, a snapshot can be taken of the states of the component's input and output signals without interfering with the normal operation of the assembled board. The snapshot is taken on the rising edge of TCK and is captured in the boundry-scan register. The data can then be viewed by shifting through the component's TDO output.

The user must be aware that the TAP controller clock can only operate at a frequency up to 50 MHz, while the RLDRAM 3 clock operates significantly faster. Because there is a large difference between the clock frequencies, it is possible that during the capture-DR state, an input or output will undergo a transition. The TAP may then try to capture a signal while in transition (metastable state). This will not harm the device, but there is no guarantee as to the value that will be captured. Repeatable results may not be possible.

To ensure that the boundary-scan register will capture the correct value of a signal, the RLDRAM signal must be stabilized long enough to meet the TAP controller's capture setup plus hold time (^{t}CS plus ^{t}CH). The RLDRAM clock input might not be captured correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE/PRELOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the CK and CK# captured in the boundary-scan register.

After the data is captured, it is possible to shift out the data by putting the TAP into the shift-DR state. This places the boundary-scan register between the TDI and TDO balls.

BYPASS

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a shift-DR state, the bypass register is placed between TDI and TDO. The advantage of the BYPASS instruction is that it shortens the boundary-scan path when multiple devices are connected together on a board.

Reserved for Future Use

The remaining instructions are not implemented but are reserved for future use. Do not use these instructions.

Figure 70: JTAG Operation - Loading Instruction Code and Shifting Out Data

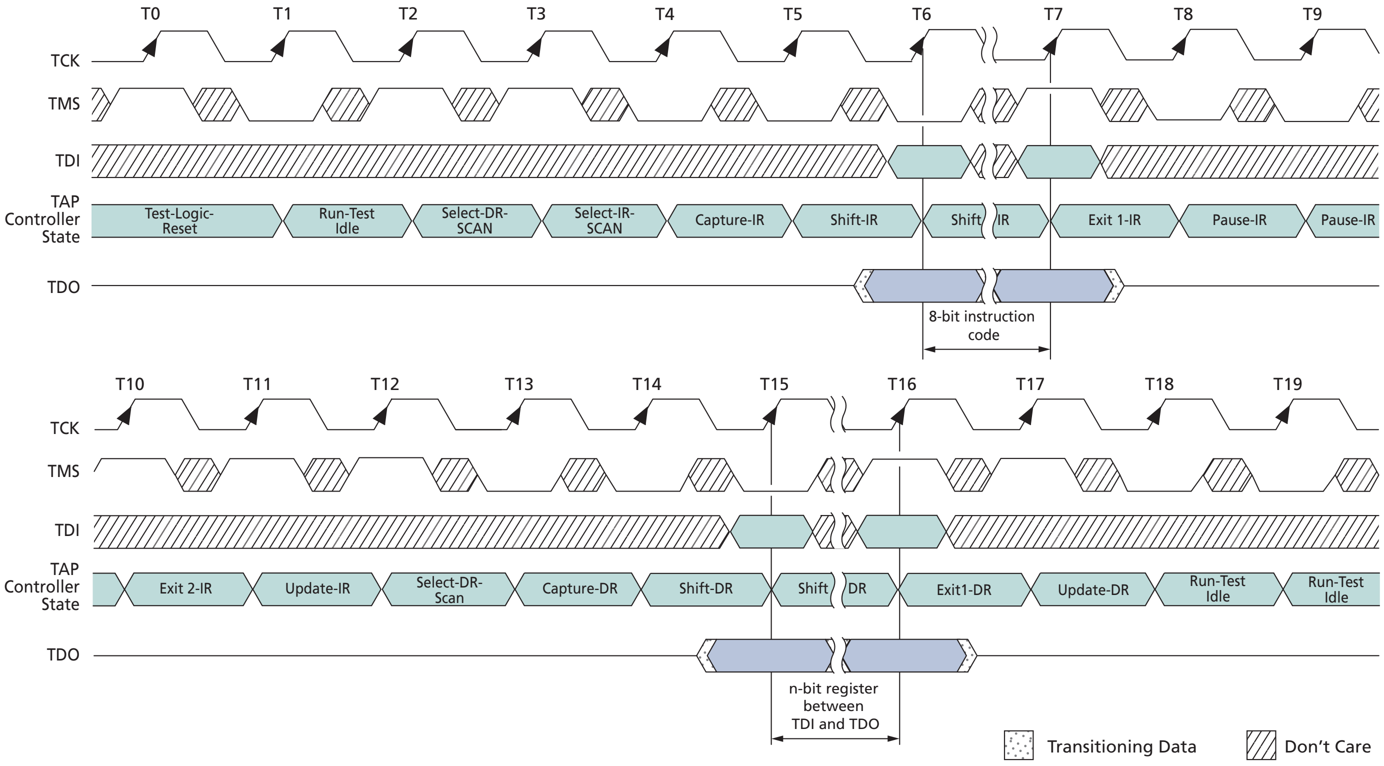

T0
T1
T2
T3
T4
T5
T6
T7
T8
T9
TCK
TMS
TDI
TAP Controller State
Test-Logic-Reset
Run-Test Idle
Select-DR-SCAN
Select-IR-SCAN
Capture-IR
Shift-IR
Shift IR
Exit 1-IR
Pause-IR
Pause-IR
TDO
8-bit instruction code
T10
T11
T12
T13
T14
T15
T16
T17
T18
T19
TCK
TMS
TDI
TAP Controller State
Exit 2-IR
Update-IR
Select-DR-Scan
Capture-DR
Shift-DR
Shift DR
Exit1-DR
Update-DR
Run-Test Idle
Run-Test Idle
TDO
n-bit register between TDI and TDO
Transitioning Data
Don't Care

Figure 71: TAP Timing

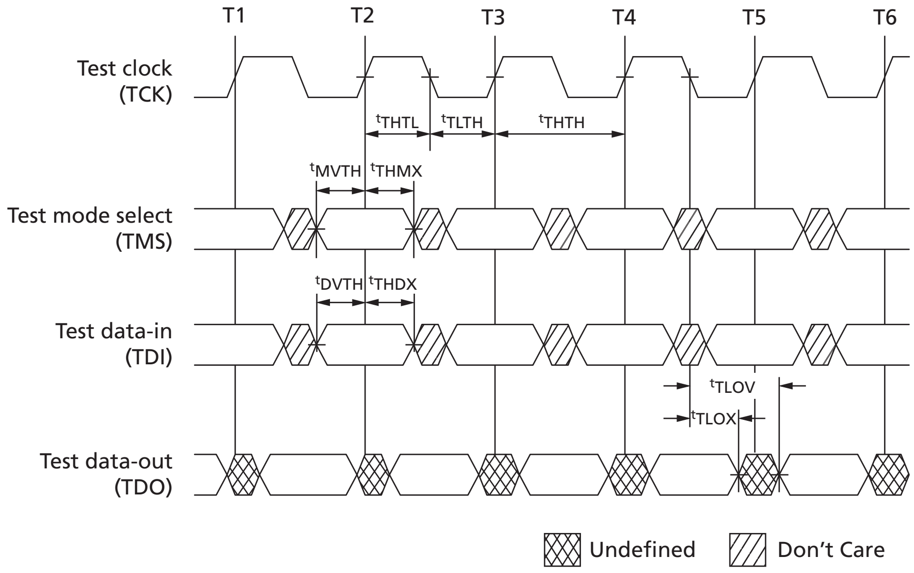

T1
T2
T3
T4
T5
T6
Test clock (TCK)
tTHTL
tTLTH
tTHTH
tMVTH
tTHMX
Test mode select (TMS)
tDVTH
tTHDX
Test data-in (TDI)
tTLOV
tTLOX
Test data-out (TDO)
Undefined
Don't Care

Table 43: TAP Input AC Logic Levels

0°C ≤ T_C ≤ +95°C; +1.28V ≤ V_{DD} ≤ +1.42V, unless otherwise noted

Description	Symbol	Min	Max	Units
Input HIGH (logic 1) voltage	V_{IH}	V_{REF} + 0.225	-	V
Input LOW (logic 0) voltage	V_{IL}	-	V_{REF} - 0.225	V

Note: 1. All voltages referenced to V_{SS} (GND).

Table 44: TAP AC Electrical Characteristics

0°C ≤ T_C ≤ +95°C; +1.28V ≤ V_{DD} ≤ +1.42V

Description	Symbol	Min	Max	Units
Clock				
Clock cycle time	^tTHTH	20		ns
Clock frequency	^fTF		50	MHz
Clock HIGH time	^tTHTL	10		ns
Clock LOW time	^tTLTH	10		ns
TDI/TDO times				
TCK LOW to TDO unknown	^tTLOX	0		ns
TCK LOW to TDO valid	^tTLOV		10	ns
TDI valid to TCK HIGH	^tDVTH	5		ns
TCK HIGH to TDI invalid	^tTHDX	5		ns
Setup times				
TMS setup	^tMVTH	5		ns

Table 44: TAP AC Electrical Characteristics (Continued)

0°C ≤ T_C ≤ +95°C; +1.28V ≤ V_{DD} ≤ +1.42V

Description	Symbol	Min	Max	Units
Capture setup	^tCS	5		ns
Hold times				
TMS hold	^tTHMX	5		ns
Capture hold	^tCH	5		ns

Note: 1. ^tCS and ^tCH refer to the setup and hold time requirements of latching data from the boundary-scan register.

Table 45: TAP DC Electrical Characteristics and Operating Conditions

0°C ≤ T_C ≤ +95°C; +1.28V ≤ V_{DD} ≤ +1.42V, unless otherwise noted

Description	Condition	Symbol	Min	Max	Units	Notes
Input HIGH (logic 1) voltage		V_{IH}	V_{REF} + 0.15	V_{DDQ}	V	1, 2
Input LOW (logic 0) voltage		V_{IL}	V_{SSQ}	V_{REF} - 0.15	V	1, 2
Input leakage current	0V ≤ V_{IN} ≤ V_{DD}	I_{LI}	-5.0	5.0	µA	
Output leakage current	Output disabled, 0V ≤ V_{IN} ≤ V_{DDQ}	I_{LO}	-5.0	5.0	µA	
Output low voltage	I_{OLC} = 100µA	V_{OL1}		0.2	V	1
Output low voltage	I_{OLT} = 2mA	V_{OL2}		0.4	V	1
Output high voltage	$\lvert I_{OHC}\rvert$ = 100µA	V_{OH1}	V_{DDQ} - 0.2		V	1
OUTPUT HIGH VOLTAGE	$\lvert I_{OHT}\rvert$ = 2mA	V_{OH2}	V_{DDQ} - 0.4		V	1

Notes:
1. All voltages referenced to V_{SS} (GND).
2. See AC Overshoot/Undershoot Specifications section for overshoot and undershoot limits.

Table 46: Identification Register Definitions

Instruction Field	All Devices	Description
Revision number (31:28)	abcd	ab = 00 for Die Revision A cd = 00 for x18, 01 for x36
Device ID (27:12)	00jkidef10100111	def = 000 for 576Mb, 001 for 1Gb Double Die Package, 010 for 1Gb Monolithic i = 0 for common I/O jk = 10 for RLDRAM 3
ISSI JEDEC ID code (11:1)	00011010101	Enables unique identification of RLDRAM vendor
ID register presence indicator (0)	1	Indicates the presence of an ID register

Table 47: Scan Register Sizes

Register Name	Bit Size
Instruction	8
Bypass	1
ID	32
Boundary scan	121

Table 48: Instruction Codes

Instruction	Code	Description
Extest	0000 0000	Captures I/O ring contents; Places the boundary-scan register between TDI and TDO; This operation does not affect RLDRAM 3 operations.
ID code	0010 0001	Loads the ID register with the vendor ID code and places the register between TDI and TDO; This operation does not affect RLDRAM 3 operations.
Sample/preload	0000 0101	Captures I/O ring contents; Places the boundary-scan register between TDI and TDO.
Clamp	0000 0111	Selects the bypass register to be connected between TDI and TDO; Data driven by output balls are determined from values held in the boundary-scan register.
High-Z	0000 0011	Selects the bypass register to be connected between TDI and TDO; All outputs are forced into High-Z.
Bypass	1111 1111	Places the bypass register between TDI and TDO; This operation does not affect RLDRAM operations.

Table 49: Boundary Scan (Exit)

Bit#	Ball	Bit#	Ball	Bit#	Ball
1	N8	42	L7	83	M3
2	N8	43	K7	84	M3
3	M11	44	H1	85	M5
4	M11	45	H4	86	M5
5	M9	46	G2	87	L2
6	M9	47	G3	88	L2
7	L12	48	F1	89	L4
8	L12	49	F5	90	L4
9	L10	50	F4	91	L6
10	L10	51	F2	92	L6
11	L8	52	D1	93	K1
12	L8	53	F7	94	K1
13	K13	54	D7	95	K3
14	K13	55	C7	96	K3
15	K11	56	A13	97	J4
16	K11	57	B7	98	J4

Table 49: Boundary Scan (Exit) (Continued)

Bit#	Ball	Bit#	Ball	Bit#	Ball
17	J10	58	E7	99	J6
18	J10	59	D13	100	K5
19	J8	60	F12	101	J2
20	K9	61	F10	102	A4
21	J12	62	F9	103	A4
22	A10	63	E2	104	A6
23	A10	64	E12	105	A6
24	A8	65	F6	106	B3
25	A8	66	F8	107	B3
26	B11	67	G7	108	B5
27	B11	68	H7	109	B5
28	B9	69	G5	110	C2
29	B9	70	G9	111	C2
30	C12	71	H6	112	C4
31	C12	72	H8	113	C4
32	C10	73	F13	114	C6
33	C10	74	G11	115	C6
34	C8	75	G12	116	E4
35	C8	76	H10	117	E4
36	E10	77	H3	118	D3
37	E10	78	H11	119	D3
38	D11	79	H13	120	E6
39	D11	80	M7	121	D5
40	E8	81	N6	-	-
41	D9	82	N6	-	-

Table 50: Ordering Information

Commercial Range: T_C = 0° to +95°C

Frequency	Speed (tCK)	tRC(min)	Order Part No.	Organization	Package
1066 MHz	0.93ns	8ns	IS49RL18320-093EBL	32M x 18	168 FBGA, Lead-free
			IS49RL36160-093EBL	16M x 36	168 FBGA, Lead-free
		10ns	IS49RL18320-093BL	32M x 18	168 FBGA, Lead-free
			IS49RL36160-093BL	16M x 36	168 FBGA, Lead-free
933 MHz	1.07ns	8ns	IS49RL18320-107EBL	32M x 18	168 FBGA, Lead-free
			IS49RL36160-107EBL	16M x 36	168 FBGA, Lead-free
		10ns	IS49RL18320-107BL	32M x 18	168 FBGA, Lead-free
			IS49RL36160-107BL	16M x 36	168 FBGA, Lead-free
800 MHz	1.25ns	8ns	IS49RL18320-125FBL	32M x 18	168 FBGA, Lead-free
			IS49RL36160-125FBL	16M x 36	168 FBGA, Lead-free
		10ns	IS49RL18320-125EBL	32M x 18	168 FBGA, Lead-free
			IS49RL36160-125EBL	16M x 36	168 FBGA, Lead-free
		12ns	IS49RL18320-125BL	32M x 18	168 FBGA, Lead-free
			IS49RL36160-125BL	16M x 36	168 FBGA, Lead-free

Industrial Range: T_C = -40° to +95°C

Frequency	Speed (tCK)	tRC(min)	Order Part No.	Organization	Package
1066 MHz	0.93ns	8ns	IS49RL18320-093EBLI	32M x 18	168 FBGA, Lead-free
			IS49RL36160-093EBLI	16M x 36	168 FBGA, Lead-free
		10ns	IS49RL18320-093BLI	32M x 18	168 FBGA, Lead-free
			IS49RL36160-093BLI	16M x 36	168 FBGA, Lead-free
933 MHz	1.07ns	8ns	IS49RL18320-107EBLI	32M x 18	168 FBGA, Lead-free
			IS49RL36160-107EBLI	16M x 36	168 FBGA, Lead-free
		10ns	IS49RL18320-107BLI	32M x 18	168 FBGA, Lead-free
			IS49RL36160-107BLI	16M x 36	168 FBGA, Lead-free
800 MHz	1.25ns	8ns	IS49RL18320-125FBLI	32M x 18	168 FBGA, Lead-free
			IS49RL36160-125FBLI	16M x 36	168 FBGA, Lead-free
		10ns	IS49RL18320-125EBLI	32M x 18	168 FBGA, Lead-free
			IS49RL36160-125EBLI	16M x 36	168 FBGA, Lead-free
		12ns	IS49RL18320-125BLI	32M x 18	168 FBGA, Lead-free
			IS49RL36160-125BLI	16M x 36	168 FBGA, Lead-free

Revision History

Rev. C, Production – 12/12

- Changed the units from nS to CK for tWTR specification
- Corrected values from 0.935 to 0.9375 in the speed bin table
- Added reference to -125F on front page, part number guide, speed bin table, and tRC_MRS table
- Added a -125F column into the IDD table
- Updated the Imbref4 IDD values for most fields. This increase is necessary because a mistake in the char test used to set these limits caused the values to be incorrect
- Corrected typo in the tIS/tIH derating table. (tIH - 0.4 CMD/ADDR slew rate, CK/CK# 4.0 V/ns)
- Changed definition of NOP command to specify the states of WE# & REF#
- Added note on the leaded (PA) package to "Consult factory"
- Updated READ-to-WRITE timing diagram from BL = 4 to BL = 2. The WRITE-to-READ timing diagram is BL = 2 (I did not want customers to think that a NOP was required when transitioning from a READ to a WRITE)
- Changed wording in Note 3 of ZQ calibration description
- Added note to general description, which explains using a X36 devices with only 2 QK/QK# sets instead of all 4.
- Modified ball out to reflect the ballout required to support the X18 DDP and the 2Gb monolithic devices
- Added note to Iref that states: "all other balls not under test = 0V"
- Added updates to -125F speed bin table and tRC_MRS table to meet customer request to support CL=12, tRC_MRS = 6 for tCK=1.334ns

Rev. B, Advance – 1/12

- Changed tQKQx,min to tQKQx,max in figure 52 read data valid window
- Added Vext information to Note 1 of Input/Output Capacitance table
- Added Table 38 tRC_MRS values
- Updated tIS/tIH(base) values on page 50 to 85,120,170 & 65,100, 120
- Corrected error in High-Z description. replaced "boundry-scan" with "bypass"
- Added verbage in SAMPLE/PRELOAD description, specifying which edge of TCK is used to capture the states of the pins.
- Changed JTAG boundary scan order. Now L7=bit 42, K7=bit 43, J6=bit 99, K5=bit 100
- Updated Figure 70 "JTAG Operation" to match actual operation of the device.
- Changed QKx, QKx# to DKx, DKx# in table 33 & 34 Derating values for tDS/tDH.
- Changed Cjtag min from 2.0 to 1.5.
- Corrected typo in X36 functional block diagram. Changed DQ1/DK1# to DK1/DK1#.
- Added RESET# and MF pin Ci Max spec into Input/Output Capacitance table 6.
- Listed QVLD with the QK/QK# signals in Table 6.
- Changed tDS Base value from 15 to -15 in Table 33.
- Corrected errors in VSEH min, VSEL max and VILdiff(AC) max definitions.
- Updated Speed bin table 26 to fill in tCK gaps by adjusting tCKmin values for -107E, RL=5, -125, RL=6,9,14,15.

- Updated table 38 tRC_MRS values to reflect the speed bin table changes
- Changed the Cimax (CMD, ADDR) spec from 2.1 to 2.25
- Changed the Cjtag max from 5.3 to 4.5
- Added X18 & X36 IDD values.
- updated tCKQK AC timing specifications.
- Added in the thermal impedance values

Rev. A, Advance – 6/11

- Initial release

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