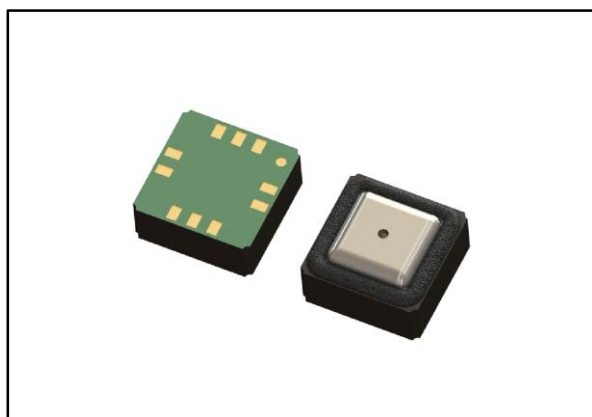


## MEMS pressure sensor: 260-1260 hPa absolute digital output barometer with water resistant package

Datasheet - production data



### Features

- Pressure sensor with water resistant package
- 260 to 1260 hPa absolute pressure range
- Current consumption down to 3  $\mu$ A
- High overpressure capability: 20x full scale
- Embedded temperature compensation
- 24-bit pressure data output
- 16-bit temperature data output
- ODR from 1 Hz to 75 Hz
- SPI and I<sup>2</sup>C interfaces
- Embedded FIFO
- Interrupt functions: Data Ready, FIFO flags, pressure thresholds
- Supply voltage: 1.7 to 3.6
- ECOPACK<sup>®</sup> lead-free compliant

### Applications

- Wearable devices
- Altimeter and barometer for portable devices
- GPS applications
- Weather station equipment

### Description

The LPS35HW is an ultra-compact piezoresistive pressure sensor which functions as a digital output barometer. The device comprises a sensing element and an IC interface which communicates through I<sup>2</sup>C or SPI from the sensing element to the application.

The sensing element, which detects absolute pressure, consists of a suspended membrane manufactured using a dedicated process developed by ST.

The LPS35HW is available in a holed ceramic LGA package. It is guaranteed to operate over a temperature range extending from -40 °C to +85 °C. The package is holed to allow external pressure to reach the sensing element.

Table 1: Device summary table

| Order code | Temperature range [°C] | Package   | Packing       |
|------------|------------------------|-----------|---------------|
| LPS35HWTR  | -40 to +85 °C          | CCLGA-10L | Tape and reel |
| LPS35HW    |                        | CCLGA-10L | Tray          |

---

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# 1 Block diagram and pin description

Figure 1: Block diagram

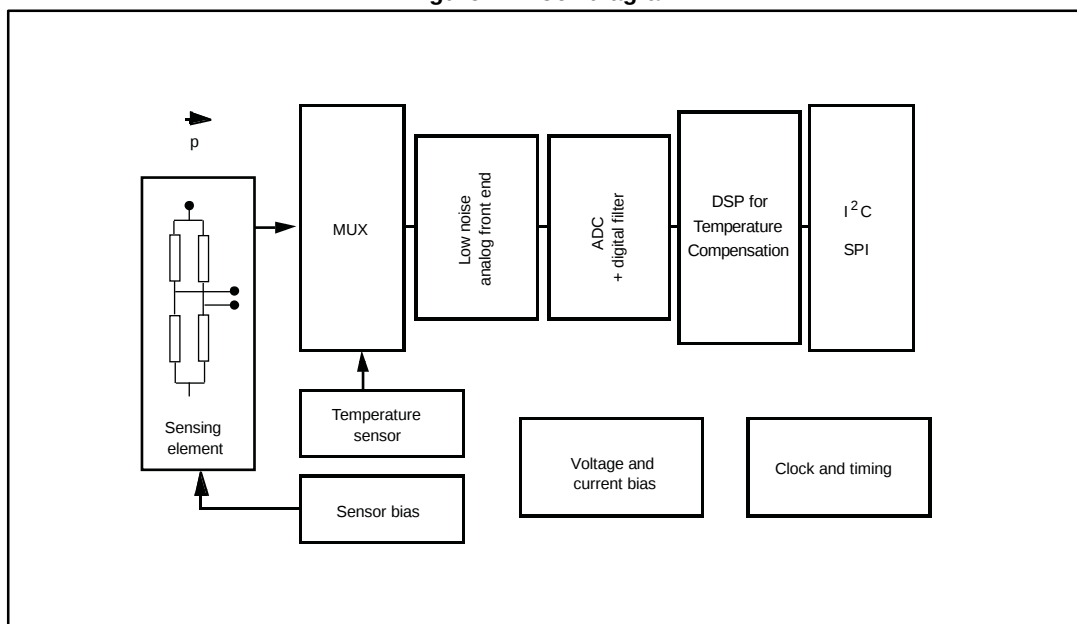


Figure 2: Pin connections (bottom view)

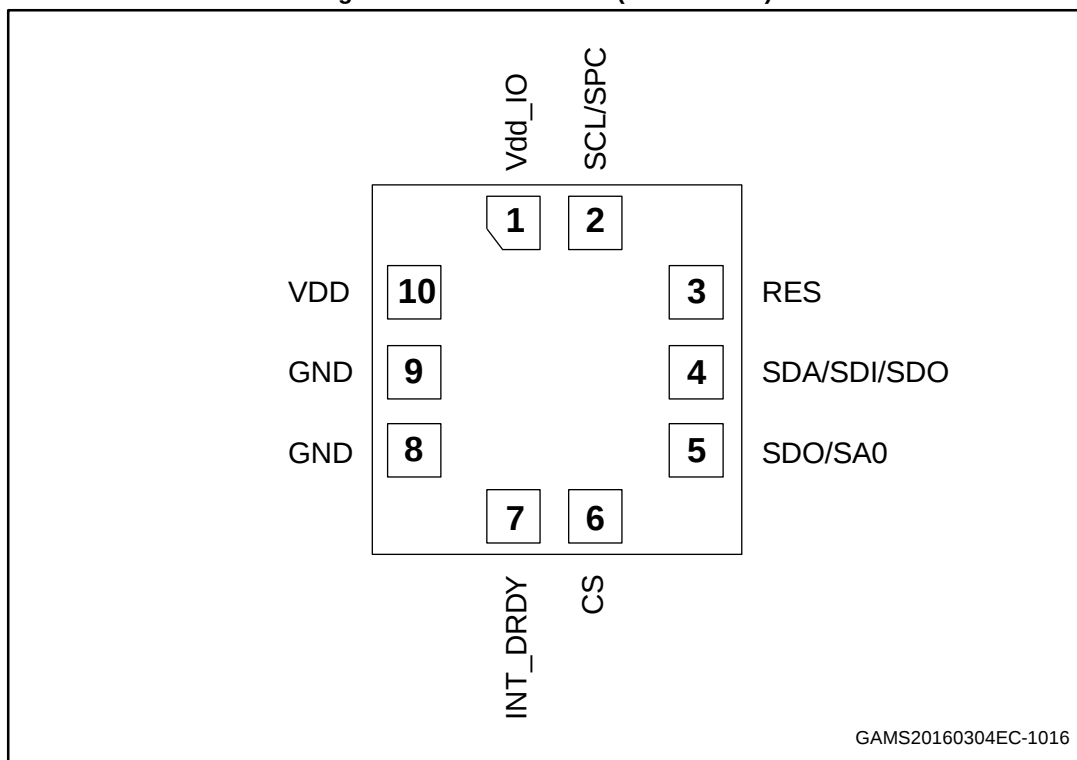


Table 2: Pin description

| Pin number | Name                  | Function                                                                                                                                                                |
|------------|-----------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1          | Vdd_IO                | Power supply for I/O pins                                                                                                                                               |
| 2          | SCL SPC               | I <sup>2</sup> C serial clock (SCL)<br>SPI serial port clock (SPC)                                                                                                      |
| 3          | Reserved              | Connect to GND                                                                                                                                                          |
| 4          | SDA<br>SDI<br>SDI/SDO | I <sup>2</sup> C serial data (SDA)<br>4-wire SPI serial data input (SDI)<br>3-wire serial data input/output (SDI/SDO)                                                   |
| 5          | SDO SA0               | 4-wire SPI serial data output (SDO)<br>I <sup>2</sup> C less significant bit of the device address (SA0)                                                                |
| 6          | CS                    | SPI enable<br>I <sup>2</sup> C/SPI mode selection<br>(1: SPI idle mode / I <sup>2</sup> C communication enabled; 0: SPI communication mode / I <sup>2</sup> C disabled) |
| 7          | INT_DRDY              | Interrupt or Data Ready                                                                                                                                                 |
| 8          | GND                   | 0 V supply                                                                                                                                                              |
| 9          | GND                   | 0 V supply                                                                                                                                                              |
| 10         | VDD                   | Power supply                                                                                                                                                            |

## 2 Mechanical and electrical specifications

### 2.1 Mechanical characteristics

VDD= 1.8 V, T = 25 °C, unless otherwise noted.

Table 3: Pressure and temperature sensor characteristics

| Symbol                                    | Parameter                                    | Test condition                                 | Min. | Typ. <sup>a</sup>         | Max. | Unit    |
|-------------------------------------------|----------------------------------------------|------------------------------------------------|------|---------------------------|------|---------|
| <b>Pressure sensor characteristics</b>    |                                              |                                                |      |                           |      |         |
| PT <sub>op</sub>                          | Operating temperature range                  |                                                | -40  |                           | +85  | °C      |
| PT <sub>full</sub>                        | Full accuracy temperature range              |                                                | 0    |                           | +65  | °C      |
| P <sub>op</sub>                           | Operating pressure range                     |                                                | 260  |                           | 1260 | hPa     |
| P <sub>bits</sub>                         | Pressure output data                         |                                                |      | 24                        |      | bits    |
| P <sub>sens</sub>                         | Pressure sensitivity                         |                                                |      | 4096                      |      | LSB/hPa |
| P <sub>AccRel</sub>                       | Relative accuracy over pressure <sup>b</sup> | P= 800 - 1100 hPa<br>T = 25 °C                 |      | ±0.1                      |      | hPa     |
| P <sub>AccT</sub>                         | Absolute accuracy over temperature           | Pop<br>T= 0 to 65 °C<br>After OPC <sup>c</sup> |      | ±1                        |      | hPa     |
|                                           |                                              | Pop<br>T= 0 to 65 °C no OPC <sup>c</sup>       |      | ±4                        |      |         |
| ODR <sub>res</sub>                        | Pressure output data rate <sup>a</sup>       |                                                |      | 1<br>10<br>25<br>50<br>75 |      | Hz      |
| <b>Temperature sensor characteristics</b> |                                              |                                                |      |                           |      |         |
| T <sub>op</sub>                           | Operating temperature range                  |                                                | -40  |                           | +85  | °C      |
| T <sub>sens</sub>                         | Temperature sensitivity                      |                                                |      | 100                       |      | LSB/°C  |
| T <sub>acc</sub>                          | Temperature absolute accuracy                | T= 0 to 65 °C                                  |      | ±1.5                      |      | °C      |

<sup>a</sup> Typical specifications are not guaranteed.

<sup>b</sup> By design.

<sup>c</sup> OPC: One Point Calibration, see registers RPDS\_L/H (18h,19h).

| Symbol           | Parameter                                 | Test condition | Min. | Typ. <sup>a</sup>         | Max. | Unit |
|------------------|-------------------------------------------|----------------|------|---------------------------|------|------|
| ODR <sub>T</sub> | Output temperature data rate <sup>a</sup> |                |      | 1<br>10<br>25<br>50<br>75 |      | Hz   |

## 2.2 Electrical characteristics

VDD= 1.8 V, T = 25 °C, unless otherwise noted.

Table 4: Electrical characteristics

| Symbol | Parameter                         | Test condition            | Min. | Typ. <sup>b</sup> | Max.    | Unit |
|--------|-----------------------------------|---------------------------|------|-------------------|---------|------|
| VDD    | Supply voltage                    |                           | 1.7  |                   | 3.6     | V    |
| Vdd_IO | IO supply voltage                 |                           | 1.7  |                   | Vdd+0.1 | V    |
| Idd    | Supply current                    | @ODR 1 Hz<br>LC_EN bit =0 |      | 15                |         | μA   |
|        |                                   | @ODR 1 Hz<br>LC_EN bit =1 |      | 3                 |         |      |
| IddPdn | Supply current in power-down mode |                           |      | 1                 |         | μA   |

1. Typical specifications are not guaranteed.

## 2.3 Communication interface characteristics

### 2.3.1 SPI serial peripheral interface

Subject to general operating conditions for Vdd and TOP.

Table 5: SPI slave timing values

| Symbol               | Parameter            | Value <sup>c</sup> |      | Unit |
|----------------------|----------------------|--------------------|------|------|
|                      |                      | Min.               | Max. |      |
| t <sub>c</sub> (SPC) | SPI clock cycle      | 100                |      | ns   |
| f <sub>c</sub> (SPC) | SPI clock frequency  |                    | 10   | MHz  |
| t <sub>su</sub> (CS) | CS setup time        | 6                  |      | ns   |
| t <sub>h</sub> (CS)  | CS hold time         | 8                  |      |      |
| t <sub>su</sub> (SI) | SDI input setup time | 5                  |      |      |
| t <sub>h</sub> (SI)  | SDI input hold time  | 15                 |      |      |

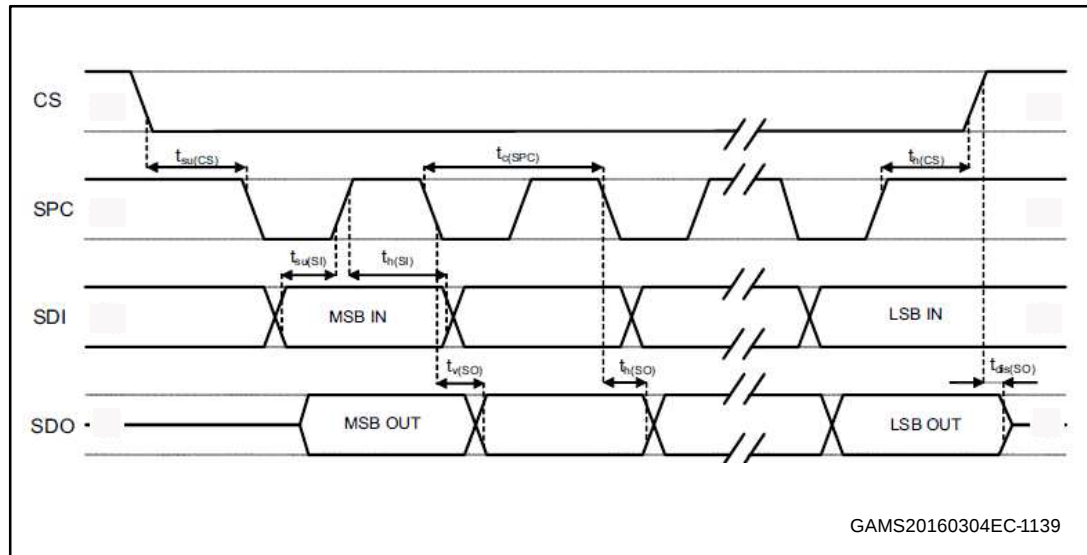
<sup>a</sup> Output data rate is configured acting on ODR[2:0] in CTRL\_REG1 (10h)

<sup>b</sup> Typical specifications are not guaranteed.

<sup>c</sup> Values are guaranteed at 10 MHz clock frequency for SPI with both 4 and 3 wires, based on characterization results, not tested in production.

| Symbol        | Parameter               | Value <sup>c</sup> |      | Unit |
|---------------|-------------------------|--------------------|------|------|
|               |                         | Min.               | Max. |      |
| $t_{V(SO)}$   | SDO valid output time   |                    | 50   |      |
| $t_{H(SO)}$   | SDO output hold time    | 9                  |      |      |
| $t_{dis(SO)}$ | SDO output disable time |                    | 50   |      |

Figure 3: SPI slave timing diagram



Measurement points are done at  $0.2 \cdot V_{DD\_IO}$  and  $0.8 \cdot V_{DD\_IO}$ , for both ports.

### 2.3.2 I2C inter - IC control interface

Subject to general operating conditions for  $V_{DD}$  and TOP.

Table 6: I<sup>2</sup>C slave timing values

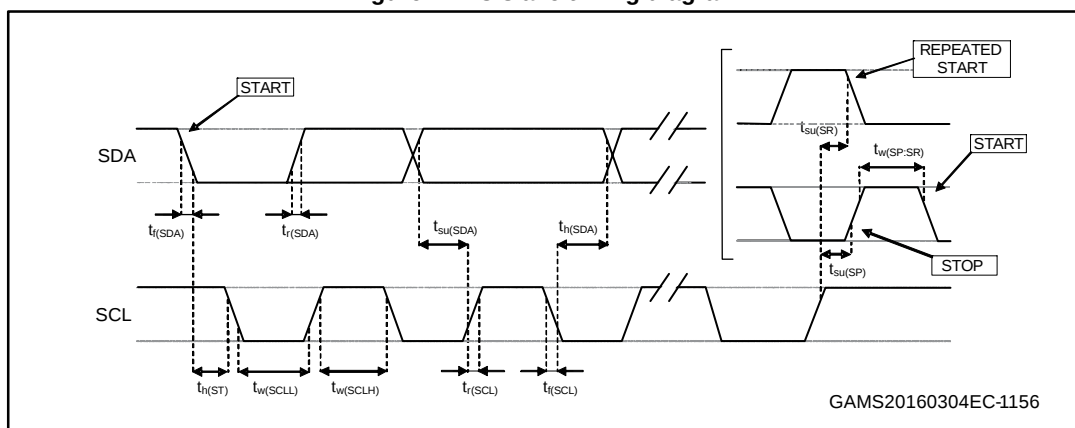
| Symbol        | Parameter           | I <sup>2</sup> C standard mode <sup>a</sup> |      | I <sup>2</sup> C fast mode <sup>b</sup> |      | Unit    |
|---------------|---------------------|---------------------------------------------|------|-----------------------------------------|------|---------|
|               |                     | Min.                                        | Max. | Min.                                    | Max. |         |
| $f_{(SCL)}$   | SCL clock frequency | 0                                           | 100  | 0                                       | 400  | kHz     |
| $t_{W(SCLL)}$ | SCL clock low time  | 4.7                                         |      | 1.3                                     |      | $\mu s$ |
| $t_{W(SCLH)}$ | SCL clock high time | 4.0                                         |      | 0.6                                     |      |         |
| $t_{su(SDA)}$ | SDA setup time      | 250                                         |      | 100                                     |      | ns      |
| $t_{H(SDA)}$  | SDA data hold time  | 0.01                                        | 3.45 | 0                                       | 0.9  | $\mu s$ |

<sup>a</sup> Data based on standard I<sup>2</sup>C protocol requirement, not tested in production.

<sup>b</sup>  $C_b$  = total capacitance of one bus line, in pF.

| Symbol             | Parameter                                      | I <sup>2</sup> C standard mode <sup>a</sup> |      | I <sup>2</sup> C fast mode <sup>b</sup> |      | Unit |
|--------------------|------------------------------------------------|---------------------------------------------|------|-----------------------------------------|------|------|
|                    |                                                | Min.                                        | Max. | Min.                                    | Max. |      |
| tr(SDA)<br>tr(SCL) | SDA and SCL rise time                          |                                             | 1000 | 20+<br>0.1Cb(2)                         | 300  | ns   |
| tf(SDA)<br>tf(SCL) | SDA and SCL fall time                          |                                             | 300  | 20+ 0.1C<br>(2)<br>b                    | 300  |      |
| th(ST)             | START condition hold time                      | 4                                           |      | 0.6                                     |      | μs   |
| tsu(SR)            | Repeated START condition setup time            | 4.7                                         |      | 0.6                                     |      |      |
| tsu(SP)            | STOP condition setup time                      | 4                                           |      | 0.6                                     |      |      |
| tw(SP:SR)          | Bus free time between STOP and START condition | 4.7                                         |      | 1.3                                     |      |      |

Figure 4: I2C slave timing diagram



Measurement points are done at  $0.2 \cdot V_{dd\_IO}$  and  $0.8 \cdot V_{dd\_IO}$ , for both ports.

## 2.4 Absolute maximum ratings

Stress above those listed as “Absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 7: Absolute maximum ratings

| Symbol           | Ratings                            | Maximum value       | Unit |
|------------------|------------------------------------|---------------------|------|
| Vdd              | Supply voltage                     | -0.3 to 4.8         | V    |
| Vdd_IO           | I/O pins supply voltage            | -0.3 to 4.8         | V    |
| Vin              | Input voltage on any control pin   | -0.3 to Vdd_IO +0.3 | V    |
| P                | Overpressure                       | 2                   | MPa  |
| T <sub>STG</sub> | Storage temperature range          | -40 to +125         | °C   |
| ESD              | Electrostatic discharge protection | 2 (HBM)             | kV   |

*Note: Supply voltage on any pin should never exceed 4.8 V.*

|                                                                                    |                                                                                                                      |
|------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------|
|   | This device is sensitive to mechanical shock, improper handling can cause permanent damage to the part.              |
|  | This device is sensitive to electrostatic discharge (ESD), improper handling can cause permanent damage to the part. |

## 3 Functionality

The LPS35HW is a high resolution, digital output pressure sensor packaged in an HLGA full- mold package. The complete device includes a sensing element based on a piezoresistive Wheatstone bridge approach, and an IC interface which communicates a digital signal from the sensing element to the application.

### 3.1 Sensing element

An ST proprietary process is used to obtain a silicon membrane for MEMS pressure sensors. When pressure is applied, the membrane deflection induces an imbalance in the Wheatstone bridge piezoresistances whose output signal is converted by the IC interface.

### 3.2 IC interface

The complete measurement chain is composed of a low-noise amplifier which converts the resistance unbalance of the MEMS sensors (pressure and temperature) into an analog voltage using an analog-to-digital converter. The pressure and temperature data may be accessed through an I<sup>2</sup>C/SPI interface thus making the device particularly suitable for direct interfacing with a microcontroller. The LPS35HW features a Data-Ready signal which indicates when a new set of measured pressure and temperature data are available, thus simplifying data synchronization in the digital system that uses the device.

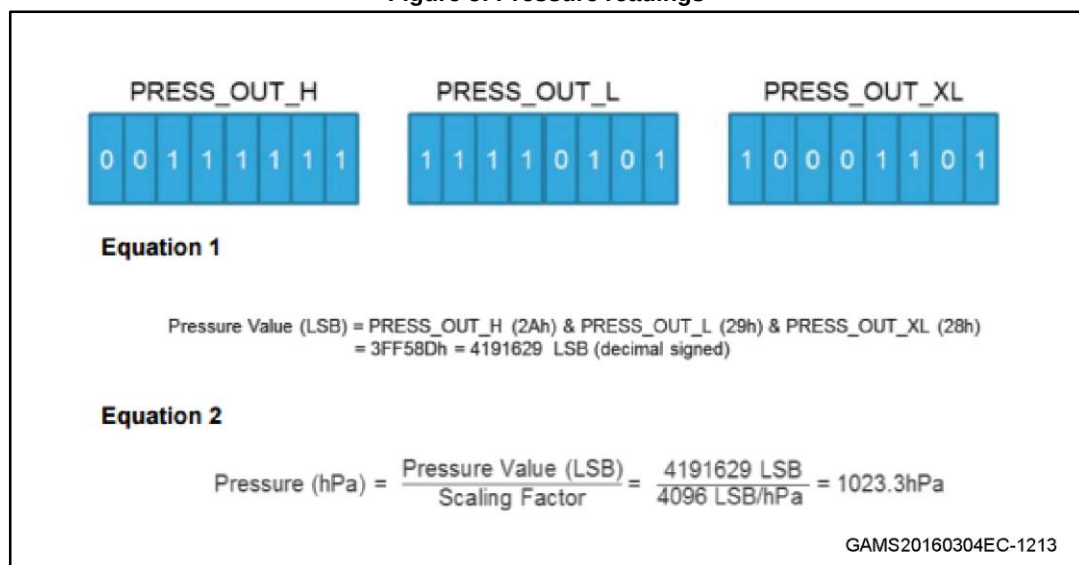
### 3.3 Factory calibration

The trimming values are stored inside the device in a non-volatile structure. When the device is turned on, the trimming parameters are downloaded into the registers to be employed during the normal operation which allows the device to be used without requiring any further calibration.

### 3.4 How to interpret pressure readings

The pressure data are stored 3 registers: PRESS\_OUT\_H (2Ah), PRESS\_OUT\_L (29h), and PRESS\_OUT\_XL (28h). The value is expressed as 2's complement. To obtain the pressure in hPa, take the two's complement of the complete word and then divide by 4096LSB/hPa.

Figure 5: Pressure readings



## 4 FIFO

The LPS35HW embeds a 32-slot of 40-bit data FIFO to store the pressure and temperature output values. This allows consistent power saving for the system, since the host processor does not need to continuously poll data from the sensor, but it can wake up only when needed and burst the significant data out from the FIFO. This buffer can work according to seven different modes: Bypass mode, FIFO mode, Stream mode, Dynamic-Stream mode, Stream-to-FIFO mode, Bypass-to-Stream and Bypass-to-FIFO mode. The FIFO buffer is enabled when the FIFO\_EN bit in [CTRL\\_REG2 \(11h\)](#) is set to '1' and each mode is selected by the FIFO\_MODE[2:0] bits in [FIFO\\_CTRL \(14h\)](#). Programmable FIFO threshold status, FIFO overrun events and the number of unread samples stored are available in the [FIFO\\_STATUS \(26h\)](#) register and can be set to generate dedicated interrupts on the INT\_DRDY pad using the [CTRL\\_REG3 \(12h\)](#) register.

FIFO\_STATUS(FTH\_FIFO) goes to '1' when the number of unread samples (FIFO\_STATUS(FSS5:0)) is greater than or equal to WTM[4:0] in [FIFO\\_CTRL \(14h\)](#). If FIFO\_CTRL(WTM4:0) is equal to 0, FIFO\_STATUS(FTH\_FIFO) goes to '0'.

FIFO\_STATUS(OVRN) is equal to '1' if a FIFO slot is overwritten. FIFO\_STATUS(FSS5:0) contains stored data levels of unread samples; when FSS[5:0] is equal to '000000' FIFO is empty, when FSS[5:0] is equal to '100000' FIFO is full and the unread samples are 32.

To guarantee the switching into and out of FIFO mode, discard the first sample acquired.

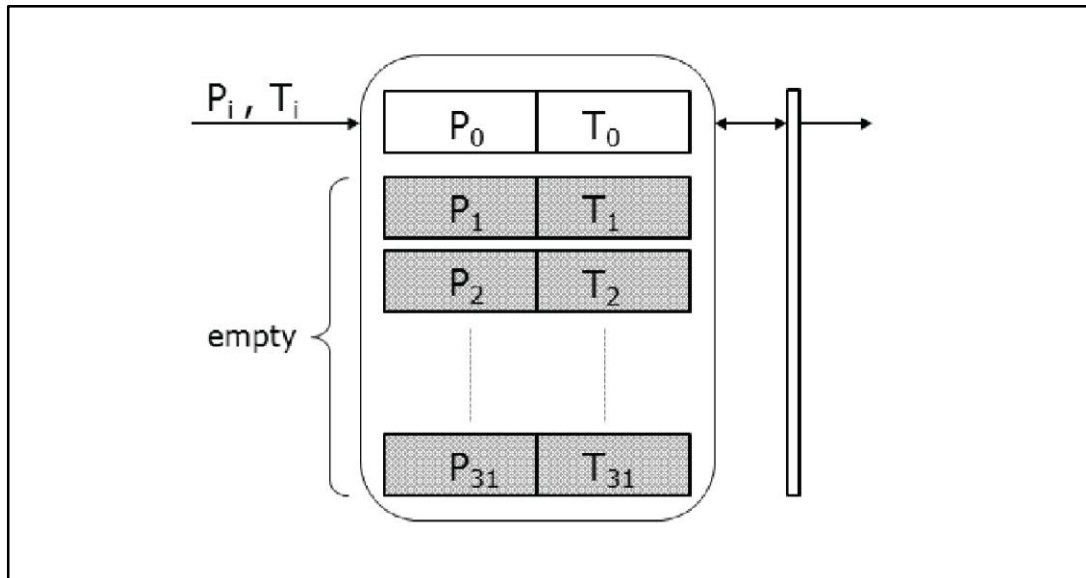
### 4.1 Bypass mode

In Bypass mode (FIFO\_CTRL(FMODE2:0)=000), the FIFO is not operational and it remains empty.

Bypass mode is also used to reset the FIFO when in FIFO mode.

As described in the next figure, for each channel only the first address is used. When new data is available, the older data is overwritten.

Figure 6: Bypass mode



## 4.2 FIFO mode

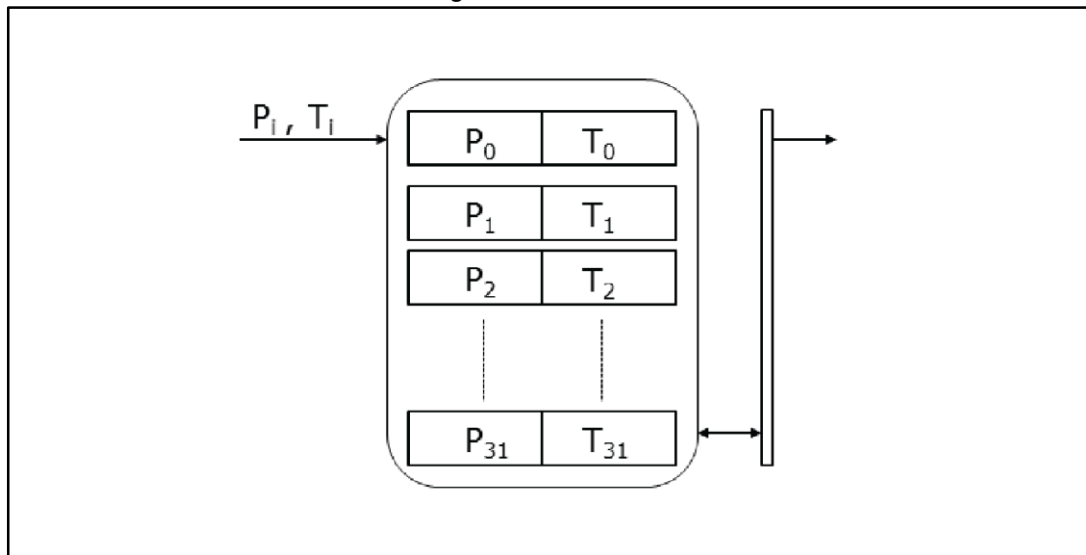
In FIFO mode ( $\text{FIFO\_CTRL}(\text{FMODE2:0}) = 001$ ) data from the output [PRESS\\_OUT\\_H\(2Ah\)](#), [PRESS\\_OUT\\_L\(29h\)](#), [PRESS\\_OUT\\_XL\(28h\)](#) and [TEMP\\_OUT\\_H\(2Ch\)](#), [TEMP\\_OUT\\_L\(2Bh\)](#) are stored in the FIFO until it is overwritten.

To reset FIFO content, Bypass mode the value '000' must be written in  $\text{FIFO\_CTRL}(\text{FMODE2:0})$ . After this reset command it is possible to restart FIFO mode writing the value '001' in  $\text{FIFO\_CTRL}(\text{FMODE2:0})$ .

FIFO buffer memorizes 32 levels of data but the depth of the FIFO can be resized by setting the  $\text{CTRL2}(\text{STOP\_ON\_FTH})$  bit. If the  $\text{STOP\_ON\_FTH}$  bit is set to '1', FIFO depth is limited to  $\text{FIFO\_CTRL}(\text{WTM4:0}) + 1$  data.

A FIFO threshold interrupt can be enabled ( $\text{F\_OVR}$  bit in  $\text{CTRL3}(12\text{h})$  in order to be raised when the FIFO is filled to the level specified by the  $\text{WTM4:0}$  bits of  $\text{FIFO\_CTRL}(14\text{h})$ . When a FIFO threshold interrupt occurs, the first data has been overwritten and the FIFO stops collecting data from the input pressure and temperature.

Figure 7: FIFO mode



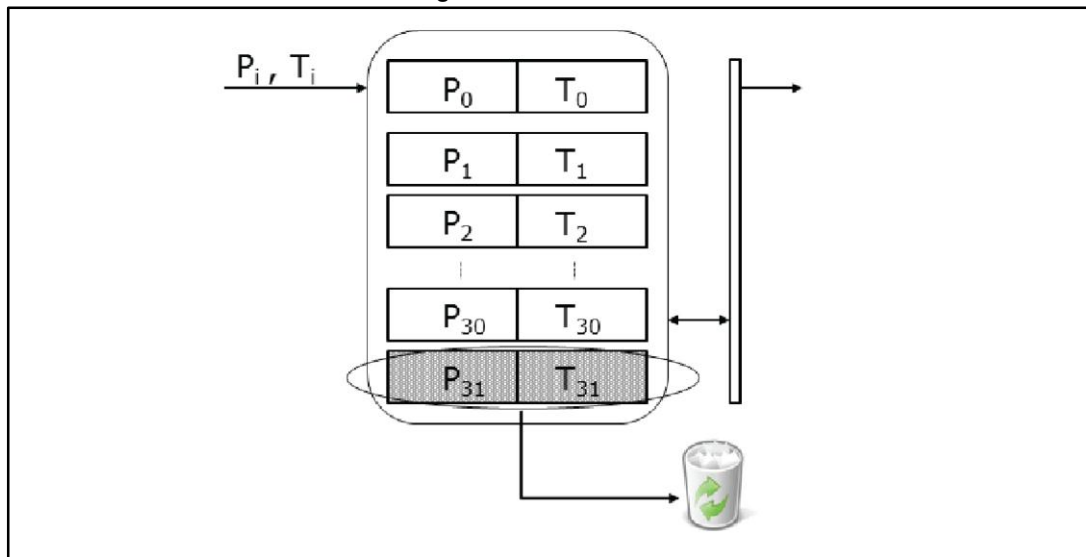
## 4.3 Stream mode

Stream mode ( $\text{FIFO\_CTRL}(\text{FMODE2:0}) = 010$ ) provides continuous FIFO update: as new data arrive, the older is discarded.

Once the entire FIFO has been read, the last data read still remains in the FIFO and hence once a new sample is acquired, the  $\text{FIFO\_STATUS}(\text{FSS5:0})$  value rises from 0 to 2.

An overrun interrupt can be enabled,  $\text{CTRL3}(\text{F\_OVR}) = '1'$ , in order to inform when the FIFO is full and eventually read its content all at once. If an overrun occurs, the oldest sample in FIFO is overwritten, so if the FIFO was empty, the lost sample has already been read.

Figure 8: Stream mode



In the latter case reading all FIFO content before an overrun interrupt has occurred, the first data read is equal to the last already read in the previous burst, so the number of new data available in FIFO depends on the previous reading.

#### 4.4 Dynamic-Stream mode

In Dynamic-Stream mode (`FIFO_CTRL(FMODE2:0) = 110`) after emptying the FIFO, the first new sample that arrives becomes the first to be read in a subsequent read burst. In this way the number of new data available in FIFO does not depend on the previous reading.

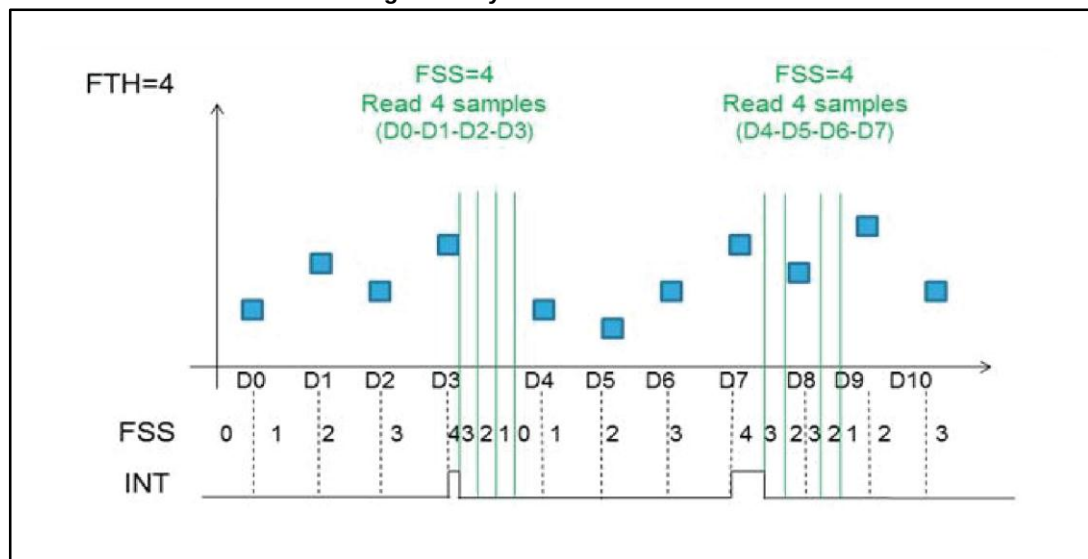
In Dynamic-Stream mode `FIFO_STATUS(FSS5:0)` is the number of new pressure and temperature samples available in the FIFO buffer.

Stream Mode is intended to be used reading all 32 samples of FIFO within an ODR after receiving an overrun signal.

Dynamic-Stream is intended to be used to read `FIFO_STATUS(FSS5:0)` samples when it is not possible to guarantee reading data within an ODR.

Also, a FIFO threshold interrupt on the `INT_DRDY` pad through `CTRL3(F_FTH)` can be enabled in order to read data from the FIFO and leave free memory slots for incoming data.

Figure 9: Dynamic-Stream mode



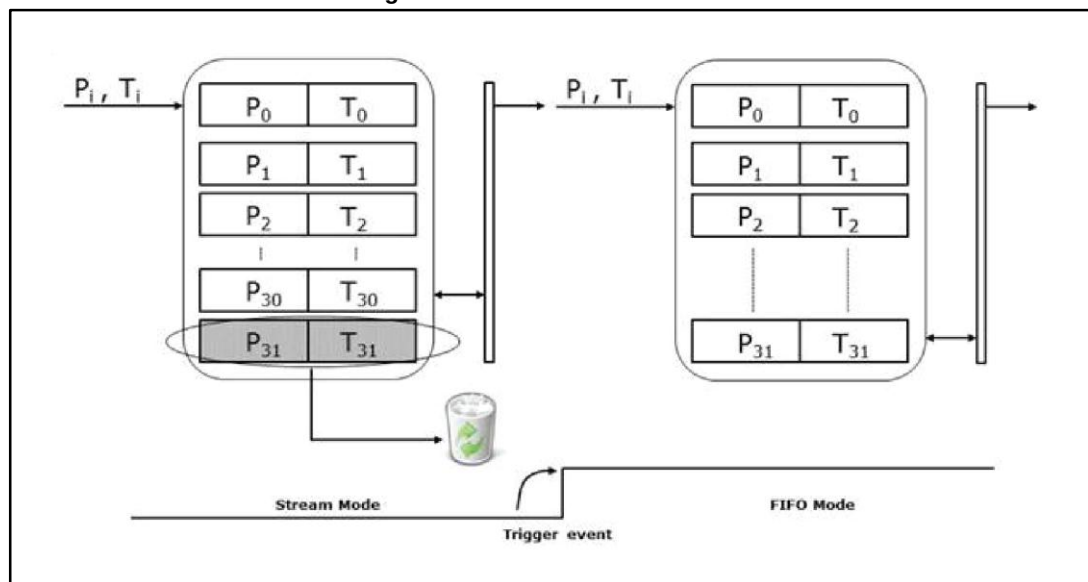
## 4.5 Stream-to-FIFO mode

In Stream-to-FIFO mode (FIFO\_CTRL(FMODE2:0) = 011), FIFO behavior changes according to the INT\_SOURCE(IA) bit. When INT\_SOURCE(IA) bit is equal to '1', FIFO operates in FIFO mode. When the INT\_SOURCE(IA) bit is equal to '0', FIFO operates in Stream mode.

An interrupt generator can be set to the desired configuration through [INTERRUPT\\_CFG\(0Bh\)](#).

The INTERRUPT\_CFG(LIR) bit should be set to '1' in order to have latched interrupt.

Figure 10: Stream-to-FIFO mode

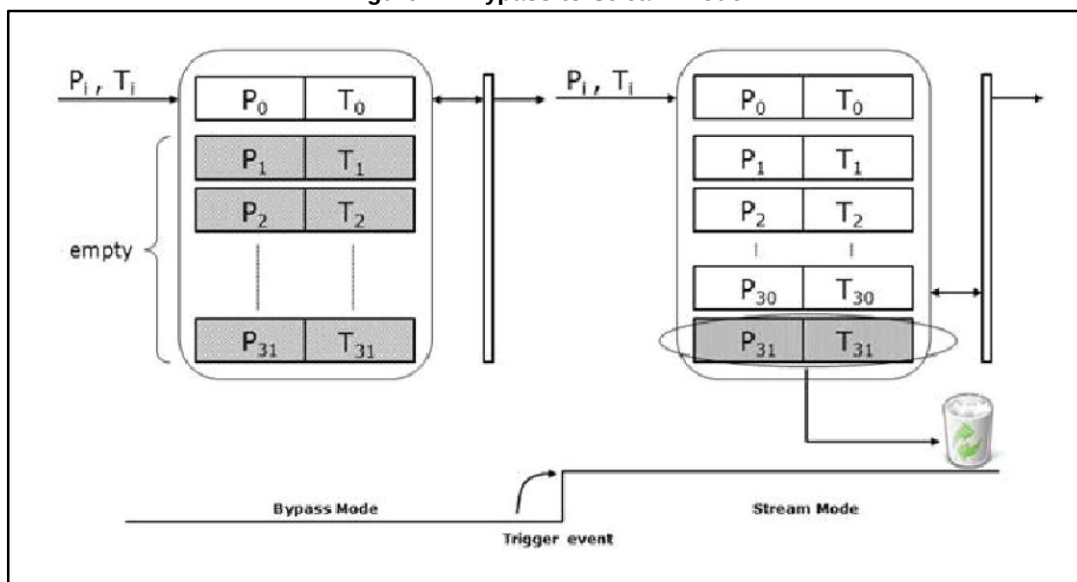


## 4.6 Bypass-to-Stream mode

In Bypass-to-Stream mode (FIFO\_CTRL(FMODE2:0) = '100'), data measurement storage inside FIFO operates in Stream mode when INT\_SOURCE(IA) is equal to '1', otherwise FIFO content is reset (Bypass mode). An interrupt generator can be set to the desired configuration through [INTERRUPT\\_CFG\(0Bh\)](#).

The INTERRUPT\_CFG(LIR) bit should be set to '1' in order to have latched interrupt.

Figure 11: Bypass-to-Stream mode

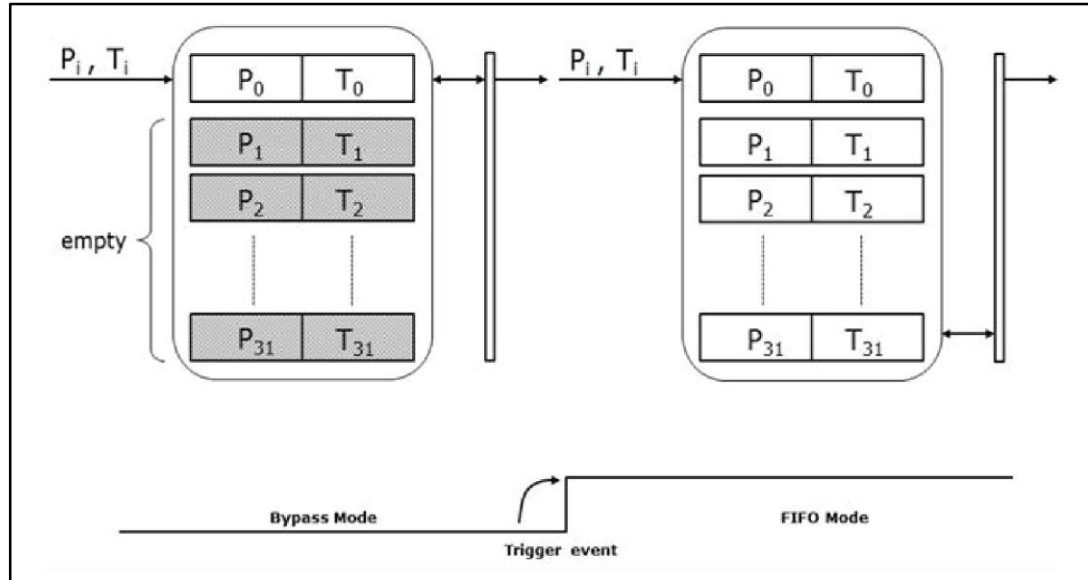


## 4.7 Bypass-to-FIFO mode

In Bypass-to-FIFO mode (FIFO\_CTRL(FMODE2:0) = '111'), data measurement storage inside FIFO operates in FIFO mode when INT\_SOURCE(IA) is equal to '1', otherwise FIFO content is reset (Bypass mode). An interrupt generator can be set to the desired configuration through [INTERRUPT\\_CFG\(0Bh\)](#).

The INTERRUPT\_CFG (LIR) bit should be set to '1' in order to have latched interrupt.

Figure 12: Bypass-to-FIFO mode



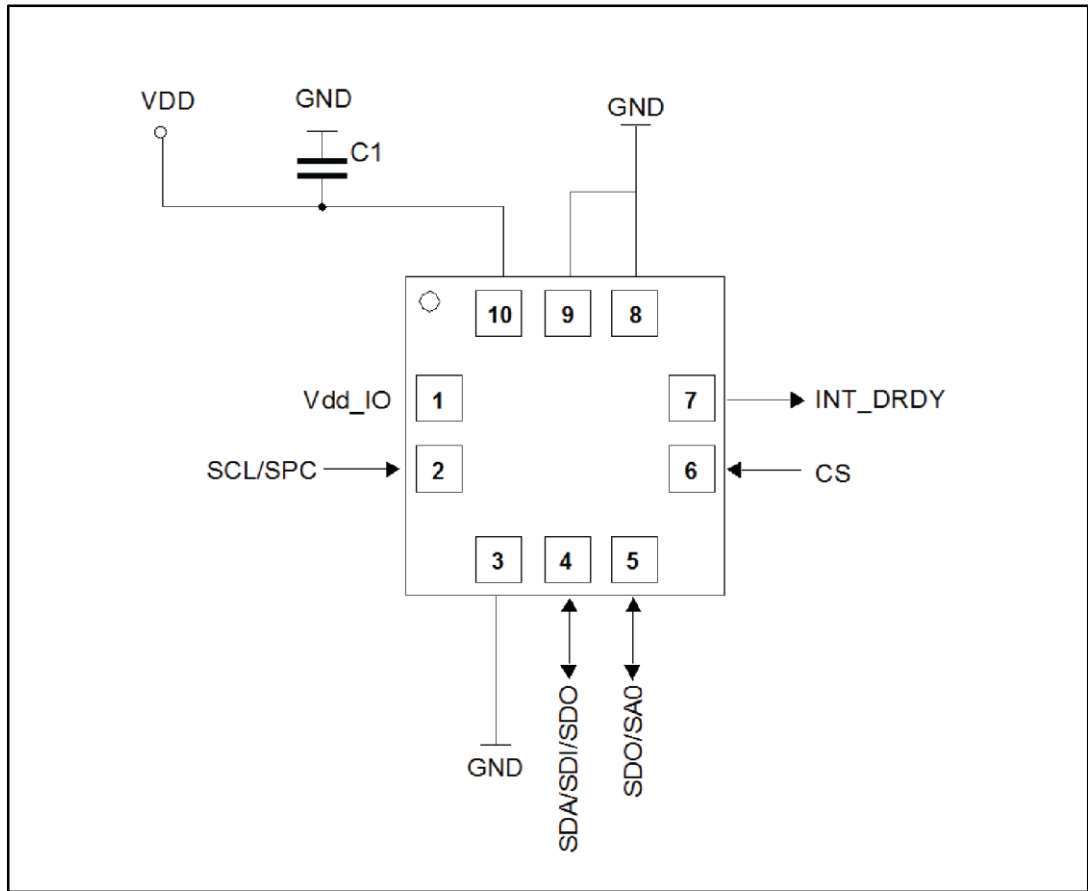
## 4.8 Retrieving data from FIFO

FIFO data is read through [PRESS\\_OUT\\_H\(2Ah\)](#), [PRESS\\_OUT\\_L\(29h\)](#), [PRESS\\_OUT\\_XL\(28h\)](#) and [TEMP\\_OUT\\_H\(2Ch\)](#), [TEMP\\_OUT\\_L\(2Bh\)](#) registers.

Each time data is read from the FIFO, the oldest data are placed in the PRESS\_OUT\_H(2Ah), PRESS\_OUT\_L(29h), PRESS\_OUT\_XL(28h), TEMP\_OUT\_H(2Ch) and TEMP\_OUT\_L(2Bh) registers and both single-read and read-burst operations can be used. The reading address is automatically updated by the device and it rolls back to 28h when register 2Ch is reached. In order to read all FIFO levels in a multiple byte reading, 160 bytes (5 output registers by 32 levels) must be read.

## 5 Application hints

Figure 13: LPS35HW electrical connections (top view)



The device power supply must be provided through the VDD line; power supply decoupling capacitor C1 (100 nF) must be placed as near as possible to the supply pads of the device. Depending on the application, an additional capacitor of 4.7  $\mu$ F could be placed on VDD line. The functionality of the device and the measured data outputs are selectable and accessible through the I<sup>2</sup>C/SPI interface. When using the I<sup>2</sup>C, CS must be tied to Vdd\_IO. All the voltage and ground supplies must be present at the same time to have proper behavior of the IC (refer to [Figure 13: "LPS35HW electrical connections \(top view\)"](#)). It is possible to remove VDD while maintaining Vdd\_IO without blocking the communication bus, in this condition the measurement chain is powered off.

## 5.1 Soldering information

The HLGA package is compliant with the ECOPACK® standard and it is qualified for soldering heat resistance according to JEDEC J-STD-020.

## 6 Digital interfaces

### 6.1 IC serial interface

The registers embedded in the LPS35HW may be accessed through both the I<sup>2</sup>C and SPI serial interfaces. The latter may be SW configured to operate either in 3-wire or 4-wire interface mode. The serial interfaces are mapped onto the same pads. To select/exploit the I<sup>2</sup>C interface, the CS line must be tied high (i.e. connected to Vdd\_IO).

**Table 8: Serial interface pin description**

| Pin name           | Pin description                                                                                                                                                    |
|--------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CS                 | SPI enable<br>I <sup>2</sup> C/SPI mode selection (1: SPI idle mode /I <sup>2</sup> Ccommunication enabled; 0: SPI communication mode / I <sup>2</sup> C disabled) |
| SCL/SPC            | I <sup>2</sup> C serial clock (SCL)<br>SPI serial port clock (SPC)                                                                                                 |
| SDA SDI<br>SDI/SDO | I <sup>2</sup> C serial data (SDA)<br>4-wire SPI serial data input (SDI)<br>3-wire serial data input /output (SDI/SDO)                                             |
| SDO<br>SA0         | SPI serial data output (SDO)<br>I <sup>2</sup> C less significant bit of the device address (SA0)                                                                  |

### 6.2 I<sup>2</sup>C serial interface

The LPS35HW I<sup>2</sup>C is a bus slave. The I<sup>2</sup>C is employed to write data into registers whose content can also be read back.

The relevant I<sup>2</sup>C terminology is given in [Table 9: "I<sup>2</sup>C terminology"](#).

**Table 9: I<sup>2</sup>C terminology**

| Term        | Description                                                                              |
|-------------|------------------------------------------------------------------------------------------|
| Transmitter | The device which sends data to the bus                                                   |
| Receiver    | The device which receives data from the bus                                              |
| Master      | The device which initiates a transfer, generates clock signals and terminates a transfer |
| Slave       | The device addressed by the master                                                       |

There are two signals associated with the I<sup>2</sup>C bus: the serial clock line (SCL) and the serial data line (SDA). The latter is a bi-directional line used for sending and receiving the data to/from the interface. Both lines have to be connected to Vdd\_IO through pull-up resistors. The I<sup>2</sup>C interface is compliant with fast mode (400 kHz) I<sup>2</sup>C standards as well as with the normal mode.

## 6.3 I2C operation

The transaction on the bus is started through a START (ST) signal. A start condition is defined as a HIGH-to-LOW transition on the data line while the SCL line is held HIGH. After this has been transmitted by the master, the bus is considered busy. The next data byte transmitted after the start condition contains the address of the slave in the first 7 bits and the eighth bit tells whether the master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, the device considers itself addressed by the master.

The slave address (SAD) associated to the LPS35HW is 101110xb. The SDO/SA0pad can be used to modify the less significant bit of the device address. If the SA0 pad is connected to voltage supply, LSb is '1' (address 1011101b), otherwise if the SA0 pad is connected to ground, the LSb value is '0' (address 1011100b). This solution permits to connect and address two different LPS35HW devices to the same I2C lines.

Data transfer with acknowledge is mandatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the data line LOW so that it remains stable low during the HIGH period of the acknowledge clock pulse. A receiver which has been addressed is obliged to generate an acknowledge after each byte of data received.

The I2C embedded inside the ASIC behaves like a slave device and the following protocol must be adhered to. After the start condition (ST) a slave address is sent, once a slave acknowledge has been returned (SAK), an 8-bit sub-address will be transmitted (SUB): the 7 LSB represent the actual register address while the MSB has no meaning. The IF\_ADD\_INC bit in CTRL2 register (11h) enables sub-address auto increment (IF\_ADD\_INC is '1' by default), so if IF\_ADD\_INC = '1' the SUB (sub-address) will be automatically increased to allow multiple data read/write.

The slave address is completed with a Read/Write bit. If the bit is '1' (Read), a repeated START (SR) condition must be issued after the two sub-address bytes; if the bit is '0' (Write) the master will transmit to the slave with direction unchanged. [Table 10: "SAD+Read/Write patterns"](#) explains how the SAD+read/write bit pattern is composed, listing all the possible configurations.

**Table 10: SAD+Read/Write patterns**

| Command | SAD[6:1] | SAD[0]=SA0 | R/W | SAD+R/W        |
|---------|----------|------------|-----|----------------|
| Read    | 101110   | 0          | 1   | 10111001 (B9h) |
| Write   | 101110   | 0          | 0   | 10111000 (B8h) |
| Read    | 101110   | 1          | 1   | 10111011 (BBh) |
| Write   | 101110   | 1          | 0   | 10111010 (BAh) |

**Table 11: Transfer when master is writing one byte to slave**

|        |    |        |     |     |     |      |     |    |
|--------|----|--------|-----|-----|-----|------|-----|----|
| Master | ST | SAD +W |     | SUB |     | DATA |     | SP |
| Slave  |    |        | SAK |     | SAK |      | SAK |    |

**Table 12: Transfer when master is writing multiple bytes to slave**

|        |    |        |     |     |     |      |     |      |     |    |
|--------|----|--------|-----|-----|-----|------|-----|------|-----|----|
| Master | ST | SAD+ W |     | SUB |     | DATA |     | DATA |     | SP |
| Slave  |    |        | SAK |     | SAK |      | SAK |      | SAK |    |

Table 13: Transfer when master is receiving (reading) one byte of data from slave

|        |    |        |     |     |     |    |        |     |      |      |    |
|--------|----|--------|-----|-----|-----|----|--------|-----|------|------|----|
| Master | ST | SAD+ W |     | SUB |     | SR | SAD+ R |     |      | NMAK | SP |
| Slave  |    |        | SAK |     | SAK |    |        | SAK | DATA |      |    |

Table 14: Transfer when master is receiving (reading) multiple bytes of data from slave

|            |        |           |         |         |         |        |           |         |          |         |          |         |          |          |        |
|------------|--------|-----------|---------|---------|---------|--------|-----------|---------|----------|---------|----------|---------|----------|----------|--------|
| Mast<br>er | S<br>T | SAD+<br>W |         | SU<br>B |         | S<br>R | SAD+<br>R |         |          | MA<br>K |          | MA<br>K |          | NMA<br>K | S<br>P |
| Slave      |        |           | SA<br>K |         | SA<br>K |        |           | SA<br>K | DAT<br>A |         | DAT<br>A |         | DAT<br>A |          |        |

Data are transmitted in byte format (DATA). Each data transfer contains 8 bits. The number of bytes transferred per transfer is unlimited. Data is transferred with the most significant bit (MSb) first. If a receiver can't receive another complete byte of data until it has performed some other functions, it can hold the clock line, SCL LOW to force the transmitter into a wait state. Data transfer only continues when the receiver is ready for another byte and releases the data line. If a slave receiver does not acknowledge the slave address (i.e. it is not able to receive because it is performing some real-time function) the data line must be kept HIGH by the slave. The master can then abort the transfer. A LOW-to-HIGH transition on the SDA line while the SCL line is HIGH is defined as a STOP condition. Each data transfer must be terminated by the generation of a STOP (SP) condition.

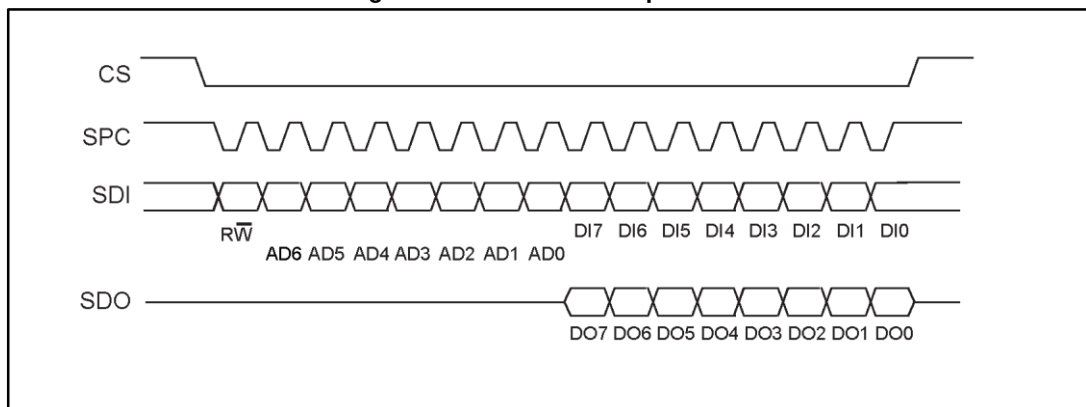
In order to read multiple bytes incrementing the register address, it is necessary to assert the most significant bit of the sub-address field. In other words, SUB(7) must be equal to 1 while SUB(6-0) represents the address of the first register to be read.

In the presented communication format MAK is Master acknowledge and NMAK is no master acknowledge.

## 6.4 SPI bus interface

The LPS35HW SPI is a bus slave. The SPI allows writing to and reading from the registers of the device. The serial interface interacts with the outside world with 4 wires: CS, SPC, SDI and SDO.

Figure 14: Read and write protocol



**CS** is the serial port enable and it is controlled by the SPI master. It goes low at the start of the transmission and returns to high at the end. **SPC** is the serial port clock and it is controlled by the SPI master. It is stopped high when **CS** is high (no transmission). **SDI** and **SDO** are respectively the serial port data input and output. Those lines are driven at the falling edge of SPC and should be captured at the rising edge of SPC. Both the read

register and write register commands are completed in 16 clock pulses or in multiples of 8 in the case of multiple read/write bytes. Bit duration is the time between two falling edges of SPC. The first bit (bit 0) starts at the first falling edge of SPC after the falling edge of CS while the last bit (bit 15, bit 23,...) starts at the last falling edge of SPC just before the rising edge of CS. bit0: RW bit. When 0, the data DI(7:0) is written into the device. When 1, the data DO(7:0) from the device is read. In the latter case, the chip will drive SDO at the start of bit 8.

**bit1-7:** address AD(6:0). This is the address field of the indexed register.

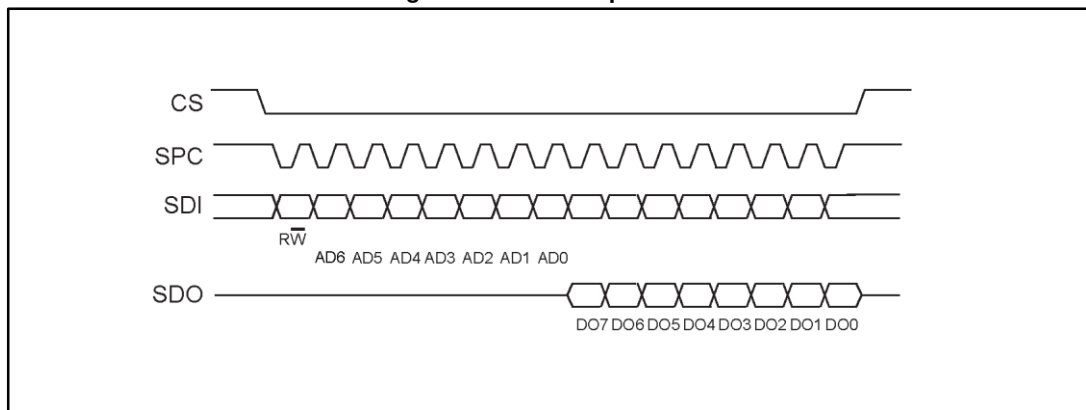
**bit8-15:** data DI(7:0) (write mode). This is the data that is written into the device (MSb first).

**bit8-15:** data DO(7:0) (read mode). This is the data that is read from the device (MSb first). In multiple read/write commands further blocks of 8 clock periods are added. When the IF\_ADD\_INC bit is 0, the address used to read/write data remains the same for every block. When the IF\_ADD\_INC bit is 1, the address used to read/write data is incremented at every block.

The function and the behavior of SDI and SDO remain unchanged.

## 6.5 SPI read

Figure 15: SPI read protocol



The SPI read command is performed with 16 clock pulses. The multiple byte read command is performed by adding blocks of 8 clock pulses to the previous one.

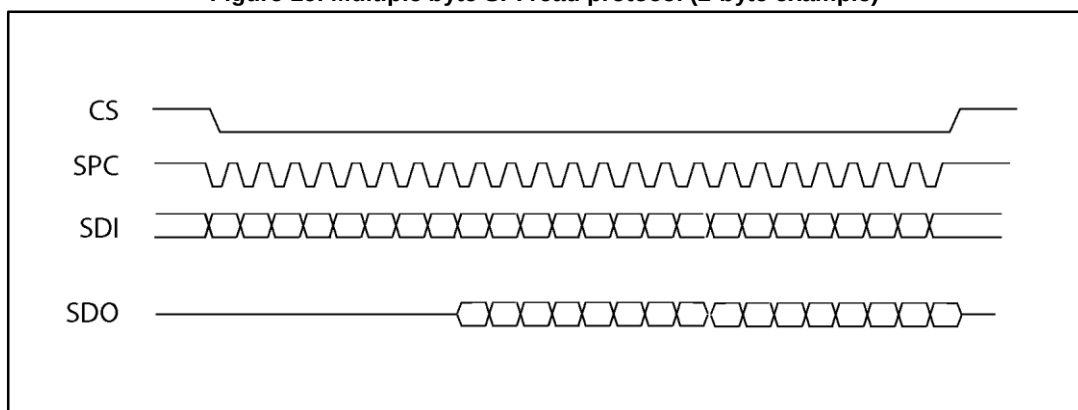
**bit0:** READ bit. The value is 1.

**bit1-7:** address AD(6:0). This is the address field of the indexed register.

**bit8-15:** data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

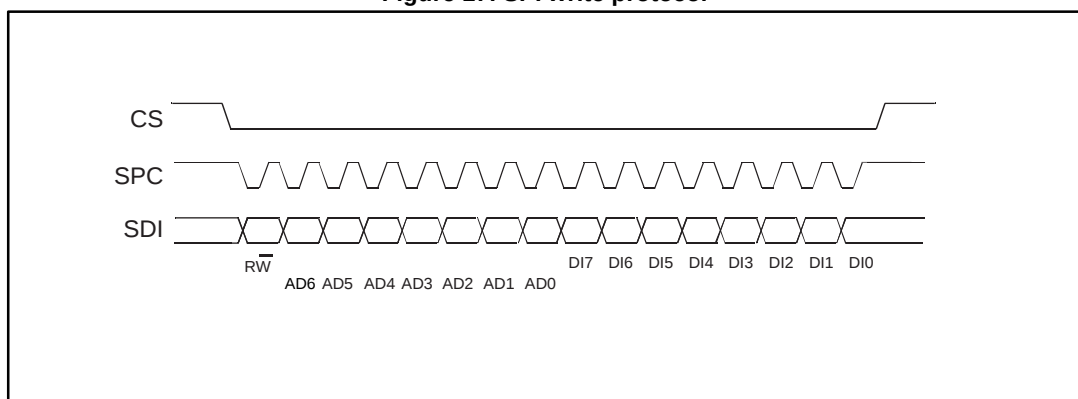
**bit16-...:** data DO(...-8). Further data in multiple byte reads.

Figure 16: Multiple byte SPI read protocol (2-byte example)



## 6.6 SPI write

Figure 17: SPI write protocol

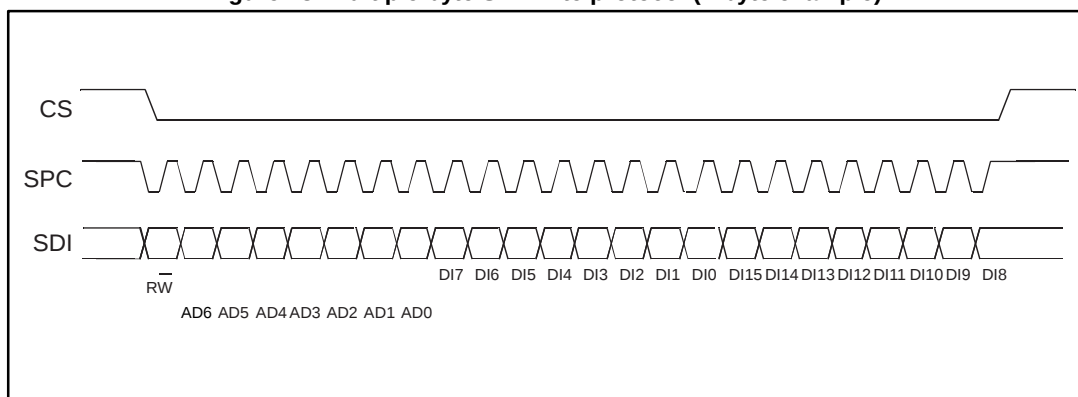


The SPI write command is performed with 16 clock pulses. The multiple byte write command is performed by adding blocks of 8 clock pulses to the previous one. **bit0**: WRITE bit. The value is 0. **bit1-7**: address AD(6:0). This is the address field of the indexed register.

**bit8-15**: data DI(7:0) (write mode). This is the data that is written in the device (MSb first).

**bit16-...**: data DI(...-8). Further data in multiple byte writes.

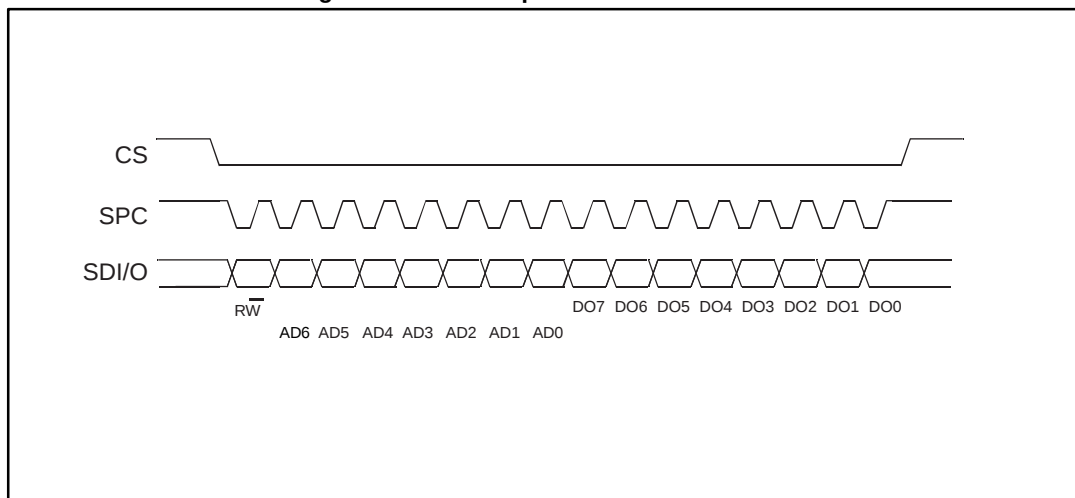
Figure 18: Multiple byte SPI write protocol (2-byte example)



## 6.7 SPI read in 3-wire mode

A 3-wire mode is entered by setting bit SIM to '1' (SPI serial interface mode selection) in CTRL\_REG1.

Figure 19: SPI read protocol in 3-wire mode



The SPI read command is performed with 16 clock pulses:

**bit0:** READ bit. The value is 1.

**bit1-7:** address AD(6:0). This is the address field of the indexed register.

**bit8-15:** data DO(7:0) (read mode). This is the data that is read from the device (MSb first).  
A multiple read command is also available in 3-wire mode.

## 7 Registers address map

[Table 15](#) provides a quick overview of the 8-bit registers embedded in the device.

**Table 15: Registers address map**

| Register name | Type | Register address | Default  | Function and comment |
|---------------|------|------------------|----------|----------------------|
|               |      | Hex              | Binary   |                      |
| Reserved      |      | 00 -0A           | -        | Reserved             |
| INTERRUPT_CFG | R/W  | 0B               | 00000000 |                      |
| THS_P_L       | R/W  | 0C               | 00000000 |                      |
| THS_P_H       | R/W  | 0D               | 00000000 |                      |
| Reserved      | -    | 0E               | -        | Reserved             |
| WHO_AM_I      | R    | 0F               | 10110001 | Who am I             |
| CTRL_REG1     | R/W  | 10               | 00000000 |                      |
| CTRL_REG2     | R/W  | 11               | 00010000 |                      |
| CTRL_REG3     | R/W  | 12               | 00000000 | Interrupt control    |
| Reserved      | -    | 13               | -        | Reserved             |
| FIFO_CTRL     | R/W  | 14               | 00000000 |                      |
| REF_P_XL      | R/W  | 15               | 00000000 |                      |
| REF_P_L       | R/W  | 16               | 00000000 |                      |
| REF_P_H       | R/W  | 17               | 00000000 |                      |
| RPDS_L        | R/W  | 18               | 00000000 |                      |
| RPDS_H        | R/W  | 19               | 00000000 |                      |
| RES_CONF      | R/W  | 1A               | 00000000 |                      |
| Reserved      | -    | 1B- 24           | -        | Reserved             |
| INT_SOURCE    | R    | 25               | -        |                      |
| FIFO_STATUS   | R    | 26               | -        |                      |
| STATUS        | R    | 27               | -        |                      |
| PRESS_OUT_XL  | R    | 28               | -        |                      |
| PRESS_OUT_L   | R    | 29               | -        |                      |
| PRESS_OUT_H   | R    | 2A               | -        |                      |
| TEMP_OUT_L    | R    | 2B               | -        |                      |
| TEMP_OUT_H    | R    | 2C               | -        |                      |
| Reserved      | -    | 2D- 32           | -        | Reserved             |
| LPFP_RES      | R    | 33               | -        |                      |

Registers marked as Reserved must not be changed. Writing to those registers may cause permanent damage to the device.

To guarantee the proper behavior of the device, all register addresses not listed in the above table must not be accessed and the content stored in those registers must not be changed.

The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered up.

## 8 Register description

The device contains a set of registers which are used to control its behavior and to retrieve pressure and temperature data. The register address, made up of 7 bits, is used to identify them and to read/write the data through the serial interface.

### 8.1 INTERRUPT\_CFG (0Bh)

Table 16: INTERRUPT\_CFG (0Bh) register

| 7        | 6         | 5        | 4        | 3       | 2   | 1   | 0   |
|----------|-----------|----------|----------|---------|-----|-----|-----|
| AUTORIFP | RESET_ARP | AUTOZERO | RESET_AZ | DIFF_EN | LIR | PLE | PHE |

|           |                                                                                                                                                                                                                     |
|-----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| AUTORIFP  | AUTORIFP: AutoRifP function enable. Default value: 0. (0: normal mode; 1:AutoRifP enabled)                                                                                                                          |
| RESET_ARP | Reset AutoRifP function. Default value: 0.(0: normal mode; 1: reset AutoRifP function)                                                                                                                              |
| AUTOZERO  | Autozero enable. Default value: 0.<br>(0: normal mode; 1:Autozero enabled)                                                                                                                                          |
| RESET_AZ  | Reset Autozero function. Default value: 0. (0: normal mode; 1: reset Autozero function)                                                                                                                             |
| DIFF_EN   | Interrupt generation enable. Default value: 0<br>(0: interrupt generation disabled; 1: interrupt generation enabled)                                                                                                |
| LIR       | Latch interrupt request to the INT_SOURCE register. Default value: 0. (0: interrupt request not latched; 1: interrupt request latched)                                                                              |
| PLE       | Enable interrupt generation on differential pressure low event. Default value: 0.(0: disable interrupt request; 1: enable interrupt request on measured differential pressure value lower than preset threshold)    |
| PHE       | Enable interrupt generation on differential pressure high event. Default value: 0. (0: disable interrupt request; 1: enable interrupt request on measured differential pressure value higher than preset threshold) |

To generate an interrupt event based on a user defined threshold, DIFF\_EN bit must be set to '1' and the threshold values stored in THS\_P\_L (0Ch) and THS\_P\_H (0Dh).

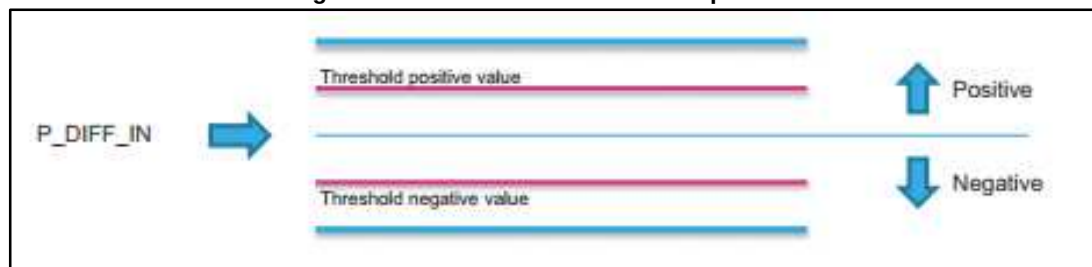
When DIFF\_EN = '1', PHE bit or PLE bit or both bits have to be enabled. PHE and PLE bits enable the interrupt generation on the positive or negative event respectively.

When DIFF\_EN is enabled and AUTOZERO or AUTORIFP is enabled, the defined pressure threshold values in THS\_P (0Ch, 0Dh) is compared with:

$P\_DIFF\_IN = \text{measured pressure} - \text{pressure reference}$

The value of pressure reference is assigned depending on the AUTOZERO and AUTORIFP modes reported in the next two paragraphs.

Figure 20: "Threshold based" interrupt event



If AUTOZERO bit is set to '1', the measured pressure is used as reference on the register REF\_P (15h, 16h and 17h). From now on, the output pressure registers PRESS\_OUT (PRESS\_OUT\_H(2Ah), PRESS\_OUT\_L(29h) and PRESS\_OUT\_XL(28h)) are updated and the same value is also used for the interrupt generation:  $PRESS\_OUT = \text{measured pressure} - REF\_P$

After the first conversion AUTOZERO bit is automatically set to '0'. To return back to normal mode, RESET\_AZ bit has to be set to '1'. This reset also the content of the REF\_P registers. If AUTORIFP bit is set to '1', the measured pressure is used as reference on the register REF\_P (15h, 16h and 17h). The output registers PRESS\_OUT (PRESS\_OUT\_H(2Ah), PRESS\_OUT\_L(29h) and PRESS\_OUT\_XL(28h)) show the difference between the measured pressure and the content of the RPDS registers (18h and 19h):  $PRESS\_OUT = \text{measured pressure} - RPDS * 256$

After the first conversion AUTORIFP bit is automatically set to '0'. To return back to normal mode, RESET\_ARP bit has to be set to '1'.

## 8.2 THS\_P\_L (0Ch)

Least significant bits of the threshold value for pressure interrupt generation.

## 8.3 THS\_P\_H (0Dh)

Most significant bits of the threshold value for pressure interrupt generation.

| 7     | 6     | 5     | 4     | 3     | 2     | 1    | 0    |
|-------|-------|-------|-------|-------|-------|------|------|
| THS15 | THS14 | THS13 | THS12 | THS11 | THS10 | THS9 | THS8 |

|           |                                                                                                                                                   |
|-----------|---------------------------------------------------------------------------------------------------------------------------------------------------|
| THS[15:8] | This register contains the high part of threshold value for pressure interrupt generation. Refer to <a href="#">Section 10.2: "THS_P_L (0Ch)"</a> |
|-----------|---------------------------------------------------------------------------------------------------------------------------------------------------|

## 8.4 WHO\_AM\_I

Device Who am I

Table 17: WHO\_AM\_I register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |

## 8.5 CTRL\_REG1 (10h)

Control register 1

Table 18: CTRL\_REG1 (10h) register

| 7              | 6    | 5    | 4    | 3       | 2        | 1   | 0   |
|----------------|------|------|------|---------|----------|-----|-----|
| 0 <sup>a</sup> | ODR2 | ODR1 | ODR0 | EN_LPFP | LPFP_CFG | BDU | SIM |

|                  |                                                                                                                                  |
|------------------|----------------------------------------------------------------------------------------------------------------------------------|
| ODR [2:0]        | Output data rate selection. Default value: 000 Refer to <a href="#">Table 19: "Output data rate bit configurations"</a> .        |
| EN_LPFP          | Enable low-pass filter on pressure data. Default value: 0 (0: Low-pass filter disabled; 1: Low-pass filter enabled)              |
| LPFP_CFG         | LPF_CFG: Low-pass configuration register. Default value: 0 Refer to <a href="#">Table 20: "Low-pass filter configurations"</a> . |
| BDU <sup>b</sup> | Block data update. Default value: 0 (0: continuous update; 1: output registers not updated until MSB and LSB have been read)     |
| SIM              | SPI Serial Interface Mode selection. Default value: 0 (0: 4-wire interface; 1: 3-wire interface)                                 |

Table 19: Output data rate bit configurations

| ODR2 | ODR1 | ODR0 | Pressure (Hz)                      | Temperature (Hz) |
|------|------|------|------------------------------------|------------------|
| 0    | 0    | 0    | Power down / One shot mode enabled |                  |
| 0    | 0    | 1    | 1 Hz                               | 1 Hz             |
| 0    | 1    | 0    | 10 Hz                              | 10 Hz            |
| 0    | 1    | 1    | 25 Hz                              | 25 Hz            |
| 1    | 0    | 0    | 50 Hz                              | 50 Hz            |
| 1    | 0    | 1    | 75 Hz                              | 75 Hz            |

When ODR bits are set to '000' the device is in **Power down mode**. When the device is in power-down mode, almost all internal blocks of the device are switched off to minimize power consumption. I<sup>2</sup>C interface is still active to allow communication with the device. The configuration registers content is preserved and output data registers are not updated, therefore keeping the last data sampled in memory before going into power-down mode.

If ONE\_SHOT bit in CTRL\_REG2(11h) is set to '1', **One-shot mode** is triggered and a new acquisition starts when it is required. This enabling is effective only if the device was previously in power-down mode (ODR bits set to '000'). Once the acquisition is completed and the output registers updated, the device automatically enters in power down mode. ONE\_SHOT bit self-clears itself.

When ODR bits are set to a value different than '000', the device is in **Continuous mode** and automatically acquires a set of data (pressure and temperature) at the frequency selected through ODR[2,0] bits.

<sup>a</sup> This bit must be set to '0' for proper operation of the device

<sup>b</sup> To guarantee the correct behavior of BDU feature, the PRESS\_OUT\_H (2Ah) must be the last address read.

Once the additional low pass filter has been enable through the EN\_LPFP bit, it is possible to configure the device bandwidth acting on LPFP\_CFG bit. Refer to [Table 20: "Low-pass filter configurations"](#).

Table 20: Low-pass filter configurations

| EN_LPFP | LPFP_CFG | Additional low pass filter status | Device bandwidth |
|---------|----------|-----------------------------------|------------------|
| 0       | x        | Disabled                          | ODR/2            |
| 1       | 0        | Enabled                           | ODR/9            |
| 1       | 1        | Enabled                           | ODR/20           |

The **BDU** bit is used to inhibit the update of the output registers between the reading of upper and lower register parts. In default mode (BDU = '0'), the lower and upper register parts are updated continuously. When the BDU is activated (BDU = '1'), the content of the output registers is not updated until PRESS\_OUT\_H is read, avoiding the reading of values related to different samples.

## 8.6 CTRL\_REG2 (11h)

Control register 2

| 7    | 6       | 5           | 4          | 3       | 2       | 1              | 0        |
|------|---------|-------------|------------|---------|---------|----------------|----------|
| BOOT | FIFO_EN | STOP_ON_FTH | IF_ADD_INC | I2C_DIS | SWRESET | 0 <sup>a</sup> | ONE_SHOT |

|             |                                                                                                                                                          |
|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------|
| BOOT        | Reboot memory content. Default value: 0.<br>(0: normal mode; 1: reboot memory content). The bit is self-cleared when the BOOT is completed.              |
| FIFO_EN     | FIFO enable. Default value: 0.(0: disable; 1: enable)                                                                                                    |
| STOP_ON_FTH | Stop on FIFO threshold. Enable FIFO watermark level use. Default value 0 (0: disable; 1: enable)                                                         |
| IF_ADD_INC  | Register address automatically incremented during a multiple byte access with a serial interface (I2C or SPI). Default value 1.<br>(0: disable; 1enable) |
| I2C_DIS     | Disable I2C interface. Default value 0. (0: I2C enabled;1: I2C disabled)                                                                                 |
| SWRESET     | Software reset. Default value: 0.<br>(0: normal mode; 1: software reset).<br>The bit is self-cleared when the reset is completed.                        |
| ONE_SHOT    | One-shot enable. Default value: 0.<br>(0: idle mode; 1: anew dataset is acquired)                                                                        |

The **BOOT** bit is used to refresh the content of the internal registers stored in the Flash memory block. At device power-up the content of the Flash memory block is transferred to the internal registers related to the trimming functions to allow correct behavior of the device itself. If for any reason the content of the trimming registers is modified, it is sufficient to use this bit to restore the correct values. When the BOOT bit is set to '1', the content of the internal Flash is copied inside the corresponding internal registers and is used to calibrate the device. These values are factory trimmed and they are different for

<sup>a</sup> This bit must be set to '0' for proper operation of the device.

every device. They allow correct behavior of the device and normally they should not be changed. At the end of the boot process the BOOT bit is set again to '0' by hardware. The BOOT bit takes effect after one ODR clock cycle.

**SWRESET** is the software reset bit. The following device registers (INTERRUPT\_CFG, THS\_P\_L, THS\_P\_H, CTRL\_REG1, CTRL\_REG2, CTRL\_REG3, FIFO\_CTRL, RIF\_P\_XL, RIF\_P\_L, RIF\_P\_H) are reset to the default value if the SWRESET bit is set to '1'. SWRESET bit comes back to '0' by hardware.

The **ONE\_SHOT** bit is used to start a new conversion when the ODR[2,0] bits in CTRL\_REG1(10h) are set to '000'. Writing a '1' in ONE\_SHOT triggers a single measurement of pressure and temperature. Once the measurement is done, the ONE\_SHOT bit will self-clear, the new data are available in the output registers, and the STATUS\_REG bits are updated.

## 8.7 CTRL\_REG3 (12h)

Control register 3 - INT\_DRDY pin control register

**Table 21: CTRL\_REG3 (12h) register**

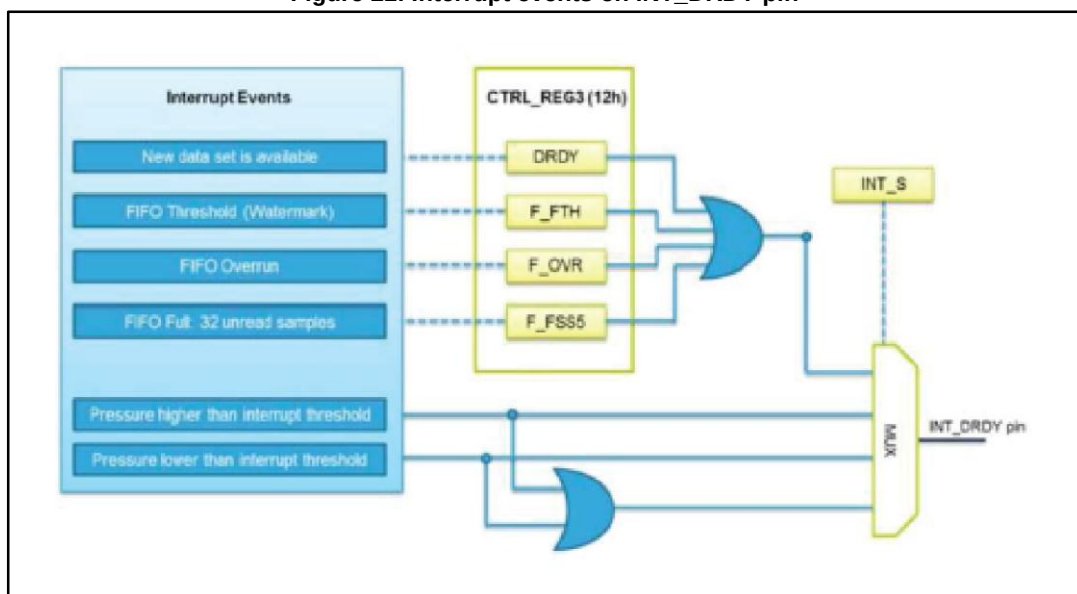
| 7       | 6     | 5      | 4     | 3     | 2    | 1      | 0      |
|---------|-------|--------|-------|-------|------|--------|--------|
| INT_H_L | PP_OD | F_FSS5 | F_FTH | F_OVR | DRDY | INT_S2 | INT_S1 |

|            |                                                                                                                              |
|------------|------------------------------------------------------------------------------------------------------------------------------|
| INT_H_L    | Interrupt active-high/low. Default value: 0.(0: active high; 1: active low)                                                  |
| PP_OD      | Push-pull/open drain selection on interrupt pads. Default value: 0. (0: push-pull; 1: open drain)                            |
| F_FSS5     | FIFO full flag on INT_DRDY pin. Default value: 0. (0: Disable; 1: Enable)                                                    |
| F_FTH      | FIFO threshold (Watermark) status on INT_DRDY pin. Default value: 0. (0: Disable; 1: Enable)                                 |
| F_OVR      | FIFO overrun interrupt on INT_DRDY pin. Default value: 0. (0: Disable; 1: Enable)                                            |
| DRDY       | Data-ready signal on INT_DRDY pin. Default value: 0. (0: Disable; 1: Enable)                                                 |
| INT_S[2:1] | Data signal on INT_DRDY pin control bits. Default value: 00. Refer to <a href="#">Table 22: "Interrupt configurations"</a> . |

**Table 22: Interrupt configurations**

| INT_S2 | INT_S1 | INT_DRDY pin configuration                                               |
|--------|--------|--------------------------------------------------------------------------|
| 0      | 0      | Data signal (in order of priority: PTH_DRDY or F_FTH or F_OVR or F_FSS5) |
| 0      | 1      | Pressure high (P_high)                                                   |
| 1      | 0      | Pressure low (P_low)                                                     |
| 1      | 1      | Pressure low OR high                                                     |

Figure 21: Interrupt events on INT\_DRDY pin



## 8.8 FIFO\_CTRL (14h)

FIFO control register

Table 23: CTRL\_REG3 (12h) register

| 7       | 6       | 5       | 4    | 3    | 2    | 1    | 0    |
|---------|---------|---------|------|------|------|------|------|
| F_MODE2 | F_MODE1 | F_MODE0 | WTM4 | WTM3 | WTM2 | WTM1 | WTM0 |

|             |                                                                                                                                                                    |
|-------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| F_MODE[2:0] | FIFO mode selection. Default value: 000.<br>Refer to <a href="#">Table 24: "FIFO mode selection"</a> and <a href="#">Section 6: "FIFO"</a> for additional details. |
| WTM[4:0]    | FIFO watermark level selection.                                                                                                                                    |

Table 24: FIFO mode selection

| F_MODE2 | F_MODE1 | F_MODE0 | FIFO mode selection   |
|---------|---------|---------|-----------------------|
| 0       | 0       | 0       | Bypass mode           |
| 0       | 0       | 1       | FIFO mode             |
| 0       | 1       | 0       | Stream mode           |
| 0       | 1       | 1       | Stream-to-FIFO mode   |
| 1       | 0       | 0       | Bypass-to-Stream mode |
| 1       | 0       | 1       | Reserved              |
| 1       | 1       | 0       | Dynamic-Stream mode   |
| 1       | 1       | 1       | Bypass-to-FIFO mode   |

## 8.9 REF\_P\_XL (15h)

Reference pressure (LSB data)

Table 25: REF\_P\_XL (15h) register

| 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     |
|-------|-------|-------|-------|-------|-------|-------|-------|
| REFL7 | REFL6 | REFL5 | REFL4 | REFL3 | REFL2 | REFL1 | REFL0 |

|           |                                                                      |
|-----------|----------------------------------------------------------------------|
| REFL[7:0] | This register contains the low part of the reference pressure value. |
|-----------|----------------------------------------------------------------------|

The Reference pressure value is a 24-bit data and it is composed of [Section 10.11: "REF\\_P\\_H\\_17h"](#), [Section 10.10: "REF\\_P\\_L\\_16h"](#) and [Section 10.9: "REF\\_P\\_XL \(15h\)"](#). The value is expressed as 2's complement.

The reference pressure value is used when AUTOZERO or AUTORIFP function is enabled (refer to the [Section 10.7: "CTRL\\_REG3 \(12h\)"](#) register) and for the Autozero function (refer to the [Section 10.1: "INTERRUPT\\_CFG \(0Bh\)"](#) register).

## 8.10 REF\_P\_L\_16h

Reference pressure (middle part)

Table 26: REF\_P\_L (16h) register

| 7      | 6      | 5      | 4      | 3      | 2      | 1     | 0     |
|--------|--------|--------|--------|--------|--------|-------|-------|
| REFL15 | REFL14 | REFL13 | REFL12 | REFL11 | REFL10 | REFL9 | REFL8 |

|            |                                                                                                                                   |
|------------|-----------------------------------------------------------------------------------------------------------------------------------|
| REFL[15:8] | This register contains the mid part of the reference pressure value.<br>Refer to <a href="#">Section 10.9: "REF_P_XL (15h)"</a> . |
|------------|-----------------------------------------------------------------------------------------------------------------------------------|

## 8.11 REF\_P\_H\_17h

Reference pressure (MSB part)

Table 27: REF\_P\_H (17h) register

| 7      | 6      | 5      | 4      | 3      | 2      | 1      | 0      |
|--------|--------|--------|--------|--------|--------|--------|--------|
| REFL23 | REFL22 | REFL21 | REFL20 | REFL19 | REFL18 | REFL17 | REFL16 |

|             |                                                                                                                                    |
|-------------|------------------------------------------------------------------------------------------------------------------------------------|
| REFL[23:16] | This register contains the high part of the reference pressure value.<br>Refer to <a href="#">Section 10.9: "REF_P_XL (15h)"</a> . |
|-------------|------------------------------------------------------------------------------------------------------------------------------------|

## 8.12 RPDS\_L\_18h

Pressure offset (LSB data)

Table 28: RPDS\_L (18h) register

| 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     |
|-------|-------|-------|-------|-------|-------|-------|-------|
| RPDS7 | RPDS6 | RPDS5 | RPDS4 | RPDS3 | RPDS2 | RPDS1 | RPDS0 |

|           |                                                                   |
|-----------|-------------------------------------------------------------------|
| RPDS[7:0] | This register contains the low part of the pressure offset value. |
|-----------|-------------------------------------------------------------------|

If, after the soldering of the component, a residual offset is still present, it can be removed with a one-point calibration.

After the soldering, the measured offset can be stored in the [Section 10.13: "RPDS\\_H\\_19h"](#) and [Section 10.12: "RPDS\\_L\\_18h"](#) registers and automatically subtracted from the pressure output registers: the output pressure register PRESS\_OUT (28h, 29h and 2Ah) is provided as the difference between the measured pressure and the content of the register 256\*RPDS (18h, 19h)\*.

\*DIFF\_EN = '0', AUTOZERO = '0', AUTORIFP = '0'

## 8.13 RPDS\_H\_19h

Pressure offset (MSB data)

Table 29: RPDS\_H (19h) register

| 7      | 6      | 5      | 4      | 3      | 2      | 1     | 0     |
|--------|--------|--------|--------|--------|--------|-------|-------|
| RPDS15 | RPDS14 | RPDS13 | RPDS12 | RPDS11 | RPDS10 | RPDS9 | RPDS8 |

|            |                                                                                                                            |
|------------|----------------------------------------------------------------------------------------------------------------------------|
| RPDS[15:8] | This register contains the high part of the pressure offset value.<br>Refer to <a href="#">Section 10.12: "RPDS_L_18h"</a> |
|------------|----------------------------------------------------------------------------------------------------------------------------|

## 8.14 RES\_CONF\_1Ah

Low-power mode configuration

Table 30: RES\_CONF (1Ah) register

| 7                | 6                | 5                | 4                | 3                | 2                | 1                       | 0     |
|------------------|------------------|------------------|------------------|------------------|------------------|-------------------------|-------|
| 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | Reserved <sup>(2)</sup> | LC_EN |

### Notes:

<sup>(1)</sup>These bits must be set to '0' for proper operation of the device.

<sup>(2)</sup>The content of this bit must not be modified for proper operation of the device

|                      |                                                                                               |
|----------------------|-----------------------------------------------------------------------------------------------|
| LC_EN <sup>(1)</sup> | Low current mode enable. Default 0.<br>0: Normal mode (low-noise mode); 1: Low-current mode). |
|----------------------|-----------------------------------------------------------------------------------------------|

### Notes:

<sup>(1)</sup>The LC\_EN bit must be changed only with the device in power down and not during operation. Once LC\_EN bit is configured, it affects both One-shot mode and Continuous mode.

## 8.15 INT\_SOURCE\_25h

Interrupt source

**Table 31: INT\_SOURCE (25h) register**

| 7           | 6 | 5 | 4 | 3 | 2  | 1  | 0  |
|-------------|---|---|---|---|----|----|----|
| BOOT_STATUS | 0 | 0 | 0 | 0 | IA | PL | PH |

|             |                                                                                                                           |
|-------------|---------------------------------------------------------------------------------------------------------------------------|
| BOOT_STATUS | If '1' indicates that the Boot (Reboot) phase is running.                                                                 |
| IA          | Interrupt active.<br>(0: no interrupt has been generated;<br>1: one or more interrupt events have been generated).        |
| PL          | Differential pressure Low.<br>(0: no interrupt has been generated;<br>1: Low differential pressure event has occurred).   |
| PH          | Differential pressure High.<br>(0: no interrupt has been generated;<br>1: High differential pressure event has occurred). |

## 8.16 FIFO\_STATUS\_26h

FIFO status

**Table 32: FIFO\_STATUS (26h) register**

| 7        | 6   | 5    | 4    | 3    | 2    | 1    | 0    |
|----------|-----|------|------|------|------|------|------|
| FTH_FIFO | OVR | FSS5 | FSS4 | FSS3 | FSS2 | FSS1 | FSS0 |

|          |                                                                                                                                        |
|----------|----------------------------------------------------------------------------------------------------------------------------------------|
| FTH_FIFO | FIFO threshold status.<br>(0: FIFO filling is lower than treshold level,<br>1: FIFO filling is equal or higher than treshold level).   |
| OVR      | FIFO overrun status.<br>(0: FIFO is not completely full;<br>1: FIFO is full and at least one sample in the FIFO has been overwritten). |
| FSS[5:0] | FIFO stored data level.<br>(000000: FIFO empty, 100000: FIFO is full and has 32 unread samples).                                       |

**Table 33: FIFO\_STATUS example: OVR/FSS details**

| FTH    | OVRN | FSS5 | FSS4 | FSS3 | FSS2 | FSS1 | FSS0 | Description      |
|--------|------|------|------|------|------|------|------|------------------|
| 0      | 0    | 0    | 0    | 0    | 0    | 0    | 0    | FIFO empty       |
| -- (1) | 0    | 0    | 0    | 0    | 0    | 0    | 1    | 1 unread sample  |
| ...    |      |      |      |      |      |      |      |                  |
| --(1)  | 0    | 1    | 0    | 0    | 0    | 0    | 0    | 32 unread sample |

| FTH | OVRN | FSS5 | FSS4 | FSS3 | FSS2 | FSS1 | FSS0 | Description                               |
|-----|------|------|------|------|------|------|------|-------------------------------------------|
| 1   | 1    | 1    | 0    | 0    | 0    | 0    | 0    | At least one sample have been overwritten |

**Notes:**

<sup>(1)</sup>When the number of unread samples in FIFO is greater than the threshold level set in register [Section 10.8: "FIFO\\_CTRL \(14h\)"](#), FTH value is '1'.

## 8.17 STATUS\_27h

Status register

**Table 34: STATUS (27h) register**

| 7  | 6  | 5    | 4    | 3  | 2  | 1    | 0    |
|----|----|------|------|----|----|------|------|
| -- | -- | T_OR | P_OR | -- | -- | T_DA | P_DA |

|      |                                                                                                                                |
|------|--------------------------------------------------------------------------------------------------------------------------------|
| T_OR | Temperature data overrun.<br>(0: no overrun has occurred;<br>1: a new data for temperature has overwritten the previous one)   |
| P_OR | Pressure data overrun.<br>(0: no overrun has occurred;<br>1: new data for pressure has overwritten the previous one)           |
| T_DA | Temperature data available.<br>(0: new data for temperature is not yet available;<br>1: new data for temperature is available) |
| P_DA | Pressure data available.<br>(0: new data for pressure is not yet available;<br>1: new data for pressure is available)          |

This register is updated every ODR cycle.

## 8.18 PRESS\_OUT\_XL\_28h

Pressure output value (LSB)

**Table 35: PRESS\_OUT\_XL (28h) register**

| 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     |
|-------|-------|-------|-------|-------|-------|-------|-------|
| POUT7 | POUT6 | POUT5 | POUT4 | POUT3 | POUT2 | POUT1 | POUT0 |

|           |                                                                   |
|-----------|-------------------------------------------------------------------|
| POUT[7:0] | This register contains the low part of the pressure output value. |
|-----------|-------------------------------------------------------------------|

The pressure output value is a 24-bit data that contains the measured pressure. It is composed of [Section 10.20: "PRESS\\_OUT\\_H\\_2Ah"](#), [Section 10.19: "PRESS\\_OUT\\_L\\_29h"](#) and [Section 10.18: "PRESS\\_OUT\\_XL\\_28h"](#). The value is expressed as 2's complement.

The output pressure register PRESS\_OUT is provided as the difference between the measured pressure and the content of the register RPDS (18h, 19h)\*.

Please refer to section [Section 5.4: "How to interpret pressure readings"](#) for additional info.

\*DIFF\_EN = '0', AUTOZERO = '0', AUTORIFP = '0'

**8.19 PRESS\_OUT\_L\_29h**

Pressure output value (mid part)

**Table 36: PRESS\_OUT\_L (29h) register**

| 7      | 6      | 5      | 4      | 3      | 2      | 1     | 0     |
|--------|--------|--------|--------|--------|--------|-------|-------|
| POUT15 | POUT14 | POUT13 | POUT12 | POUT11 | POUT10 | POUT9 | POUT8 |

|            |                                                                                                                                   |
|------------|-----------------------------------------------------------------------------------------------------------------------------------|
| POUT[15:8] | This register contains the mid part of the pressure output value.<br>Refer to <a href="#">Section 10.18: "PRESS_OUT_XL_28h"</a> . |
|------------|-----------------------------------------------------------------------------------------------------------------------------------|

**8.20 PRESS\_OUT\_H\_2Ah**

Pressure output value (MSB)

| 7      | 6      | 5      | 4      | 3      | 2      | 1      | 0      |
|--------|--------|--------|--------|--------|--------|--------|--------|
| POUT23 | POUT22 | POUT21 | POUT20 | POUT19 | POUT18 | POUT17 | POUT16 |

|             |                                                                                                                                   |
|-------------|-----------------------------------------------------------------------------------------------------------------------------------|
| POUT[23:16] | This register contains the low part of the pressure output value.<br>Refer to <a href="#">Section 10.18: "PRESS_OUT_XL_28h"</a> . |
|-------------|-----------------------------------------------------------------------------------------------------------------------------------|

**8.21 TEMP\_OUT\_L\_2Bh**

Temperature output value (LSB)

**Table 37: TEMP\_OUT\_L (2Bh) register**

| 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     |
|-------|-------|-------|-------|-------|-------|-------|-------|
| TOUT7 | TOUT6 | TOUT5 | TOUT4 | TOUT3 | TOUT2 | TOUT1 | TOUT0 |

|           |                                                                      |
|-----------|----------------------------------------------------------------------|
| TOUT[7:0] | This register contains the low part of the temperature output value. |
|-----------|----------------------------------------------------------------------|

The temperature output value is a 16-bit data that contains the measured temperature. It is composed of [Section 10.22: "TEMP\\_OUT\\_H\\_2Ch"](#), and [Section 10.21: "TEMP\\_OUT\\_L\\_2Bh"](#). The value is expressed as 2's complement.

## 8.22 TEMP\_OUT\_H\_2Ch

Temperature output value (MSB)

Table 38: TEMP\_OUT\_H (2Ch) register

| 7      | 6      | 5      | 4      | 3      | 2      | 1     | 0     |
|--------|--------|--------|--------|--------|--------|-------|-------|
| TOUT15 | TOUT14 | TOUT13 | TOUT12 | TOUT11 | TOUT10 | TOUT9 | TOUT8 |

|            |                                                                       |
|------------|-----------------------------------------------------------------------|
| TOUT[15:8] | This register contains the high part of the temperature output value. |
|------------|-----------------------------------------------------------------------|

The temperature output value is a 24-bit data that contains the measured temperature. It is composed of [Section 10.20: "PRESS\\_OUT\\_H\\_2Ah"](#), and [Section 10.18: "PRESS\\_OUT\\_XL\\_28h"](#). The value is expressed as 2's complement.

## 8.23 LPFP\_RES\_33h

Low-pass filter reset register.

If the LPFP is active, in order to avoid the transitory phase, the filter can be reset by reading this register before getting out pressure measurements.

## 9 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

### 9.1 CCLGA10L package information

Figure 22: Ceramic CCLGA 10L package outline

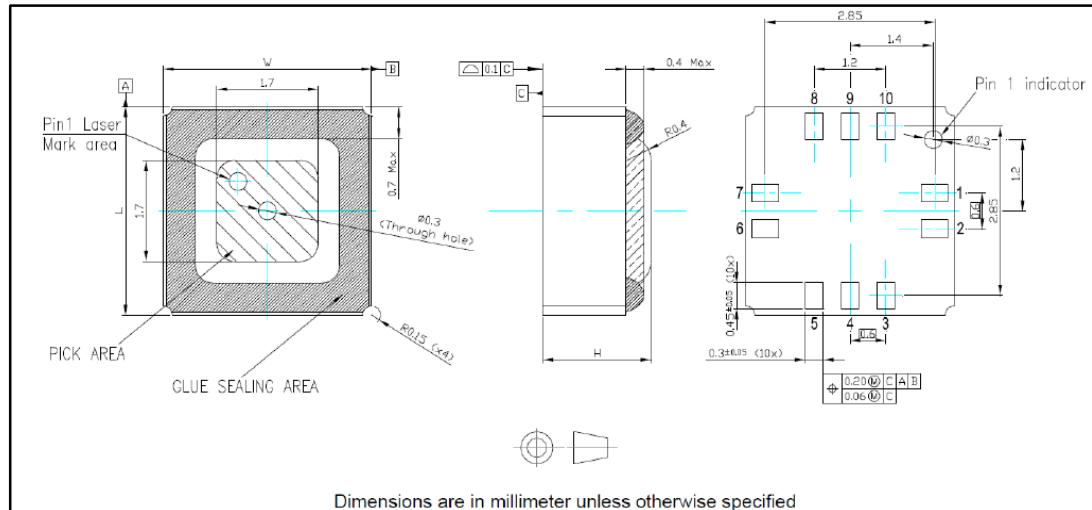
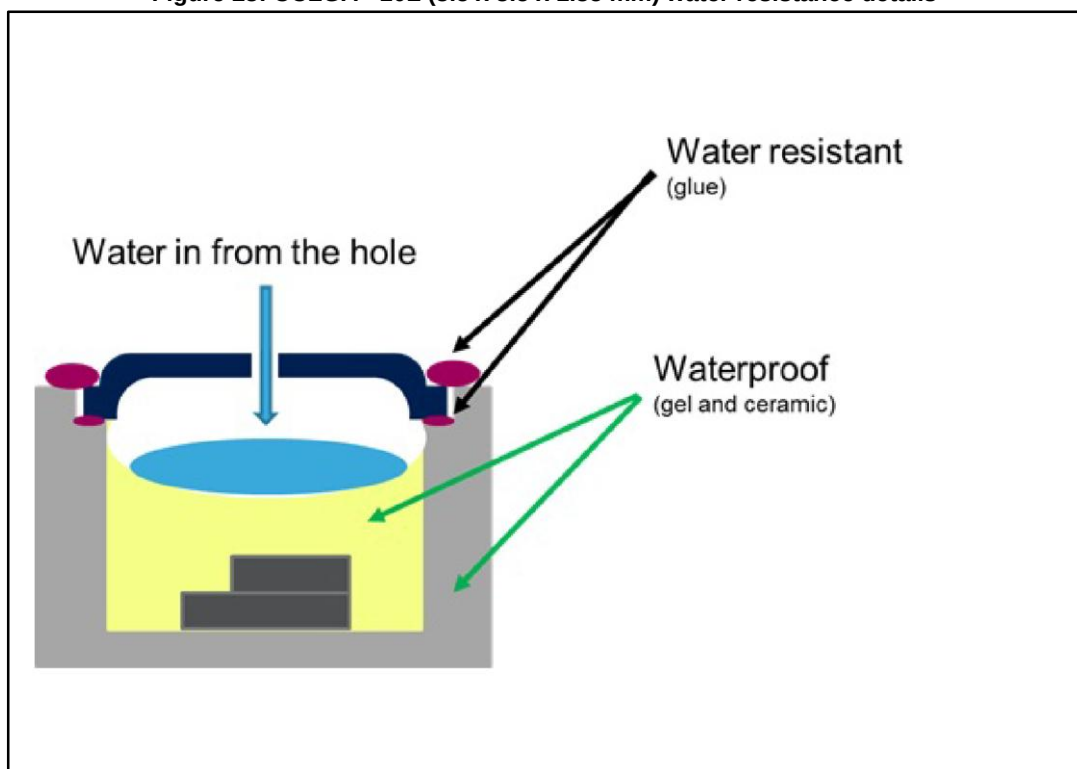


Table 39: CCLGA (3.5 x 3.5 x 1.85 mm) package mechanical data

| Item   | Dimension (mm) | Tolerance (mm) |
|--------|----------------|----------------|
| Length | 3.5            | ±0.15          |
| Width  | 3.5            | ±0.15          |
| Height | 1.85           | ±0.15          |

Figure 23: CCLGA - 10L (3.5 x 3.5 x 1.85 mm) water resistance details



## 9.2 CCLGAA10L packing information

Figure 24: Carrier tape information for CCLGA10L package

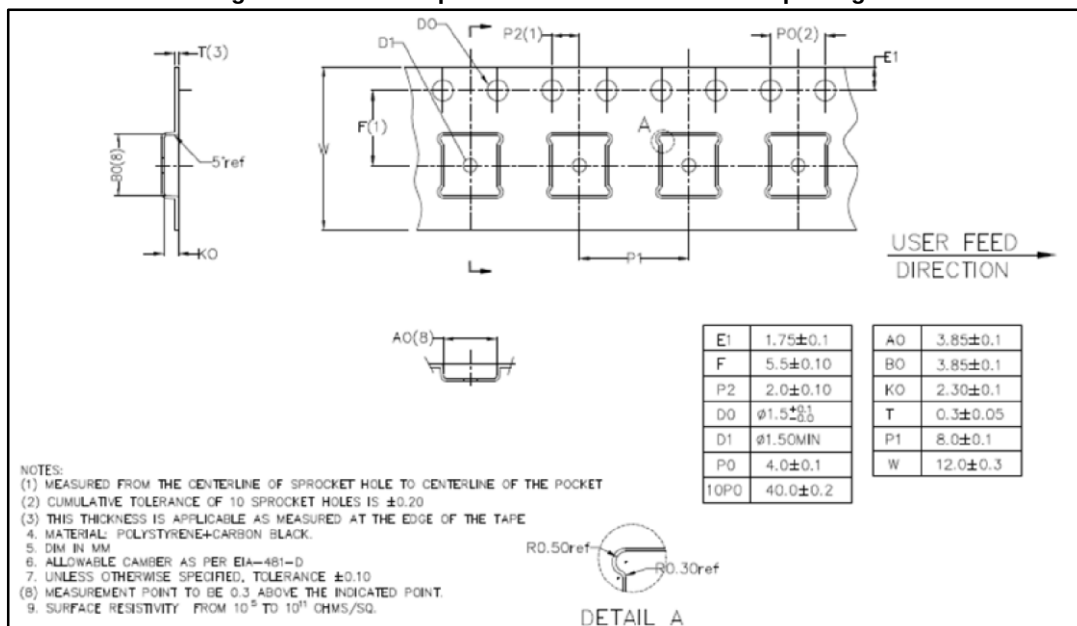


Figure 25: CCLGA10L tape and reel package orientation

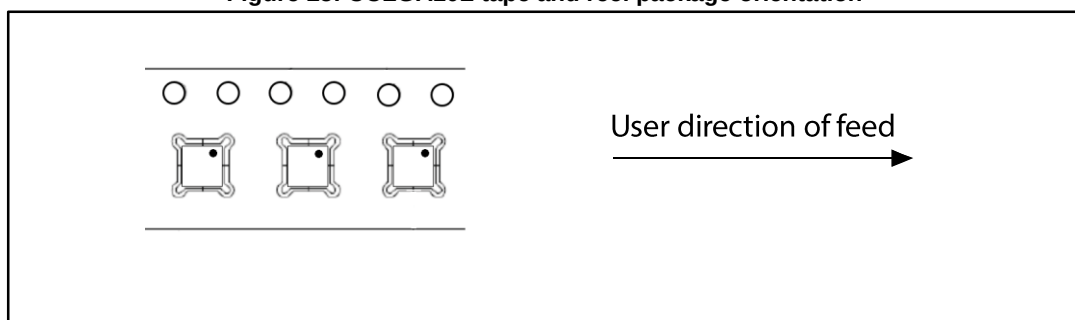


Figure 26: Reel information carrier tape CCLGA10L package

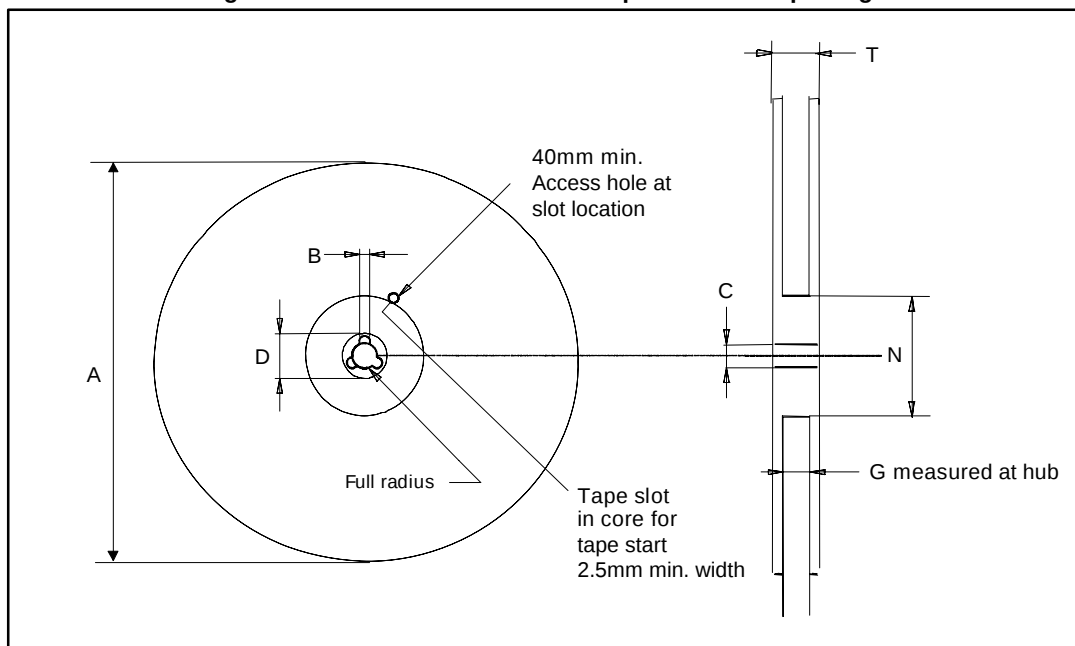


Table 40: Reel dimensions for carrier tape of CCLGA10L package

| Reel dimensions (mm) |            |
|----------------------|------------|
| A (max)              | 330        |
| B (min)              | 1.5        |
| C                    | 13 ±0.25   |
| D (min)              | 20.2       |
| N (min)              | 60         |
| G                    | 12.4 +2/-0 |
| T (max)              | 18.4       |

## 10 Revision history

Table 41: Document revision history

| Date        | Version | Changes          |
|-------------|---------|------------------|
| 18-Jul-2016 | 1       | Initial release. |

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